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Revision history

Revision	Date	Description	Author
1	June 30 2022	Initial version (*)	D. Wind
1.1	July 13 2022	aligned with DLC Plan small modifications	D. Wind

(*) based on original C125 DLC Plan DOC-503511 by Ad van Pinxteren et al.

TABLE OF CONTENTS

1 PURPOSE EARLY PRE-PT-F DLC PLAN

This document describes the Early PRE- PT-F Device Level Characterization Plan for the process transfer of C125 from NXP ICN8 fab to DTJX 12 inch fab as second source. The name for this transfer project is "Transfer C125 from ICN8 to DTJX (second source)".

Early PRE-PT-F device level characterization is meant to de-risk the project and measure critical I-V and C-V curves in advance to safeguard there are no roadblocks from device performance point-of-view at the Process Transfer project gate meeting for process Freeze (PT-F). The full DLC program (DOC-541286), will be performed on devices on silicon with the process freeze conditions and reported at PT-V/R gate meeting.

To be able to review the device performance from DTJX silicon in an early stage -even before process freeze- the devices described in section2 need to be measured on DTJX wafers. This Early DLC program will also help the engineers in DTJX fab to become familiar with the measurement structures and measurement program debugging on the I-V and C-V curves can be performed in advance. Verification measurements of same devices can be made on an 8" ICN8 reference wafer. Since this is the first process transfer of BG A&L to a 12" waferfab extra checks are required on centre versus edge. Especially the parameters that can be impacted by strain /stress like beta of a MOS transistor via de mobility needs some attention.

All the measurement conditions have been specified in detail (section3)

Output (section4): Provide results in a report presenting the C-V or I-V plots and also a data dump with raw data in ascii format.

2 DESCRIPTION OF DEVICES

2.1 Device List

The devices to be measured are MOS capacitors, junction diodes, transistors and resistors. All devices are in the PCM, just some extra tests could be done on the WLR PEM modules later on if needed for more details.
The requirement is to measure I-V characteristics of devices at 3 temperatures: -40, 25 and 125°C unless specified otherwise.
NB: measurements at 3 TEMPs on same devices in order to see correct temperature coefficients.

CV curves of 2 MOS capacitors N/P type and 3 Junction capacitors N+/P-, P+/N- and N-/P- type at T=25degC only.
IV curves of the MOScaps and Diodes are not very useful in general for -40degC, so 25 and 125 degC is sufficient.

The gds files and the documentation have been delivered.
< Include GDSfile PCM>

Device list

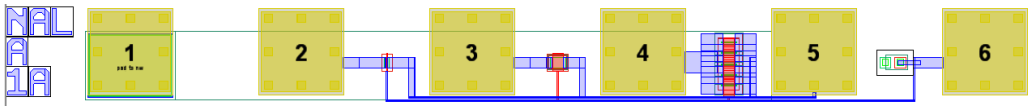
Device	PCM	Measurement	Purpose
Capacitors		C-V I-V(T)	Check Cox Tox, Poly depletion, leakage, Bdn
MOScap N plate	NAL_C	C-V I-V(T)	N+POLY on Pwell
MOScap P plate	NAL_D	C-V I-V(T)	P+POLY on Nwell
Diodes		C-V , I-V(T)	Check Cjun, leakage, Bdn
JunCap N+/P-	NAL_B	C-V , I-V(T)	large area diode ODN+ p02 ; PW p01
JunCap P+/N-	NAL_B	C-V , I-V(T)	large area diode ODP+ p11 ; NW p12
JunCap N-/P-	NAL_B	C-V , I-V(T)	large NWell area NW p12 ; Psub p01
Transistors		All I-V_MOS	Check I-V(T) , key parameters, e.g. Beta,Vt, Ion, Ioff, SVT_slope
NMOS10/10,10/0.6,10/0.5	NAL_A/C	I-V_MOS, Bdn	All regions, check Bdns
PMOS10/10,10/0.6,10/0.5	NAL_A/C	I-V_MOS,Bdn	All regions, check Bdns
NMOS 10/0.6 10/0.5	NAL_A/C	HCI risk check	Check weak-avalanche current (Isub_max) at Vds=5, 5.5, 6V
NMOS 10/0.6 wafermap	NAL_A	Ileak	Check uniformity Ileak position effect T=25 and T=125degC
PMOS10/0.6 wafermap	NAL_A	Ileak	Check uniformity Ileak position effect T=25 and T=125degC
Vt(L) Vt-roll-off Nch and Pch	NAL_A/C	Vt-Lin;Vt-gm,..	Check L-scaling for W=10um; C1MOD 41019/20
Vt(T) Nch and Pch	NAL_A/C	keypars	Check T-scaling for W=10/0.6 and W=10/10;
I_Wmin Nch and Pch	NAL_A/C	keypars	Check current levels 5x0.75/10
Resistors		I-V_RES	Check R(T,V) . TCR, VCR
Rsq OD/P+	NAL_B	I-V(T)	
Rsq OD/N+	NAL_B	I-V(T)	
Rsq PS/OD/N+	NAL_D	I-V(T)	
Res PS/OD/N+	NAL_D	I-V(T)	
Res EPI (pinched by NW)	NAL_F	I-V(T)	
Res NW_LOCOS	NAL_F	I-V(T)	

2.2 Modules in the PCM

The devices described in the Device List table section 2.1 can be found in different modules in the PCM. In this section the modules in the PCM are described.

2.2.1 Module NAL_A_1A

Module A can be divided in 2 parts: the P-channels and the N-channels.

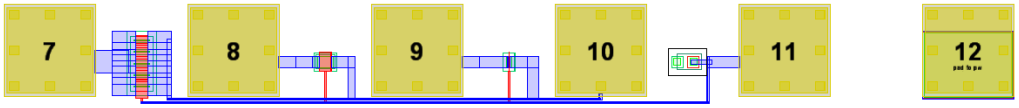


P-channels: 10/0.6, 10/10 and 5x 0.75/10

With protection diode on the gate and common source and gate pad.

pin connections Pch devices:

1 NW connection
2 P-channel 10/0.6 drain
3 P-channel 10/10 drain
4 P-channel 5x 0.75/10 drain
5 Common source pin 5
6 Common gate with protection



N-channels: 10/0.6, 10/10 and 5x 0.75/10
With protection diode on the gate and common source and gate pad.
pin connections Nch devices:
7 N-channel 5x 0.75/10 drain
8 N-channel 10/10 drain
9 N-channel 10/0.6 drain
10 Common source pin
11 Common gate with protection
12 PW connection

2.2.2 Module NAL_B_1A

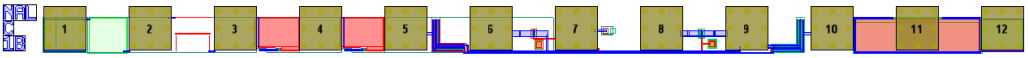
In module B the Rsq OD/N+ and OD/P+ can be tested and the Junction Diodes
pin connections active van der Pauw resistor Rsq OD/N+:
1 PW connection
2 sense low Vsl
3 force low Ifl
4 force high Ifh
5 sense high Vsh
pin connections active van der Pauw resistor Rsq OD/P+:
8 sense high Vsh
9 force high Ifh
10 force low Ifl
11 sense low Vsl
12 NW connection

N+/P- diode p02 ODN+ p01 PWell/Psubstr

P+/N- diode p11 ODP+ p12 Nwell

N-/P- diode p12 Nwell p01 Pwell/Psubstr

2.2.3 Module NAL_C_1B



Module C contains the N- and P-channels 100/0.6 and 10/0.5.

pin connections

1 NW connection

5 Drain P100/0.6

6 Drain P10/0.5

7 Common gate with protection

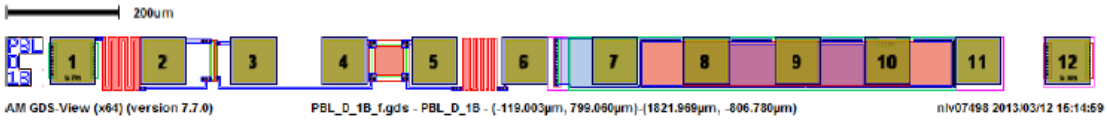
8 Drain N10/0.5

9 Common source

10 Drain N100/0.6

12 PWell connection

2.2.4 Module NAL_D_1B



In module D 3 PS resistors can be tested, Rsq PS on ODN+, R PS 1.2µm on LOCOS and the R PS 0.6 on LOCOS.

pin connections for the poly van der Pauw resistor Rsq PS on ODN+ :

1 Force current low Ifl

2 Sense voltage low Vsl

3 Sense voltage high Vsh

6 Force current high Ifh

pin connections for the poly resistor R PS 1.2µm :

1 Force current low Correction PS1

2 Force current high Correction PS1

2 Force high RPS773

3 Force low RPS773

R PS 1.2µm = RPS773 – Correction PS1

pin connections for the R PS 0.6µm :

5 Force high RPS428

4 Force low RPS428

6 Force high Correction PS2

1 Force low Correction PS2

R PS 1.2µm = RPS428 – Correction PS2 + Correction

2.2.5 Module NAL_F_1B

In module F the Res EPI (pinched by NW) and the Res NW_LOCOS can be tested.

pin connections for the EPI resistor:

1 Force low Res EPI (PW connection)

9 Force high Res EPI (P+ connection)

10 Res EPI (NW connection)

pin connections for the Res NW_LOCOS:

1 Force low (PW connection)

10 Force low (NW connection)

11 Force high (NW connection)

3 DESCRIPTION OF MEASUREMENTS

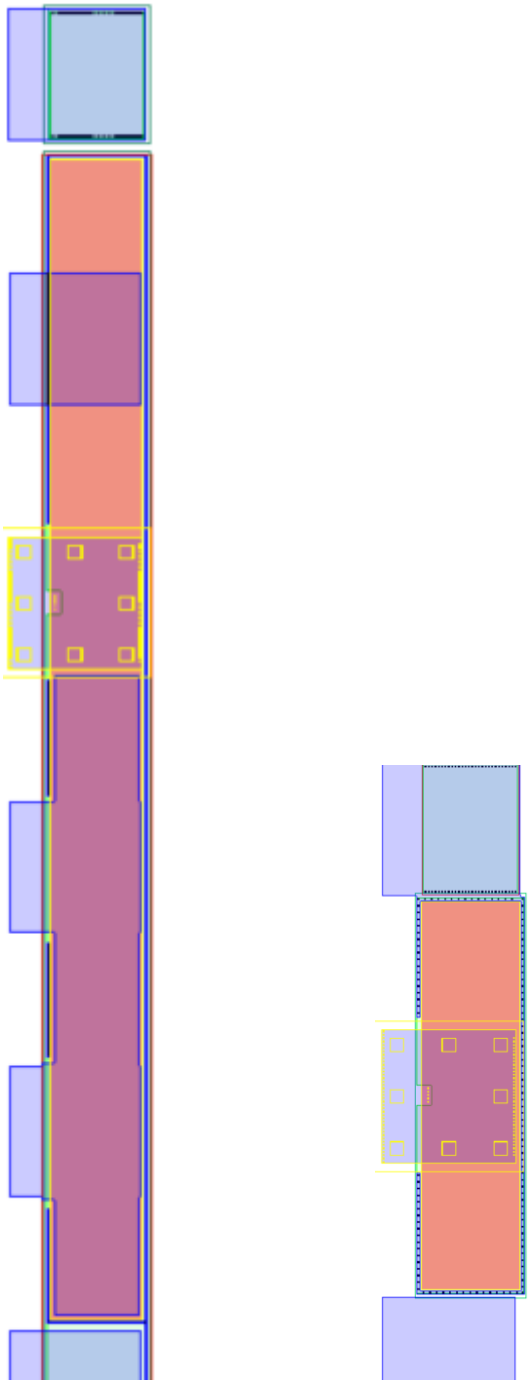
3.1 MOSCAP measurements

In order to check the gate oxide performance C-V and I-V measurements are done on capacitors.

From the many possible combinations the plate caps in the PCM selected are

MosCapP P+POLY on Nwell capacitor (NAL_D)

MosCapN N+POLY on Pwell capacitor(NAL_C); note different area



3.1.1 C-V measurements

CV measurements are done by sweeping the gate voltage from accumulation to inversion.

For the 5V process (5.5V max) DC sweep from -5.5V to +5.5V for MosCapN and +5.5V to -5.5V for MosCapP. Measurement settings for ac signal Vosc=20mV, Freq=100kHz. Check phase of the measurement to be close to -90deg. Use AVG=16 and Medium int. time for noise reduction.

Prior to measurements perform "Open Correction" to get rid of cabling parasitic capacitance.

From the C-V curve you could extract TOX, VT, VFB, Poly-depletion factor.

3.1.2 I-V measurements

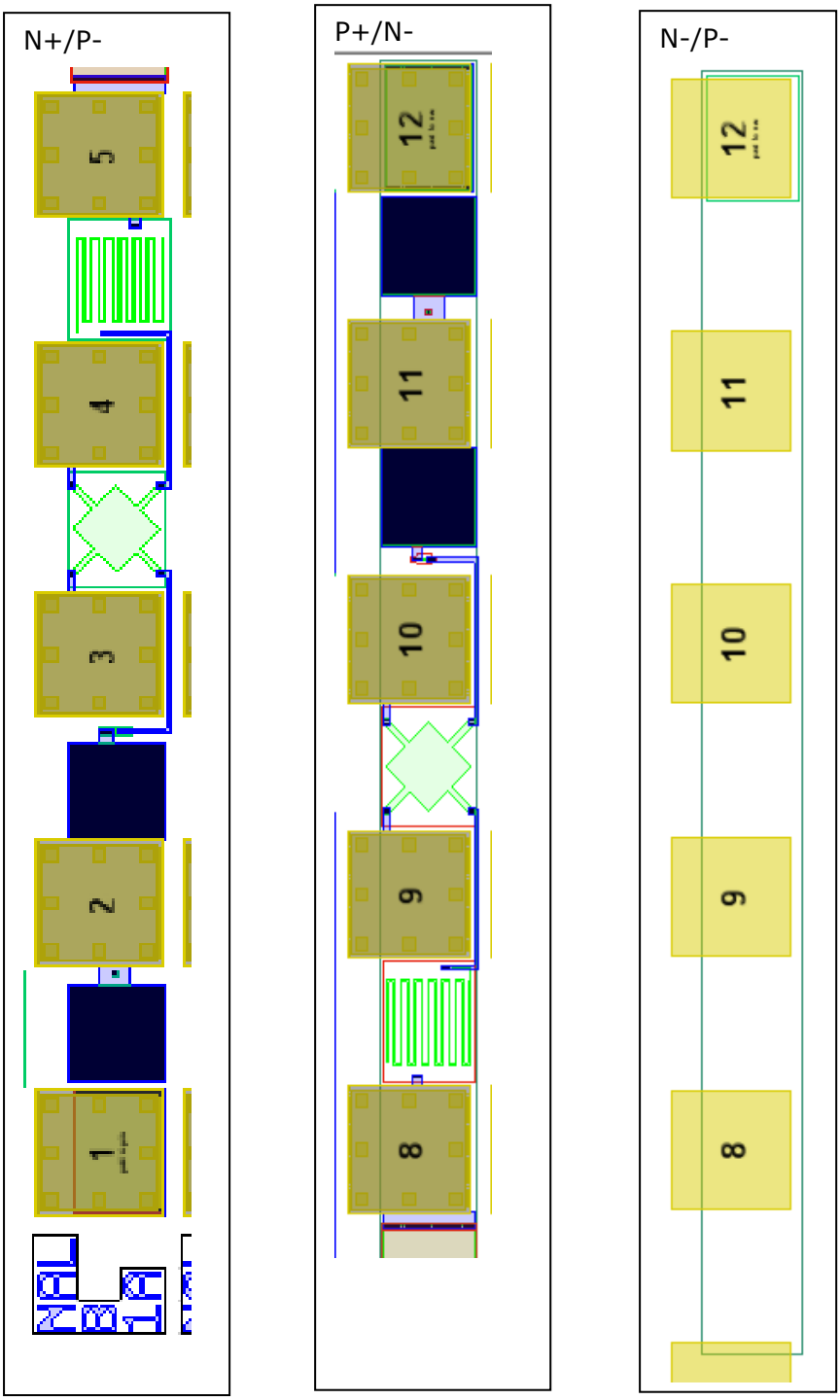
The gate oxide capacitor under standard operating conditions is considered leakage free. However , all the capacitors will show leakage (F-N tunneling) as soon as field across the plates becomes high enough. For gate oxide quality comparison the leakage behaviour can be compared also at higher TEMPs, although tunnelling mechanism is not so much dependent on TEMP. Sweep voltage on the POLY plate (gate) from 0 to +15V and 0 to -15V. NB. since these sweeps up to high voltage levels (far beyond the std Vsupply_max=5.5V) can cause damage to the device it is advised to measure on fresh devices and also test a few devices until Gate Oxide Breakdown (destructive).

Repeat the measurement and store first I-V results and 2nd I-V result to see if soft-leakage effect occurs.

Monitor both currents , on gate node as well as on well node, to check there is no other leakage path.

3.2 Diode measurements

The junction diodes need C-V and I-V measurements. For junction leakage esp. the higher TEMP (125degC) is important. The comparison on C-V curves will tell if junction profiles are the same.



N+/P- Note all the ODN+ connected , incl resistor modules is part of the diode

P+/N- Similar structure in PCM NAL_B and same holds for ODP+

N-/P- the Nwell to substrate diode contains the OPD+ structures as in the middle, but total junction diode can be tested independently.

3.2.1 C-V measurements

CV measurements for junction diodes are done by sweeping the gate voltage from reverse (Vsupply_max 5.5V) to forward (0.5V). T=25degC only is good enough.

Measurement settings for ac signal Vosc=20mV, Freq=100kHz. Check phase of the measurement to be close to -90deg. Use AVG=16 and Medium int. time for noise reduction.

Prior to measurements perform "Open Correction" to get rid of cabling parasitic capacitance.

From the C-V curve you can extract grading coefficient, Cj0 and VD.

3.2.2 I-V measurements

The junction diode leakage behaviour should be compared. To do so the forward and reverse leakage behaviour can be measured at TEMP=25 and 125degC. Sweep voltage over the junction from reverse 5.5V to forward 0.5V.

For junction breakdown measurements in reverse sweep higher up. Can be from 0 to 15V or 20V or even 25V for the N-P- junction. NB. since these sweeps are up to high voltage levels (far beyond the standard Vsupply_max=5.5V), they can cause damage to the device and it is advised to measure on fresh devices and also test the devices until Junction Breakdown occurs. Repeat the measurement and store first I-V results and 2nd I-V result to see if soft-leakage effect and if Vbdn walk-out occurs. Set current compliance, eg to 1mA to keep device alive.

Monitor both currents, on anode as well as on kathode, to check there is no other leakage path.

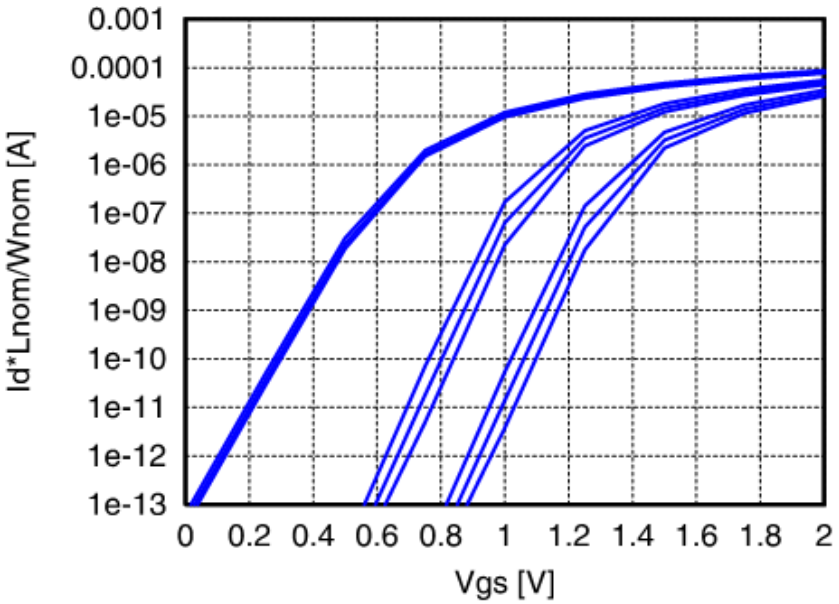
3.3 Transistor measurements

The transistors to be tested are for N- and P-channel the 10/10, 10/0.6, 10/0.5 5x0.75/10 and the 100/0.6. For the measurements on the N- and P-channel the bias conditions are described in below paragraphs. For each measurement a graph is shown as an example.

3.3.1 Sub threshold region

Vds= 1.667 , 3.33, 5 V
Vbs= 0, 2.5 and 5V
Vgs= sweep from -0.5 to 2V; steps 25mV

Measure id, ib
plot log(id)-vg and log(ib)-vg (separate graphs)

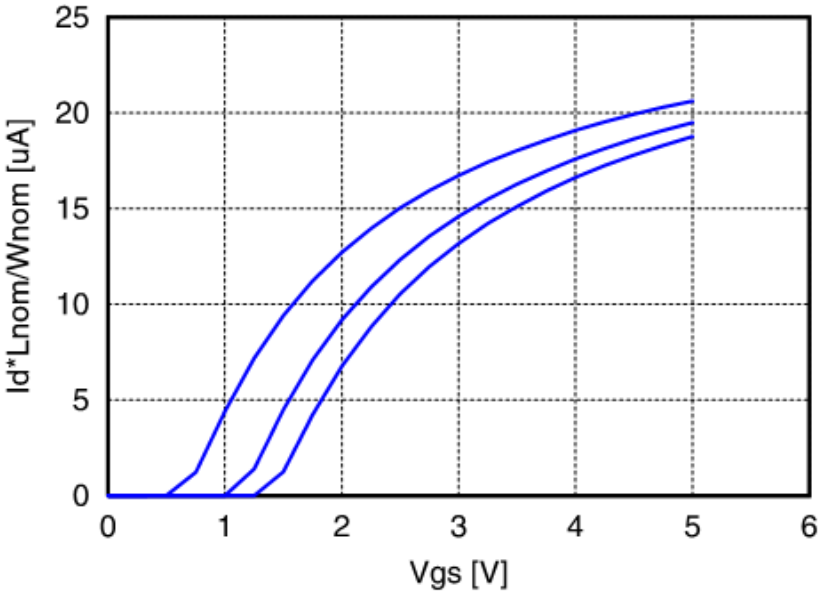


Example id-vg

3.3.2 Linear region

Vds= 100mV
Vbs= 0, 2.5 and 5V
Vgs= sweep from 0 to 5V; step 50mV

Measure id
plot log(id)-vg

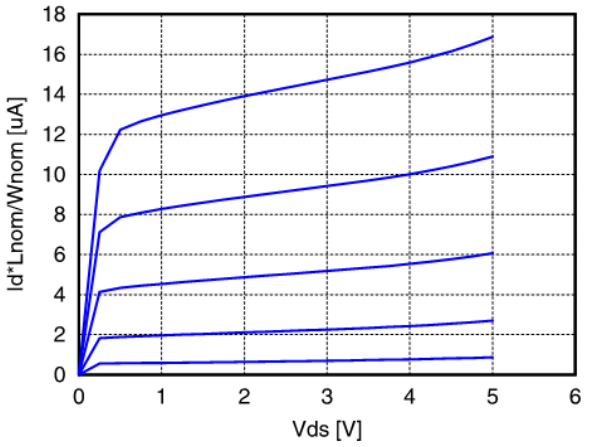


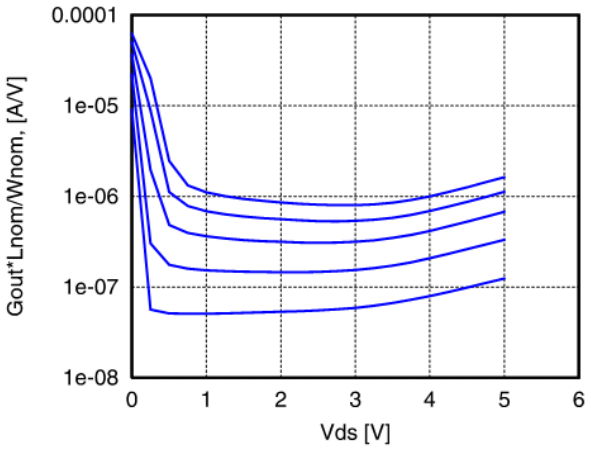
Example id-vg

3.3.3 Saturation region (low Vgs)

Vgs = 0.6 to 1.2V in steps of 100mV
Vbs = 0V
Vds = sweep from 0 to 5V ; step 100mV

Measure id
calculate gds ; gds=did/dvd (first derivative)
plot id-vd and plot gds-vd

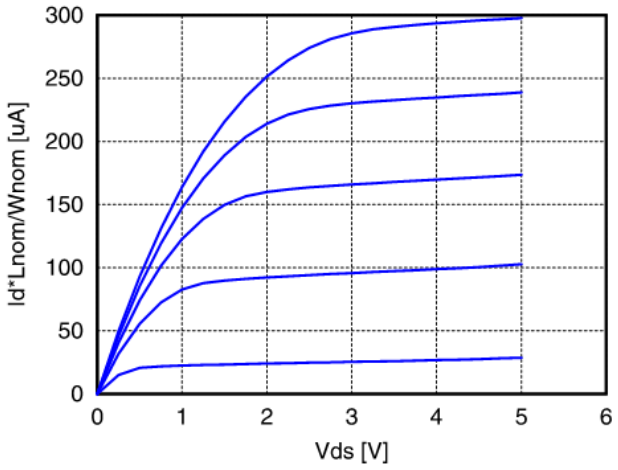


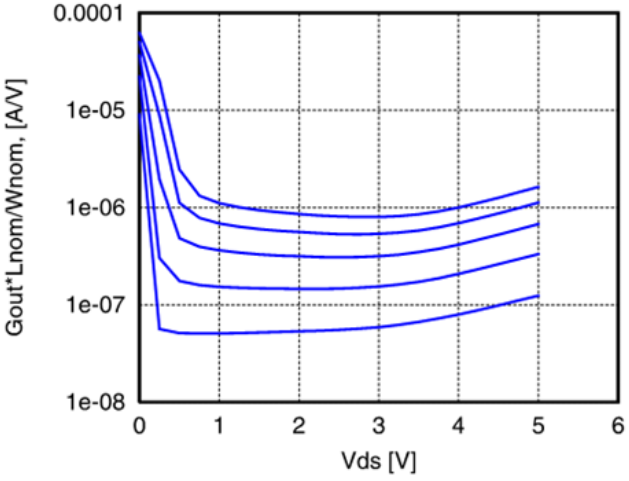


Example id-vd and gds-vd

3.3.4 Saturation region (high Vgs)

Vgs = 1, 2, 3, 4 and 5 V
Vbs = 0V
Vds = sweep 0 to 5V; step 100mV
measure id
calculate gds ; gds=did/dvd (first derivative)
plot id-vd and plot gds-vd



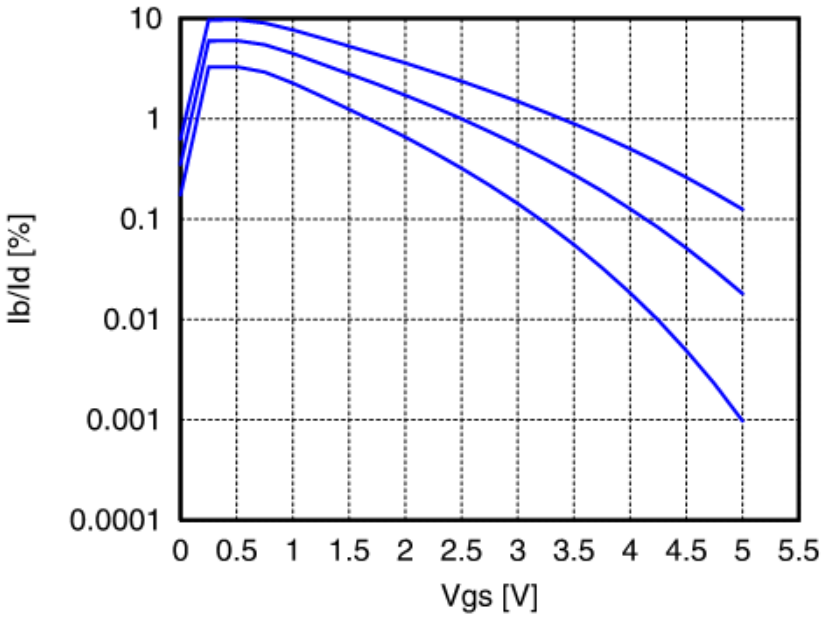


Example id-vd and gds-vd

3.3.5 Avalanche currents

Vds = 4.5, 5 and 5.5 V
Vbs = 0V
Vgs = sweep 0 to 5.5 V

Measure id, ib
Plot ib – Vg and Log(ib/id)



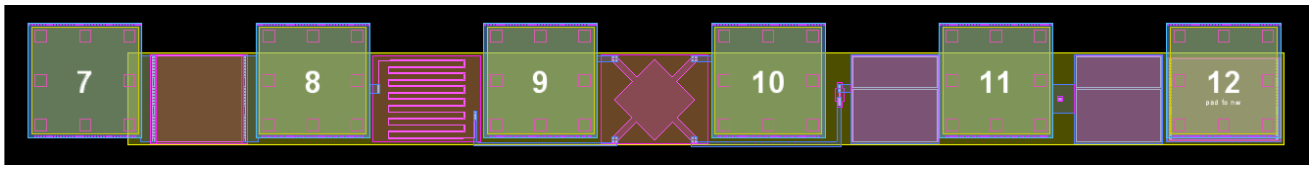
Example ib/id -vg

3.4 Resistor measurements

I-V characteristics should be measured. Use a sweep voltage or -current below the PCM settings given. The PCM measurements are spot measurements, for device char a sweep is requested, e.g. force current sweep: Ihigh sweep 1uA →100uA, step 1uA; Measure Vhigh, set V_compliance= 5V, Calculate R2p[i]=Vhigh[i]/Ihigh[i].

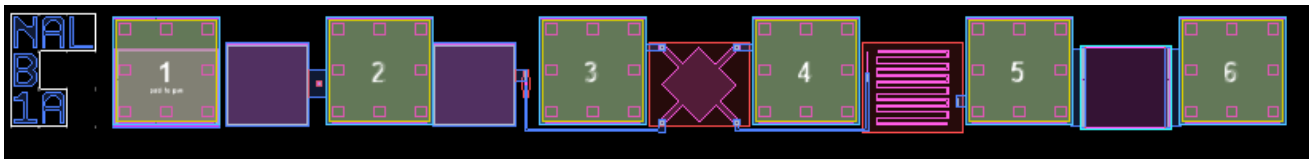
In below paragraphs the settings for the resistor measurements are given according PCM test. For these parameters no graphs are available but are easy to make with a Parameter Analyzer.

3.4.1 Rsq ODP+ (Module NAL_B_1A)



This parameter is tested with a four point resistance measurement with the settings below:
A current of -4.53mA is forced on the force high terminal (pin 10) and the voltage is clamped at 5V.
The force low terminal (p in 9) is connected to GND.
The sense high terminal (pin 11) is connected to the Voltage meter VSH.
The sense low terminal (pin 8) is connected to the Voltage meter VSL.
Rsq=4.53*(VSH-VSL)/Iforce

3.4.2 Rsq ODN+ (Module NAL_B_1A)



This parameter is tested with a four point resistance measurement with the settings below:

A current of 4.53mA is forced on the force high terminal (pin 4) and the voltage is clamped at 5V.

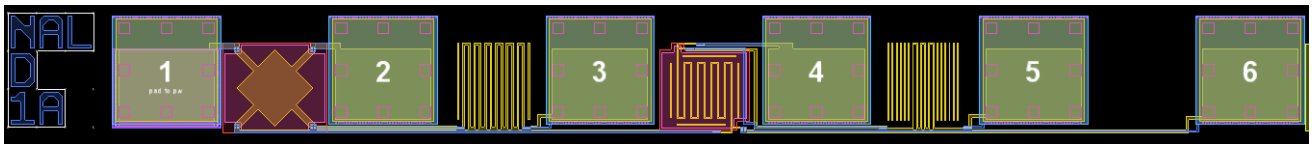
The force low terminal (p in 3) is connected to GND.

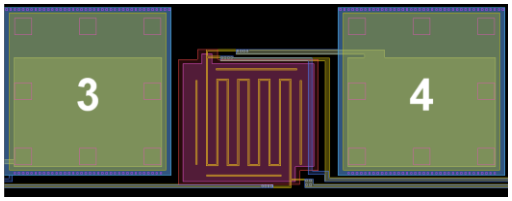
The sense high terminal (pin 5) is connected to the Voltage meter VSH.

The sense low terminal (pin 2) is connected to the Voltage meter VSL.

Rsq=4.53*(VSH-VSL)/Iforce

3.4.3 Res PS/ODN+ (Module NAL_D_1B)





This parameter is tested with a four point resistance measurement with the settings below:

A voltage of 1V is forced on the force high terminal (pin 4) and the current is clamped at 5mA.

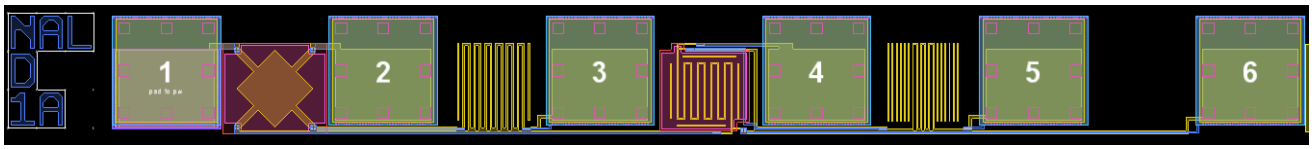
The force low terminal (pin 1) is connected to GND.

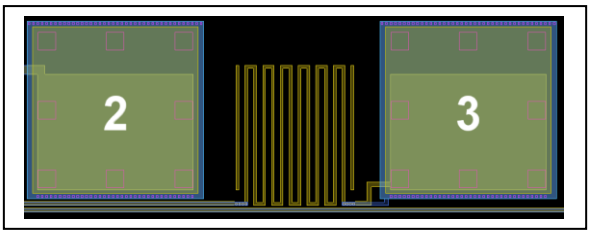
The sense high terminal (pin 5) is connected to the Voltage meter VSH.

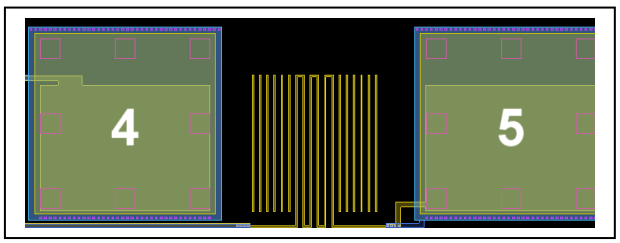
The sense low terminal (pin 6) is connected to the Voltage meter VSL.

The result R4p=(VSH-VSL)/Iforce.

3.4.4 Rsh PS/ODN+ (Module NAL_D_1B)







This parameter is tested on 2 different structures with different POLY line width with a two point resistance measurement Wps=0.6um between pad 4 and 5 and Wps=1.2um between pad 2 and 3. The measured results are corrected due to the combined bond pad structures. The settings and correction method is explained below:

Correction PS1 (1 side vdPauw) is measured:

A current of 1mA with a clamp of 15V is forced on the force high terminal (pin 2).

The force low terminal (pin 1) is connected to GND.

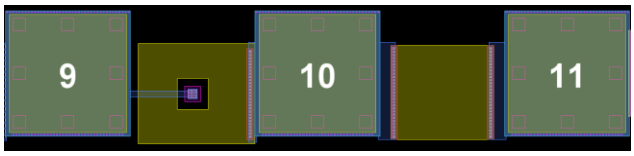
The result of Correction PS1 is the quotient of the measured voltage and forced current.

Correction PS2 is measured:
A current of 1 mA with a clamp of 5 V is forced on the force high terminal (pin 6).
The force low terminal (pin 1) is connected to GND.
The result of Correction PS2 is the quotient of the measured voltage and forced current.

The RPS773 is tested on the structure with a width of 1.2µm:
A current of 100nA with a clamp of 15V is forced on the force high terminal (pin 3).
The force low terminal (pin 1) is connected to GND.
The result of RPS773 is the quotient of the measured voltage and forced current.
R PS 1.2µ = RPS773 – Correction PS1.

The RPS428 is tested on the structure with a width of 0.6µm:
A current of 100nA with a clamp of 5V is forced on the force high terminal (pin 5).
The force low terminal (pin 4) is connected to GND.
The result of RPS428 is the quotient of the measured voltage and forced current.
R PS 0.6µ = RPS428 – Correction PS1+Correction PS2

3.4.5 Epi-resistor (Module NAL_F_1B)



This parameter is tested with a two point resistance measurement with the settings below:
A voltage of 100mV is forced on the force high terminal (pin 9) and the current is clamped at 5mA.
The force low terminal (pin 1 and pin 10) are connected to GND.
The result is the quotient of the forced voltage and measured current.

3.4.6 NW below LOCOS resistor (Module NAL_F_1B)

This parameter is PCM tested with a two point resistance measurement with the

settings below:

A current of 50µA is forced on the force high terminal (pin 10) and the voltage is clamped at 400mV.

The force low terminal (pin 1 and pin 11) are connected to GND.

The result is the quotient of the measured voltage and forced current.

4 OUTPUT : RESULTS

4.1 Report with Plots

For easy comparison of measured device characteristics a report with plots is required in which results of devices on DTJX wafer center versus edge are combined. The reference data of the devices measured on the motherfab wafer (centre only) should be included as well. From the 3 curves in the plot and the known acceptance criteria per device region we can judge if the performance is good or further process tweaking might be needed.

4.2 Raw measurement Data Dump

For easy comparison with simulation data the raw data of all the measurements for C-V and I-V need to be dumped in fixed format. The format is not that critical , as long as each individual measurement file has clear name identifiers from which lot-wafer-die-position-device and measurement conditions can be retrieved.

Expected e.g. excel files or txt files with measurement data in delimited columns.
DTJX_center , lot_waferID, POS, deviceID, meas conditions, V, I
DTJX_edge , lot_waferID, POS, deviceID, meas conditions, V, I
motherfab , lot_waferID, POS, deviceID, meas conditions, V, I

simulated curves (slow-nom-fast window) to be added by Nijmegen FrontEnd Team

A template proposal with formatting will be sent later to agree on.