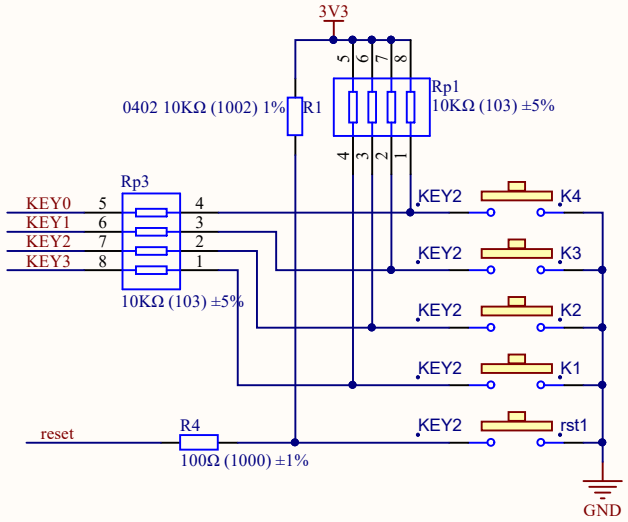
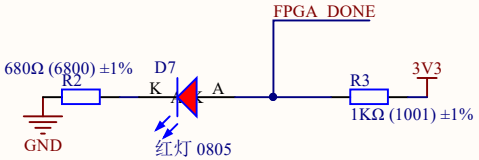
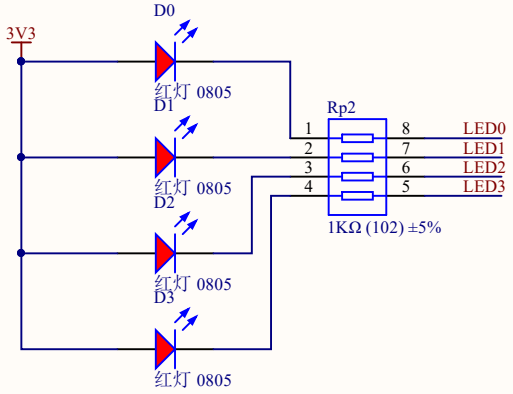


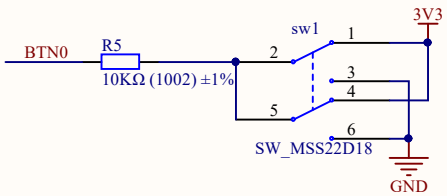
KEY (reset)

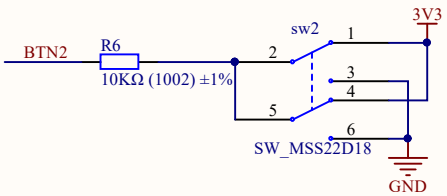


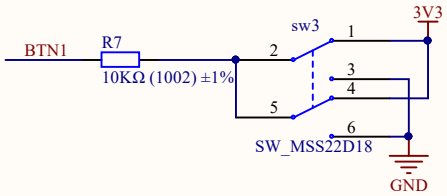
FPGA DONE LED

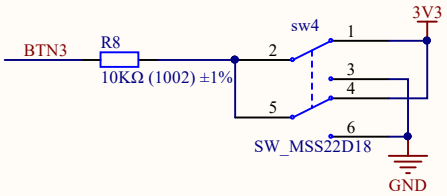


USER LED

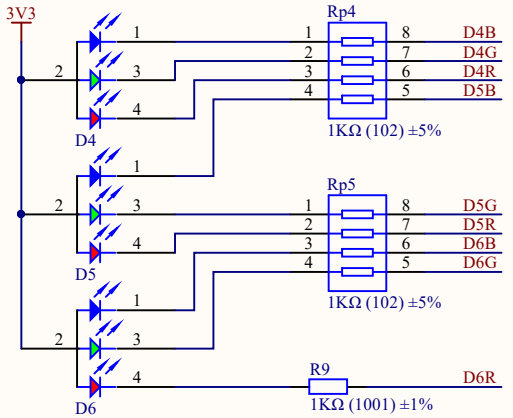






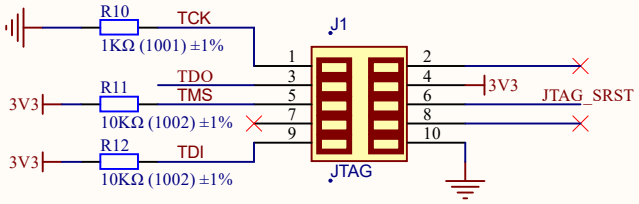


SWITCH

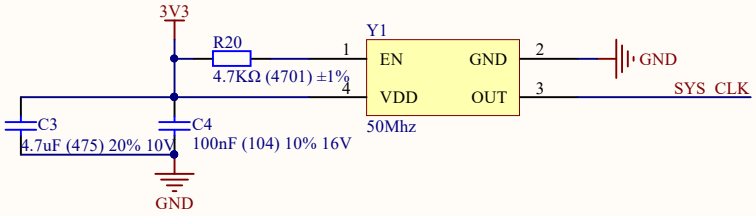


RBG LED

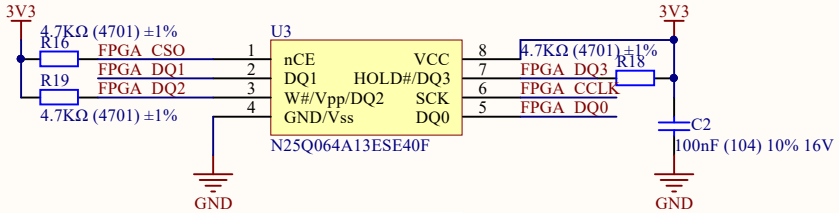
Title		
Size A4	Number	Revision
Date: 2018/3/24		Sheet of
File: G:\SX\..\1_LED_KEY.SchDoc		Drawn By:



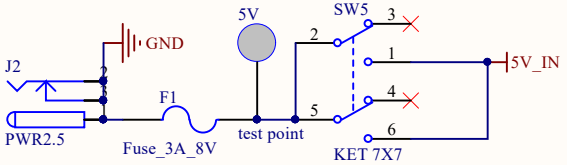
JTAG



有源晶振
50M

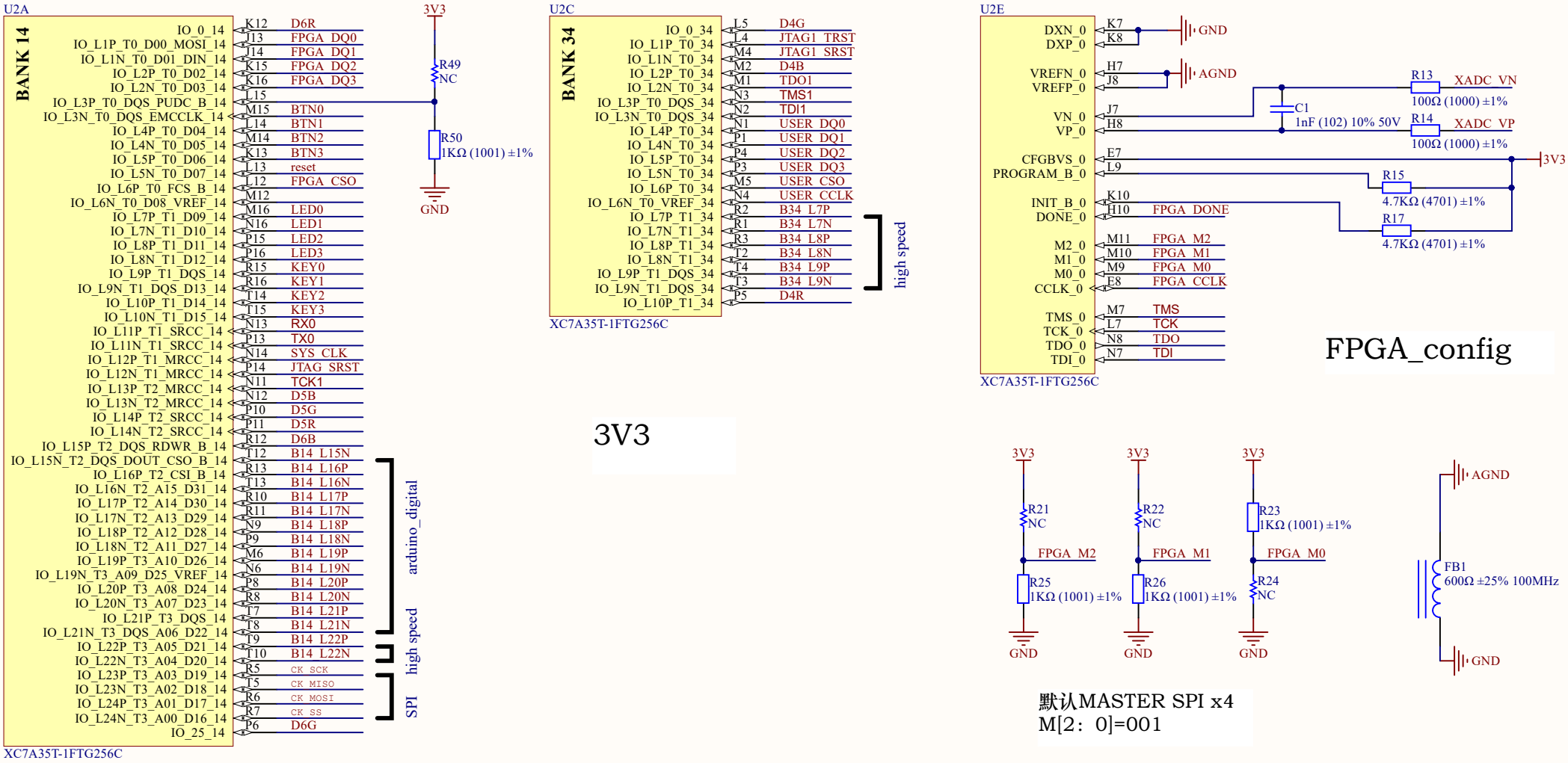


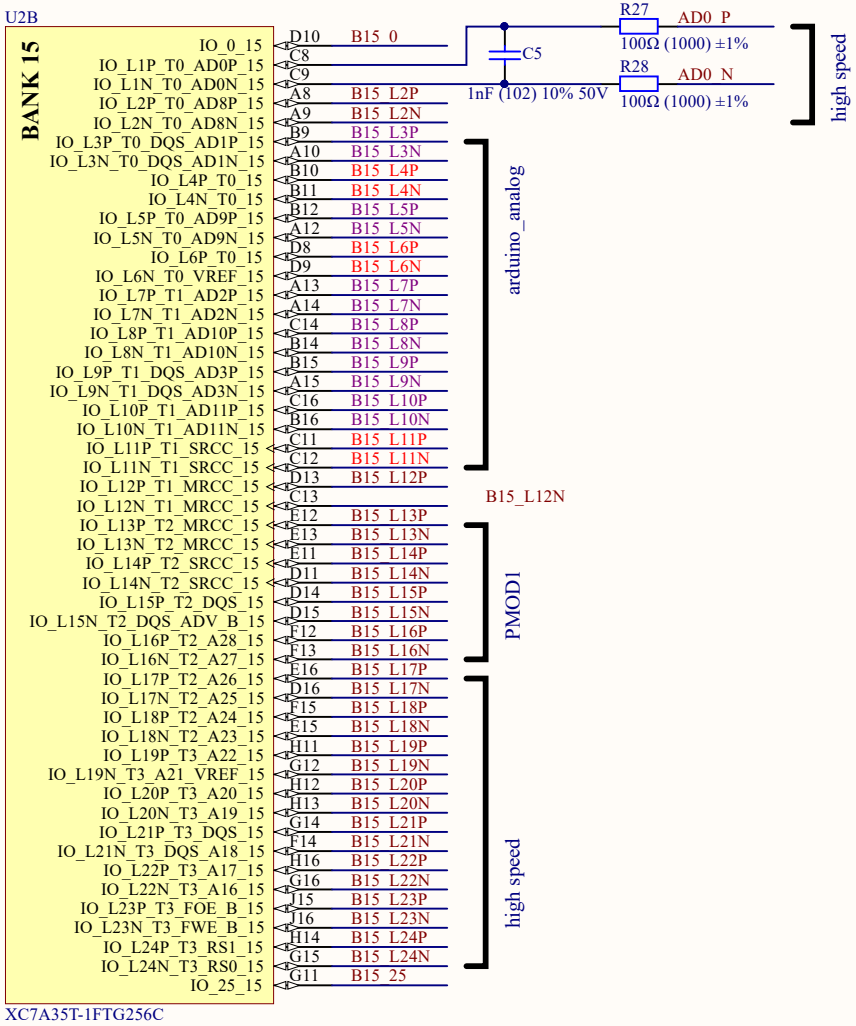
FLASH



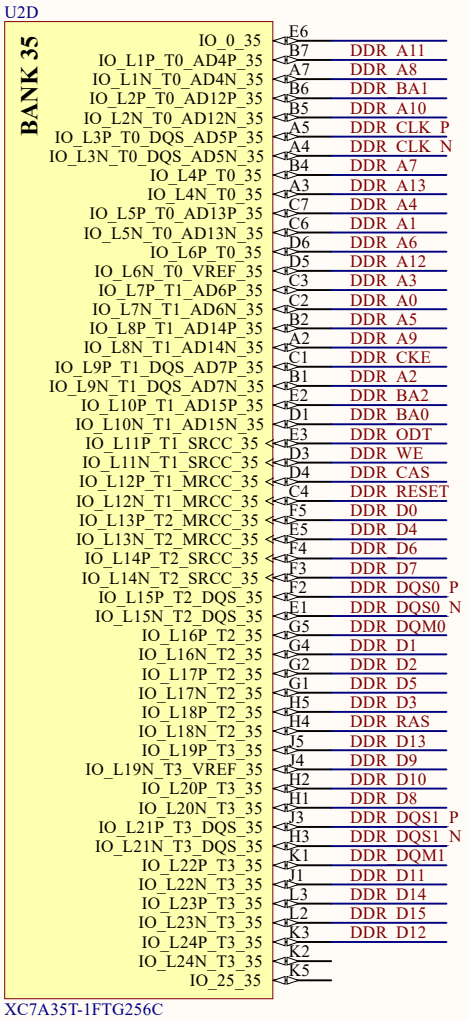
5V供电

Title		
Size: A4	Number	Revision
Date: 2018/3/24		Sheet of
File: G:\SX\..\2 XTAL JTAG FLASH (2).SchDoc		Drawn By:


U2A
BANK 14
IO_0_14
IO_L1P_T0_D00_MOSI_14
IO_L1N_T0_D01_DIN_14
IO_L2P_T0_D02_14
IO_L2N_T0_D03_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L4P_T0_D04_14
IO_L4N_T0_D05_14
IO_L5P_T0_D06_14
IO_L5N_T0_D07_14
IO_L6P_T0_FCS_B_14
IO_L6N_T0_D08_VREF_14
IO_L7P_T1_D09_14
IO_L7N_T1_D10_14
IO_L8P_T1_D11_14
IO_L8N_T1_D12_14
IO_L9P_T1_DQS_14
IO_L9N_T1_DQS_D13_14
IO_L10P_T1_D14_14
IO_L10N_T1_D15_14
IO_L11P_T1_SRCC_14
IO_L11N_T1_SRCC_14
IO_L12P_T1_MRCC_14
IO_L12N_T1_MRCC_14
IO_L13P_T2_MRCC_14
IO_L13N_T2_MRCC_14
IO_L14P_T2_SRCC_14
IO_L14N_T2_SRCC_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L16P_T2_CSI_B_14
IO_L16N_T2_A15_D31_14
IO_L17P_T2_A14_D30_14
IO_L17N_T2_A13_D29_14
IO_L18P_T2_A12_D28_14
IO_L18N_T2_A11_D27_14
IO_L19P_T3_A10_D26_14
IO_L19N_T3_A09_D25_VREF_14
IO_L20P_T3_A08_D24_14
IO_L20N_T3_A07_D23_14
IO_L21P_T3_DQS_14
IO_L21N_T3_DQS_A06_D22_14
IO_L22P_T3_A05_D21_14
IO_L22N_T3_A04_D20_14
IO_L23P_T3_A03_D19_14
IO_L23N_T3_A02_D18_14
IO_L24P_T3_A01_D17_14
IO_L24N_T3_A00_D16_14
IO_25_14
K12 D6R
J13 FPGA_DQ0
J14 FPGA_DQ1
K15 FPGA_DQ2
K16 FPGA_DQ3
L15
M15 BTN0
L14 BTN1
M14 BTN2
K13 BTN3
L13 reset
L12 FPGA_CSO
M12
M16 LED0
N16 LED1
P15 LED2
P16 LED3
R15 KEY0
R16 KEY1
T14 KEY2
T15 KEY3
N13 RX0
P13 TX0
N14 SYS_CLK
P14 JTAG_SRST
N11 TCK1
N12 D5B
P10 D5G
P11 D5R
R12 D6B
T12 B14_L15N
R13 B14_L16P
T13 B14_L16N
R10 B14_L17P
R11 B14_L17N
N9 B14_L18P
P9 B14_L18N
M6 B14_L19P
N6 B14_L19N
P8 B14_L20P
R8 B14_L20N
T7 B14_L21P
T8 B14_L21N
T9 B14_L22P
T10 B14_L22N
R5 CK_SCK
T5 CK_MISO
R6 CK_MOSI
R7 CK_SS
P6 D6G
arduino_digital
high speed
SPI
XC7A35T-1FTG256C
3V3
R49
NC
R50
1KΩ (1001) ±1%
GND
3V3
U2C
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
L5 D4G
L4 JTAG1_TRST
M4 JTAG1_SRST
M2 D4B
M1 TDO1
N3 TMS1
N2 TDI1
N1 USER_DQ0
P1 USER_DQ1
P4 USER_DQ2
P3 USER_DQ3
M5 USER_CSO
N4 USER_CCLK
R2 B34_L7P
R1 B34_L7N
R3 B34_L8P
T2 B34_L8N
T4 B34_L9P
T3 B34_L9N
P5 D4R
high speed
XC7A35T-1FTG256C
3V3
U2E
DXN_0
DXP_0
VREFN_0
VREFP_0
VN_0
VP_0
CFGBVS_0
PROGRAM_B_0
INIT_B_0
DONE_0
M2_0
M1_0
M0_0
CCLK_0
TMS_0
TCK_0
TDO_0
TDI_0
K7
K8
H7
J8
J7
H8
E7
L9
K10
H10 FPGA_DONE
M11 FPGA_M2
M10 FPGA_M1
M9 FPGA_M0
E8 FPGA_CCLK
M7 TMS
L7 TCK
N8 TDO
N7 TDI
GND
AGND
C1
1nF (102) 10% 50V
R13 XADC_VN
100Ω (1000) ±1%
R14 XADC_VP
100Ω (1000) ±1%
3V3
R15
4.7KΩ (4701) ±1%
R17
4.7KΩ (4701) ±1%
XC7A35T-1FTG256C
FPGA_config
3V3
3V3
3V3
R21
NC
R22
NC
R23
1KΩ (1001) ±1%
FPGA_M2
FPGA_M1
FPGA_M0
R25
1KΩ (1001) ±1%
R26
1KΩ (1001) ±1%
R24
NC
GND
GND
GND
AGND
FB1
600Ω ±25% 100MHz
GND
默认MASTER SPI x4
M[2：0]=001
Title
Size
A4
Number
Revision
Date: 2018/3/24
Sheet of
File: G:\SX\..\3_BANK1434conf.SchDoc
Drawn By:

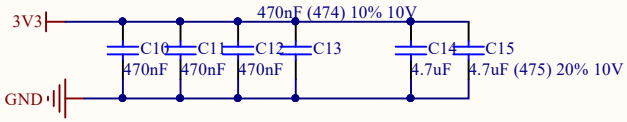


3V3

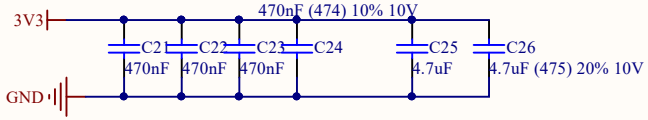


1V5

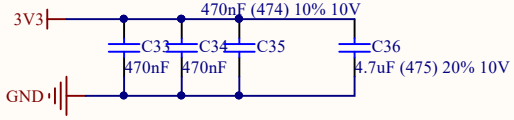
Title		
Size: A4	Number	Revision
Date: 2018/3/24		Sheet of
File: G:\SX\..\3_BANK1535.SchDoc		Drawn By:



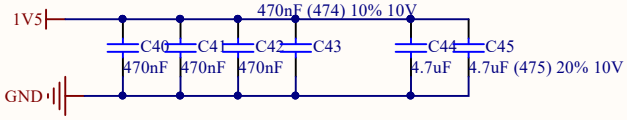
for VCCO_14



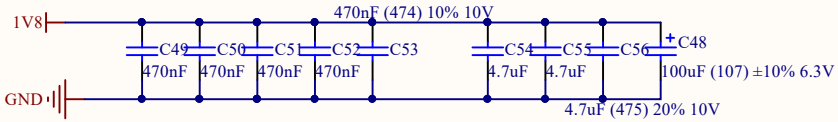
for VCCO_15



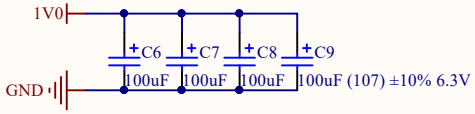
for VCCO_34

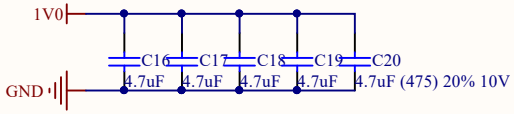


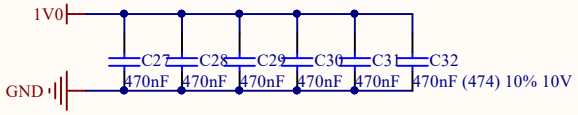
for VCCO_35



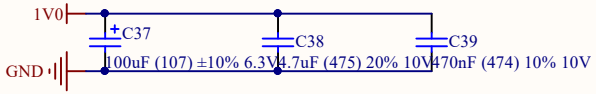
for VCCAUX&VCCBATT_0



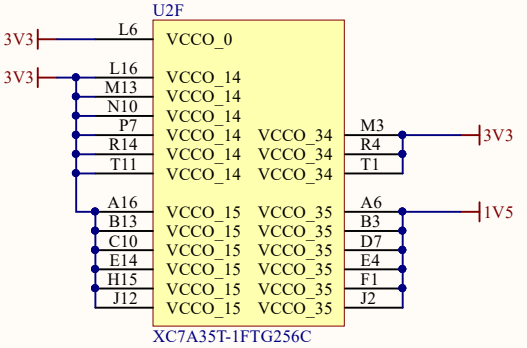


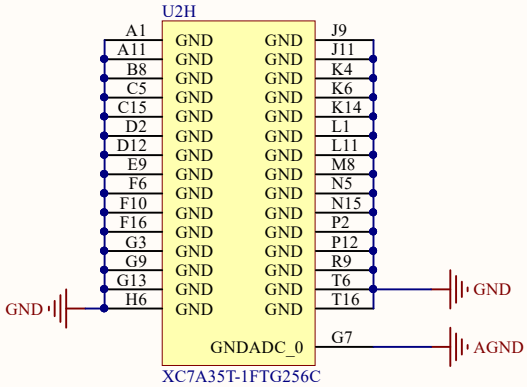


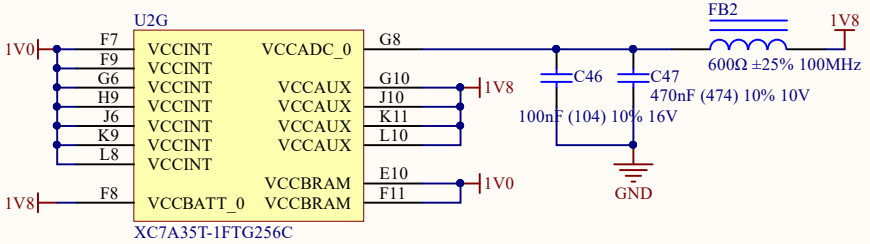
for VCCINT



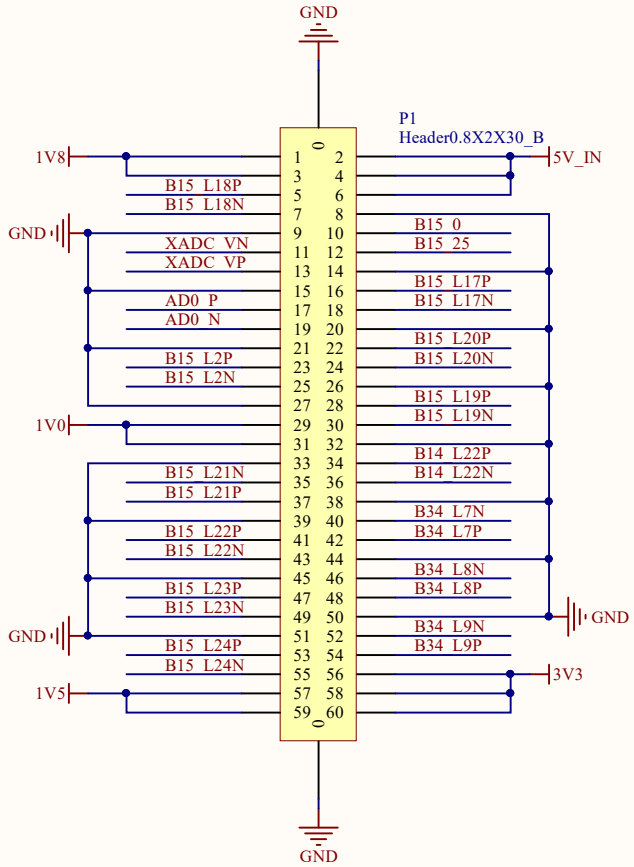
for VCCBRAM



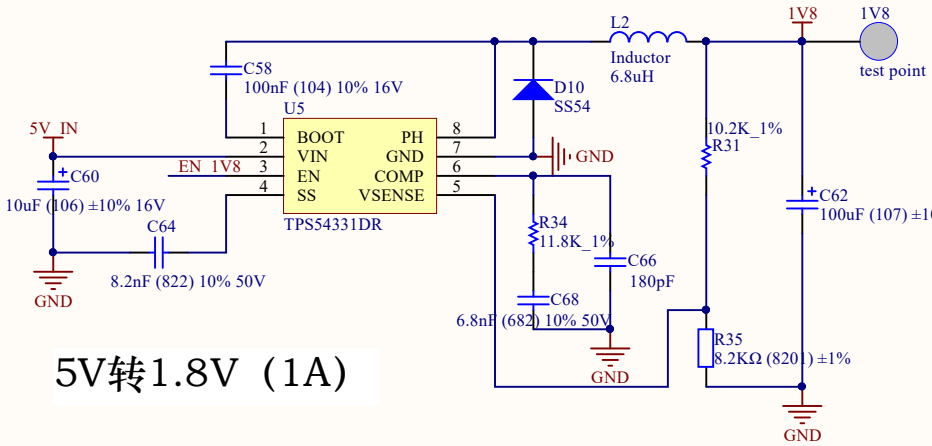




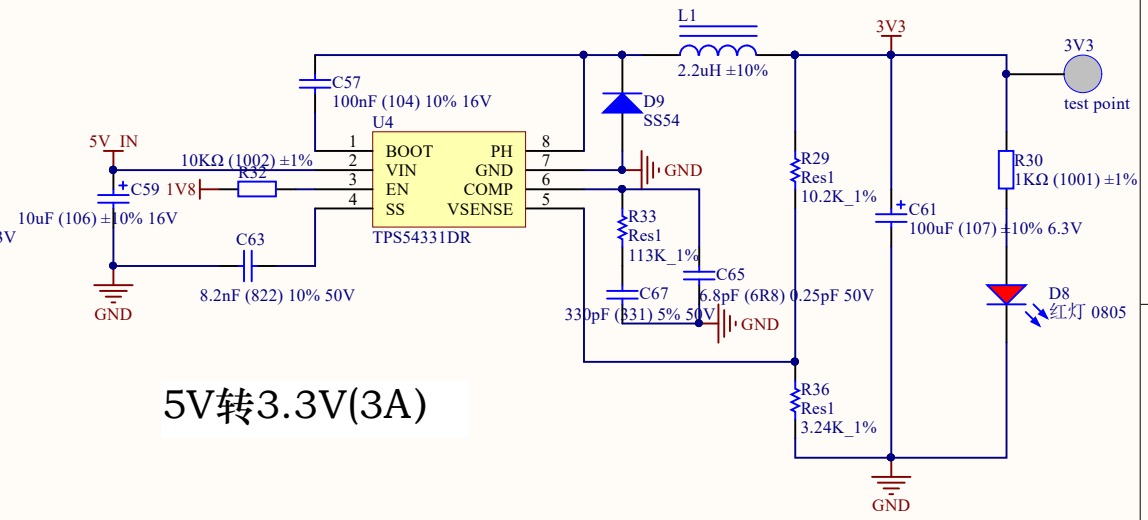
Title		
Size A4	Number	Revision
Date: 2018/3/24		Sheet of
File: G:\SX\..\4 FPGA PWR.SchDoc		Drawn By:



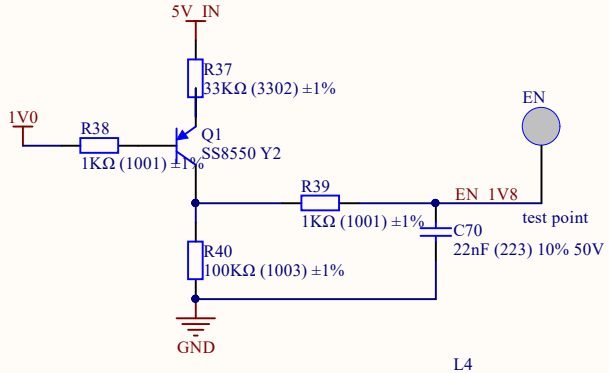
Title			
Size A4	Number		Revision
Date:	2018/3/24	Sheet of	
File:	G:\SX\..\5_HEADER (2).SchDoc	Drawn By:	

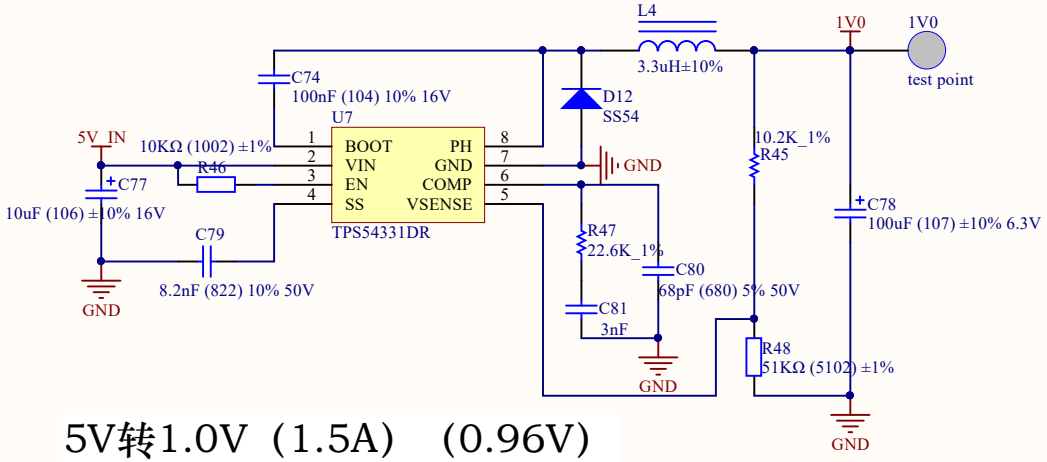


5V转1.8V（1A）

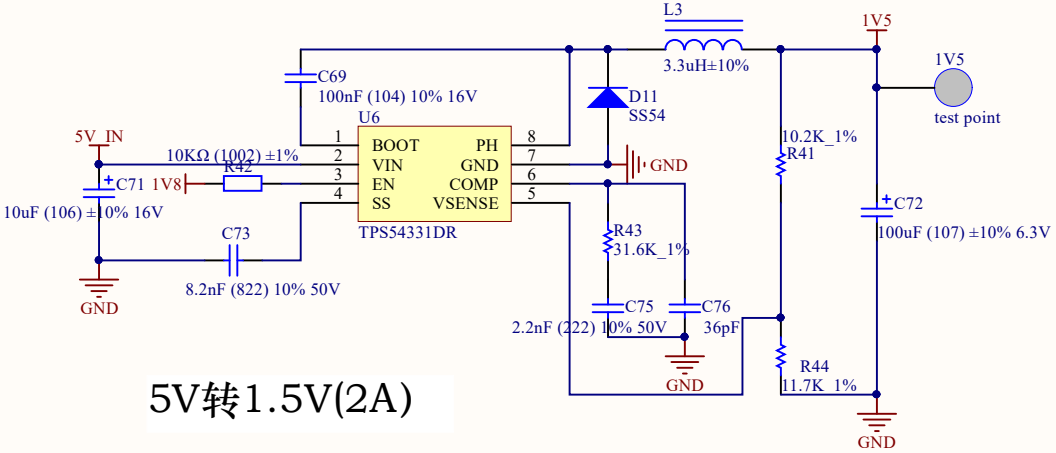


5V转3.3V(3A)



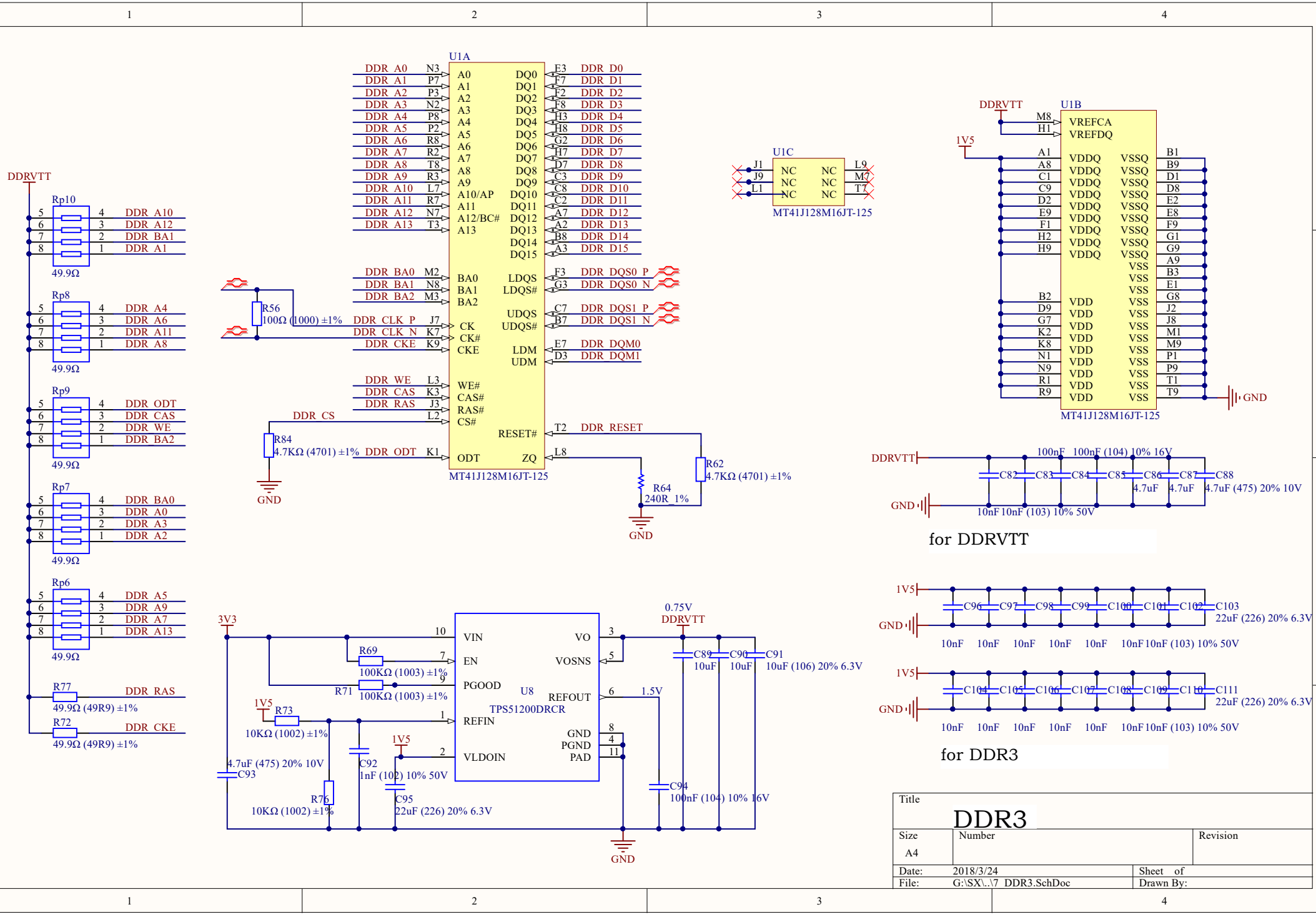


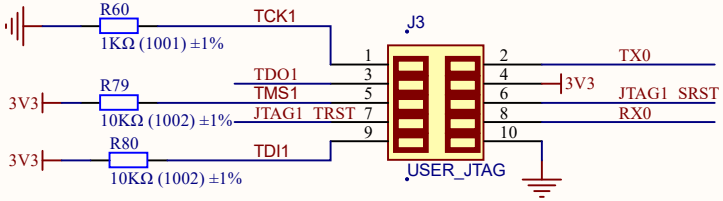
5V转1.0V（1.5A） (0.96V)



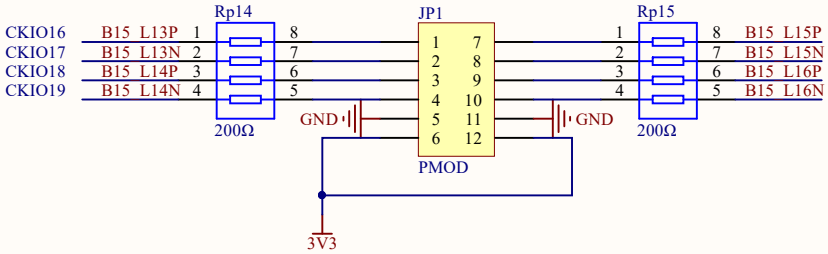
5V转1.5V(2A)

Title		
Size A4	Number	Revision
Date: 2018/3/24		Sheet of
File: G:\SX\..\6 POWER1.SchDoc		Drawn By:

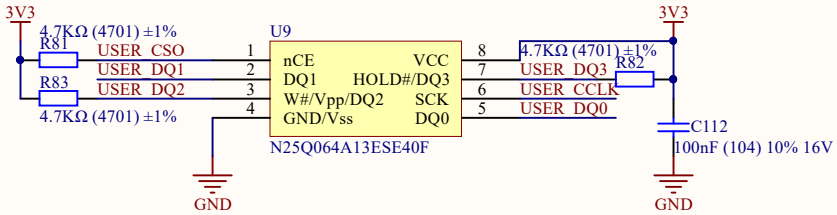

U1A
MT41J128M16JT-125
U1C
MT41J128M16JT-125
U1B
MT41J128M16JT-125
DDRVTT
1V5
GND
3V3
0.75V
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13
DDR_BA0
DDR_BA1
DDR_BA2
DDR_CLK_P
DDR_CLK_N
DDR_CKE
DDR_WE
DDR_CAS
DDR_RAS
DDR_CS
DDR_ODT
DDR_RESET
DDR_DQM0
DDR_DQM1
DDR_DQS0_P
DDR_DQS0_N
DDR_DQS1_P
DDR_DQS1_N
DDR_D0
DDR_D1
DDR_D2
DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D7
DDR_D8
DDR_D9
DDR_D10
DDR_D11
DDR_D12
DDR_D13
DDR_D14
DDR_D15
Rp10
Rp8
Rp9
Rp7
Rp6
49.9Ω
R56
100Ω (1000) ±1%
R84
4.7KΩ (4701) ±1%
R62
4.7KΩ (4701) ±1%
R64
240R_1%
R77
49.9Ω (49R9) ±1%
R72
49.9Ω (49R9) ±1%
for DDRVTT
for DDR3
U8
TPS51200DRCR
VIN
EN
PGOOD
REFIN
VLDOIN
VO
VOSNS
REFOUT
GND
PGND
PAD
R69
100KΩ (1003) ±1%
R71
100KΩ (1003) ±1%
R73
10KΩ (1002) ±1%
R76
10KΩ (1002) ±1%
C92
1nF (102) 10% 50V
C93
4.7uF (475) 20% 10V
C95
22uF (226) 20% 6.3V
C94
100nF (104) 10% 16V
C89
10uF
C90
10uF
C91
10uF (106) 20% 6.3V
1.5V
100nF (104) 10% 16V
4.7uF
4.7uF (475) 20% 10V
10nF (103) 10% 50V
22uF (226) 20% 6.3V
Title
DDR3
Size
A4
Number
Revision
Date:
2018/3/24
Sheet of
File:
G:\SX\..\7 DDR3.SchDoc
Drawn By:



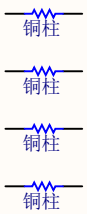
USER JTAG



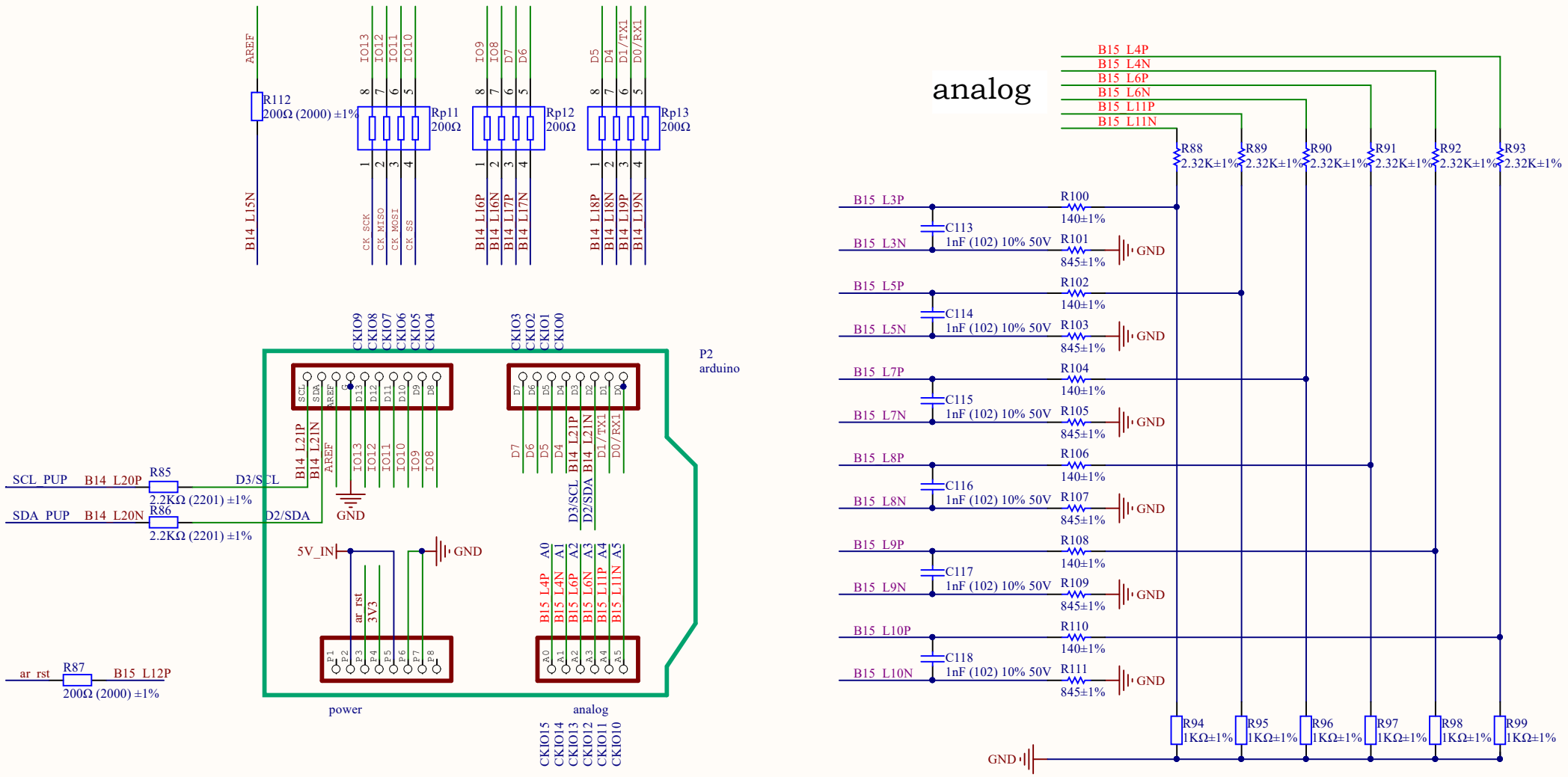
PMOD(塑高5.0)



USER FLASH



Title: 蜂鸟		
Size: A4	Number:	Revision:
Date: 2018/3/24		Sheet of
File: G:\SX\..\8_JTAG1_FLASH1_PMOD.SchDoc		Drawn By:



Title	arduino(塑高8.0)	
Size: A4	Number	Revision
Date: 2018/3/24		Sheet of
File: G:\SX\..\9 arduino.SchDoc		Drawn By: