

Shixin Wang

### Question #1

- How many arithmetic instructions are required by this algorithm?

In each iteration of the loop, there is one arithmetic instruction:  $\text{sum} += i$ . Since the loop runs  $N$  times, the total number of arithmetic instructions is  $N$ .

- How many memory accesses are required by this algorithm?

There are no memory accesses for accessing and using the loop index variable or updating the accumulator variable, as per the assumptions. Therefore, there are no memory accesses required by this algorithm.

- How many clocks are required by this algorithm?

Since 1 OP requires 5 clock cycles and each arithmetic instruction is considered as 1 OP, the total number of clocks required for arithmetic instructions is  $5N$ .

- What is the CPI (cycles per instruction) required by this algorithm?

The CPI (cycles per instruction) for this algorithm is 5, as each arithmetic instruction takes 5 clock cycles.

- What is the estimated execution time for this algorithm in seconds or fractions of seconds, not counting the print and any problem setup?

Given that the CPU clock is 1 GHz, the estimated execution time can be calculated by dividing the total number of clocks required by the CPU clock frequency:

$$\begin{aligned}\text{Estimated execution time} &= \text{Total clocks} / \text{CPU clock frequency} \\ &= (5N) / 1,000,000,000 \text{ seconds} = N / 200,000,000 \text{ seconds}\end{aligned}$$

## Question #2

- How many arithmetic instructions are required by this algorithm?

In each iteration of the loop, there is one arithmetic instruction:  $\text{sum} += A[i]$ . Since the loop runs  $N$  times, the total number of arithmetic instructions is  $N$ .

- How many memory accesses are required by this algorithm?

In each iteration of the loop, there is one memory access to read the value from the list  $A$ :  $A[i]$ . Since the loop runs  $N$  times, the total number of memory accesses to read the list  $A$  is  $N$ .

- How many clocks are required by this algorithm?

Since 1 OP requires 5 clock cycles and each arithmetic instruction is considered as 1 OP, the total number of clocks required for arithmetic instructions is  $5N$ .

In addition, 1 memory access requires 100 clock cycles. Therefore, the total number of clocks required for memory accesses is  $100N$ .

The overall number of clocks required by the algorithm is the sum of the clocks required for arithmetic instructions and memory accesses:  $5N + 100N = 105N$ .

- What is the CPI (cycles per instruction) required by this algorithm?

The CPI (cycles per instruction) for this algorithm can be calculated by dividing the total number of clocks required by the total number of arithmetic instructions:

$$\begin{aligned}\text{CPI} &= \text{Total clocks} / \text{Total arithmetic instructions} \\ &= (5N + 100N) / N = 105\end{aligned}$$

- What is the estimated execution time for this algorithm in seconds or fractions of seconds, not counting the print and any problem setup?

Given that the CPU clock is 1 GHz, the estimated execution time can be calculated by dividing the total number of clocks required by the CPU clock frequency:

$$\begin{aligned}\text{Estimated execution time} &= \text{Total clocks} / \text{CPU clock frequency} \\ &= (5N + 100N) / 1,000,000,000 \text{ seconds} \\ &= 21N / 200,000,000 \text{ seconds}\end{aligned}$$