实验六 系统编程实验

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十进制计数器

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

ENTITY wanglei IS   //实体 wanglei

 PORT(clr,clk: IN std_logic;     //输入端为clr(清零)和clk(时钟脉冲信号)
 bcd_q:buffer std_logic_vector(3 downto 0); //四位二进制数代表当前计数状态
 led:OUT std_logic_vector(6 DOWNTO 0)); //长为8的向量代表LED的显示状态

END wanglei;     //结束实体描述

ARCHITECTURE behavioral OF wanglei IS   //创建结构体behavioral
BEGIN

 process(CLR,CLK)   //进程进行
 begin

 IF clr='0' then    //如果有clr信号
   bcd_q <= (OTHERS => '0');    //四位全部置零
 ELSIF rising_edge(clk) THEN    //否则当出现时钟上升沿
   IF bcd_q < "1001" THEN   //判断当前状态是否小于9
     bcd_q <= bcd_q +'1';  //计数+1
   ELSE bcd_q <= (OTHERS => '0');   //否则置零
   END IF;  //结束if
 END IF;    //结束大if

 case bcd_q is   //列举bcd_q的状态，对应LED的发光方式
     when "0000"=>led<="1111110";   //计数为0
     when "0001"=>led<="0110000";   //计数为1
     when "0010"=>led<="1101101";   //计数为2
     when "0011"=>led<="1111001";   //计数为3
     when "0100"=>led<="0110011";   //计数为4
     when "0101"=>led<="1011011";   //计数为5
     when "0110"=>led<="1011111";   //计数为6
     when "0111"=>led<="1110000";   //计数为7
     when "1000"=>led<="1111111";   //计数为8
     when "1001"=>led<="1111011";   //计数为9
     WHEN OTHERS=>led<="-------";    //其他情况LED熄灭
 end case;

 end process;   //结束进程
END behavioral; //结束结构体behavioral
```