HIGH-VOLTAGE MIXED-SIGNAL IC

UC1609

65x192 STN Controller-Driver

MP Specifications **October 2, 2012**

ULTRACHIP

The Coolest LCD Driver, Ever!

Table of Content

INTRODUCTION 3
MAIN APPLICATIONS 3
FEATURE HIGHLIGHTS 3
ORDERING INFORMATION 4
BLOCK DIAGRAM 5
PIN DESCRIPTION 6
RECOMMENDED COG LAYOUT 8
CONTROL REGISTERS 9
COMMAND TABLE 11
COMMAND DESCRIPTION 12
LCD VOLTAGE SETTING 20
V_{LCD} QUICK REFERENCE 21
LCD DISPLAY CONTROLS 23
ITO LAYOUT AND LC SELECTION 24
HOST INTERFACE 26
DISPLAY DATA RAM (DDRAM) 34
RESET & POWER MANAGEMENT 36
MULTI-TIME PROGRAM (MTP) NV MEMORY 41
MTP OPERATION FOR LCM MAKERS 44
ESD CONSIDERATION 48
ABSOLUTE MAXIMUM RATINGS 49
SPECIFICATIONS 50
AC CHARACTERISTICS 51
PHYSICAL DIMENSIONS 57
ALIGNMENT MARK INFORMATION 58
PAD COORDINATES 59
TRAY INFORMATION 63
REVISION HISTORY 64

UC1609

Single-Chip, Ultra-Low Power
65COM by 192SEG
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1609c is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power column and row drivers, the IC contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, PDA, and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver supports 65x192 graphics STN LCD panels.
- Support both row ordered and column ordered display buffer RAM access.
- A software-readable ID pin to support configurable vender identification.
- Support both row-ordered and column-ordered display buffer RAM access.
- Support industry standard 8-bit parallel bus (8080 or 6800 mode), 4-wire and 3-wire serial buses (S8 and S9), and 2-wire I^2C serial interface.
- Ultra-low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display, Bias Ratio and Frame Rate allow many flexible power management options.
- Software programmable frame rates at 76, 95, 132 and 168 Hz.
- Four software programmable temperature compensation coefficients.
- 7-x internal charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.
- On-chip Power-ON Reset makes RST pin optional.
- Very low pin count (10-pin) allows exceptional image quality in COG format on conventional ITO glass.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- V_{DD} (digital) range (Typ.): 1.8V ~ 3.3V
  V_{DD} (analog) range (Typ.): 2.7V ~ 3.3V
  V_{LCD} range: 4.8V ~ 11.5V
- Available in gold bump dies
- COM/SEG bump information
  Bump pitch: 27.6 μM
  Bump gap: 12 μM
  Bump surface: 1560 $μM^2$

ORDERING INFORMATION

Part Number	MTP	I^2C	Description
UC1609cGAA	Yes	Yes	Gold Bumped Die

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I^2C

The implementation of I^2C is already included and tested in all silicon.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

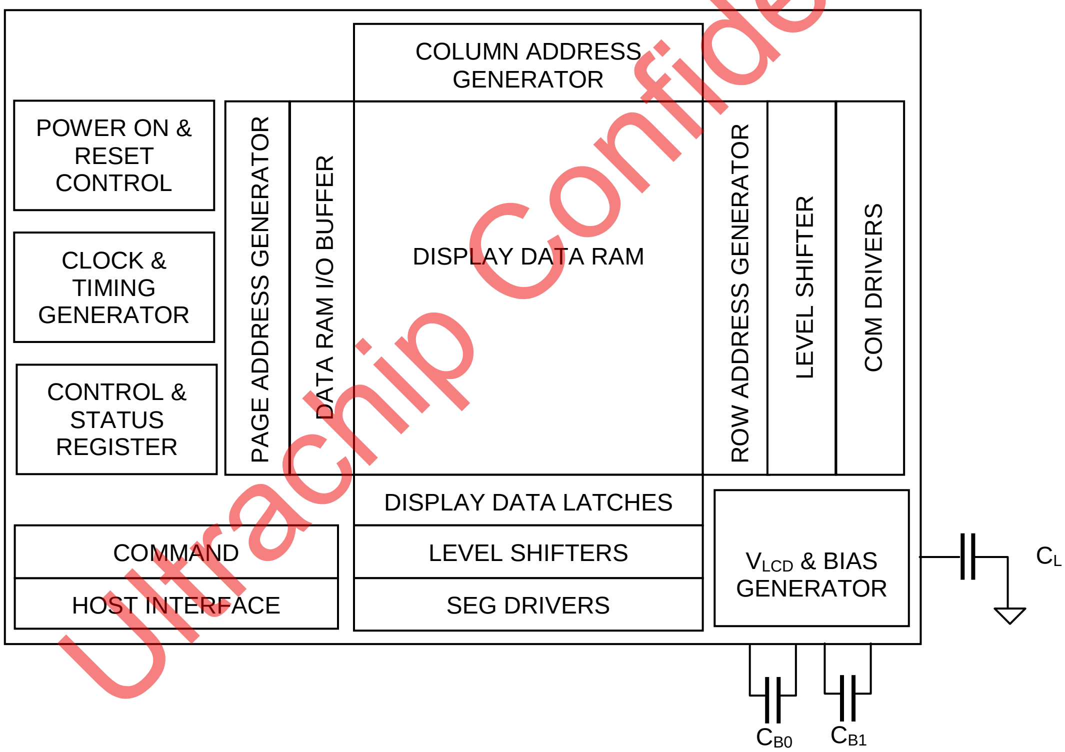
UltraChip believes the information contained in this document to be accurate and reliable. However, it is subject to change without notice. No responsibility is assumed by UltraChip for its use, nor for infringement of patents or other rights of third parties. No part of this publication may be reproduced, or transmitted in any form or by any means without the prior consent of UltraChip Inc. UltraChip's terms and conditions of sale apply at all times.

CONTACT DETAILS

UltraChip Inc. (Headquarter)
4F, No. 618, Recom Road,
Neihu District, Taipei 114,
Taiwan, R. O. C.

Tel: +886 (2) 8797-8947
Fax: +886 (2) 8797-8910
Sales e-mail: sales@ultrachip.com
Web site: http://www.ultrachip.com

BLOCK DIAGRAM

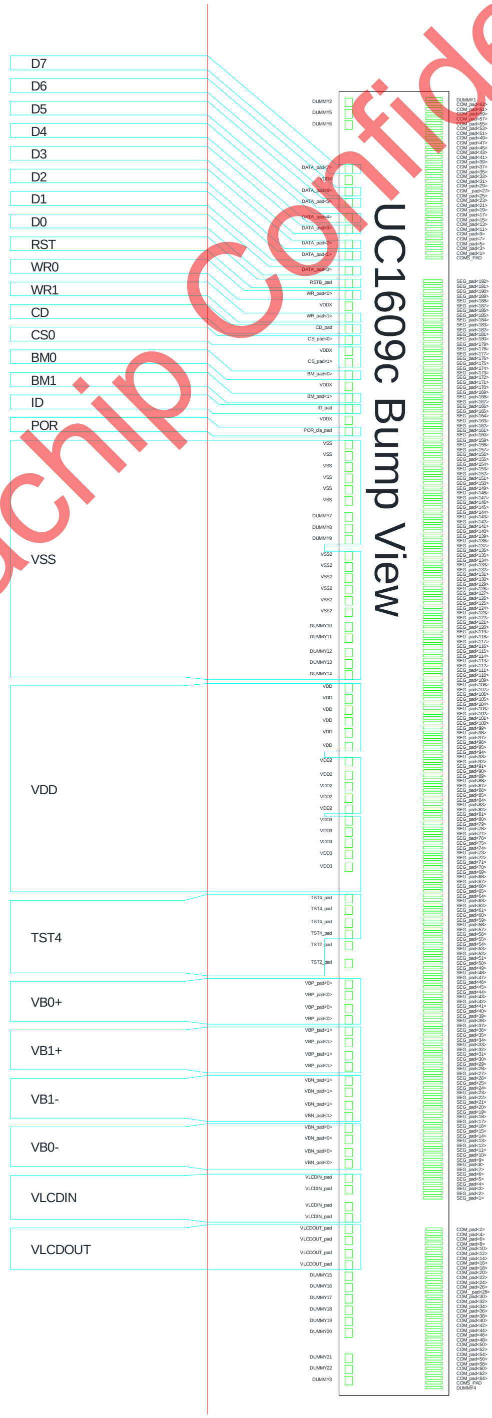


PIN DESCRIPTION

<table>
<tr><th>Pin Name
(Pad Name)</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">MAIN POWER SUPPLY</td></tr>
<tr><td>V_{DD}
V_{DD2}
V_{DD3}</td><td>PWR</td><td>6
5
5</td><td>V_{DD} supplies for Display Data RAM and digital logic, V_{DD2} supplies for V_{LCD} and V_D generator, V_{DD3} supplies for V_{BIAS} and other analog circuits.
V_{DD2}/V_{DD3} should be connected to the same power source. But V_{DD} can be connected to a source voltage no higher than V_{DD2}/V_{DD3}.
Please maintain the following relationship:
$V_{DD}+1.3V \geq V_{DD2/3} \geq V_{DD}$
ITO trace resistance needs to be minimized for V_{DD2}/V_{DD3}.</td></tr>
<tr><td>V_{SS}
V_{SS2}</td><td>GND</td><td>6
6</td><td>Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. In COG applications, minimize the ITO resistance for both V_{SS} and V_{SS2}.</td></tr>
<tr><td colspan="4">LCD POWER SUPPLY & VOLTAGE CONTROL</td></tr>
<tr><td>V_{B0+}
(VBP_pad<0>)
V_{B0-}
(VBN_pad<0>)
V_{B1+}
(VBP_pad<1>)
V_{B1-}
(VBN_pad<1>)</td><td>PWR</td><td>4
4
4
4</td><td>LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. See the “LCD Voltage Setting” section for more details.
In COG application, the resistance of these ITO traces directly affects the SEG driving strength of the resulting LCD module. Minimize these trace resistance is critical in achieving high quality image.</td></tr>
<tr><td>V_{LCDIN}
(VLCDIN_pad)
V_{LCDOUT}
(VLCDOUT_pad)</td><td>PWR</td><td>4
4</td><td>Main LCD Power Supply. When internal V_{LCD} is used, connect these pins together. When external V_{LCD} source is used, connect external V_{LCD} source to V_{LCDIN} pins and leave V_{LCDOUT} open.
Capacitor C_L should be connected between V_{LCD} and V_{SS}. In COG applications, keep the ITO trace resistance around 70 Ω .</td></tr>
<tr><td colspan="4">• Recommended capacitor values:
C_B: 2.2µF/5V or 300x(LCD load capacitance), whichever is higher.
C_L: 330nF/16V is appropriate for most applications.</td></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1
(BM_pad<0>
~ <1>)</td><td>I</td><td>1
1</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and D[7] by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>D[7]</th><th>Mode</th><th>Remark</th></tr>
<tr><td>11</td><td>Data</td><td>6800/8-bit</td><td></td></tr>
<tr><td>10</td><td>Data</td><td>8080/8-bit</td><td></td></tr>
<tr><td>00</td><td>--</td><td>4-wire SPI w/ 8-bit token</td><td>(S8: conventional)</td></tr>
<tr><td>01</td><td>0</td><td>3-wire SPI w/ 9-bit token</td><td>(S9: conventional)</td></tr>
<tr><td>01</td><td>1</td><td>2-wire serial (I^2C)</td><td></td></tr>
</table></td></tr>
<tr><td>CS1/A3
CS0/A2
(CS_pad<0>~<1>)</td><td>I</td><td>1
1</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[7:0] will be of high impedance.
In I^2C mode, these two pins specifies bits 3~2 of UC1609c’ device address (A[3:2]).</td></tr>
<tr><td>RST
(RSTB_pad)</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1609c has built-in Power-On Reset, the RST pin is not required for proper chip operation.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
</table>

<table>
<tr><th>Pin Name
(Pad Name)</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td>CD
(CD_pad)</td><td>I</td><td>1</td><td>Select Control data or Display data for read/write operation. In S9, CD pin is not used. Connect CD to V_{SS} when not used.
"L": Control data "H": Display data</td></tr>
<tr><td>ID
(ID_pad)</td><td>I</td><td>1</td><td>ID may be used for production identification.
Connect ID to V_{DD} for "H" or V_{SS} for "L".</td></tr>
<tr><td>WR0
WR1
(WR_pad<0>~<1>)</td><td>I</td><td>1
1</td><td>WR [1:0] controls the read/write operation of the host interface. See Host Interface section for details.
In parallel mode, the meaning of WR[1:0] depends on which interface it is in, 6800 or 8080 mode. In serial interface modes, these two pins are not used, Connect them to V_{SS}.</td></tr>
<tr><td>D7~D0
(DATA_pad<7>
~ <0>)</td><td>I/O</td><td>8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[5:3] to SDA.
<table>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>8-bit (BM=1x)</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>s8 (BM=00)</td><td>--</td><td>--</td><td>SDA</td><td>SDA</td><td>SDA</td><td>--</td><td>--</td><td>SCK</td></tr>
<tr><td>S9 (BM=01)</td><td>0</td><td>--</td><td>SDA</td><td>SDA</td><td>SDA</td><td>--</td><td>--</td><td>SCK</td></tr>
<tr><td>I^2C (BM=01)</td><td>1</td><td>--</td><td>SDA</td><td>SDA</td><td>SDA</td><td>--</td><td>--</td><td>SCK</td></tr>
</table>
For better drive ability, connect D[5:3] together.
Always connect unused pins to either V_{SS} or V_{DD}.</td></tr>
<tr><th colspan="4">HIGH VOLTAGE LCD DRIVER OUTPUT</th></tr>
<tr><td>SEG1~192
(SEG_pad<1>
~ <192>)</td><td>HV</td><td>192</td><td>SEG (column) driver outputs. Support up to 192 pixels.
Leave unused SEG drivers open-circuit.</td></tr>
<tr><td>COM1~64
(COM_pad<1>
~ <64>)</td><td>HV</td><td>64</td><td>COM (row) driver outputs. Support up to 64 rows.
When designing LCM, always start from COM1. If the LCM has N pixel rows and N is less than 64, set CEN to be N-1, and leave COM drivers [N+1 ~ 64] open-circuit.</td></tr>
<tr><td>CIC
(COMS_pad)</td><td>HV</td><td>2</td><td>Icon driver outputs. Leave it open if not used.</td></tr>
<tr><th colspan="4">MISC. PINS</th></tr>
<tr><td>V_{DDX}</td><td></td><td>5</td><td>Auxiliary V_{DD}. This pin is connected to the main V_{DD} bus within the IC. It's provided to facilitate chip configurations in COG application.
There's no need to connect V_{DDX} to main V_{DD} externally and it should <u>NOT</u> be used to provide V_{DD} power to the chip.</td></tr>
<tr><td>TST4
(TST4_pad)</td><td>I</td><td>4</td><td>TST4 is used as one of the high voltage power supply for MTP programming operation.
For COG designs, please wire out TST4 with trace resistance between 30~50 Ω.</td></tr>
<tr><td>TST2
(TST2_pad)</td><td>I/O</td><td>2</td><td>Test I/O pins. Leave these pins open during normal use.</td></tr>
<tr><td>POR
(POR_dis_pad)</td><td></td><td>1</td><td>Power-ON Reset control.
Connect the POR pin to V_{DD} for "H"; to Vss for "L" to control the POR register.
"L": Power-ON Reset Enable.
"H": Power-ON Reset Disabled.</td></tr>
<tr><td>Dummy
(Dummy1~22)</td><td></td><td>22</td><td>Dummy pins are NOT connected inside the IC.</td></tr>
<tr><td colspan="4">Note: Several control registers will specify "0 based index" for COM and SEG electrodes. In those situations, COM<u>x</u> or SEG<u>x</u> will correspond to index <u>x</u>-1, and the value range for those index register will be 0~63 for COM and 0~191 for SEG.</td></tr>
</table>

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The operation condition, V_{DD}=1.8V (typical), should be satisfied under all operating conditions. UC1609c' peak current (I_{DD}) can be up to ~15mA during high speed data-write to UC1609c' on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD} and V_{SS} ITO trances in COG modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop to below 1.7V and cause the IC to malfunction.

CONTROL REGISTERS

UC1609c contains registers, which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, Command Table and Command Description.

Name: The Symbolic reference of the register. Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after Power-Up-Reset and System-Reset.

Name	Bits	Default	Description
SL	6	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (64). Setting SL outside of this range causes undefined effect on the displayed image.
CA	8	00H	Display Data RAM Column Address. Value range is **0** ~ 191. (Used in Host to Display Data RAM access)
PA	4	0H	Display Data Page Row Address. Value range is **0** ~ 8. (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_D. 00b: 6 01b: 7 10b: 8 **11b: 9**
TC	2	0H	Temperature Compensation (per ^{o}C) **00b: -0.00%** 01b: -0.05% 10b: -0.10% 11b: -0.15%
PM	8	49H	Electronic Potentiometer to fine tune V_D and V_{LCD}
PMO	6	00H	PM offset.
PC	3	6H	Power Control. PC[1:0]: low pump charge current select 00b: 0.6mA 01b: 1.0mA **10b: 1.4mA** 11b: 2.3mA PC[2]: to program the build-in charge pump stages 0b: External V_{LCD} **1b: Internal V_{LCD} (7x charge pump)**
AC	3	1H	Address Control: AC[0]: WA: Automatic column/row Wrap Around (Default **1: ON**) AC[1]: Auto-Increment order **0: Column (CA) first** 1: Page (PA) first AC[2]: RID: RA (row address) auto increment direction (**L:+1** H:-1)
DC	3	0H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**)
LC	6	08H	LCD Control: LC[0]: Reserved (always set to **0**) LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: **0:OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **0:OFF**) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 76 fps **01b: 95 fps** 10b: 132 fps 11b: 168 fps LC[5] : Partial Display. **0b: Disabled**. Mux-Rate = CEN+1 (DST, DEN not used) 1b: Enabled. Mux-Rate = DEN-DST+1

Name	Bits	Default	Description
CEN DST DEN	6 6 6	3FH 00H 3FH	COM scanning end (last COM with full line cycle, 0-based index) Display start (first COM with active scan pulse, 0-based index) Display end (last COM with active scan pulse, 0-based index) Please maintain the following relationship: CEN = "the actual number of pixel rows on the LCD" – 1 CEN ⩾ DEN ⩾ DST+ 9
MTPC	5	00H	MTP Programming Control: MTPC[2:0] : MTP command **000 : Idle** 001 : Read 010 : Erase 011 : Program 1XX : For UltraChip debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. **0: Ignore** 1: Use
MTPM	6	00H	MTP Write Mask. For each bit, Bit =1: program, Bit=0: no action.
APC		N/A	Advanced Program Control. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
ID	1	PIN	Access the connected status of ID pins.
POR	1	PIN	Power-ON Reset control. Controlled by the POR pin. "L": Power-ON Reset Enable. "H": Power-ON Reset Disabled.

COMMAND TABLE

The following is a list of host commands supported by UC1609c

C/D : 0 / 1 – Control / Data W/R : 0 / 1 – Write / Read Cycle D7~D0 : # Useful Data bits, – Don't Care

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	ID	MX	MY	WA	DE	WS	MD	MS	Get Status	N/A
				VER	POR	#	#	#	#	#	#	PMO[5:0]	
4.	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA [3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA [7:4]	0
5.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6.	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	110b
7.	Set Adv. Program Control	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0],	N/A
	(double-byte command)			#	#	#	#	#	#	#	#	R = 0~3	
8.	Set Scroll Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
9.	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
10.	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	49H
	(double-byte command)			#	#	#	#	#	#	#	#		
11.	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[5]	0b
12.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13.	Set Frame Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	01b
14.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
15.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
16.	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
17.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	0	Set LC[2:1]	00b
18.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
19.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
20.	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only.	N/A
	(double-byte command)			#	#	#	#	#	#	#	#	Do not use.	
21.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 9
22.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[5:0]	63D
				--	--	#	#	#	#	#	#		
23.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[5:0]	0
				--	--	#	#	#	#	#	#		
24.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[5:0]	63D
				--	--	#	#	#	#	#	#		
25.	Set MTP Operation Control	0	0	1	1	1	1	1	0	0	0	Set MTPC[4:0]	00H
				--	--	--	#	#	#	#	#		
26.	Set MTP Write Mask	0	0	1	1	1	1	1	0	0	1	Set MTPM[5:0]	0
				--	--	#	#	#	#	#	#		
27.	Set V_{MTP1} Potentiometer	0	0	1	1	1	1	0	1	0	0	Set VMTP1[7:0]	N/A
				#	#	#	#	#	#	#	#		
28.	Set V_{MTP2} Potentiometer	0	0	1	1	1	1	0	1	0	1	Set VMTP2[7:0]	N/A
				#	#	#	#	#	#	#	#		
29.	Set MTP Write Timer	0	0	1	1	1	1	0	1	1	0	Set MTPWT[7:0]	N/A
				#	#	#	#	#	#	#	#		
30.	Set MTP Read Timer	0	0	1	1	1	1	0	1	1	1	Set MTPRT[7:0]	N/A
				#	#	#	#	#	#	#	#		
Serial Read Command (Enabled only in S8/S9 mode)													
31.	Get Status	0	0	1	1	1	1	1	1	1	0	Get Status	N/A
		0	1	ID	MX	MY	WA	DE	WS	MD	MS	PMO[5:0]	
				VER	POR	#	#	#	#	#	#		
32.	Read Data	0	0	1	1	1	1	1	1	1	1		FFH
		1	1	#	#	#	#	#	#	#	#		

Any bit pattern other than those listed above may result in NOP (No Operation).

COMMAND DESCRIPTION

1. Write Data Byte to Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data write to SRAM							

2. Read Data Byte from Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data read from SRAM							

Write/Read Data Byte (Command 1,2) access Display Data RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increase or decrease automatically after each bus cycle, depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of the page, and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches the end of the page, CA will be reset to 0 and PA will increase or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM, PA will be wrapped around to the other end of RAM and continue.

3. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	ID	MX	MY	WA	DE	WS	MD	MS
	0	1	VER	POR	PMO5	PMO4	PMO3	PMO2	PMO1	PMO0

Status1 definitions:

ID: Provide access to ID pins connection status.

MX: Status of register LC[1], mirror X.

MY: Status of register LC[2], mirror Y.

WA: Status of register AC[0]. Automatic column/row wrap around.

DE: Display Enable flag. DE=1 when display is enabled.

WS: MTP Operation succeeded

MD: MTP Option (1 for MTP version, 0 for non-MTP version)

MS: MTP action status

Status2 definitions:

Ver: IC Version, **0**~ 1.

POR: Power-ON Reset control.

PMO[5:0]: PM offset value. Default: **00H**

4. Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	**0**	**0**	**0**	**1**	CA7	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA value range: **0**~191

5. Set Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b= -0.00%/ ^{o}C 01b= -0.05%/ ^{o}C 10b= -0.10%/ ^{o}C 11b= -0.15%/^{o}C

6. Set Power Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Power Control PC[2:0]	0	0	**0**	**0**	**1**	**0**	**1**	PC2	PC1	PC0

PC[1:0] : to select low-pump charge current
00b: 0.6mA 01b: 1.0mA **10b: 1.4mA** 11b: 2.3mA

Set PC[2] : to program the build-in charge pump stages.
0b: External V_{LCD} **1b: Internal V_{LCD} (7x charge pump)**

7. Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control APC[R][7:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	R	R
(Double-byte command)	0	0	APC7	APC6	APC5	APC4	APC3	APC2	APC1	APC0

For UltraChip only. Please Do <u>*NOT*</u> use.

8. Set Scroll Line

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line SL[5:0]	0	0	**0**	**1**	SL5	SL4	SL3	SL2	SL1	SL0

Set the scroll line number.

Scroll line setting will scroll the displayed image up by *SL* rows. Icon output CIC will not be affected by `Set Scroll Line` command.

Image row 0	row 0
:	:
Image row N-1	:
Image row N	
:	
:	
Image row 63	row 63

SL=0

Image row N	row 0
:	:
:	:
Image row 63	
Image row 0	
:	
Image row N-1	row 63

SL=N

9. Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address PA[3:0]	0	0	**1**	**0**	**1**	**1**	PA3	PA2	PA1	PA0

Set the SRAM page address before write/read memory from host interface. Each page of SRAM corresponds to 8 COM lines on LCD panel, except for the last page. The last page corresponds to the icon output CIC.

Possible value = **0**~8.

10. Set V_{BIAS} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer PM [7:0]	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section `LCD Voltage Setting` for more detail.

Effective range: 0 ~ 255 (Default: **49H**)

11. Set Partial Display Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [5]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**0**	LC5

This command is used to enable partial display function.

LC[5] : **0b: Disable Partial Display**, Mux-Rate = CEN+1 (DST, DEN not used.)
1b: Enable Partial Display, Mux-Rate = DEN-DST+1

12. Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control. It controls the auto-increment behavior of CA and PA.

AC[0] – WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and CA or PA will increase by one.

AC[1] – Auto-Increment order
0 : column (CA) increasing (+1) first until CA reach CA boundary, then PA will increase by (+/-1).
1 : page (PA) increasing (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

AC[2] – PID, page address (PA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether page address will be adjusted by +1 or -1.

13. Set Frame Rate

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Frame Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [3] for frame rate setting

00b: 76 fps **01b: 95 fps** 10b: 132 fps 11b: 168 fps
(fps: frame-per-second)

14. Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM. (Default: **0**)

15. Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM. (Default: **0**)

16. Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	DC2

This command is for programming register DC[2]. When DC[2] is set to 1, UC1609c will first exit from sleep mode, restore the power and then turn on COM drivers and SEG drivers. (Default: **0**)

17. Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Control LC[2:1]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	**0**

Set LC[2:1] for COM (row) mirror (MY), SEG (column) mirror (MX). (Default: **00b**)

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 63-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

18. System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset.

Control register values will be reset to their default values. Data store in RAM will not be affected.

19. NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

20. Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(Double byte command)	0	0	For test only							

This command is used for UltraChip production testing. Please do <u>*NOT*</u> use.

21. Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:

00b= 6   01b= 7   10b= 8   **11b= 9**

22. Set COM End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN [5:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	**-**	**-**	*CEN* register parameter					

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 64 pixel rows, the LCM designer should set CEN to $N-1$ (where N is the number of pixel rows) and use COM1 through COM-N as COM driver electrodes. (Default: **63**)

23. Set Partial Display Start

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST [5:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(Double-byte command)	0	0	**-**	**-**	*DST* register parameter					

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

24. Set Partial Display End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN [5:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(Double-byte command)	0	0	**-**	**-**	*DEN* register parameter					

This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

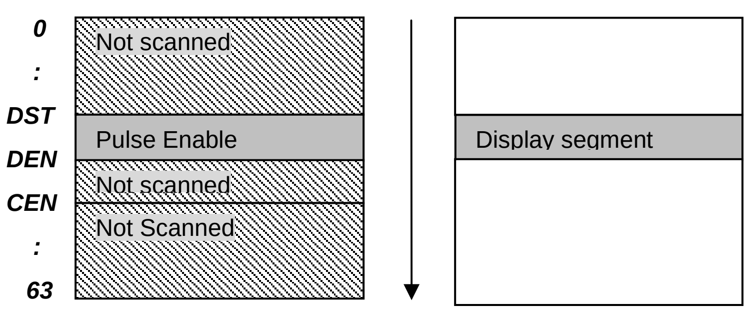
When LC[5]=1b, the Mux-Rate is narrowed down to DEN – DST + 1. When MUX rate is reduced, reduce the frame rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be reduced.

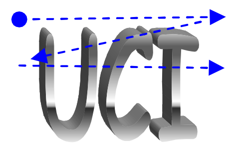
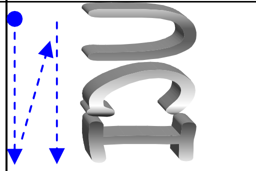
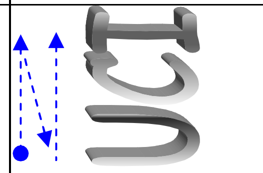
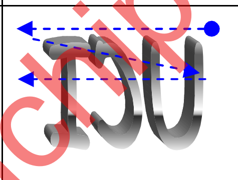
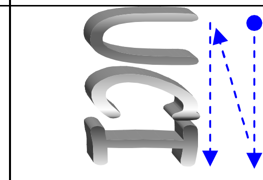
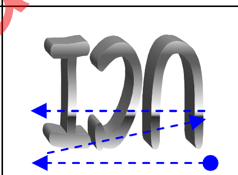
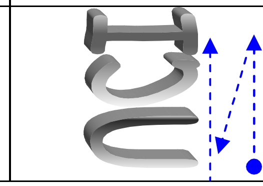
For minimum power consumption, set LC[5]=1b, set (DST, DEN, CEN) to minimize Mux rate, use slowest frame rate which satisfies the flicker requirement, set PC[0]=0b, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement. When Mux-Rate is under 16, it is recommended to set BR=6 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.

Keep CEN ⩾ DEN ⩾ DST+ 9

Scan Method **Display Result:**



Display Data Direction	Function Setting			Image in DDRAM (Physical origin: upper left corner)	Display Data Direction	Function Setting			Image in DDRAM (Physical origin: upper left corner)
	AIO AC[1]	MX LC[1]	RID AC[2]			AIO AC[1]	MX LC[1]	RID AC[2]	
Normal	0	0	0		X-Y Exchange	1	0	0	
Y-mirror	0	0	1		X-Y Exchange Y-mirror	1	0	1	
X-mirror	0	1	0		X-Y Exchange X-mirror	1	1	0	
X-mirror Y-mirror	0	1	1		X-Y Exchange X-mirror Y-mirror	1	1	1	

25. Set MTP Operation Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC [4:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**
	0	0	**-**	**-**	**-**	MTPC4	MTPC3	MTPC2	MTPC1	MTPC0

This command is for MTP operation control: (MTPC[4:0] : default: **D0H**)

MTPC[2:0] : MTP command
000 : Sleep 001 : MTP Read 010 : MTP Erase 011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (set H to active MTP value)

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

26. Set MTP Write Mask

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM [5:0]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**
(Double-byte command)	0	0	**-**	**-**	MTPM[5:0]					

This command enables Write to each of the individual MTP bits. When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to “1”. MTPM[x]=0 means no Write action for x-th bit. And the content of this bit will not change.

The amount of “programming current” increases with the number of 1’s in MTPM. If the “programming current” appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1’s evenly into these cycles.

MTPM[5:0] : Set PMO value   (Default: **00H**)

27. Set V_{MTP1} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set VMTP1 [7:0]	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
(Double-byte command)	0	0	VMTP1[7:0]							

This command is for fine tuning V_{OPT1} setting (with BR=00).

28. Set V_{MTP2} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set VMTP2 [7:0]	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
(Double-byte command)	0	0	VMTP2[7:0]							

This command is for fine tuning V_{MTP2} setting (with BR=11).

29. Set MTP Write Timer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPWT [7:0]	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
(Double-byte command)	0	0	MTPWT[7:0]							

This command is only valid when MTPC[3]=1.

30. Set MTP Read Timer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPRT [7:0]	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
(Double-byte command)	0	0	MTPRT[7:0]							

This command is only valid when MTPC[3]=1.

Serial Read Command (Enable only in S8/S9 mode):

31. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
	0	1	ID	MX	MY	WA	DE	WS	MD	MS
	0	1	VER	POR	PMO5	PMO4	PMO3	PMO2	PMO1	PMO0

See command 3.

32. Read Data Byte from Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data (double-byte command)	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	1	1	#	#	#	#	#	#	#	#

See command 2 for more information.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1609c via registers CEN, DST, DEN, and partial display control flags LC[5].

Combined with low power partial display mode and a low bias ratio of 6, UC1609c can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_D, i.e.

$$BR = V_{LCD}/V_D,$$

where

$V_D = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

UC1609c supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	6	7	8	**9**

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	**–0.00**	–0.05	–0.10	–0.15

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[2].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and *TC* (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in °C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

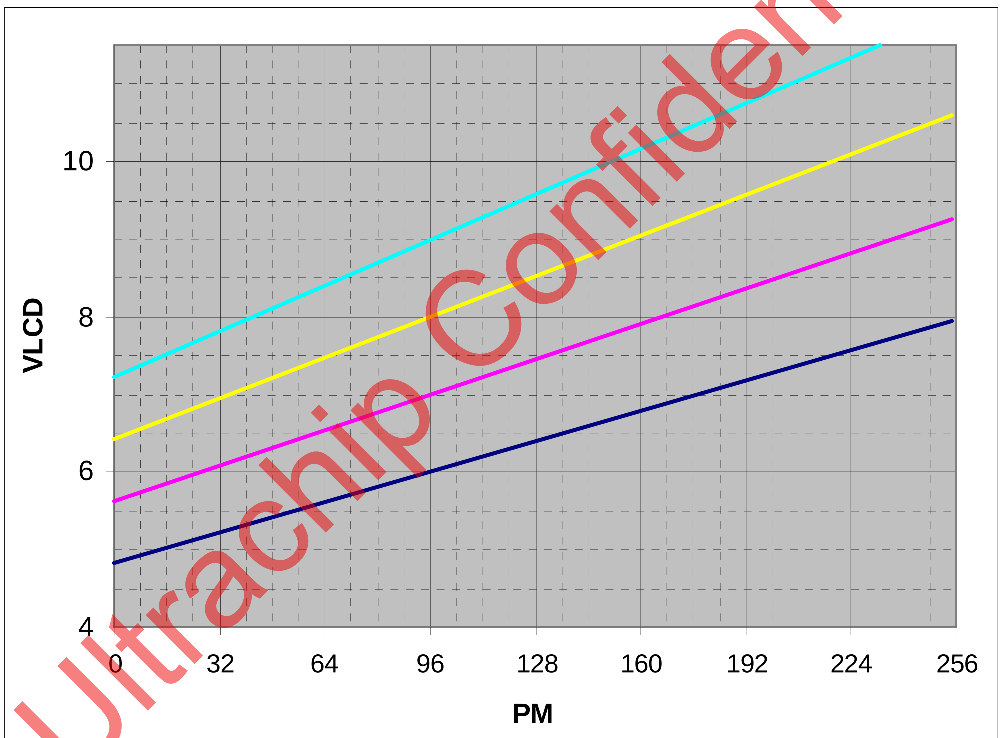
Black-and-white STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best result, software based approach for V_{LCD} adjustment or MTP is the recommended method for V_{LCD} fine-tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1609c is designed to handle LCD panels with loading up to ~24nF using 20-Ω/Sq ITO glass with $V_{DD2/3} \geqslant 2.6V$. For larger LCD panels, use lower resistance ITO glass packaging.

V_{LCD} QUICK REFERENCE



V_{LCD} Programming Curve.

BR	C_{V0} (V)	C_{PM} (mV)	PM	V_{LCD} Range (V)
6	4.821	12.266	0	4.82
			255	7.95
7	5.619	14.298	0	5.62
			255	9.27
8	6.420	16.343	0	6.42
			255	10.59
9	7.217	18.378	0	7.22
			233	11.50

Note:

1. For good product reliability, keep V_{LCD} under **11.5V** over all temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

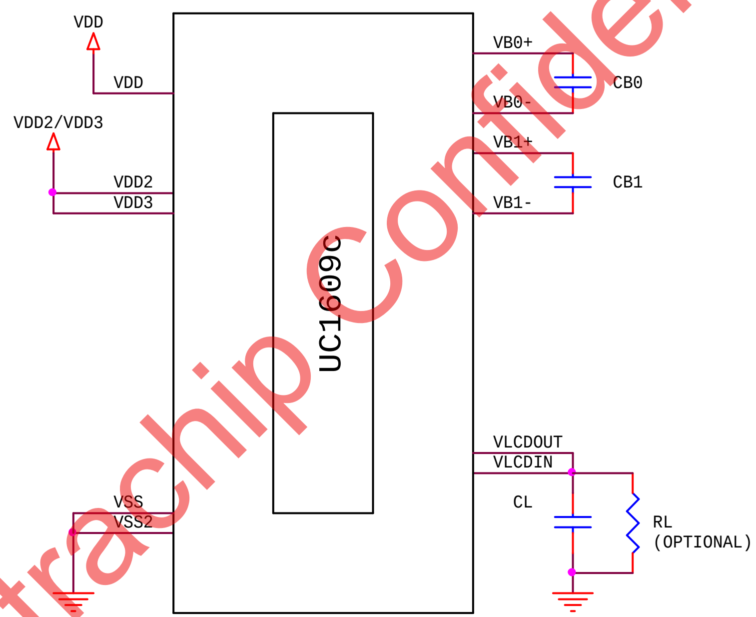


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

C_{Bx} : 2.2 µF/5V or 300x LCD load capacitance, whichever is higher.

C_L : 330nF(16V) is appropriate for most applications.

R_L: 3.3M~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1609c contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

4 different frame rates are provided for system design flexibility. The frame rate is controlled by register LC[4:3]. When Mux-Rate is above 45, Frame rate: 76fps, 95fps, 132fps, and 168 fps.

When Mux-Rate is lowered to 44, 33, 22, and 17, frame rate will be scaled down automatically by 1.5, 2, 3, and 4 times to reduce power consumption.

Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG and COM drivers are in idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming conventions are: COM*x*, where x = 1~64, refers to the row driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display Enable* command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1609c will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1",and UC1609c will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL DISPLAY

UC1609c provides flexible control of Mux Rate and active display area. Please refer to commands `Set COM End`, `Set Partial Display Start`, and `Set Partial Display End` for more detail.

ITO LAYOUT AND LC SELECTION

Since COM scanning pulses of UC1609c can be as short as 91µS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 9.23\mu S$$

where

- C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.
- R_{ROW}: ITO resistance over one row of pixels within the active area
- R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} – RC_{MIN} | < 2.76\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worst case values for all calculations)

SEG TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 6.30\mu S$$

where

- C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / (# of column), where C_{LCD} is the LCD panel capacitance.
- R_{COL}: ITO resistance over one column of pixels within the active area
- R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too large, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, and crosstalk will increase.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/65	1/9	13.3%	10.6%	9.6%
1/65	1/8	13.1%	10.5%	9.5%

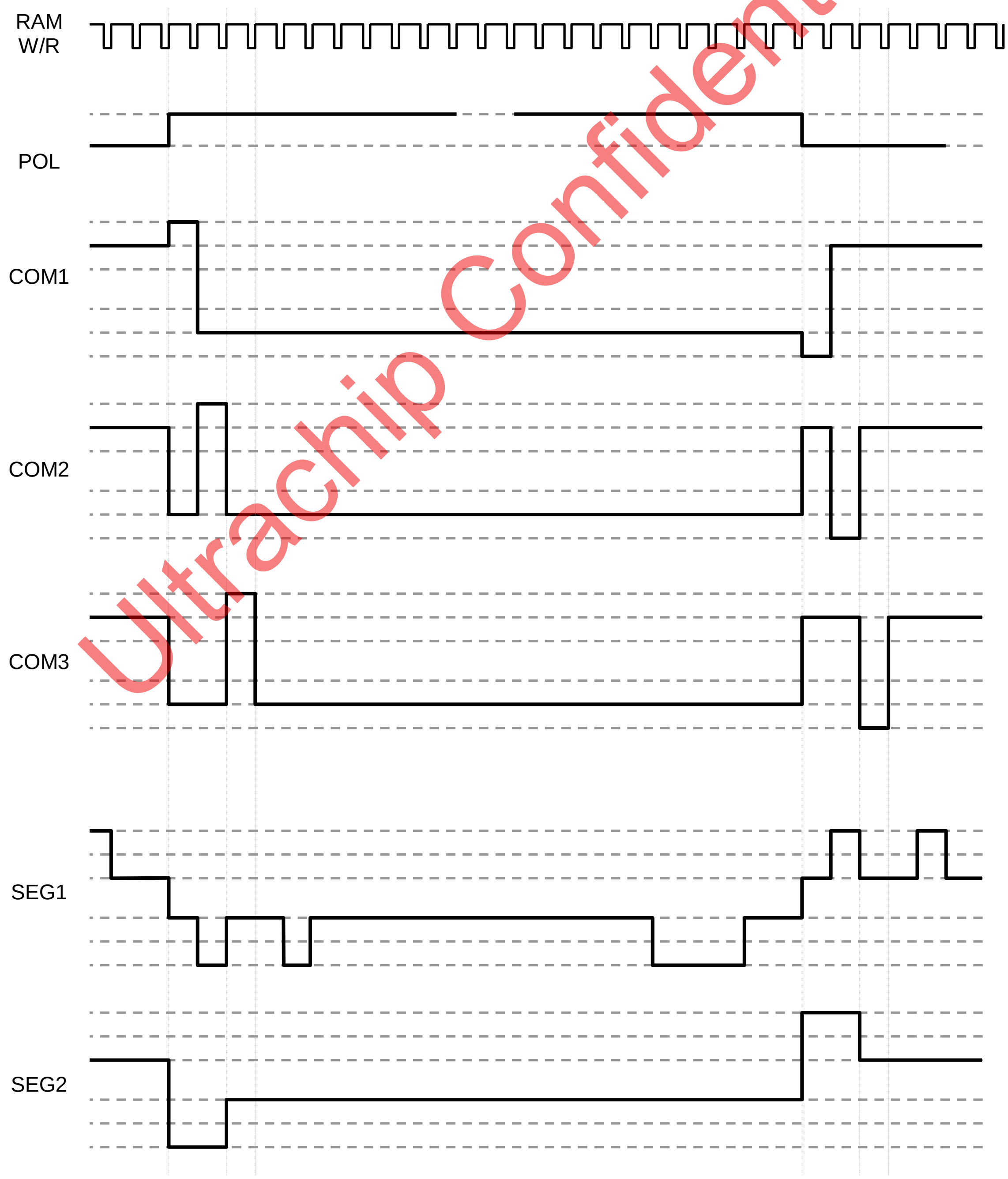


FIGURE 2: COM and SEG Electrode Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1609c supports two (2) 8-bit parallel bus protocols and three (3) serial bus protocols. Designers can choose either the 8-bit parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules and minimize connector pins.

		Bus Type				
		8080	**6800**	**S8 (4-wire)**	**S9 (3-wire)**	**I^2C (2-wire)**
Width		8-bit	8-bit	Serial		
Access		Read / Write		Read (status) / Write		R / W
Control & Data Pins	BM[1:0]	10	11	00	01	01
	D[7]	Data	Data	--	0	1
	CS[1:0]	Chip Select				A[3:2]
	CD	Control/Data			0	
	WR0	$\overline{WR}$	R/$\overline{W}$	0		
	WR1	$\overline{RD}$	EN	0		
	D[6,2,1]	Data		--		
	D[5:3], D[0]	Data		D[5:3]=SDA, D[0]=SCK		

Connect unused control pins and data bus pins to V_{DD} for "H" or V_{SS} for "L".

	CS Disable Bus Interface	CS Init. Bus State	RESET Init. Bus State
8-bit	✓	–	✓
S8 or S9	✓	✓	✓
I^2C	–	–	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- RESET can be pin reset / soft reset / power on reset.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1609c internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipeline. This architecture requires that, every time memory address is modified, either in parallel mode or serial mode, by either `Set CA` or `Set PA` command, a dummy read cycle need to be performed before the actual data can propagate through the pipeline and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

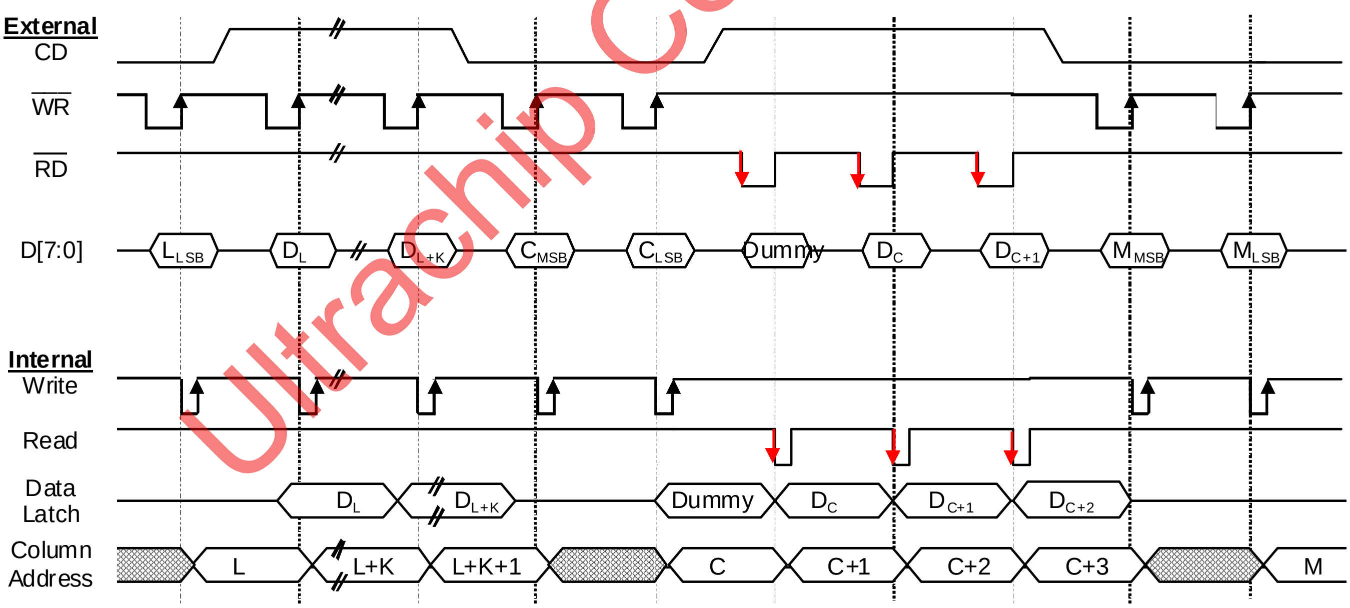


Figure 3: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1609c supports three serial modes, one 4-wire SPI mode (S8), one 3-wire SPI mode (S9) and one 2-wire SPI mode (I^2C). Bus interface mode is determined by the wiring of the BM[1:0] and D[7]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Pins CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, these 8 bits will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

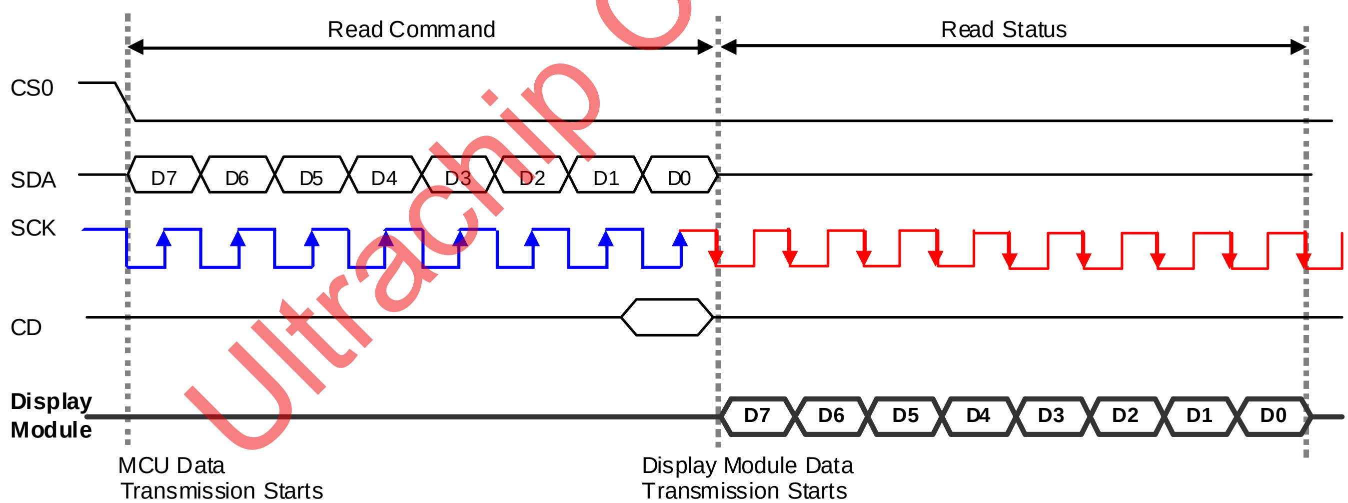


FIGURE 4.a: 4-wire Serial Interface (S8) – Read

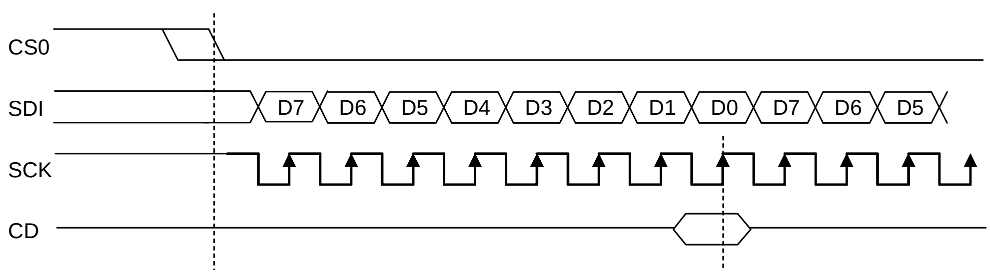


Figure 4.b: 4-wire Serial Interface (S8) – Write

S9 (3-WIER) INTERFACE

Pins CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 (or CS1) for each byte of data/command is recommended but optional.

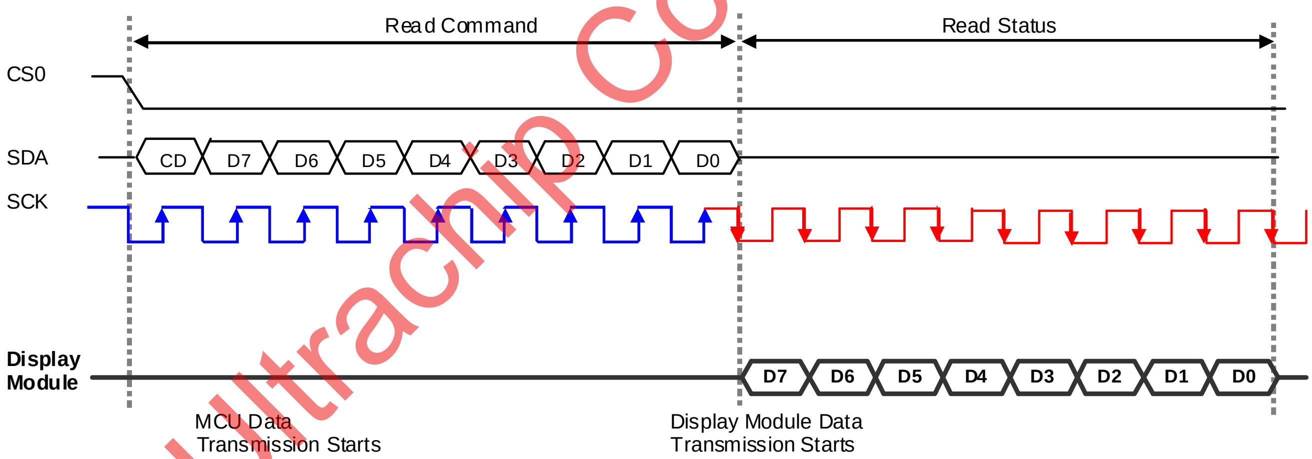


FIGURE 5.a: 3-wire Serial Interface (S9) – Read

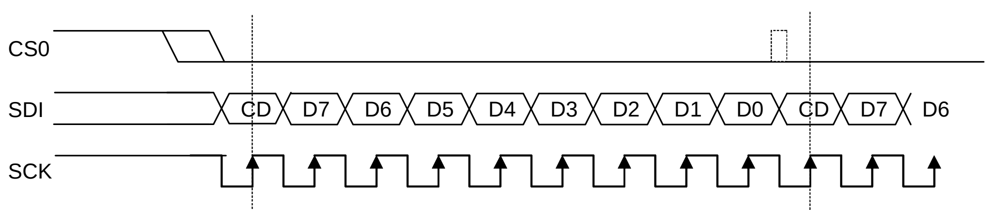
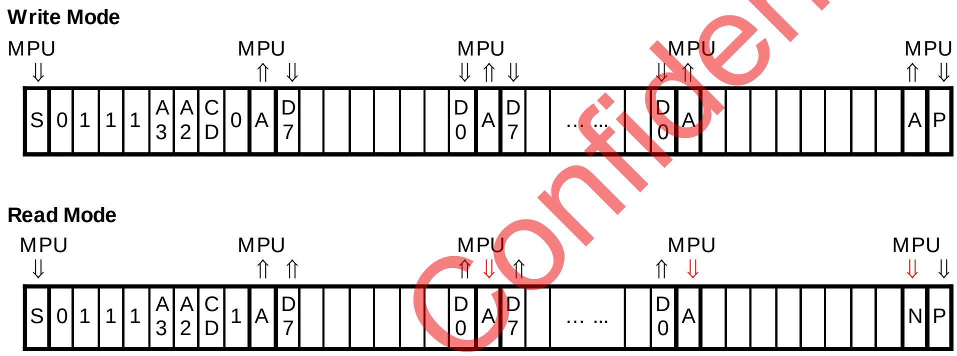


Figure 5.b: 3-wire Serial Interface (S9) – Write

I^{2}C (2-WIRE) INTERFACE



When BM[1:0] is set to "LH" and D[7] is set to "H", UC1609c is configured as an I^{2}C bus signaling protocol compliant slave device. Please refer to I^{2}C standard for details of the bus signaling protocol, and AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and is used to configure UC1609c' device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I^{2}C mode.

Each UC1609c I^{2}C interface sequence starts with a "S" (Start) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

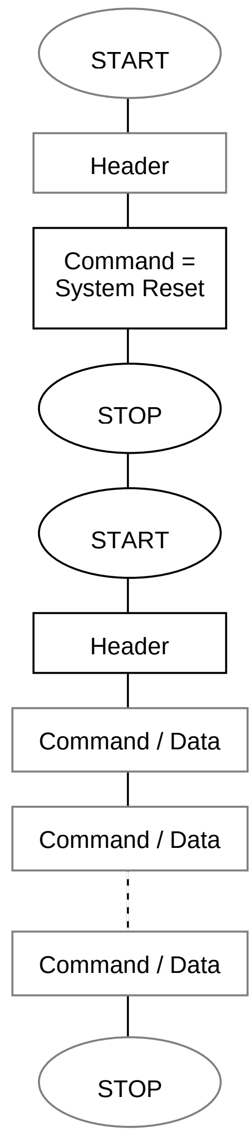
Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I^{2}C mode and should be connected to V_{SS}.

The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1609c will send out a "A" (Acknowledge signal, pull to "L"). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1609c) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE mode), or an N (Not Acknowledged, in READ mode) is sent by the bus master.

When using I^{2}C serial mode, if command `System Reset` is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a "System Reset" command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



HOST INTERFACE REFERENCE CIRCUIT

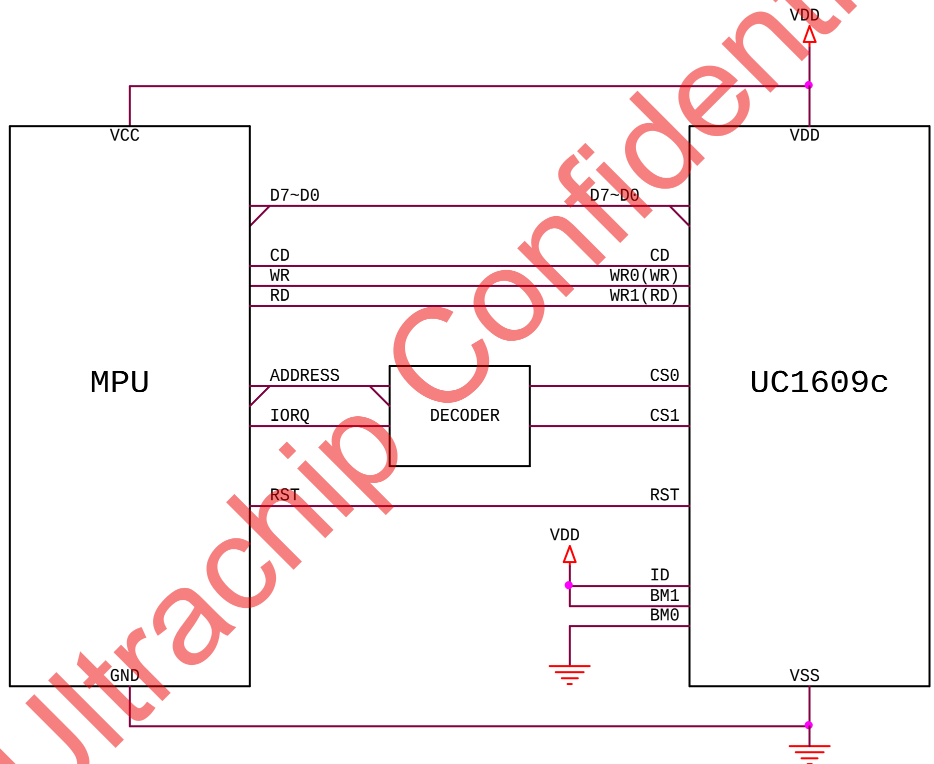


FIGURE 6: 8080/8bit parallel mode reference circuit

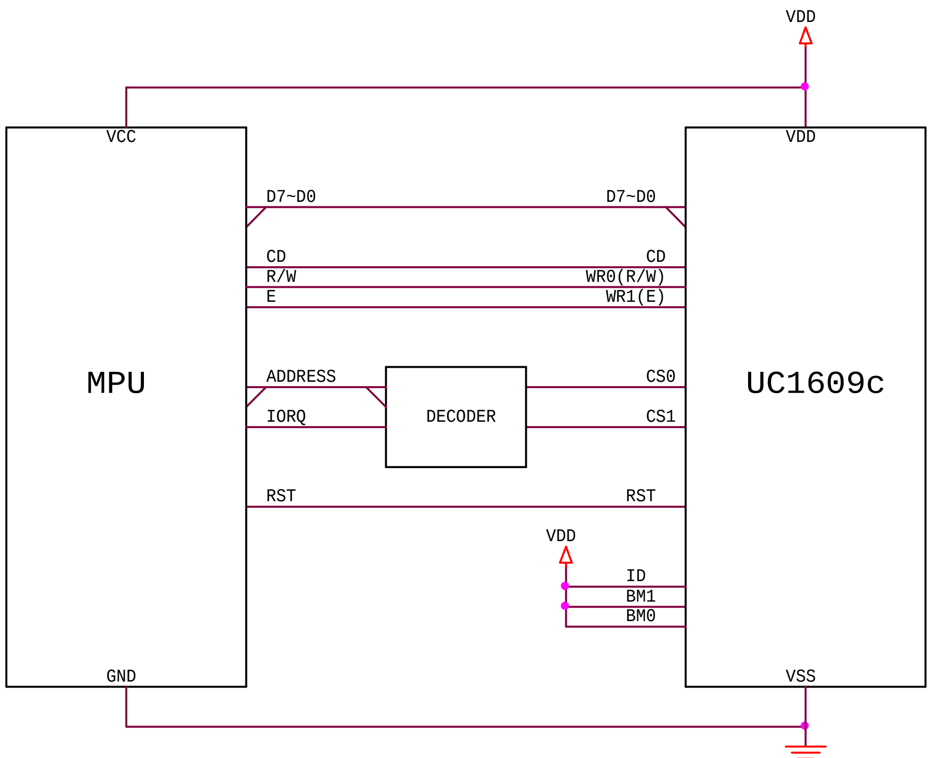


FIGURE 7: 6800/8bit parallel mode reference circuit

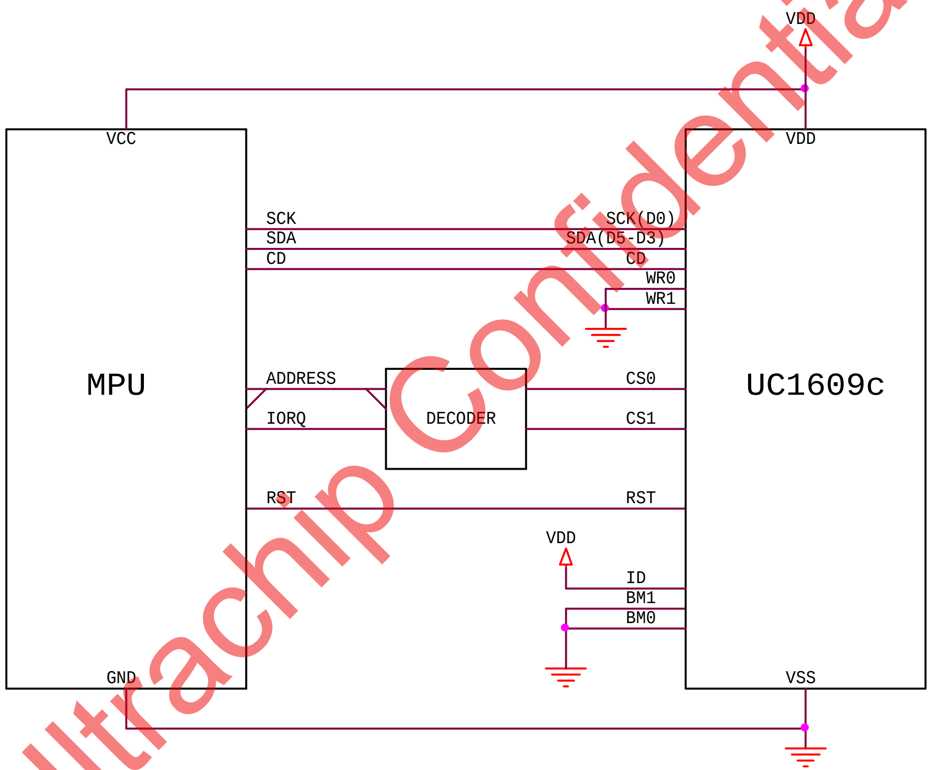


FIGURE 8: Serial-8 serial mode reference circuit

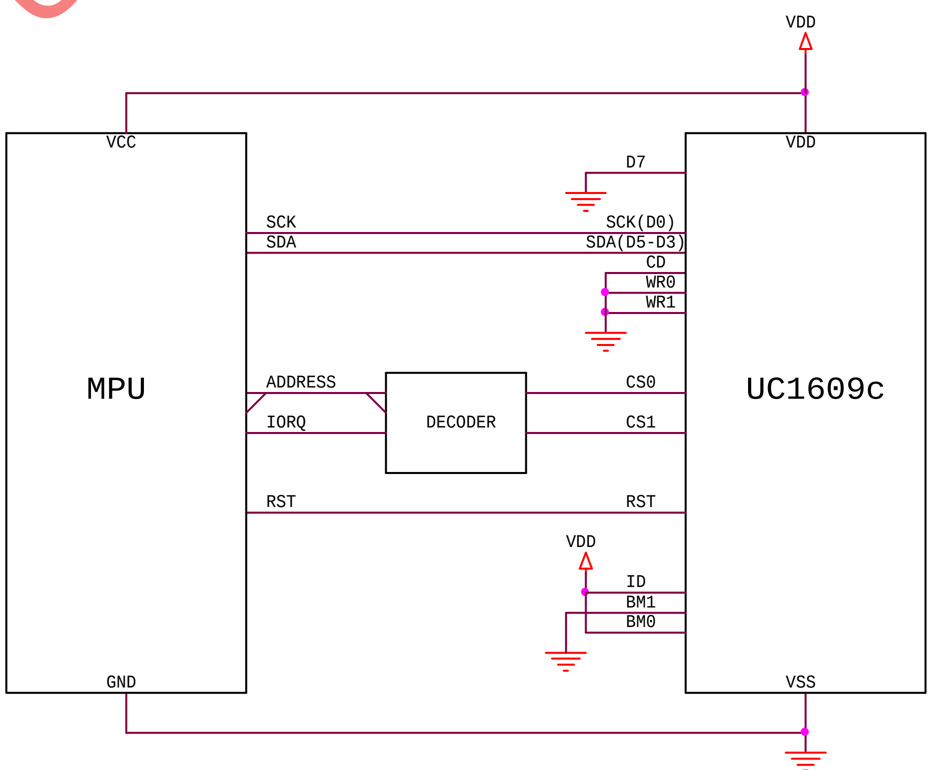


FIGURE 9: Serial-9 serial mode reference circuit

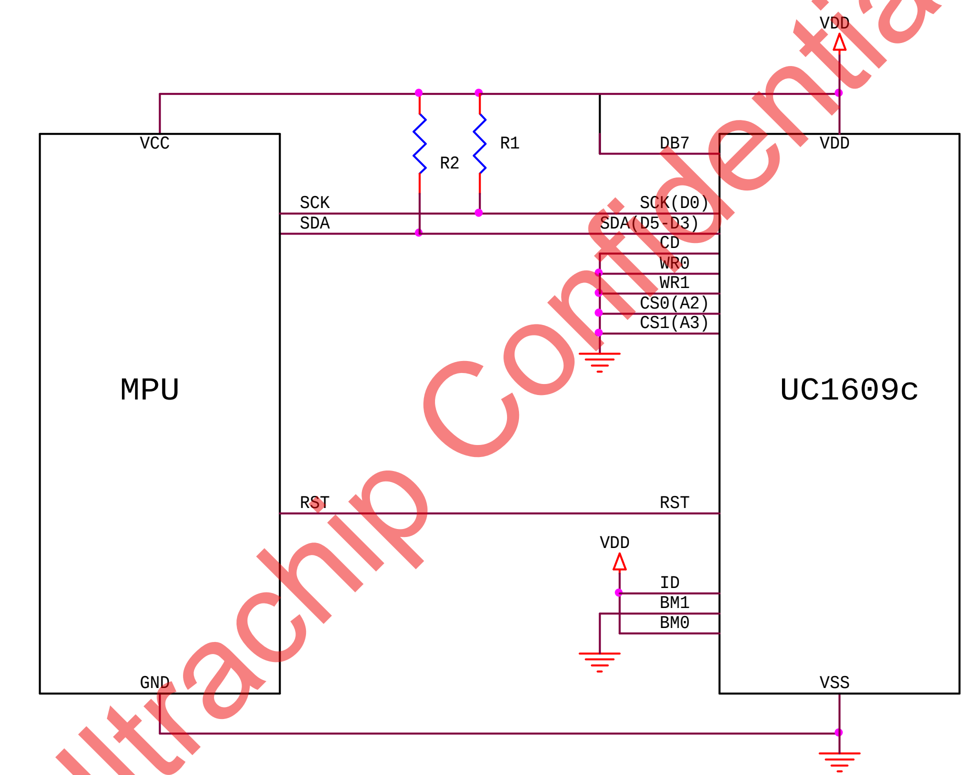


FIGURE 10: I^2C serial mode reference circuit

Note

- The ID pins are for production control. The connection will affect the content of D[7] of the 1-st byte of the `Get Status` command. Connect to V_{DD} for "H" or V_{SS} for "L".
- RST pin is optional. When the RST pin is not used, connect it to V_{DD}.
- When using I^2C serial mode, CS1/0 are user configurable and affect A[3:2] of device address.
- R1, R2: 2k ~ 10k Ω, use lower resistor for bus speed up to 3.6MHz, use higher resistor for lower power.
- When using Read function:

(8080) Set WR1=0 (6800) Set WR1=1 → data output will be enabled. (Serial) Set SCK=0	(8080) Set WR1=1 (6800) Set WR1=0 → data output will be disabled. (Serial) Set SCK=1

- It is REQUIRED to set MPU's data port to 1 before Data Read or Status Read actions.

DISPLAY DATA RAM (DDRAM)

DATA ORGANIZATION

The input display data is stored to a dual port static DDRAM (DDRAM, for Display Data RAM) organized as 65x192.

After setting CA and RA, the subsequent data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of row (191), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increase or decrease, depending on the setting of row Increment Direction (RID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 7), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (191–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[2]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed R*m* scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1-st line period of each field
Line = *SL*
Otherwise
Line = Mod(*Line*+1, 64)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produce the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches *64*.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MR -1*, *64*)
Otherwise
Line = Mod(*Line-1* , *64*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

PA[3:0]	0	Line Address	SEG1	SEG2	Page	Panel Location	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
0000	D0	R0	1	0	Page 0	COM1	R0	R16	R63	R15
	D1	R1	1	0		COM2	R1	R17	R62	R14
	D2	R2	1	1		COM3	R2	R18	R61	R13
	D3	R3	1	1		COM4	R3	R19	R60	R12
	D4	R4	1	0		COM5	R4	R20	R59	R11
	D5	R5	0	0		COM6	R5	R21	R58	R10
	D6	R6	0	1		COM7	R6	R22	R57	R9
	D7	R7	0	1		COM8	R7	R23	R56	R8
0001	D0	R8			Page 1	COM9	R8	R24	R55	R7
	D1	R9				COM10	R9	R25	R54	R6
	D2	R10				COM11	R10	R26	R53	R5
	D3	R11				COM12	R11	R27	R52	R4
	D4	R12				COM13	R12	R28	R51	R3
	D5	R13				COM14	R13	R29	R50	R2
	D6	R14				COM15	R14	R30	R49	R1
	D7	R15				COM16	R15	R31	R48	R0
0010	D0	R16			Page 2	COM17	R16	R32	R47	R63
	D1	R17				COM18	R17	R33	R46	R62
	D2	R18				COM19	R18	R34	R45	R61
	D3	R19				COM20	R19	R35	R44	R60
	D4	R20				COM21	R20	R36	R43	R59
	D5	R21				COM22	R21	R37	R42	R58
	D6	R22				COM23	R22	R38	R41	R57
	D7	R23				COM24	R23	R39	R40	R56
0011	D0	R24			Page 3	COM25	R24	R40	R39	R55
	D1	R25				COM26	R25	R41	R38	R54
	D2	R26				COM27	R26	R42	R37	R53
	D3	R27				COM28	R27	R43	R36	R52
	D4	R28				COM29	R28	R44	R35	R51
	D5	R29				COM30	R29	R45	R34	R50
	D6	R30				COM31	R30	R46	R33	R49
	D7	R31				COM32	R31	R47	R32	R48
0100	D0	R32			Page 4	COM33	R32	R48	R31	R47
	D1	R33				COM34	R33	R49	R30	R46
	D2	R34				COM35	R34	R50	R29	R45
	D3	R35				COM36	R35	R51	R28	R44
	D4	R36				COM37	R36	R52	R27	R43
	D5	R37				COM38	R37	R53	R26	R42
	D6	R38				COM39	R38	R54	R25	R41
	D7	R39				COM40	R39	R55	R24	R40
0101	D0	R40			Page 5	COM41	R40	R56	R23	R39
	D1	R41				COM42	R41	R57	R22	R38
	D2	R42				COM43	R42	R58	R21	R37
	D3	R43				COM44	R43	R59	R20	R36
	D4	R44				COM45	R44	R60	R19	R35
	D5	R45				COM46	R45	R61	R18	R34
	D6	R46				COM47	R46	R62	R17	R33
	D7	R47				COM48	R47	R63	R16	R32
0110	D0	R48			Page 6	COM49	R48	R0	R15	R31
	D1	R49				COM50	R49	R1	R14	R30
	D2	R50				COM51	R50	R2	R13	R29
	D3	R51				COM52	R51	R3	R12	R28
	D4	R52				COM53	R52	R4	R11	R27
	D5	R53				COM54	R53	R5	R10	R26
	D6	R54				COM55	R54	R6	R9	R25
	D7	R55				COM56	R55	R7	R8	R24
0111	D0	R56			Page 7	COM57	R56	R8	R7	R23
	D1	R57				COM58	R57	R9	R6	R22
	D2	R58				COM59	R58	R10	R5	R21
	D3	R59				COM60	R59	R11	R4	R20
	D4	R60				COM61	R60	R12	R3	R19
	D5	R61				COM62	R61	R13	R2	R18
	D6	R62				COM63	R62	R14	R1	R17
	D7	R63				COM64	R63	R15	R0	R16
1000	D0	R64			Page 8	CIC	R64	R64	R64	R64

MX=0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG128	SEG129	SEG130	SEG131	SEG132
MX=1	SEG132	SEG131	SEG130	SEG129	SEG128	SEG127	SEG126	SEG125	SEG5	SEG4	SEG3	SEG2	SEG1

Example for memory mapping: let MX = 0, MY = 0, SL = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1 (D7-D0) : 0001 1111b

⇒ Page 0 SEG 2 (D7-D0) : 1100 1100b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1609c has two different types of Reset:

Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by connecting the RST pin to ground.

In the following discussions, Reset means *System Reset*.

The differences between pin reset and software reset are

Procedure (Restoring to default value)	Pin Reset (Power On Reset)	Software Reset
Column Address : CA[7:0]=0	V	V
Page Address : PA[3:0]=0	V	V
RAM Address Control : AC[2:0]=001b	V	V
Temp. Compensation : TC[1:0]=00b	V	X
Power Control : PC[2:0]=110b	V	X
Scroll Line : SL[5:0]=0	V	X
Vbias Potentiometer : PM[7:0]=49h	V	X
Partial Display Control : LC[5]=0b	V	X
Frame Rate : LC[4:3]	V	X
All-Pixel-On : DC[1]=0b	V	X
Inverse Display : DC[0]=0b	V	X
Display Enable : DC[2]=0b	V	X
LCD Mapping Control : LC[2:1]=00b	V	X
Test Control	V	X
LCD Bias Ratio : BR[1:0]=11b	V	X
COM End : CEN[6:0]=63d	V	X
Partial Display Command	V	X
MTP Function Control	V	X

RESET STATUS

When UC1609c enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1609c has three operating modes (OM):
Reset, Sleep, Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of UC1609c' internal clock. To ensure consistent system states, wait at least 10µS after issuing the `Set Display Enable` command or triggering `System Reset`.

Action	Mode	OM
RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1609c consumes very little energy in Sleep mode (typically under 5µA).

EXITING SLEEP MODE

UC1609c contains internal logic to check whether V_{LCD} and V_D are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1609c internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

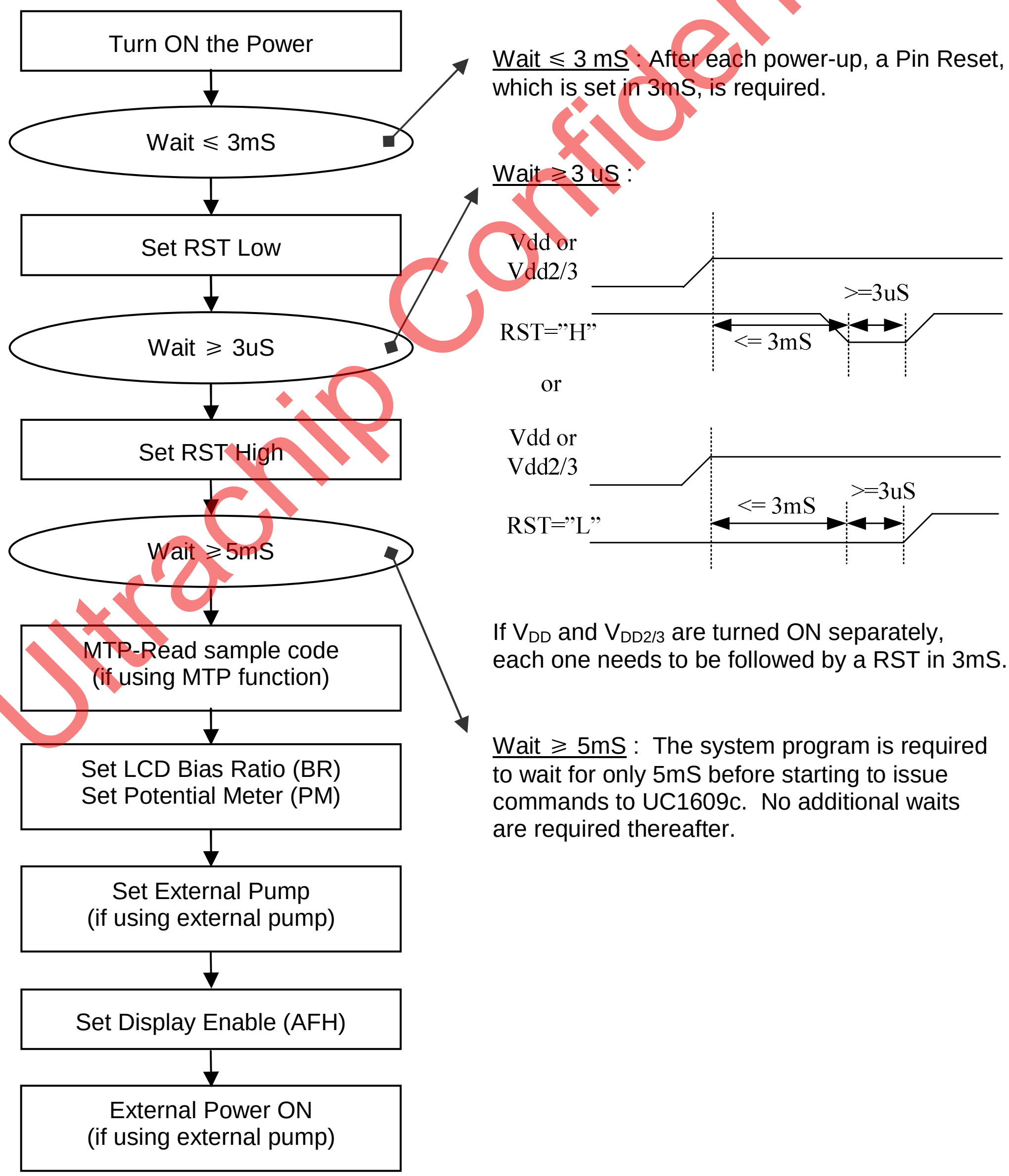


FIGURE 11: Reference Power-Up Sequence

There's no delay needed while turning ON V_{DD} and $V_{DD2/3}$, and either one can be turned ON first.

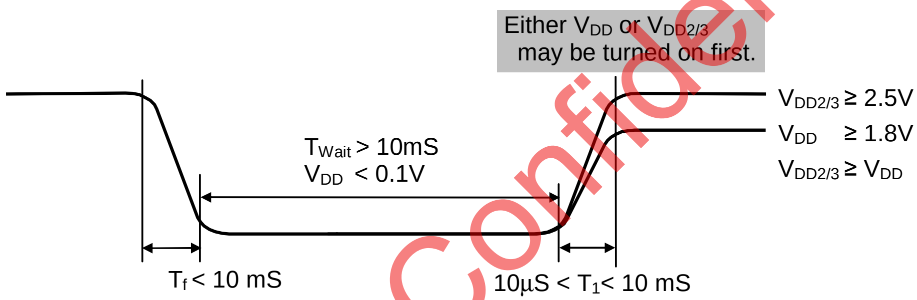


Figure 12: Power Off-On Sequence

ENTER/EXIT SLEEP MODE SEQUENCE

UC1609c enters Sleep mode from Display mode by issuing Set Display OFF command. To exit Sleep mode, Set Display ON.

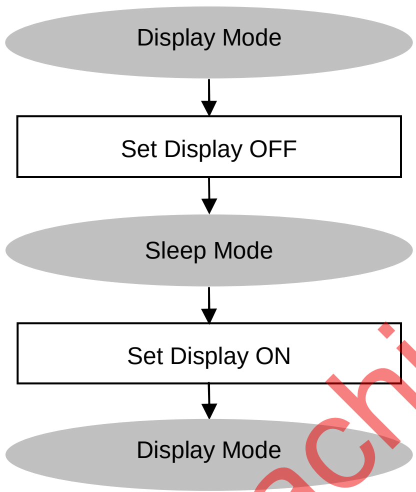


Figure 13 : Enter/Exit Sleep Mode Sequence

Power-Down Sequence

To prevent the charge stored in capacitor C_L causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

When internal V_{LCD} is not used, UC1609c will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

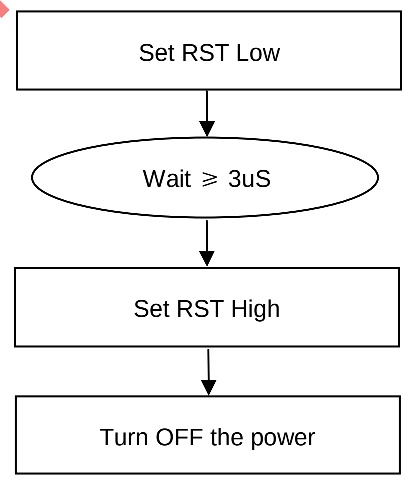


FIGURE 14: Reference Power-Down Sequence

SAMPLE COMMAND SEQUENCES FOR POWER MANAGEMENT

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type	Required:	These items are required
	Customized:	These items are not necessary if customer parameters are the same as default
	Advanced:	We recommend new users to skip these commands and use default values.
	Optional:	These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R											Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R											Wait ≤ 3 mS	
R											Set RST pin Low	Wait 3uS after RST is Low
R											Set RST pin High	Wait 5mS after RST is High
C	0	0	1	1	1	1	0	1	0	0	Set V MTP1 Potentiometer	Set MTP V_{LCD}
C	0	0	1	0	0	0	0	0	1	1		MTP2: 83h (6.4V)
C	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
C	0	0	0	0	0	0	0	0	1	1		MTP5: 03h (10mS)
C	0	0	1	1	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	1	1	1	1	1	1	MTPM1	Ex: To read MTPM[5:0], set the value to 00111111b
C	0	0	1	1	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
C	0	0	-	-	0	1	1	0	0	1		Set MTPC[2:0]=010
C											Wait 150 mS	
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
R	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping Control	
A	0	0	1	0	1	0	0	0	0	#	Set Frame Rate	Fine tune for power, flicker, contrast.
R	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	
C	0 0	0 0	1 0	1 0	1 0	1 1	1 1	0 0	0 0	0 1	Set MTP function	Set MTP use & MTP read
C											Wait ≤ 50 mS	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

Note: Issue the commands in blue color only when using MTP functions.

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R											Set RST pin Low	Wait 3 uS after RST is Low
R											Set RST pin High	
R											Draining capacitor	Wait ~3mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

MULTI-TIME PROGRAM (MTP) NV MEMORY

OVERVIEW

MTP feature is available for UC1609c such that LCM makers can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1609c:

MTP-Erase, MTP-Program, MTP-Read.

MTP-Program requires an external power source supplied to TST4 pin. MTP allows to program at least 10 times and should be performed only by the LCM makers.

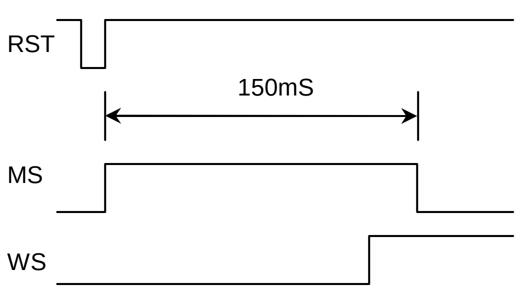
MTP-Read is facilitated by the internal DC-DC converter built-in on UC1609c, no external power source is required, and it is performed automatically after hardware RESET (power-ON and pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1609c, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the *Read Status* commands will exhibit the following waveforms.

MTP-read Sample Code



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

Although user can use *Read Status* command in a polling loop to make sure {MS, WS}={0, 1} before proceeding with the normal operations, however, it may be simpler to just issue `Set Display Enable` command every 0.5~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above "Periodical re-initializing" approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software *RESET* command. This enables the ICs to turn on display faster without the delay caused by MTP-READ.

It is recommended to use software *RESET* for normal operation control purpose and hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

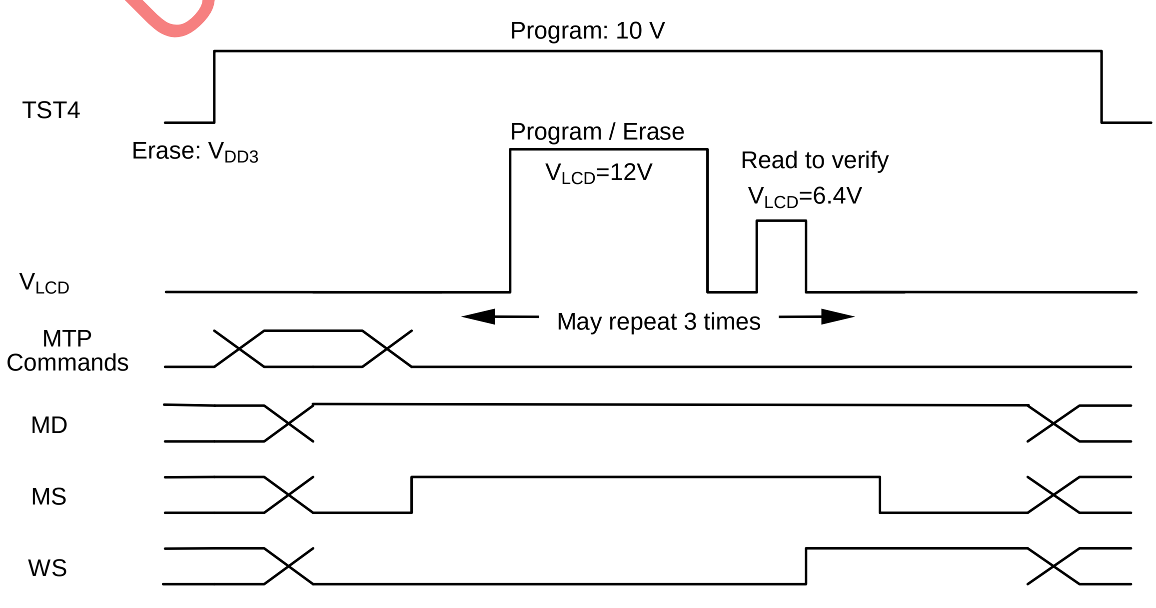
No external power source is required for MTP Erase and Read operation. For these MTP operations, TST4 should be open, or connected to V_{DD3}.

	V_{LCD}	TST4 (external input)
Program	MTP3 : FFh (12V)	10V (1mA per bit)
Erase	MTP3 : FFh (12V)	Floating or V_{DD3}
Read	MTP2 : 83h (6.4V)	Floating or V_{DD3}

Note: Do Erase before Program and program one bit at a time.

2. Read MTP status bits

With normal Get Status method (CD=0, W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

3. MTP Cell Value Usage

There are 6 MTP cell bits. They are divided into two groups for different purpose.

MTP[5:0] : V_{LCD} Trim
When PMO[5]=1: PM with trim = PM – PMO[4:0]
When PMO[5]=0: PM with trim = PM + PMO[4:0]

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, and Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type
- Required: These items are required
- Customized: These items are not necessary if customer parameters are the same as default
- Advanced: We recommend new users to skip these commands and use default values.
- Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R											Set RST pin Low	Wait 3uS after RST is Low
R											Set RST pin High	Wait 5mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	1	0	0	0	0	0	1	1		MTP2: 83h (6.4V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	1	1	1	1	1	1	1	1		MTP3: FFh (12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	0	1	1	0	1		MTP4: 4Dh (200mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	0	1	1		MTP5: 03h (10mS)
R	0	0	1	1	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	0	0	0	0	0	1	MTPM	Ex: To program MTPM[0] to be 1, set the value to 00000001b *
R												Apply TST4 voltage Program: 10V
R	0	0	1	1	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0, WS=1
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R											Set RST pin Low	Wait 3uS after RST is Low
R											Set RST pin High	Wait 5mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	1	0	0	0	0	0	1	1		MTP2: 83h (6.4V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	1	1	1	1	1	1	1	1		MTP3: FFh (12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	0	1	1	0	1		MTP4: 4Dh (200mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	0	1	1		MTP5: 03h (10mS)
R	0	0	1	1	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	0	0	1	1	1	1	MTPM1	Ex: To erase MTPM[3:0], set the value to 00001111b *
R	0	0	1	1	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0 WS=1
R											V_{DD}=0V	Power OFF

* It is recommended that users clear first all the bits to be programmed.

MTP Read Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R											Set RST pin Low	Wait 3uS after RST is Low
R											Set RST pin High	Wait 5mS
R	0	0	1	1	1	1	0	1	0	0	Set $V_{MTP}1$ Potentiometer	Set MTP V_{LCD}
R	0	0	1	0	0	0	0	0	1	1		MTP2: 83h (6.4V)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	0	1	1		MTP5: 03h (10mS)
R	0	0	1	1	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	1	1	1	1	1	1	MTPM1	Ex: To read MTPM[5:0], set the value to 00111111b *
R	0	0	1	1	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	1	1	0	0	1		Set MTPC[2:0]=010
R											Wait 150mS	
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0, WS=1
R											(other initialization settings for starting the IC)	

* It is recommended that users read first all the bits to be programmed.

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is, therefore, highly recommended that LCM makers strictly follow the “JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices” when manufacturing LCM.

The following pins in UC1609c require special “ESD Sensitivity” consideration in particular:

Pins \ Test Mode		Machine Mode		Human Body Mode	
		V_{DD}	V_{SS}	V_{DD}	V_{SS}
LCD Driver		200V	200V	2.0KV	2.0KV
LCM Digital Interface		300V	300V	3.0KV	3.0KV
LCM HV Interface	TST1/2/4	300V	300V	3.0KV	3.0KV
	C_B pins	300V	300V	2.0KV	2.5KV
	V_{LCDIN}	250V	250V	2.0KV	2.5KV
	V_{LCDOUT}	300v	300V	3.0KV	3.0KV
PWR/GND		–	300V	–	3.0KV

According to UltraChip’s Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134 – notes 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.2	V
V_{LCD}	LCD Generated voltage	-0.3	+13.2	V
V_{IN} / V_{OUT}	Any input/output	-0.4	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Notes

1. V_{DD} is based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.7	1.8~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.6	2.7~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant 2.6V, 25^{o}C$		4.8~11.5	11.5	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant 2.6V, 25^{o}C$	0.80		1.32	V
V_{IL}	Input logic LOW				$0.1V_{DD}$	V
V_{IH}	Input logic HIGH		$0.9V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
I_{SB}	Standby current	$V_{DD} = V_{DD2/3} = 3.3V$, Temp = $85^{o}C$			50	μA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{0(SEG)}$	SEG output impedance	$V_{LCD} = 9V$		2200	2800	Ω
$R_{0(COM)}$	COM output impedance	$V_{LCD} = 9V$		2200	2800	Ω
F_{FR}	Average Frame Rate	LC[4:3] = 01b	-10%	95	+10%	Hz

POWER CONSUMPTION

$V_{DD} = 2.7V$,
$V_{LCD} = 8.54V$
Mux Rate = 65,
Temperature = $25^{o}C$,
Bias Ratio = 11b,
Frame Rate = 01b,
Bus mode = 6800,
C_L = 330nF,
PM = 73,
PMO = 00H,
C_{B0} / C_{B1} = 2.2μF,
All outputs are open circuit.

Display Pattern	Conditions	Typ.	Max.
All-ON	Bus = idle	196	392
All-OFF	Bus = idle	197	394
2-pixel checker	Bus = idle	222	444
-	Bus = idle (standby current)	-	5

AC CHARACTERISTICS

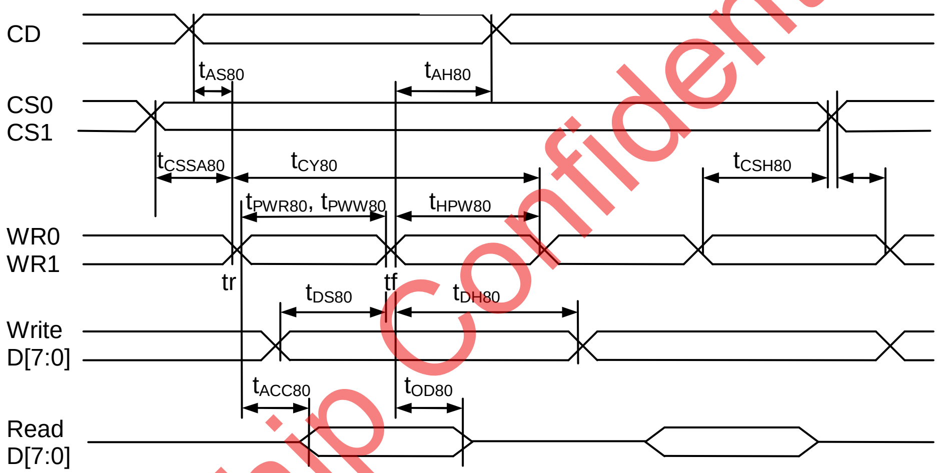


FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		5 10	–	nS
t_{CSSA80} t_{CSH80}	CS1, CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY80} t_{PWR80} / t_{PWW80} t_{HPW80}	WR0, WR1	System Cycle time Pulse width High pulse width		170 / 110 70 / 40 70 / 40	–	nS
t_{DS80} t_{DH80}	D7~D0 (Write)	Data setup time Data hold time		35 5	–	nS
t_{ACC80} t_{OD80}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– –	70 40	nS
(1.7V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		5 10	–	nS
t_{CSSA80} t_{CSH80}	CS1, CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY80} t_{PWR80} / t_{PWW80} t_{HPW80}	WR0, WR1	System cycle time Pulse width High pulse width		270 / 190 120 / 80 120 / 80	–	nS
t_{DS80} t_{DH80}	D7~D0 (Write)	Data setup time Data hold time		60 5	–	nS
t_{ACC80} t_{OD80}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– –	120 80	nS

Note: tr (rising time), tf (falling time) : ≤ 15nS

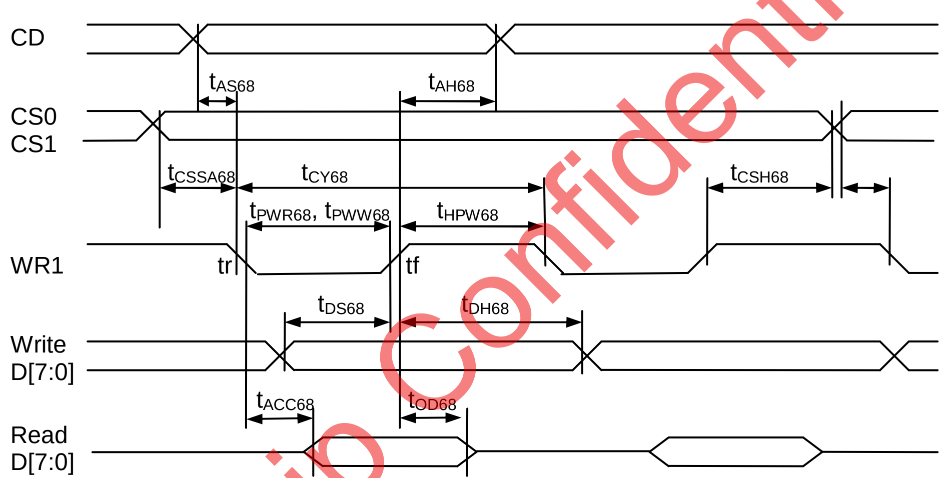


FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68}	CD	Address setup time		5	–	nS
t_{AH68}		Address hold time		10		
t_{CSSA68}	CS1, CS0	Chip select setup time		5	–	nS
t_{CSH68}		Chip select hold time		5		
t_{CY68}	WR1	System cycle time		170 / 110	–	nS
t_{PWR68} / t_{PWW68}		Pulse width		70 / 40		
t_{HPW68}		High pulse width		70 / 40		
t_{DS68}	D7~D0 (Write)	Data setup time		35	–	nS
t_{DH68}		Data hold time		5		
t_{ACC68}	D7~D0 (Read)	Read access time	C_L = 100pF	–	70	nS
t_{OD68}		Output disable time		–	40	
(1.7V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68}	CD	Address setup time		5	–	nS
t_{AH68}		Address hold time		10		
t_{CSSA68}	CS1, CS0	Chip select setup time		5	–	nS
t_{CSH68}		Chip select hold time		5		
t_{CY68}	WR1	System cycle time		270 / 190	–	nS
t_{PWR68} / t_{PWW68}		Pulse width		120 / 80		
t_{HPW68}		High pulse width		120 / 80		
t_{DS68}	D7~D0 (Write)	Data setup time		60	–	nS
t_{DH68}		Data hold time		5		
t_{ACC68}	D7~D0 (Read)	Read access time	C_L = 100pF	–	120	nS
t_{OD68}		Output disable time		–	80	

Note: tr (Rising time), tf (falling time) : ≤ 15nS

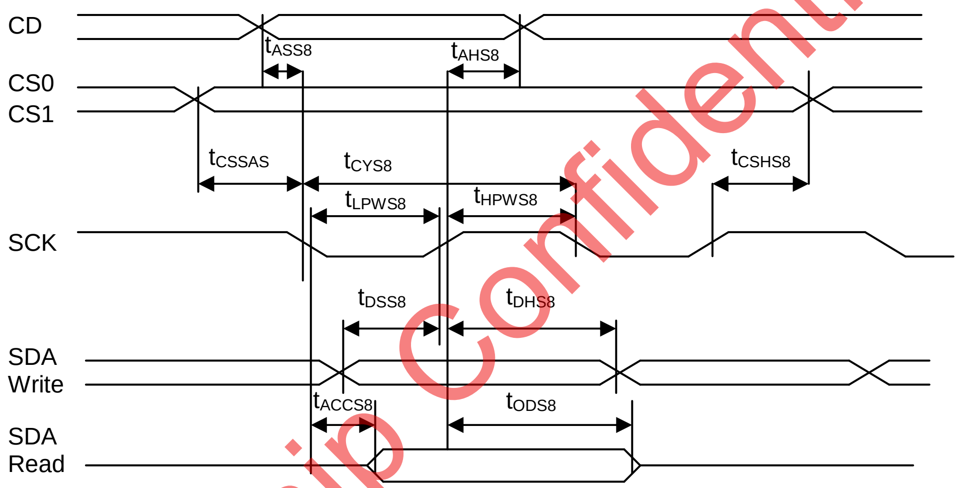


FIGURE 17: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)				(Read / Write)		
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		5 10	–	nS
t_{CSSAS8} t_{CSHS8}	CS1, CS0	Chip select setup time Chip select hold time		10 10	–	nS
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	System Cycle time Low pulse width High pulse width		190 / 80 80 / 25 80 / 25	–	nS
t_{DSS8} t_{DHS8}	SDA (Write)	Data setup time Data hold time		25 10	–	nS
t_{ACC8} t_{OD8}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– –	80 30	nS
(1.7V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		5 10	–	nS
t_{CSSAS8} t_{CSHS8}	CS1, CS0	Chip select setup time Chip select hold time		10 10	–	nS
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	System Cycle time Low pulse width High pulse width		230 / 110 100 / 40 100 / 40	– – –	nS nS nS
t_{DSS8} t_{DHS8}	SDA (Write)	Data setup time Data hold time		24 10	–	nS
t_{ACC8} t_{OD8}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– –	100 60	nS

Note: tr (Rising time), tf (falling time) : ≤ 15nS

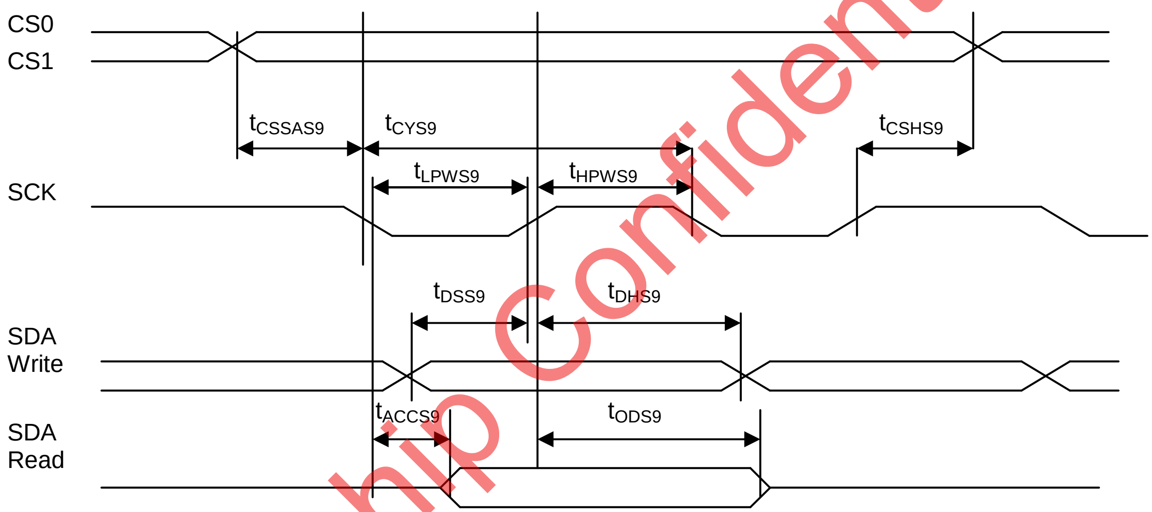


FIGURE 18: Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85 °C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1, CS0	Chip select setup time Chip select hold time		10 10	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width		190 / 80 80 / 25 80 / 25	–	nS
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		25 10	–	nS
t_{ACC9} t_{OD9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– –	80 30	nS
(1.7V ≤ V_{DD} < 2.5V, Ta= –30 to +85 °C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1, CS0	Chip select setup time		10 10	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width		230 / 110 100 / 40 100 / 40	–	nS
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		24 15	–	nS
t_{ACC9} t_{OD9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– –	100 60	nS

Note: tr (Rising time), tf (falling time) : ≤ 15nS

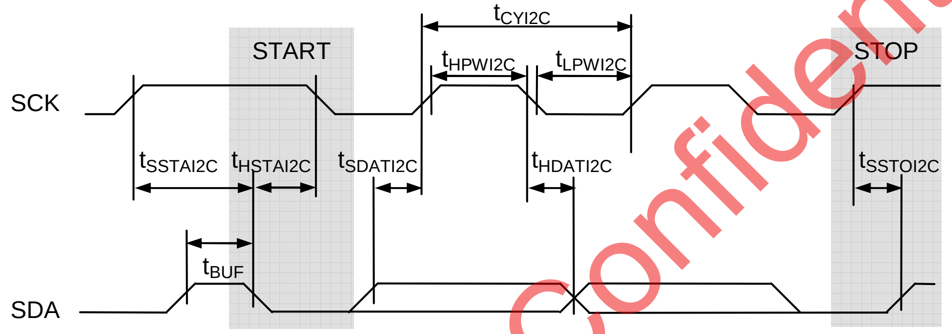


FIGURE 19: Serial bus timing characteristics (for I^{2}C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)				(Read / Write)		
t_{CYI2C}		SCK cycle time		610 / 305		
t_{HPWI2C}	SCK	High pulse width		290 / 110	–	nS
t_{LPWI2C}		Low pulse width		290 / 165		
$t_{SSTAI2C}$		Setup time – START		28		
$t_{HSTAI2C}$		Hold time – START		55		
t_{SDAI2C}	SCK SDA	Setup time – Data		40	–	nS
t_{HDAI2C}		Hold time – Data		11		
$t_{SSTOI2C}$		Setup time – STOP		28		
t_{BUF}	SDA	Bus Free time between STOP and START		165	–	nS
(1.7V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{CYI2C}		SCK cycle time		780 / 360		
t_{HPWI2C}	SCK	High pulse width		375 / 130	–	nS
t_{LPWI2C}		Low pulse width		375 / 200		
$t_{SSTAI2C}$		Setup time – START		33		
$t_{HSTAI2C}$		Hold time – START		80		
t_{SDAI2C}	SCK SDA	Setup time – Data		80	–	nS
t_{HDAI2C}		Hold time – Data		11		
$t_{SSTOI2C}$		Setup time – STOP		33		
t_{BUF}	SDA	Bus Free Time between STOP and START		220	–	nS

Note: tr (Rising time), tf (falling time) : ≤ 15nS

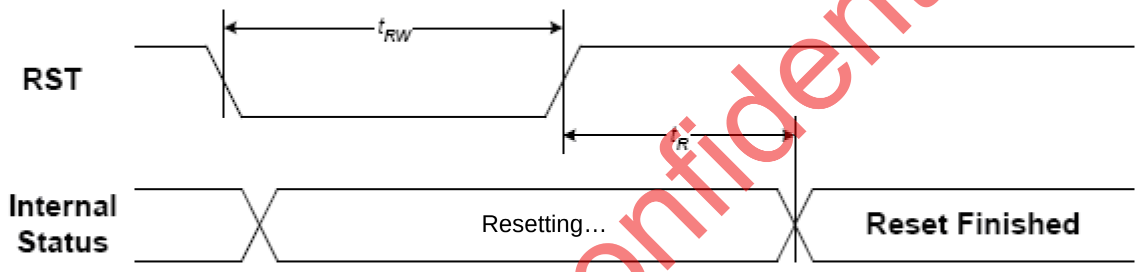


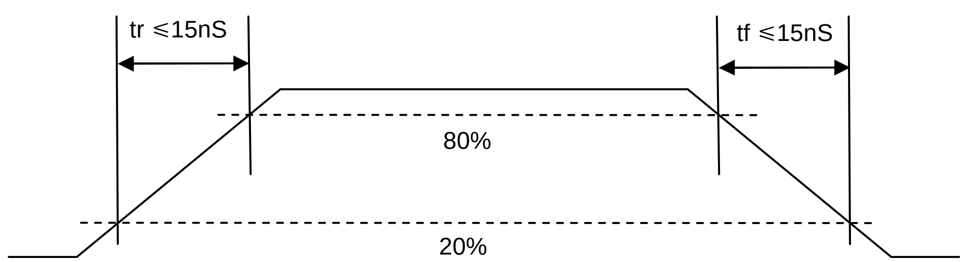
FIGURE 20: Reset Characteristics

(1.7V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
t_{RW}	RST	Reset low pulse width		3	–	μS
t_R	RST, Internal Status	Reset to Internal Status pulse delay		6	–	mS

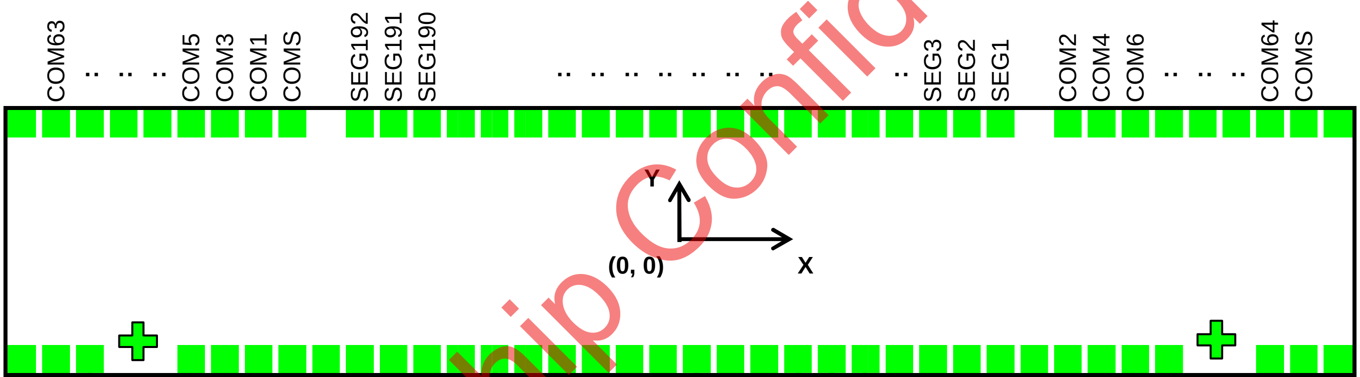
Note:

For each mode, the signal's rising and falling times (tr, tf) are stipulated to be equal to or less than 15nS each.



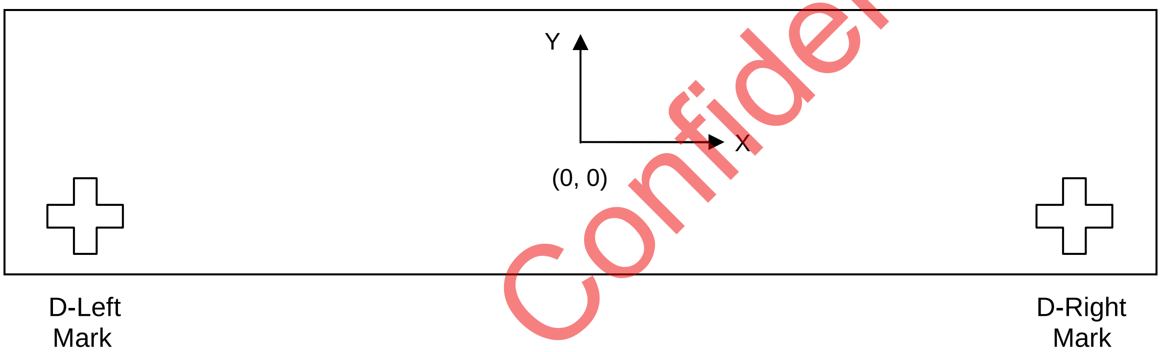
PHYSICAL DIMENSIONS

Circuit / Bump View:

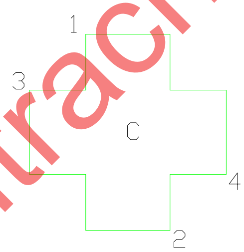


Die Size:	(7500 µM ± 40 µM) x (667 µM ± 40 µM)	**Bump Size:**	15.6 µM x 100 µM
Die Thickness:	400 µM ± 20 µM	**Bump Pitch:**	27.6 µM
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2 µM	**Shear Force:**	>5 g /µM^2
Hardness:	90 Hv ± 25 Hv	**Bump Area:**	1560 µM^2
Bump Height:	10 µM ± 3 µM	**Coordinate origin:**	Chip center
	(H_{MAX} – H_{MIN}) within die ≤ 2 µM	**Pad reference:**	Pad center

ALIGNMENT MARK INFORMATION



Shape of the alignment mark:

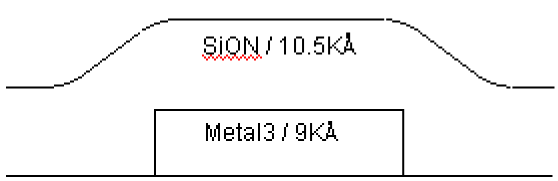


Remark:
The cross mark itself is symmetric both horizontally and vertically.

Coordinates:

Point	D-Left Mark (+)		D-Right Mark (+)	
	X	Y	X	Y
1	-3486.5	-243	3449.4	-243
2	-3466.5	-293	3469.4	-293
3	-3501.5	-258	3434.4	-258
4	-3451.5	-278	3484.4	-278
C	-3476.5	-268	3459.4	-268

Top Metal and Passivation:



FOR PROCESS CROSS-SECTION

Remark:
Alignment marks are on Metal3 and under Passivation

PAD COORDINATES

#	PAD	X	Y	W	H
1	DUMMY2	-3686	-276.5	50	45
2	DUMMY5	-3621	-276.5	50	45
3	DUMMY6	-3556	-276.5	50	45
4	DATA_pad<7>	-3303.55	-276.5	50	45
5	VDDX	-3238.55	-276.5	50	45
6	DATA_pad<6>	-3173.55	-276.5	50	45
7	DATA_pad<5>	-3108.55	-276.5	50	45
8	DATA_pad<4>	-3021.85	-276.5	50	45
9	DATA_pad<3>	-2956.85	-276.5	50	45
10	DATA_pad<2>	-2870.15	-276.5	50	45
11	DATA_pad<1>	-2805.15	-276.5	50	45
12	DATA_pad<0>	-2718.45	-276.5	50	45
13	RSTB_pad	-2644.65	-276.5	50	45
14	WR_pad<0>	-2579.65	-276.5	50	45
15	VDDX	-2514.65	-276.5	50	45
16	WR_pad<1>	-2449.65	-276.5	50	45
17	CD_pad	-2384.65	-276.5	50	45
18	CS_pad<0>	-2319.65	-276.5	50	45
19	VDDX	-2254.65	-276.5	50	45
20	CS_pad<1>	-2189.65	-276.5	50	45
21	BM_pad<0>	-2117.85	-276.5	50	45
22	VDDX	-2052.85	-276.5	50	45
23	BM_pad<1>	-1987.85	-276.5	50	45
24	ID_pad	-1922.85	-276.5	50	45
25	VDDX	-1857.85	-276.5	50	45
26	POR_dis_pad	-1792.85	-276.5	50	45
27	VSS	-1718.75	-276.5	50	45
28	VSS	-1653.75	-276.5	50	45
29	VSS	-1588.75	-276.5	50	45
30	VSS	-1523.75	-276.5	50	45
31	VSS	-1458.75	-276.5	50	45
32	VSS	-1393.75	-276.5	50	45
33	DUMMY7	-1301.6	-276.5	50	45
34	DUMMY8	-1236.6	-276.5	50	45
35	DUMMY9	-1171.6	-276.5	50	45
36	VSS2	-1079.45	-276.5	50	45
37	VSS2	-1014.45	-276.5	50	45
38	VSS2	-949.45	-276.5	50	45
39	VSS2	-884.45	-276.5	50	45
40	VSS2	-819.45	-276.5	50	45
41	VSS2	-754.45	-276.5	50	45
42	DUMMY10	-669.8	-276.5	50	45
43	DUMMY11	-604.8	-276.5	50	45
44	DUMMY12	-522.3	-276.5	50	45
45	DUMMY13	-457.3	-276.5	50	45
46	DUMMY14	-392.3	-276.5	50	45
47	VDD	-320.15	-276.5	50	45
48	VDD	-255.15	-276.5	50	45
49	VDD	-190.15	-276.5	50	45

#	PAD	X	Y	W	H
50	VDD	-125.15	-276.5	50	45
51	VDD	-60.15	-276.5	50	45
52	VDD	18.7	-276.5	50	45
53	VDD2	105.4	-276.5	50	45
54	VDD2	184.25	-276.5	50	45
55	VDD2	249.25	-276.5	50	45
56	VDD2	314.25	-276.5	50	45
57	VDD2	379.25	-276.5	50	45
58	VDD3	444.25	-276.5	50	45
59	VDD3	509.25	-276.5	50	45
60	VDD3	574.25	-276.5	50	45
61	VDD3	639.25	-276.5	50	45
62	VDD3	712.65	-276.5	50	45
63	TST4_pad	893	-276.5	50	45
64	TST4_pad	958	-276.5	50	45
65	TST4_pad	1034	-276.5	50	45
66	TST4_pad	1099	-276.5	50	45
67	TST2_pad	1164	-276.5	50	45
68	TST2_pad	1265.45	-276.5	50	45
69	VBP_pad<0>	1385.35	-276.5	50	45
70	VBP_pad<0>	1450.35	-276.5	50	45
71	VBP_pad<0>	1525.5	-276.5	50	45
72	VBP_pad<0>	1590.5	-276.5	50	45
73	VBP_pad<1>	1655.5	-276.5	50	45
74	VBP_pad<1>	1720.5	-276.5	50	45
75	VBP_pad<1>	1795.65	-276.5	50	45
76	VBP_pad<1>	1860.65	-276.5	50	45
77	VBN_pad<1>	1942.65	-276.5	50	45
78	VBN_pad<1>	2007.65	-276.5	50	45
79	VBN_pad<1>	2082.8	-276.5	50	45
80	VBN_pad<1>	2147.8	-276.5	50	45
81	VBN_pad<0>	2212.8	-276.5	50	45
82	VBN_pad<0>	2277.8	-276.5	50	45
83	VBN_pad<0>	2352.95	-276.5	50	45
84	VBN_pad<0>	2417.95	-276.5	50	45
85	VLCDIN_pad	2501.95	-276.5	50	45
86	VLCDIN_pad	2566.95	-276.5	50	45
87	VLCDIN_pad	2663.95	-276.5	50	45
88	VLCDIN_pad	2728.95	-276.5	50	45
89	VLCDOUT_pad	2793.95	-276.5	50	45
90	VLCDOUT_pad	2858.95	-276.5	50	45
91	VLCDOUT_pad	2934.95	-276.5	50	45
92	VLCDOUT_pad	2999.95	-276.5	50	45
93	DUMMY15	3064.95	-276.5	50	45
94	DUMMY16	3129.95	-276.5	50	45
95	DUMMY17	3194.95	-276.5	50	45
96	DUMMY18	3259.95	-276.5	50	45
97	DUMMY19	3324.95	-276.5	50	45
98	DUMMY20	3389.95	-276.5	50	45

#	PAD	X	Y	W	H
99	DUMMY21	3536	-276.5	50	45
100	DUMMY22	3601	-276.5	50	45
101	DUMMY3	3666	-276.5	50	45
102	DUMMY4	3704.2	243	15.6	100
103	COMS_PAD	3676.6	243	15.6	100
104	COM_pad<64>	3649	243	15.6	100
105	COM_pad<62>	3621.4	243	15.6	100
106	COM_pad<60>	3593.8	243	15.6	100
107	COM_pad<58>	3566.2	243	15.6	100
108	COM_pad<56>	3538.6	243	15.6	100
109	COM_pad<54>	3511	243	15.6	100
110	COM_pad<52>	3483.4	243	15.6	100
111	COM_pad<50>	3455.8	243	15.6	100
112	COM_pad<48>	3428.2	243	15.6	100
113	COM_pad<46>	3400.6	243	15.6	100
114	COM_pad<44>	3373	243	15.6	100
115	COM_pad<42>	3345.4	243	15.6	100
116	COM_pad<40>	3317.8	243	15.6	100
117	COM_pad<38>	3290.2	243	15.6	100
118	COM_pad<36>	3262.6	243	15.6	100
119	COM_pad<34>	3235	243	15.6	100
120	COM_pad<32>	3207.4	243	15.6	100
121	COM_pad<30>	3179.8	243	15.6	100
122	COM__pad<28>	3152.2	243	15.6	100
123	COM_pad<26>	3124.6	243	15.6	100
124	COM_pad<24>	3097	243	15.6	100
125	COM_pad<22>	3069.4	243	15.6	100
126	COM_pad<20>	3041.8	243	15.6	100
127	COM_pad<18>	3014.2	243	15.6	100
128	COM_pad<16>	2986.6	243	15.6	100
129	COM_pad<14>	2959	243	15.6	100
130	COM_pad<12>	2931.4	243	15.6	100
131	COM_pad<10>	2903.8	243	15.6	100
132	COM_pad<8>	2876.2	243	15.6	100
133	COM_pad<6>	2848.6	243	15.6	100
134	COM_pad<4>	2821	243	15.6	100
135	COM_pad<2>	2793.4	243	15.6	100
136	SEG_pad<1>	2613.2	235.5	15.6	115
137	SEG_pad<2>	2585.6	235.5	15.6	115
138	SEG_pad<3>	2558	235.5	15.6	115
139	SEG_pad<4>	2530.4	235.5	15.6	115
140	SEG_pad<5>	2502.8	235.5	15.6	115
141	SEG_pad<6>	2475.2	235.5	15.6	115
142	SEG_pad<7>	2447.6	235.5	15.6	115
143	SEG_pad<8>	2420	235.5	15.6	115
144	SEG_pad<9>	2392.4	235.5	15.6	115
145	SEG_pad<10>	2364.8	235.5	15.6	115
146	SEG_pad<11>	2337.2	235.5	15.6	115
147	SEG_pad<12>	2309.6	235.5	15.6	115
148	SEG_pad<13>	2282	235.5	15.6	115

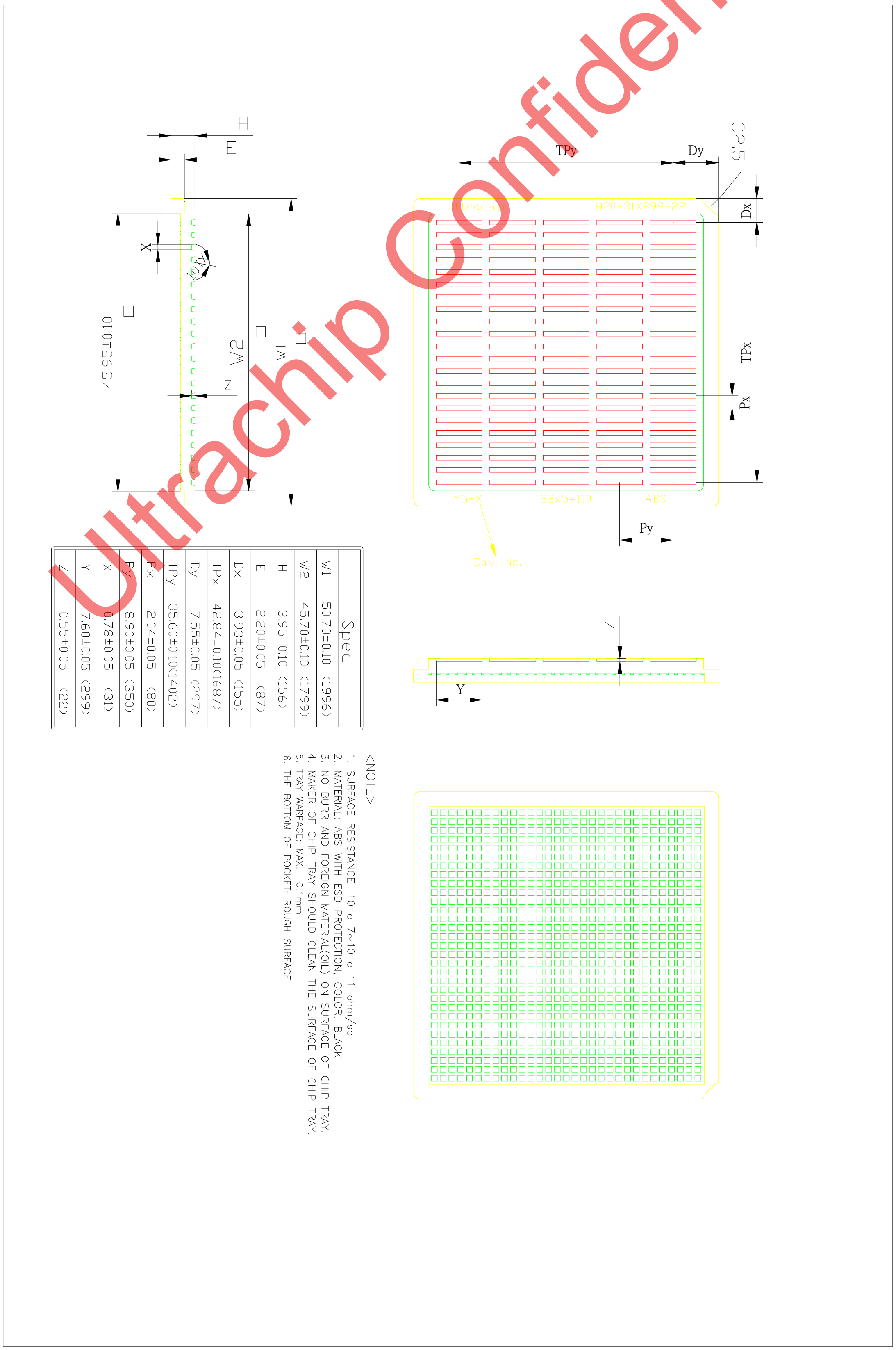
#	PAD	X	Y	W	H
149	SEG_pad<14>	2254.4	235.5	15.6	115
150	SEG_pad<15>	2226.8	235.5	15.6	115
151	SEG_pad<16>	2199.2	235.5	15.6	115
152	SEG_pad<17>	2171.6	235.5	15.6	115
153	SEG_pad<18>	2144	235.5	15.6	115
154	SEG_pad<19>	2116.4	235.5	15.6	115
155	SEG_pad<20>	2088.8	235.5	15.6	115
156	SEG_pad<21>	2061.2	235.5	15.6	115
157	SEG_pad<22>	2033.6	235.5	15.6	115
158	SEG_pad<23>	2006	235.5	15.6	115
159	SEG_pad<24>	1978.4	235.5	15.6	115
160	SEG_pad<25>	1950.8	235.5	15.6	115
161	SEG_pad<26>	1923.2	235.5	15.6	115
162	SEG_pad<27>	1895.6	235.5	15.6	115
163	SEG_pad<28>	1868	235.5	15.6	115
164	SEG_pad<29>	1840.4	235.5	15.6	115
165	SEG_pad<30>	1812.8	235.5	15.6	115
166	SEG_pad<31>	1785.2	235.5	15.6	115
167	SEG_pad<32>	1757.6	235.5	15.6	115
168	SEG_pad<33>	1730	235.5	15.6	115
169	SEG_pad<34>	1702.4	235.5	15.6	115
170	SEG_pad<35>	1674.8	235.5	15.6	115
171	SEG_pad<36>	1647.2	235.5	15.6	115
172	SEG_pad<37>	1619.6	235.5	15.6	115
173	SEG_pad<38>	1592	235.5	15.6	115
174	SEG_pad<39>	1564.4	235.5	15.6	115
175	SEG_pad<40>	1536.8	235.5	15.6	115
176	SEG_pad<41>	1509.2	235.5	15.6	115
177	SEG_pad<42>	1481.6	235.5	15.6	115
178	SEG_pad<43>	1454	235.5	15.6	115
179	SEG_pad<44>	1426.4	235.5	15.6	115
180	SEG_pad<45>	1398.8	235.5	15.6	115
181	SEG_pad<46>	1371.2	235.5	15.6	115
182	SEG_pad<47>	1343.6	235.5	15.6	115
183	SEG_pad<48>	1316	235.5	15.6	115
184	SEG_pad<49>	1288.4	235.5	15.6	115
185	SEG_pad<50>	1260.8	235.5	15.6	115
186	SEG_pad<51>	1233.2	235.5	15.6	115
187	SEG_pad<52>	1205.6	235.5	15.6	115
188	SEG_pad<53>	1178	235.5	15.6	115
189	SEG_pad<54>	1150.4	235.5	15.6	115
190	SEG_pad<55>	1122.8	235.5	15.6	115
191	SEG_pad<56>	1095.2	235.5	15.6	115
192	SEG_pad<57>	1067.6	235.5	15.6	115
193	SEG_pad<58>	1040	235.5	15.6	115
194	SEG_pad<59>	1012.4	235.5	15.6	115
195	SEG_pad<60>	984.8	235.5	15.6	115
196	SEG_pad<61>	957.2	235.5	15.6	115
197	SEG_pad<62>	929.6	235.5	15.6	115
198	SEG_pad<63>	902	235.5	15.6	115

#	PAD	X	Y	W	H
199	SEG_pad<64>	874.4	235.5	15.6	115
200	SEG_pad<65>	846.8	235.5	15.6	115
201	SEG_pad<66>	819.2	235.5	15.6	115
202	SEG_pad<67>	791.6	235.5	15.6	115
203	SEG_pad<68>	764	235.5	15.6	115
204	SEG_pad<69>	736.4	235.5	15.6	115
205	SEG_pad<70>	708.8	235.5	15.6	115
206	SEG_pad<71>	681.2	235.5	15.6	115
207	SEG_pad<72>	653.6	235.5	15.6	115
208	SEG_pad<73>	626	235.5	15.6	115
209	SEG_pad<74>	598.4	235.5	15.6	115
210	SEG_pad<75>	570.8	235.5	15.6	115
211	SEG_pad<76>	543.2	235.5	15.6	115
212	SEG_pad<77>	515.6	235.5	15.6	115
213	SEG_pad<78>	488	235.5	15.6	115
214	SEG_pad<79>	460.4	235.5	15.6	115
215	SEG_pad<80>	432.8	235.5	15.6	115
216	SEG_pad<81>	405.2	235.5	15.6	115
217	SEG_pad<82>	377.6	235.5	15.6	115
218	SEG_pad<83>	350	235.5	15.6	115
219	SEG_pad<84>	322.4	235.5	15.6	115
220	SEG_pad<85>	294.8	235.5	15.6	115
221	SEG_pad<86>	267.2	235.5	15.6	115
222	SEG_pad<87>	239.6	235.5	15.6	115
223	SEG_pad<88>	212	235.5	15.6	115
224	SEG_pad<89>	184.4	235.5	15.6	115
225	SEG_pad<90>	156.8	235.5	15.6	115
226	SEG_pad<91>	129.2	235.5	15.6	115
227	SEG_pad<92>	101.6	235.5	15.6	115
228	SEG_pad<93>	74	235.5	15.6	115
229	SEG_pad<94>	46.4	235.5	15.6	115
230	SEG_pad<95>	18.8	235.5	15.6	115
231	SEG_pad<96>	-8.8	235.5	15.6	115
232	SEG_pad<97>	-36.4	235.5	15.6	115
233	SEG_pad<98>	-64	235.5	15.6	115
234	SEG_pad<99>	-91.6	235.5	15.6	115
235	SEG_pad<100>	-119.2	235.5	15.6	115
236	SEG_pad<101>	-146.8	235.5	15.6	115
237	SEG_pad<102>	-174.4	235.5	15.6	115
238	SEG_pad<103>	-202	235.5	15.6	115
239	SEG_pad<104>	-229.6	235.5	15.6	115
240	SEG_pad<105>	-257.2	235.5	15.6	115
241	SEG_pad<106>	-284.8	235.5	15.6	115
242	SEG_pad<107>	-312.4	235.5	15.6	115
243	SEG_pad<108>	-340	235.5	15.6	115
244	SEG_pad<109>	-367.6	235.5	15.6	115
245	SEG_pad<110>	-395.2	235.5	15.6	115
246	SEG_pad<111>	-422.8	235.5	15.6	115
247	SEG_pad<112>	-450.4	235.5	15.6	115
248	SEG_pad<113>	-478	235.5	15.6	115

#	PAD	X	Y	W	H
249	SEG_pad<114>	-505.6	235.5	15.6	115
250	SEG_pad<115>	-533.2	235.5	15.6	115
251	SEG_pad<116>	-560.8	235.5	15.6	115
252	SEG_pad<117>	-588.4	235.5	15.6	115
253	SEG_pad<118>	-616	235.5	15.6	115
254	SEG_pad<119>	-643.6	235.5	15.6	115
255	SEG_pad<120>	-671.2	235.5	15.6	115
256	SEG_pad<121>	-698.8	235.5	15.6	115
257	SEG_pad<122>	-726.4	235.5	15.6	115
258	SEG_pad<123>	-754	235.5	15.6	115
259	SEG_pad<124>	-781.6	235.5	15.6	115
260	SEG_pad<125>	-809.2	235.5	15.6	115
261	SEG_pad<126>	-836.8	235.5	15.6	115
262	SEG_pad<127>	-864.4	235.5	15.6	115
263	SEG_pad<128>	-892	235.5	15.6	115
264	SEG_pad<129>	-919.6	235.5	15.6	115
265	SEG_pad<130>	-947.2	235.5	15.6	115
266	SEG_pad<131>	-974.8	235.5	15.6	115
267	SEG_pad<132>	-1002.4	235.5	15.6	115
268	SEG_pad<133>	-1030	235.5	15.6	115
269	SEG_pad<134>	-1057.6	235.5	15.6	115
270	SEG_pad<135>	-1085.2	235.5	15.6	115
271	SEG_pad<136>	-1112.8	235.5	15.6	115
272	SEG_pad<137>	-1140.4	235.5	15.6	115
273	SEG_pad<138>	-1168	235.5	15.6	115
274	SEG_pad<139>	-1195.6	235.5	15.6	115
275	SEG_pad<140>	-1223.2	235.5	15.6	115
276	SEG_pad<141>	-1250.8	235.5	15.6	115
277	SEG_pad<142>	-1278.4	235.5	15.6	115
278	SEG_pad<143>	-1306	235.5	15.6	115
279	SEG_pad<144>	-1333.6	235.5	15.6	115
280	SEG_pad<145>	-1361.2	235.5	15.6	115
281	SEG_pad<146>	-1388.8	235.5	15.6	115
282	SEG_pad<147>	-1416.4	235.5	15.6	115
283	SEG_pad<148>	-1444	235.5	15.6	115
284	SEG_pad<149>	-1471.6	235.5	15.6	115
285	SEG_pad<150>	-1499.2	235.5	15.6	115
286	SEG_pad<151>	-1526.8	235.5	15.6	115
287	SEG_pad<152>	-1554.4	235.5	15.6	115
288	SEG_pad<153>	-1582	235.5	15.6	115
289	SEG_pad<154>	-1609.6	235.5	15.6	115
290	SEG_pad<155>	-1637.2	235.5	15.6	115
291	SEG_pad<156>	-1664.8	235.5	15.6	115
292	SEG_pad<157>	-1692.4	235.5	15.6	115
293	SEG_pad<158>	-1720	235.5	15.6	115
294	SEG_pad<159>	-1747.6	235.5	15.6	115
295	SEG_pad<160>	-1775.2	235.5	15.6	115
296	SEG_pad<161>	-1802.8	235.5	15.6	115
297	SEG_pad<162>	-1830.4	235.5	15.6	115
298	SEG_pad<163>	-1858	235.5	15.6	115

#	PAD	X	Y	W	H
299	SEG_pad<164>	-1885.6	235.5	15.6	115
300	SEG_pad<165>	-1913.2	235.5	15.6	115
301	SEG_pad<166>	-1940.8	235.5	15.6	115
302	SEG_pad<167>	-1968.4	235.5	15.6	115
303	SEG_pad<168>	-1996	235.5	15.6	115
304	SEG_pad<169>	-2023.6	235.5	15.6	115
305	SEG_pad<170>	-2051.2	235.5	15.6	115
306	SEG_pad<171>	-2078.8	235.5	15.6	115
307	SEG_pad<172>	-2106.4	235.5	15.6	115
308	SEG_pad<173>	-2134	235.5	15.6	115
309	SEG_pad<174>	-2161.6	235.5	15.6	115
310	SEG_pad<175>	-2189.2	235.5	15.6	115
311	SEG_pad<176>	-2216.8	235.5	15.6	115
312	SEG_pad<177>	-2244.4	235.5	15.6	115
313	SEG_pad<178>	-2272	235.5	15.6	115
314	SEG_pad<179>	-2299.6	235.5	15.6	115
315	SEG_pad<180>	-2327.2	235.5	15.6	115
316	SEG_pad<181>	-2354.8	235.5	15.6	115
317	SEG_pad<182>	-2382.4	235.5	15.6	115
318	SEG_pad<183>	-2410	235.5	15.6	115
319	SEG_pad<184>	-2437.6	235.5	15.6	115
320	SEG_pad<185>	-2465.2	235.5	15.6	115
321	SEG_pad<186>	-2492.8	235.5	15.6	115
322	SEG_pad<187>	-2520.4	235.5	15.6	115
323	SEG_pad<188>	-2548	235.5	15.6	115
324	SEG_pad<189>	-2575.6	235.5	15.6	115
325	SEG_pad<190>	-2603.2	235.5	15.6	115
326	SEG_pad<191>	-2630.8	235.5	15.6	115
327	SEG_pad<192>	-2658.4	235.5	15.6	115
328	COMS_PAD	-2793.9	243	15.6	100
329	COM_pad<1>	-2821.5	243	15.6	100
330	COM_pad<3>	-2849.1	243	15.6	100
331	COM_pad<5>	-2876.7	243	15.6	100
332	COM_pad<7>	-2904.3	243	15.6	100
333	COM_pad<9>	-2931.9	243	15.6	100
334	COM_pad<11>	-2959.5	243	15.6	100
335	COM_pad<13>	-2987.1	243	15.6	100
336	COM_pad<15>	-3014.7	243	15.6	100
337	COM_pad<17>	-3042.3	243	15.6	100
338	COM_pad<19>	-3069.9	243	15.6	100
339	COM_pad<21>	-3097.5	243	15.6	100
340	COM_pad<23>	-3125.1	243	15.6	100
341	COM_pad<25>	-3152.7	243	15.6	100
342	COM__pad<27>	-3180.3	243	15.6	100
343	COM_pad<29>	-3207.9	243	15.6	100
344	COM_pad<31>	-3235.5	243	15.6	100
345	COM_pad<33>	-3263.1	243	15.6	100
346	COM_pad<35>	-3290.7	243	15.6	100
347	COM_pad<37>	-3318.3	243	15.6	100
348	COM_pad<39>	-3345.9	243	15.6	100
349	COM_pad<41>	-3373.5	243	15.6	100
350	COM_pad<43>	-3401.1	243	15.6	100
351	COM_pad<45>	-3428.7	243	15.6	100
352	COM_pad<47>	-3456.3	243	15.6	100
353	COM_pad<49>	-3483.9	243	15.6	100
354	COM_pad<51>	-3511.5	243	15.6	100
355	COM_pad<53>	-3539.1	243	15.6	100
356	COM_pad<55>	-3566.7	243	15.6	100
357	COM_pad<57>	-3594.3	243	15.6	100
358	COM_pad<59>	-3621.9	243	15.6	100
359	COM_pad<61>	-3649.5	243	15.6	100
360	COM_pad<63>	-3677.1	243	15.6	100
361	DUMMY1	-3704.7	243	15.6	100

TRAY INFORMATION



REVISION HISTORY

Revision	Contents	Date
0.6	First Release	Jun. 8, 2012
0.8	(1) The tray drawing presents. (2) The VLCD Quick Reference section is updated. (3) The Maximum Power Consumption data present. (4) Some AC timings are updated.	Jul. 24, 2012
1.0	MTP-Read related descriptions are revised.	Aug. 3, 2012
1.1	CL: 25V → 16V	Oct. 2, 2012