ST7302

Ultra-Low Power Active Matrix 240 x 320 Mono TFT Display Driver with Controller

Datasheet

Version 0.0

LIST OF CONTENT

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

The ST7302 is a single-chip controller/driver for small and medium TFT LCD display that operate at very low frame frequency to conserve power. This chip is capable of supporting up to 240H x 320V pixels and provides a standard 8-bit 8080 parallel interface, 3-wire SPI serial interface, single/dual 4-wire SPI serial interface and 2-data lane serial interface to configure the system and update the graphics content.

ST7302 is controlled using a conventional mobile driver SoC interface which supports an interface I/O voltage (VDDI) of 1.8V ~ 3.3V. ST7302 is equipped with all required charge pumps, buffer amplifiers and regulators to run directly from an unregulated coin cell battery source (Normal mode VDDA: 2.8V ~ 3.3V; 1.8V mode VDDA=1.8V). All voltages used by the TFT channel drivers are close loop regulated by ST7302 and can be adjusted in fine increments by user controlled digital register settings to optimize power and display characteristics. The built-in timing controller (TCON) supports a wide range of output timing for various pixel organizations and driver waveform generation. The combination of timing and voltage controls allows the ST7302 driver SoC to have wide compatibility with various LCD and TFT types.

2 FEATURES

Design for Low Power Active Matrix a-Si TFT Display

Single-chip TFT-LCD Controller/Driver with On-chip Frame Memory

Support for up to 240H x 320V Mono pixels

Support multiple frame rate (0.25Hz ~ 32 Hz)

Supports multiple LCD modes

- ECB or MTN
- Normally black or white

Built-in 240 x 320 x 1b internal SRAM

Frame inversion AC drive of TFTs at low refresh rates

Built-in Sequential Gate Scan Function

Microprocessor Interface

- 80 parallel 8bits
- 3/ 4-line serial interface support write-operation and read-status
- 2-data-lane serial interface

Wide Power Supply Range

- Normal Mode

  VDDI(Digital) : 1.8V ~ 3.3V

  VDDA(Analog): 2.8 ~ 3.3V
- 1.8V Mode

  VDDI(Digital)=VDDA(Analog)=1.8V

On-chip power management system

Built in charge pump circuits

- 2x boost generates: 5.5V (Normal Mode)
- High voltage +15V/-10V charge pump

Built in low power analog circuit

- On-chip oscillator circuit.
- Built-in voltage regulator with programmable contrast
- On-chip power system
  - VCOM level

    VCOMH: 3V~5V (50mV step)

    VCOML: GND
  - Source voltage

    VSH: +3V~+5V (50mV step)

    VSL: 0V~+2.5V (50mV step)
  - Gate voltage

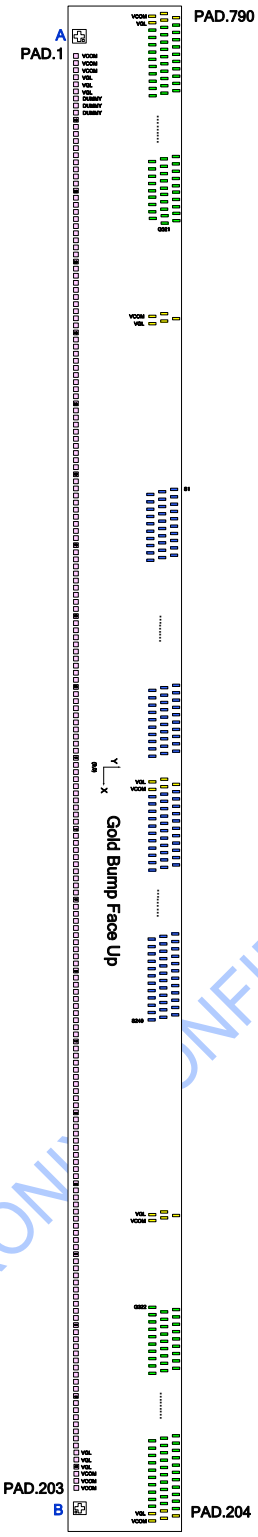
    VGH: +8V~+15V (0.5V step)

VGL: -5V~-10V (0.5V step)

- Generates 5 DC levels
  - Gate levels: VGH, VGL
  - Source levels: VSH, VSL
  - COM levels: VCOMH
- **Built-in NV memory for VSH/VSL amplitude adjustment and ID setting.**
- **COG packaging**
- **Wide operating temperature range: -30°C ~ +70°C**

3 PAD ARRANGEMENT

3.1 Configuration of Signal Pads



ST7302	
Chip Size	13000(X) x 650(Y)
Chip Thinness	200
Bump Height	9
Output Pad	13(X) x 95(Y)
I/O Pad	40(X) x 50(Y)

Unit: um

Figure 3-1 Chip

3.2 Bump

3.2.1 Output Pads

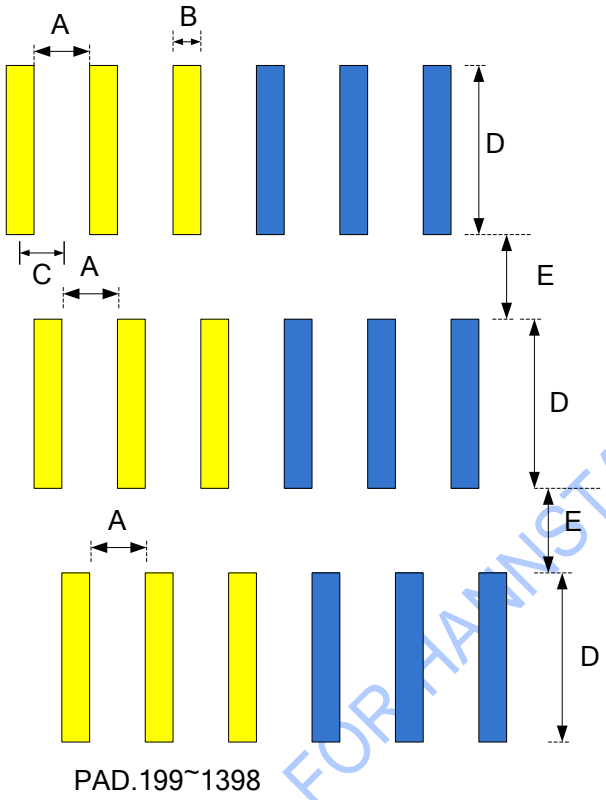
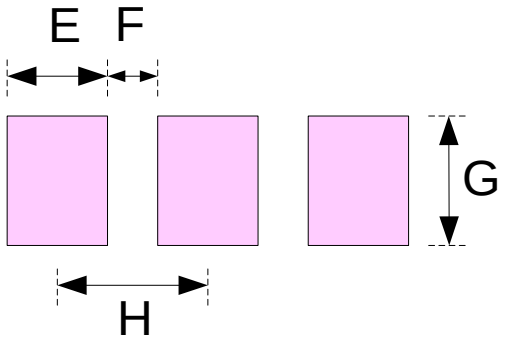


Figure 3-2 Output Pads Outline

Symbol	Item	Size (um)
A	Bump Gap (H)	17
B	Bump Width	13
C	Bump Pitch	10
D	Bump Height	95
E	Bump Gap (V)	20

3.2.2 Input Pads



Symbol	Item	Size (um)
E	Bump Width	40
F	Bump Gap	20
G	Bump Height	50
H	Bump Pitch	60

Figure 3-3 Input Pads Outline

3.2.3 Alignment Marks

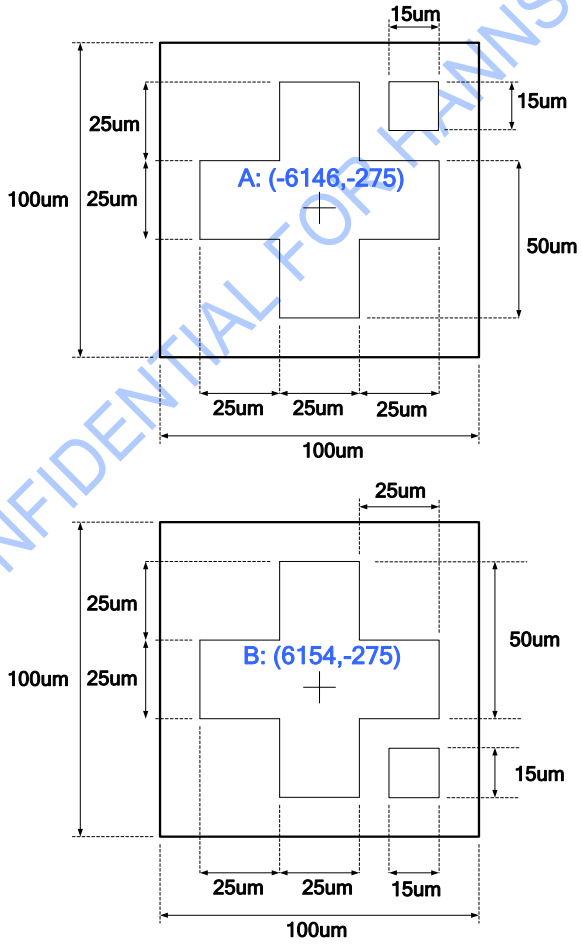


Figure 4 Alignment Marks Outline

4 PAD CENTER COORDINATES

PAD.	Name	X	Y
1	VCOM	-6056	-292.62
2	VCOM	-5996	-292.62
3	VCOM	-5936	-292.62
4	VGL	-5876	-292.62
5	VGL	-5816	-292.62
6	VGL	-5756	-292.62
7	DUMMY	-5696	-292.62
8	DUMMY	-5636	-292.62
9	DUMMY	-5576	-292.62
10	DUMMY	-5516	-292.62
11	DUMMY	-5456	-292.62
12	DUMMY	-5396	-292.62
13	DUMMY	-5336	-292.62
14	DUMMY	-5276	-292.62
15	VCOM	-5216	-292.62
16	VCOM	-5156	-292.62
17	VCOM	-5096	-292.62
18	VCOM	-5036	-292.62
19	VCOM	-4976	-292.62
20	VCOM	-4916	-292.62
21	VDDA	-4856	-292.62
22	VDDA	-4796	-292.62
23	VDDA	-4736	-292.62
24	VAGND	-4676	-292.62
25	VAGND	-4616	-292.62
26	VAGND	-4556	-292.62
27	VSI	-4496	-292.62
28	VSI	-4436	-292.62
29	VSK	-4376	-292.62
30	VSK	-4316	-292.62
31	CA1N	-4256	-292.62
32	CA1N	-4196	-292.62
33	CA1N	-4136	-292.62
34	CA1N	-4076	-292.62
35	CA1N	-4016	-292.62
36	CA1N	-3956	-292.62
37	CA1P	-3896	-292.62
38	CA1P	-3836	-292.62
39	CA1P	-3776	-292.62
40	CA1P	-3716	-292.62
41	CA1P	-3656	-292.62
42	CA1P	-3596	-292.62
43	VMV	-3536	-292.62
44	VMV	-3476	-292.62
45	VMV	-3416	-292.62
46	VMV	-3356	-292.62
47	VMV	-3296	-292.62
48	VMV	-3236	-292.62
49	CA2P	-3176	-292.62
50	CA2P	-3116	-292.62
51	CA2P	-3056	-292.62
52	CA2P	-2996	-292.62
53	CA2P	-2936	-292.62
54	CA2P	-2876	-292.62
55	CA2N	-2816	-292.62
56	CA2N	-2756	-292.62
57	CA2N	-2696	-292.62
58	CA2N	-2636	-292.62
59	CA2N	-2576	-292.62
60	CA2N	-2516	-292.62
61	CB1N	-2456	-292.62
62	CB1N	-2396	-292.62
63	CB1N	-2336	-292.62
64	CB1N	-2276	-292.62
65	CB1P	-2216	-292.62
66	CB1P	-2156	-292.62
67	CB1P	-2096	-292.62
68	CB1P	-2036	-292.62
69	AVDD	-1976	-292.62
70	AVDD	-1916	-292.62
71	AVDD	-1856	-292.62
72	AVDD	-1796	-292.62
73	AVDD	-1736	-292.62
74	AVDD	-1676	-292.62
75	CB2P	-1616	-292.62
76	CB2P	-1556	-292.62
77	CB2P	-1496	-292.62
78	CB2P	-1436	-292.62
79	CB2N	-1376	-292.62
80	CB2N	-1316	-292.62
81	CB2N	-1256	-292.62
82	CB2N	-1196	-292.62
83	CC1N	-1136	-292.62
84	CC1N	-1076	-292.62
85	CC1P	-1016	-292.62
86	CC1P	-956	-292.62
87	CC2P	-896	-292.62
88	CC2P	-836	-292.62
89	CC2N	-776	-292.62
90	CC2N	-716	-292.62
91	VGH	-656	-292.62
92	VGH	-596	-292.62
93	CD1P	-536	-292.62
94	CD1P	-476	-292.62
95	CD1N	-416	-292.62
96	CD1N	-356	-292.62
97	CD2N	-296	-292.62
98	CD2N	-236	-292.62
99	CD2P	-176	-292.62

PAD.	Name	X	Y
100	CD2P	-116	-292.62
101	VGL	-56	-292.62
102	VGL	4	-292.62
103	VSH	64	-292.62
104	VSH	124	-292.62
105	VSL	184	-292.62
106	VSL	244	-292.62
107	VCOMH	304	-292.62
108	VCOMH	364	-292.62
109	VCOML	424	-292.62
110	VCOML	484	-292.62
111	VMREF	544	-292.62
112	VMREF	604	-292.62
113	VCCO	664	-292.62
114	VCCO	724	-292.62
115	VCCI	784	-292.62
116	VCCI	844	-292.62
117	VDDA	904	-292.62
118	VDDA	964	-292.62
119	VDDA	1024	-292.62
120	VDDA	1084	-292.62
121	VDDA	1144	-292.62
122	VDDA	1204	-292.62
123	VDDR	1264	-292.62
124	VDDR	1324	-292.62
125	VDDI	1384	-292.62
126	VDDI	1444	-292.62
127	VDDI	1504	-292.62
128	VDDI	1564	-292.62
129	VDGND	1624	-292.62
130	VDGND	1684	-292.62
131	VDGND	1744	-292.62
132	VDGND	1804	-292.62
133	VAGND	1864	-292.62
134	VAGND	1924	-292.62
135	VAGND	1984	-292.62
136	VAGND	2044	-292.62
137	VAGND	2104	-292.62
138	VAGND	2164	-292.62
139	VRGND	2224	-292.62
140	VRGND	2284	-292.62
141	VDDI	2344	-292.62
142	CSB	2404	-292.62
143	A0	2464	-292.62
144	ERD	2524	-292.62
145	RWR	2584	-292.62
146	DUMMY	2644	-292.62
147	DUMMY	2704	-292.62
148	DUMMY	2764	-292.62
149	DUMMY	2824	-292.62
150	RSTB	2884	-292.62
151	VDGND	2944	-292.62
152	D0	3004	-292.62
153	D1	3064	-292.62
154	D2	3124	-292.62
155	D3	3184	-292.62
156	D4	3244	-292.62
157	D5	3304	-292.62
158	D6	3364	-292.62
159	D7	3424	-292.62
160	VDDI	3484	-292.62
161	ModeSel	3544	-292.62
162	IF1	3604	-292.62
163	IF0	3664	-292.62
164	CLS	3724	-292.62
165	CL	3784	-292.62
166	TE	3844	-292.62
167	EXTB	3904	-292.62
168	VPP	3964	-292.62
169	VPP	4024	-292.62
170	VPP	4084	-292.62
171	VPP	4144	-292.62
172	VPP	4204	-292.62
173	VPP	4264	-292.62
174	VDGND	4324	-292.62
175	TESTB	4384	-292.62
176	TESTA	4444	-292.62
177	DUMMY	4504	-292.62
178	DUMMY	4564	-292.62
179	DUMMY	4624	-292.62
180	VDDI	4684	-292.62
181	VCOM	4744	-292.62
182	VCOM	4804	-292.62
183	VCOM	4864	-292.62
184	VCOM	4924	-292.62
185	VCOM	4984	-292.62
186	VCOM	5044	-292.62
187	DUMMY	5104	-292.62
188	DUMMY	5164	-292.62
189	DUMMY	5224	-292.62
190	DUMMY	5284	-292.62
191	DUMMY	5344	-292.62
192	DUMMY	5404	-292.62
193	DUMMY	5464	-292.62
194	DUMMY	5524	-292.62
195	DUMMY	5584	-292.62
196	DUMMY	5644	-292.62
197	DUMMY	5704	-292.62
198	VGL	5764	-292.62
199	VGL	5824	-292.62
200	VGL	5884	-292.62
201	VCOM	5944	-292.62

PAD.	Name	X	Y
202	VCOM	6004	-292.62
203	VCOM	6064	-292.62
204	VCOM	6239	35.58
205	VCOM	6229	150.58
206	GTest	6219	265.58
207	VGL	6209	35.58
208	GTest	6119	150.58
209	G2	6189	265.58
210	G4	6179	35.58
211	G6	6169	150.58
212	G8	6159	265.58
213	G10	6149	35.58
214	G12	6139	150.58
215	G14	6129	265.58
216	G16	6119	35.58
217	G18	6109	150.58
218	G20	6099	265.58
219	G22	6089	35.58
220	G24	6079	150.58
221	G26	6069	265.58
222	G28	6059	35.58
223	G30	6049	150.58
224	G32	6039	265.58
225	G34	6029	35.58
226	G36	6019	150.58
227	G38	6009	265.58
228	G40	5999	35.58
229	G42	5989	150.58
230	G44	5979	265.58
231	G46	5969	35.58
232	G48	5959	150.58
233	G50	5949	265.58
234	G52	5939	35.58
235	G54	5929	150.58
236	G56	5919	265.58
237	G58	5909	35.58
238	G60	5899	150.58
239	G62	5889	265.58
240	G64	5879	35.58
241	G66	5869	150.58
242	G68	5859	265.58
243	G70	5849	35.58
244	G72	5839	150.58
245	G74	5829	265.58
246	G76	5819	35.58
247	G78	5809	150.58
248	G80	5799	265.58
249	G82	5789	35.58
250	G84	5779	150.58
251	G86	5769	265.58
252	G88	5759	35.58
253	G90	5749	150.58
254	G92	5739	265.58
255	G94	5729	35.58
256	G96	5719	150.58
257	G98	5709	265.58
258	G100	5699	35.58
259	G102	5689	150.58
260	G104	5679	265.58
261	G106	5669	35.58
262	G108	5659	150.58
263	G110	5649	265.58
264	G112	5639	35.58
265	G114	5629	150.58
266	G116	5619	265.58
267	G118	5609	35.58
268	G120	5599	150.58
269	G122	5589	265.58
270	G124	5579	35.58
271	G126	5569	150.58
272	G128	5559	265.58
273	G130	5549	35.58
274	G132	5539	150.58
275	G134	5529	265.58
276	G136	5519	35.58
277	G138	5509	150.58
278	G140	5499	265.58
279	G142	5489	35.58
280	G144	5479	150.58
281	G146	5469	265.58
282	G148	5459	35.58
283	G150	5449	150.58
284	G152	5439	265.58
285	G154	5429	35.58
286	G156	5419	150.58
287	G158	5409	265.58
288	G160	5399	35.58
289	G162	5389	150.58
290	G164	5379	265.58
291	G166	5369	35.58
292	G168	5359	150.58
293	G170	5349	265.58
294	G172	5339	35.58
295	G174	5329	150.58
296	G176	5319	265.58
297	G178	5309	35.58
298	G180	5299	150.58
299	G182	5289	265.58
300	G184	5279	35.58
301	G186	5269	150.58
302	G188	5259	265.58
303	G190	5249	35.58

PAD.	Name	X	Y
304	G192	5239	150.58
305	G194	5229	265.58
306	G196	5219	35.58
307	G198	5209	150.58
308	G200	5199	265.58
309	G202	5189	35.58
310	G204	5179	150.58
311	G206	5169	265.58
312	G208	5159	35.58
313	G210	5149	150.58
314	G212	5139	265.58
315	G214	5129	35.58
316	G216	5119	150.58
317	G218	5109	265.58
318	G220	5099	35.58
319	G222	5089	150.58
320	G224	5079	265.58
321	G226	5069	35.58
322	G228	5059	150.58
323	G230	5049	265.58
324	G232	5039	35.58
325	G234	5029	150.58
326	G236	5019	265.58
327	G238	5009	35.58
328	G240	4999	150.58
329	G242	4989	265.58
330	G244	4979	35.58
331	G246	4969	150.58
332	G248	4959	265.58
333	G250	4949	35.58
334	G252	4939	150.58
335	G254	4929	265.58
336	G256	4919	35.58
337	G258	4909	150.58
338	G260	4899	265.58
339	G262	4889	35.58
340	G264	4879	150.58
341	G266	4869	265.58
342	G268	4859	35.58
343	G270	4849	150.58
344	G272	4839	265.58
345	G274	4829	35.58
346	G276	4819	150.58
347	G278	4809	265.58
348	G280	4799	35.58
349	G282	4789	150.58
350	G284	4779	265.58
351	G286	4769	35.58
352	G288	4759	150.58
353	G290	4749	265.58
354	G292	4739	35.58
355	G294	4729	150.58
356	G296	4719	265.58
357	G298	4709	35.58
358	G300	4699	150.58
359	G302	4689	265.58
360	G304	4679	35.58
361	G306	4669	150.58
362	G308	4659	265.58
363	G310	4649	35.58
364	G312	4639	150.58
365	G314	4629	265.58
366	G316	4619	35.58
367	G318	4609	150.58
368	G320	4599	265.58
369	G322	4589	35.58
370	VCOM	3779	35.58
371	VCOM	3769	150.58
372	GTest	3759	265.58
373	VGL	3749	35.58
374	GTest	3739	150.58
375	S240	1289	35.58
376	S239	1279	150.58
377	S238	1269	265.58
378	S237	1259	35.58
379	S236	1249	150.58
380	S235	1239	265.58
381	S234	1229	35.58
382	S233	1219	150.58
383	S232	1209	265.58
384	S231	1199	35.58
385	S230	1189	150.58
386	S229	1179	265.58
387	S228	1169	35.58
388	S227	1159	150.58
389	S226	1149	265.58
390	S225	1139	35.58
391	S224	1129	150.58
392	S223	1119	265.58
393	S222	1109	35.58
394	S221	1099	150.58
395	S220	1089	265.58
396	S219	1079	35.58
397	S218	1069	150.58
398	S217	1059	265.58
399	S216	1049	35.58
400	S215	1039	150.58
401	S214	1029	265.58
402	S213	1019	35.58
403	S212	1009	150.58
404	S211	999	265.58
405	S210	989	35.58

PAD.	Name	X	Y
406	S209	979	150.58
407	S208	969	265.58
408	S207	959	35.58
409	S206	949	150.58
410	S205	939	265.58
411	S204	929	35.58
412	S203	919	150.58
413	S202	909	265.58
414	S201	899	35.58
415	S200	889	150.58
416	S199	879	265.58
417	S198	869	35.58
418	S197	859	150.58
419	S196	849	265.58
420	S195	839	35.58
421	S194	829	150.58
422	S193	819	265.58
423	S192	809	35.58
424	S191	799	150.58
425	S190	789	265.58
426	S189	779	35.58
427	S188	769	150.58
428	S187	759	265.58
429	S186	749	35.58
430	S185	739	150.58
431	S184	729	265.58
432	S183	719	35.58
433	S182	709	150.58
434	S181	699	265.58
435	S180	689	35.58
436	S179	679	150.58
437	S178	669	265.58
438	S177	659	35.58
439	S176	649	150.58
440	S175	639	265.58
441	S174	629	35.58
442	S173	619	150.58
443	S172	609	265.58
444	S171	599	35.58
445	S170	589	150.58
446	S169	579	265.58
447	S168	569	35.58
448	S167	559	150.58
449	S166	549	265.58
450	S165	539	35.58
451	S164	529	150.58
452	S163	519	265.58
453	S162	509	35.58
454	S161	499	150.58
455	S160	489	265.58
456	S159	479	35.58
457	S158	469	150.58
458	S157	459	265.58
459	S156	449	35.58
460	S155	439	150.58
461	S154	429	265.58
462	S153	419	35.58
463	S152	409	150.58
464	S151	399	265.58
465	S150	389	35.58
466	S149	379	150.58
467	S148	369	265.58
468	S147	359	35.58
469	S146	349	150.58
470	S145	339	265.58
471	S144	329	35.58
472	S143	319	150.58
473	S142	309	265.58
474	S141	299	35.58
475	S140	289	150.58
476	S139	279	265.58
477	S138	269	35.58
478	S137	259	150.58
479	S136	249	265.58
480	S135	239	35.58
481	S134	229	150.58
482	S133	219	265.58
483	S132	209	35.58
484	S131	199	150.58
485	S130	189	265.58
486	S129	179	35.58
487	S128	169	150.58
488	S127	159	265.58
489	S126	149	35.58
490	S125	139	150.58
491	S124	129	265.58
492	S123	119	35.58
493	S122	109	150.58
494	S121	99	265.58
495	VCOM	89	35.58
496	VCOM	79	150.58
497	GTest	69	265.58
498	VGL	59	35.58
499	GTest	49	150.58
500	S120	-99	35.58
501	S119	-109	150.58
502	S118	-119	265.58
503	S117	-129	35.58
504	S116	-139	150.58
505	S115	-149	265.58
506	S114	-159	35.58
507	S113	-169	150.58

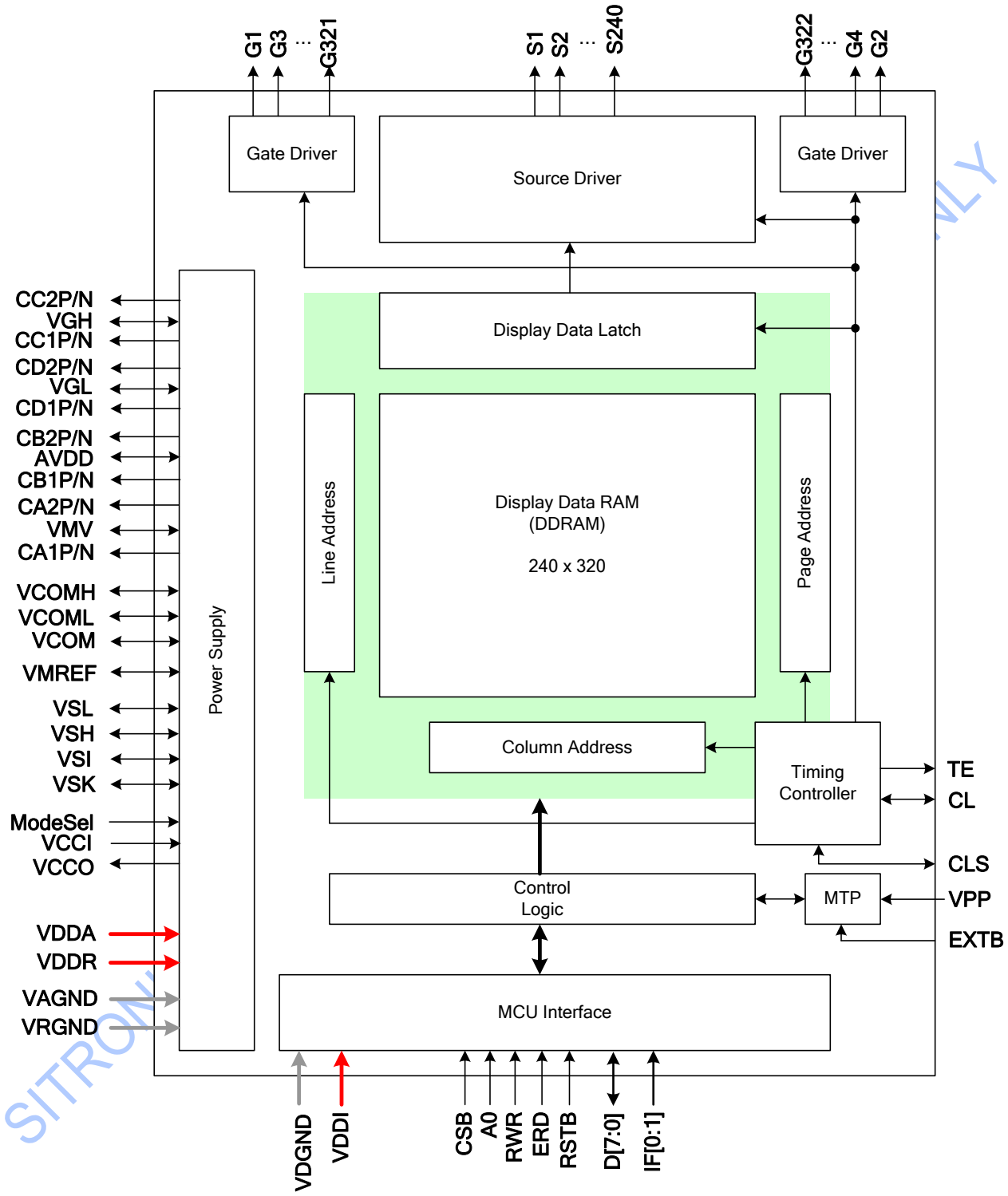
PAD.	Name	X	Y
508	S112	-179	265.58
509	S111	-189	35.58
510	S110	-199	150.58
511	S109	-209	265.58
512	S108	-219	35.58
513	S107	-229	150.58
514	S106	-239	265.58
515	S105	-249	35.58
516	S104	-259	150.58
517	S103	-269	265.58
518	S102	-279	35.58
519	S101	-289	150.58
520	S100	-299	265.58
521	S99	-309	35.58
522	S98	-319	150.58
523	S97	-329	265.58
524	S96	-339	35.58
525	S95	-349	150.58
526	S94	-359	265.58
527	S93	-369	35.58
528	S92	-379	150.58
529	S91	-389	265.58
530	S90	-399	35.58
531	S89	-409	150.58
532	S88	-419	265.58
533	S87	-429	35.58
534	S86	-439	150.58
535	S85	-449	265.58
536	S84	-459	35.58
537	S83	-469	150.58
538	S82	-479	265.58
539	S81	-489	35.58
540	S80	-499	150.58
541	S79	-509	265.58
542	S78	-519	35.58
543	S77	-529	150.58
544	S76	-539	265.58
545	S75	-549	35.58
546	S74	-559	150.58
547	S73	-569	265.58
548	S72	-579	35.58
549	S71	-589	150.58
550	S70	-599	265.58
551	S69	-609	35.58
552	S68	-619	150.58
553	S67	-629	265.58
554	S66	-639	35.58
555	S65	-649	150.58
556	S64	-659	265.58
557	S63	-669	35.58
558	S62	-679	150.58
559	S61	-689	265.58
560	S60	-699	35.58
561	S59	-709	150.58
562	S58	-719	265.58
563	S57	-729	35.58
564	S56	-739	150.58
565	S55	-749	265.58
566	S54	-759	35.58
567	S53	-769	150.58
568	S52	-779	265.58
569	S51	-789	35.58
570	S50	-799	150.58
571	S49	-809	265.58
572	S48	-819	35.58
573	S47	-829	150.58
574	S46	-839	265.58
575	S45	-849	35.58
576	S44	-859	150.58
577	S43	-869	265.58
578	S42	-879	35.58
579	S41	-889	150.58
580	S40	-899	265.58
581	S39	-909	35.58
582	S38	-919	150.58
583	S37	-929	265.58
584	S36	-939	35.58
585	S35	-949	150.58
586	S34	-959	265.58
587	S33	-969	35.58
588	S32	-979	150.58
589	S31	-989	265.58
590	S30	-999	35.58
591	S29	-1009	150.58
592	S28	-1019	265.58
593	S27	-1029	35.58
594	S26	-1039	150.58
595	S25	-1049	265.58
596	S24	-1059	35.58
597	S23	-1069	150.58
598	S22	-1079	265.58
599	S21	-1089	35.58
600	S20	-1099	150.58
601	S19	-1109	265.58
602	S18	-1119	35.58
603	S17	-1129	150.58
604	S16	-1139	265.58
605	S15	-1149	35.58
606	S14	-1159	150.58
607	S13	-1169	265.58
608	S12	-1179	35.58
609	S11	-1189	150.58

PAD.	Name	X	Y
610	S10	-1199	265.58
611	S9	-1209	35.58
612	S8	-1219	150.58
613	S7	-1229	265.58
614	S6	-1239	35.58
615	S5	-1249	150.58
616	S4	-1259	265.58
617	S3	-1269	35.58
618	S2	-1279	150.58
619	S1	-1289	265.58
620	VGL	-3739	35.58
621	GTest	-3749	150.58
622	GTest	-3759	265.58
623	VCOM	-3769	35.58
624	VCOM	-3779	150.58
625	G321	-4589	150.58
626	G319	-4599	265.58
627	G317	-4609	35.58
628	G315	-4619	150.58
629	G313	-4629	265.58
630	G311	-4639	35.58
631	G309	-4649	150.58
632	G307	-4659	265.58
633	G305	-4669	35.58
634	G303	-4679	150.58
635	G301	-4689	265.58
636	G299	-4699	35.58
637	G297	-4709	150.58
638	G295	-4719	265.58
639	G293	-4729	35.58
640	G291	-4739	150.58
641	G289	-4749	265.58
642	G287	-4759	35.58
643	G285	-4769	150.58
644	G283	-4779	265.58
645	G281	-4789	35.58
646	G279	-4799	150.58
647	G277	-4809	265.58
648	G275	-4819	35.58
649	G273	-4829	150.58
650	G271	-4839	265.58
651	G269	-4849	35.58
652	G267	-4859	150.58
653	G265	-4869	265.58
654	G263	-4879	35.58
655	G261	-4889	150.58
656	G259	-4899	265.58
657	G257	-4909	35.58
658	G255	-4919	150.58
659	G253	-4929	265.58
660	G251	-4939	35.58
661	G249	-4949	150.58
662	G247	-4959	265.58
663	G245	-4969	35.58
664	G243	-4979	150.58
665	G241	-4989	265.58
666	G239	-4999	35.58
667	G237	-5009	150.58
668	G235	-5019	265.58
669	G233	-5029	35.58
670	G231	-5039	150.58
671	G229	-5049	265.58
672	G227	-5059	35.58
673	G225	-5069	150.58
674	G223	-5079	265.58
675	G221	-5089	35.58
676	G219	-5099	150.58
677	G217	-5109	265.58
678	G215	-5119	35.58
679	G213	-5129	150.58
680	G211	-5139	265.58
681	G209	-5149	35.58
682	G207	-5159	150.58
683	G205	-5169	265.58
684	G203	-5179	35.58
685	G201	-5189	150.58
686	G199	-5199	265.58
687	G197	-5209	35.58
688	G195	-5219	150.58
689	G193	-5229	265.58
690	G191	-5239	35.58
691	G189	-5249	150.58
692	G187	-5259	265.58
693	G185	-5269	35.58
694	G183	-5279	150.58
695	G181	-5289	265.58
696	G179	-5299	35.58
697	G177	-5309	150.58
698	G175	-5319	265.58
699	G173	-5329	35.58
700	G171	-5339	150.58
701	G169	-5349	265.58
702	G167	-5359	35.58
703	G165	-5369	150.58
704	G163	-5379	265.58
705	G161	-5389	35.58
706	G159	-5399	150.58
707	G157	-5409	265.58
708	G155	-5419	35.58
709	G153	-5429	150.58
710	G151	-5439	265.58
711	G149	-5449	35.58

PAD.	Name	X	Y
712	G147	-5459	150.58
713	G145	-5469	265.58
714	G143	-5479	35.58
715	G141	-5489	150.58
716	G139	-5499	265.58
717	G137	-5509	35.58
718	G135	-5519	150.58
719	G133	-5529	265.58
720	G131	-5539	35.58
721	G129	-5549	150.58
722	G127	-5559	265.58
723	G125	-5569	35.58
724	G123	-5579	150.58
725	G121	-5589	265.58
726	G119	-5599	35.58
727	G117	-5609	150.58
728	G115	-5619	265.58
729	G113	-5629	35.58
730	G111	-5639	150.58
731	G109	-5649	265.58
732	G107	-5659	35.58
733	G105	-5669	150.58
734	G103	-5679	265.58
735	G101	-5689	35.58
736	G99	-5699	150.58
737	G97	-5709	265.58
738	G95	-5719	35.58
739	G93	-5729	150.58
740	G91	-5739	265.58
741	G89	-5749	35.58
742	G87	-5759	150.58
743	G85	-5769	265.58
744	G83	-5779	35.58
745	G81	-5789	150.58
746	G79	-5799	265.58
747	G77	-5809	35.58
748	G75	-5819	150.58
749	G73	-5829	265.58
750	G71	-5839	35.58
751	G69	-5849	150.58
752	G67	-5859	265.58
753	G65	-5869	35.58
754	G63	-5879	150.58
755	G61	-5889	265.58
756	G59	-5899	35.58
757	G57	-5909	150.58
758	G55	-5919	265.58
759	G53	-5929	35.58
760	G51	-5939	150.58
761	G49	-5949	265.58
762	G47	-5959	35.58
763	G45	-5969	150.58
764	G43	-5979	265.58
765	G41	-5989	35.58
766	G39	-5999	150.58
767	G37	-6009	265.58
768	G35	-6019	35.58
769	G33	-6029	150.58
770	G31	-6039	265.58
771	G29	-6049	35.58
772	G27	-6059	150.58
773	G25	-6069	265.58
774	G23	-6079	35.58
775	G21	-6089	150.58
776	G19	-6099	265.58
777	G17	-6109	35.58
778	G15	-6119	150.58
779	G13	-6129	265.58
780	G11	-6139	35.58
781	G9	-6149	150.58
782	G7	-6159	265.58
783	G5	-6169	35.58
784	G3	-6179	150.58
785	G1	-6189	265.58
786	VGL	-6199	35.58
787	GTest	-6209	150.58
788	GTest	-6219	265.58
789	VCOM	-6229	35.58
790	VCOM	-6239	150.58
Mark	ALIGN_L	-6146	-275
Mark	ALIGN_R	6154	-275

Unit: um

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power supply Pin

Name	Type	Description
VDDI	Power	Power Supply (Digital)
VDDA	Power	Power Supply (Analog)
VDDR	Power	Power Supply (Reference)
VCCI/VCCO	Power	VCCI is the power source of digital circuits. VCCO is the VCC output. VCCI and VCCO should be connected together.
ModeSel	I	Power Mode Selection. ModeSel = “VAGND”: 1.8V mode (VDDI=VDDA=1.8V) ModeSel = “VDDA”: Normal mode (VDDI=1.8V~3.6V ; VDDA=2.55~3.6V)
VDGND	Power	Ground (Digital)
VAGND	Power	Ground (Analog)
VRGND	Power	Ground (Reference)

6.2 Digital I/O

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin. When RSTB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>IF[1:0]</td><td>I</td><td>These pins select interface operation mode.
<table>
<tr><th>IF1</th><th>IF0</th><th>MPU interface type</th><th>Command Setting</th></tr>
<tr><td>L</td><td>L</td><td>8-bit 8080 parallel interface</td><td>None</td></tr>
<tr><td rowspan="2">L</td><td rowspan="2">H</td><td>Single 4-line serial interface</td><td>0xE4h, DB4DPI=”0” (default)</td></tr>
<tr><td>Dual 4-line serial interface</td><td>0xE4h, DB4DPI=”1”</td></tr>
<tr><td>H</td><td>L</td><td>2-data-lane serial interface</td><td>None</td></tr>
<tr><td>H</td><td>H</td><td>3-line serial interface</td><td>None</td></tr>
</table></td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pin.
CSB=“L”: This chip is selected and the MPU interface is active.
CSB=“H”: This chip is not selected and the MPU interface is disabled (D[7:0] are high impedance).</td></tr>
<tr><td>A0</td><td>I</td><td>When using 8080, Single 4SPI and Dual 4SPI mode.
It determines whether the access is related to data or command.
A0 = "H": Indicates that D[7:0] are display data;
A0 = "L": Indicates that D[7:0] are control data.
When using 3SPI and 2-Data-Lane mode.
There is no A0 pin in 3-Line and 2-Data-Lane SPI. A0 should be fixed to “H” by VDDI.</td></tr>
</table>

Name	Type	Description
RWR	I	**When using 8080** Write enable in 8080 parallel interface. **When using Dual 4SPI and 2-Data-lane mode.** Second data lane in Dual 4SPI and 2-data-lane serial interface. This pin is not used in 3-Line and Single 4-Line SPI. RWR should be connected to VDDI.
ERD	I	Read enable in 8080 interface. This pin is not used in serial interfaces and should be connected to VDDI.
D[7:0]	I/O	**When using 8-bit parallel interface: 8080 mode** 8 bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor. When CSB is “H”, D[7:0] are high impedance.
	I/O	**When using serial interface: Single/Dual 4-line SPI, 3-line SPI or 2-data-lane mode** D[7:4] : fix to “H” by VDDI. D[3:2] : serial output data (SDA_OUT). D[1] : serial input data (SDA_IN). D[0] : serial input clock (SCLK). **D1 to D3 must be connected together (SDA)** When CSB is “H”, D[7:0] are high impedance.
TE	O	Tearing effect signal is used to synchronize MCU to frame memory writing. If not used, please let this pin open.

Note:

1. After VDDI is turned ON, all MPU interface pins should not be left OPEN.

6.3 Clock System Input

Name	Type	Description
CLS	I	Clock source selection pin. CLS=”H”: enable internal clock. CLS=”L”: disable internal clock and use external clock.
CL	I/O	For external clock. If CLS=”H”: this pin is open. If CLS=”L”: this pin is the input of oscillator.

6.4 Driving Output Pin

Name	Type	Description
S1 to S240	O	Source driver output pins.
G1 to G322	O	Gate driver output pins.
VMREF	O	Monitor pin for internal regulator.
VMV	O	Power output pin for analog circuit.
AVDD	O	Power output pin for analog circuit.
VGH	O	Power output (Positive) pin for gate driver.
VGL	O	Power output (Negative) pin for gate driver.
VSH	O	Power output pin for source driver.
VSL	O	Power output pin for source driver.
VSI	O	Power output pin for source driver.
VSK	O	Power output pin for source driver.
VCOM	O	COM outputs. A power supply for the TFT-LCD common electrode.
VCOMH	O	Positive voltage output of VCOM
VCOML	O	Negative voltage output of VCOM. VCOML must be connected to ground.
CA1P/N CA2P/N	O	Capacitor connecting pins for step-up circuit. (for VMV)
CB1P/N CB2P/N	O	Capacitor connecting pins for step-up circuit. (for AVDD)
CC1P/N CC2P/N	O	Capacitor connecting pins for step-up circuit. (for VGH)
CD1P/N CD2P/N	O	Capacitor connecting pins for step-up circuit. (for VGL)

6.5 MTP Pin

Name	Type	Description
VPP	Power	The programming power supply of the built-in NVM. Apply external power 7.5V here when programming (> 8mA for successful programming). If not used, left this pin open.
EXTB	I	EXTB="L": Enable the extension operation mode. When programming MTP, connect EXTB to VDGND externally. This pin has an internal pull-high resistor. Please leave this pin OPEN after special operation.

6.6 Others

Name	Type	Description
TESTA TESTB	Test	Reserved for test only. Please leave these pins open.
GTest STest	Test	Reserved for test only. Please leave these pins open.
DUMMY	Test	Reserved for test only, Please leave these pins open.

6.7 Recommend Resistance

Item	Pin name	Resistance
Powers	VDDA, VAGND	< 3 ohm
	VDDI, VDGND, VCCO, VCCI	< 50 ohm
	VDDR, VRGND	< 100 ohm
Driving Output	CAxN/P, VMV	< 3 ohm
	CBxN/P, AVDD	< 5 ohm
	VSH, VSL, VSI, VSK	< 20 ohm
	CCxN/P, CDxN/P, VGH, VGL, VCOMH, VCOML, VCOM	< 50 ohm
	VMREF	< 100 ohm
Digital	D[7:0], CSB, RSTB, A0, RWR, ERD	< 100 ohm
	IF[1:0], CLS, CL, TE, EXTB, TESTB, TESTA, ModeSel	< 200 ohm
MTP	VPP	< 10 ohm

7 FUNCTION DESCRIPTION

ST7302 supports 8-bit parallel data bus for 8080 series CPU, 3-line/Single 4-line/Dual 4-line and 2-data-lane interface.

7.1 Microprocessor Interface

7.1.1 8080 Parallel Interface

ST7302 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig1. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Fig2. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

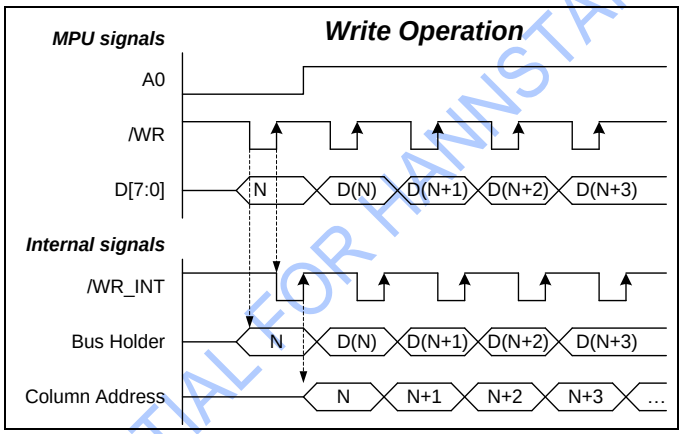


Fig1. Data Transfer: Write

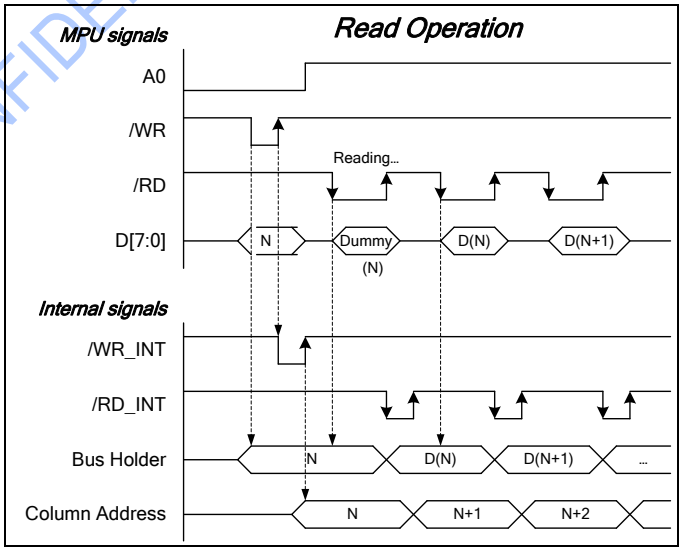
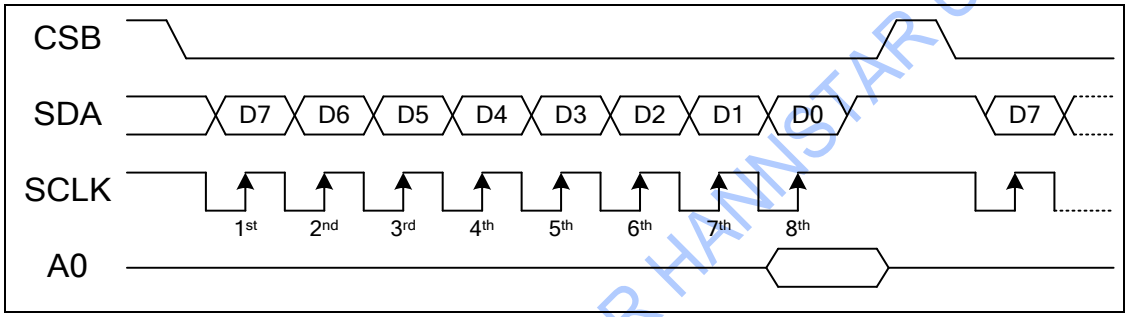


Fig2. Data Transfer: Read

7.1.2 Single 4-Line Serial Interface

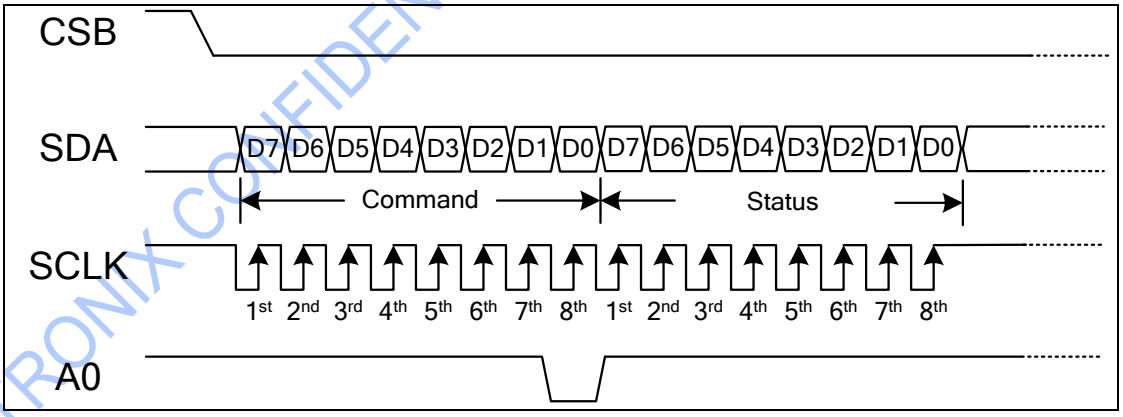
ST7302 is active when CSB is “L”, serial data (SDA) and serial clock (SCLK) inputs are enabled. When CSB is “H”, ST7302 is not active, the internal 8-bit shift register and 3-bit counter are reset. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCLK). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.



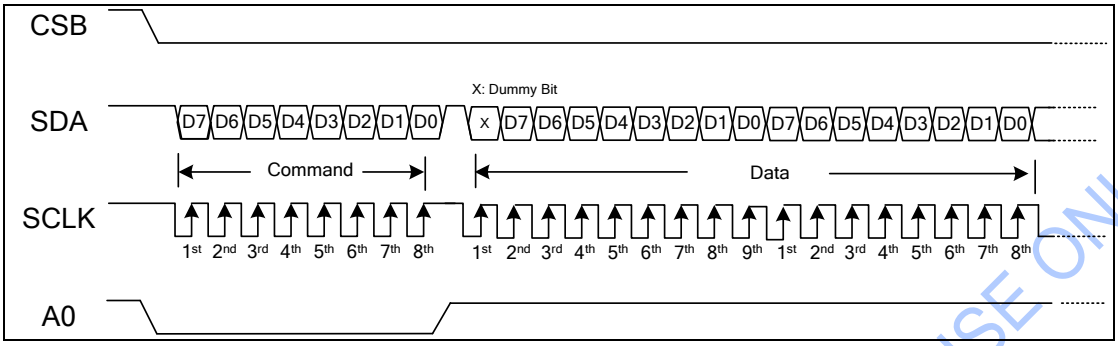
Write Operation of Single 4-Line SPI

After entering the “Read Status” instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.



Read Status Operation of Single 4-Line SPI

After entering the “Memory Read” instruction to read data, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. And when reading data from on-chip-RAM to the MCU, the first data bit will be dummy.



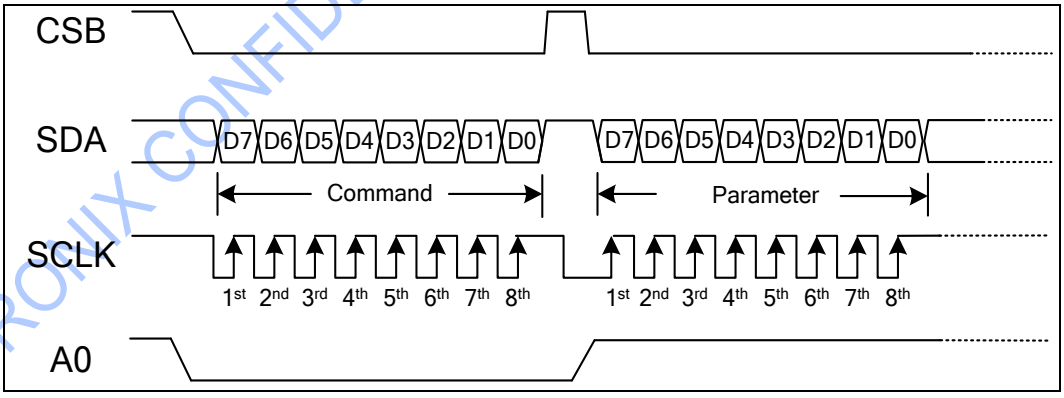
Read RAM Operation of Single 4-Line SPI Interface

7.1.3 Dual 4-Line Serial Interface

Dual 4-line serial interface use: CSB (chip enable), SCLK (serial clock), SDA (serial data input/output 1), RWR (serial data input 2) and A0.

Command write mode:

The command write protocol of dual 4-line serial interface is the same with the single 4-line serial interface. The display data/command indication is controlled by the register selection pin (A0). Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSB is high. In this state, SCLK clock pulse or SDA data have no effect. A falling edge on CSB enables the serial interface and indicates the start of data transmission.

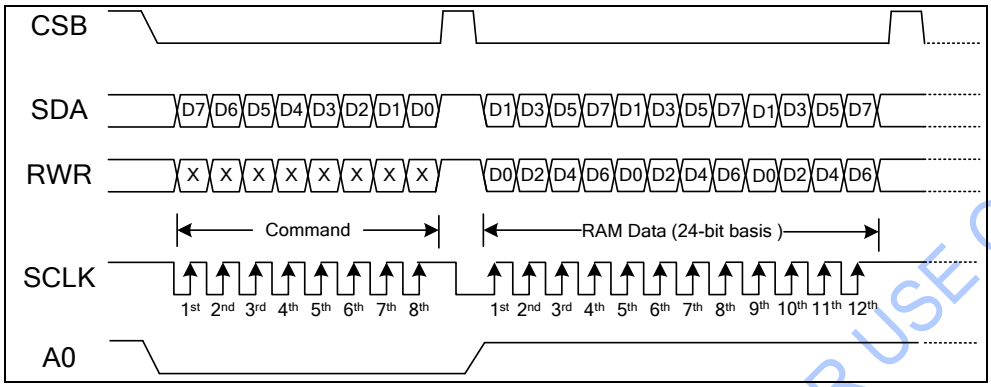


Command Write Operation of Dual 4-Line SPI

RAM write mode:

The RAM write mode of dual 4-line serial interface need use SDA pin and RWR pin to be data input pins.

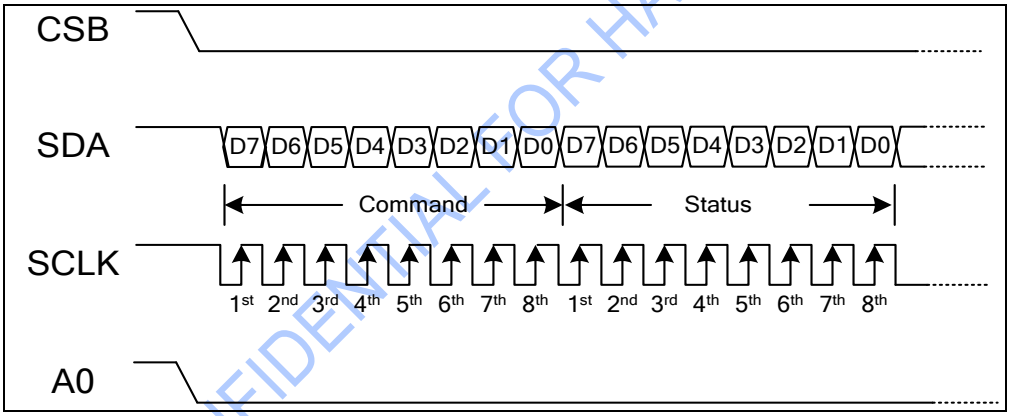
The LSB is transmitted first and the data bit will be exchanged between SDA and RWR.



RAM Write Operation of Dual 4-Line SPI

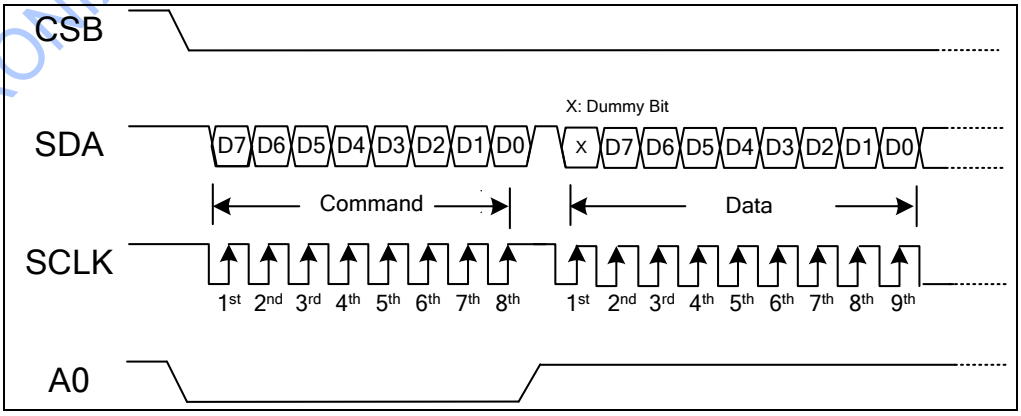
Read protocol for dual 4-line serial interface:

Read protocol (for RDID1/RDID2/RDID3 command: 8-bit read):



Read Status Operation of Dual 4-Line SPI Interface

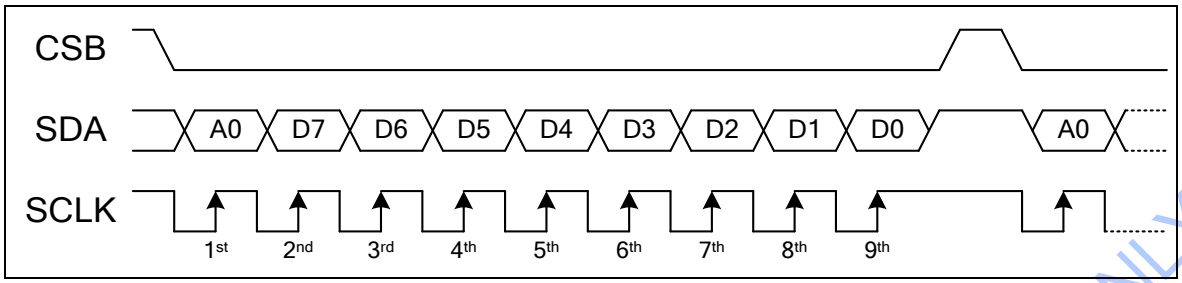
Read protocol (for RAM Data: 8-bit read):



Read RAM Operation of Dual 4-Line SPI Interface

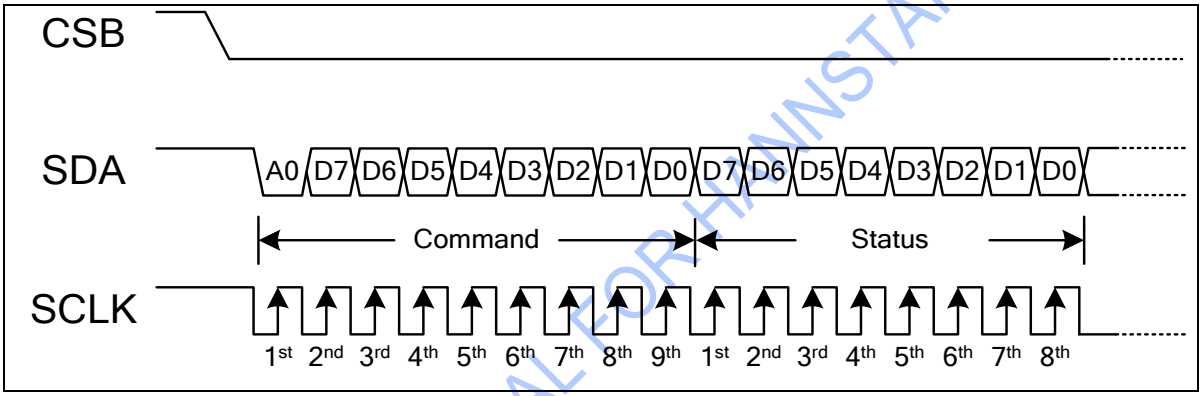
7.1.4 3-Line Serial Interface

In 3-Line interface, A0 pin is not available. The 1st output bit defines command byte or parameter byte.



Write Operation of 3-Line SPI

After entering the “Read Status” instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.



Read Status Operation of 3-Line SPI

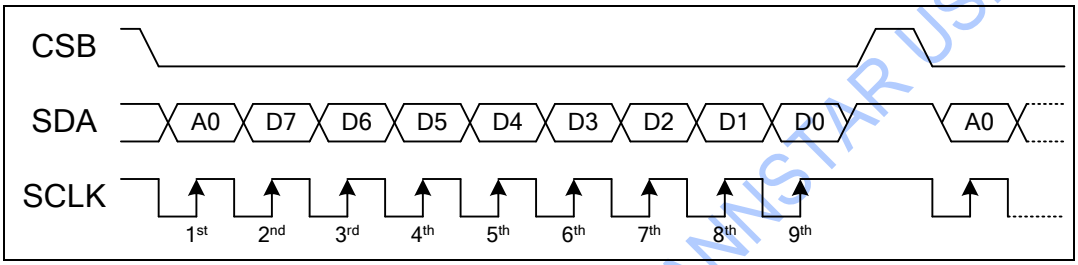
7.1.5 2-Data-Lane Serial Interface

2-wire data lane serial interface use: CSB (chip enable), SCLK (serial clock) and SDA (serial data input/output 1), and RWR (serial data input 2).

Command write mode:

The command write protocol of 2-wire data lane serial interface is the same with the 3-line serial interface, so users can ignore the input data of A0.

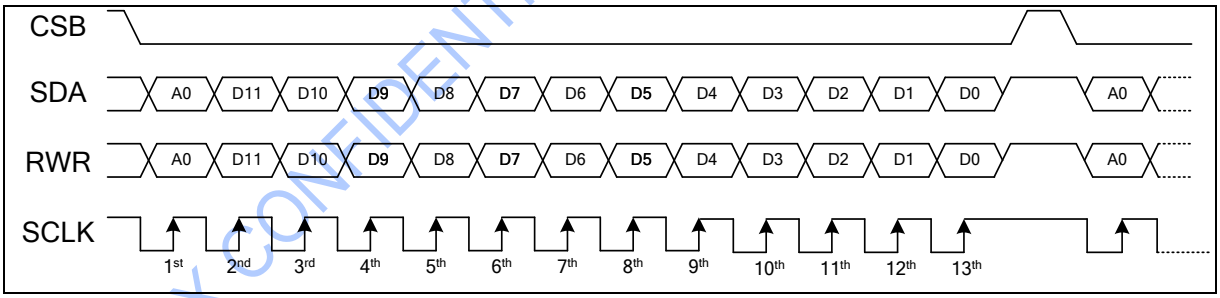
Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSB is high. In this state, SCLK clock pulse or SDA data have no effect. A falling edge on CSB enables the serial interface and indicates the start of data transmission.



Command Write Operation for 2-Data-Lane serial interface

SRAM write mode:

The SRAM write mode of 2-wire data line serial interface need use SDA pin and RWR pin to be data input pins.



Write SRAM Operation of 2-Data Lane SPI

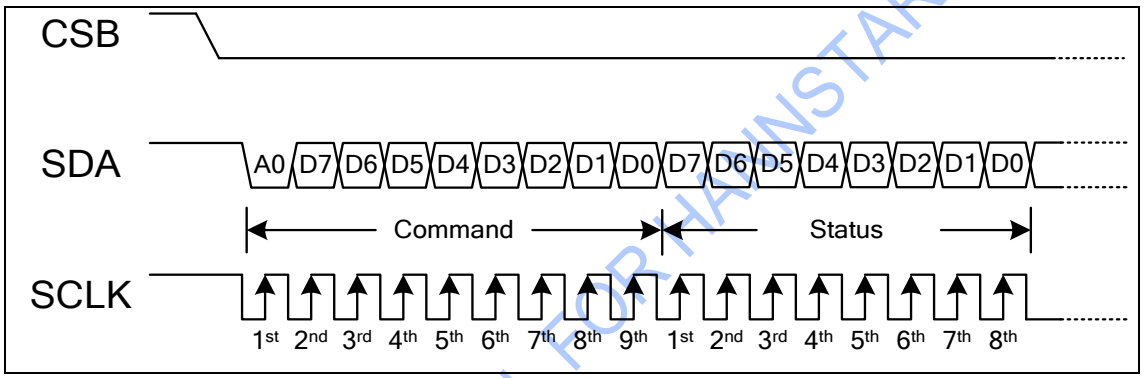
Read function:

The read mode of 2-wire data lane serial interface is the same with the 3-line serial interface and A0 pin can be ignored. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSB is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

Read protocol for 2 data lane serial interface:

Read protocol (for RDID1/RDID2/RDID3 command: 8-bit read):



Read Operation of 2-Data Lane SPI Interface

7.2 Data Coding

Use specific command for switching between data input modes.

7.2.1 Data Input Mode

(1) 8080/Single 4SPI/3SPI Interface

TYPE1: There are 4 write operations for 24-bit data. (Set by "BPS=0" of command 0x3Ah)

Command	A0	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
1st write	1	P1	P2	P3	P4	P5	P6	-	-
2nd write	1	P7	P8	P9	P10	P11	P12	-	-
3rd write	1	P13	P14	P15	P16	P17	P18	-	-
4th write	1	P19	P20	P21	P22	P23	P24	-	-

Note: - don't care

TYPE2: There are 3 write operations for 24-bit data. (Set by "BPS=1" of command 0x3Ah)

Command	A0	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
1st write	1	P1	P2	P3	P4	P5	P6	P7	P8
2nd write	1	P9	P10	P11	P12	P13	P14	P15	P16
3rd write	1	P17	P18	P19	P20	P21	P22	P23	P24

(2) Dual 4SP Interface

There are 3 write operations for 24-bit data at the same time.

Command	A0	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
1st write	1	P1	P2	P3	P4	P5	P6	P7	P8
2nd write	1	P9	P10	P11	P12	P13	P14	P15	P16
3rd write	1	P17	P18	P19	P20	P21	P22	P23	P24

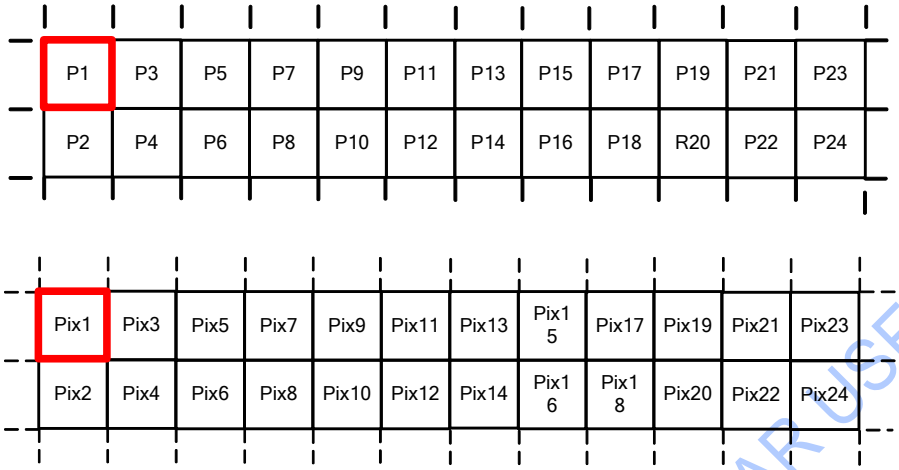
(3) 2 Data-Lane Interface

There are two write operations for 24-bit data at the same time.

Command	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	X	X	X	X	0	0	1	0	1	1	0	0
SDA	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
RWR	1	P13	P14	P15	P16	P17	P18	P19	P20	P21	P22	P23	P24

7.2.2 Data to Display Mapping

The data mapping of Mono display is as below.



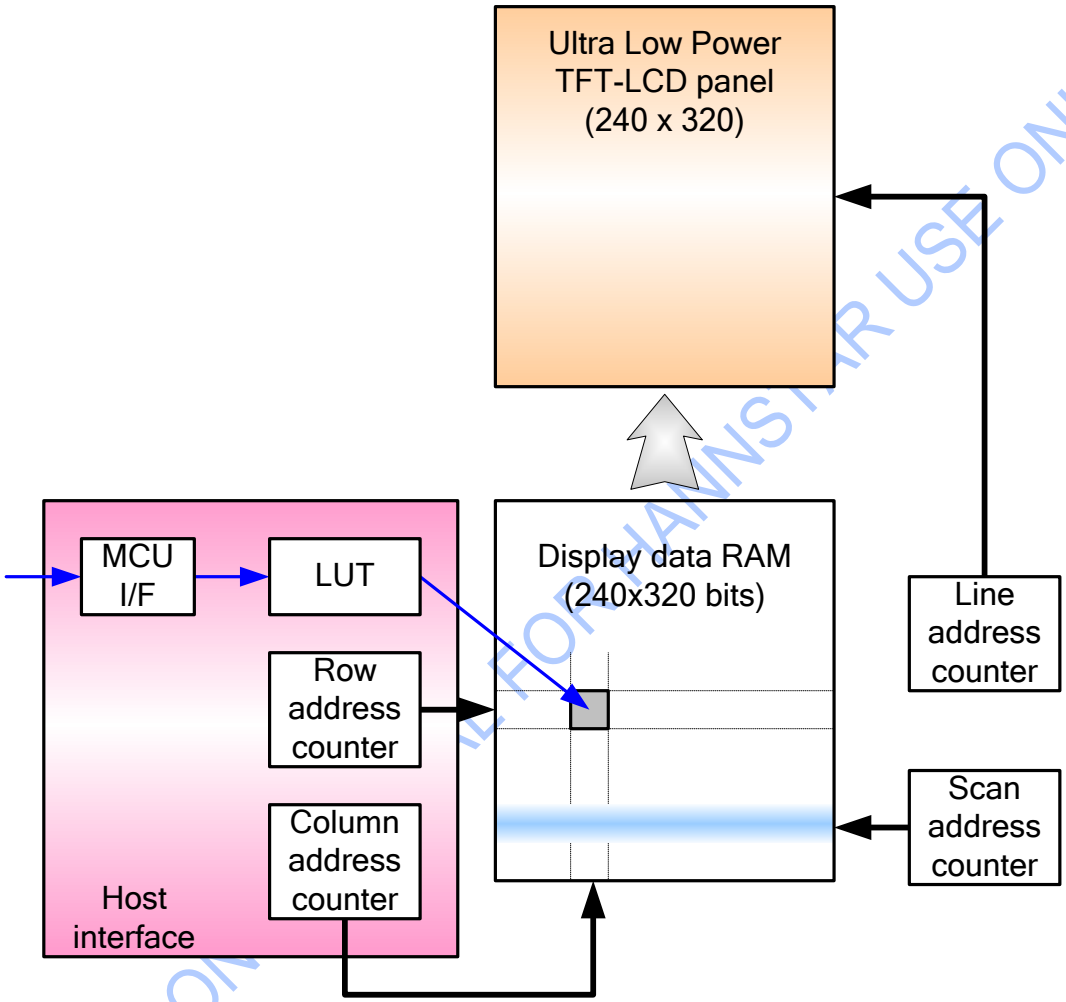
7.2.3 Memory to Display Address Mapping

PA		20											..	39											NOR	CA
NOR	INV	39											..	20											INV	
0	159	P1	P2	P3	P7	P8	P9	P13	P14	P15	P19	P20	P21	..												L1
		P4	P5	P6	P10	P11	P12	P16	P17	P18	P22	P23	P24	..												L2
1	158																									L3
																										L4
:	:	:	:	:														:	:	:						:
158	1																									L317
																										L318
159	0																									L319
																										L320
Source		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	:	S229	S230	S231	S232	S233	S234	S235	S236	S237	S238	S239	S240	Line

7.3 Display Data RAM

7.3.1 Configuration

The display module has an integrated 240 x 320 graphic type static RAM. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and interface Read or Write to the same location of the Frame Memory.



7.4 Address Control

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for 8 pixels is collected, according to the data formats. The locations of RAM are addressed by the address pointers. The address ranges are X=20 (14h) to X=39 (27h) and Y=0 to Y=159 (9Fh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

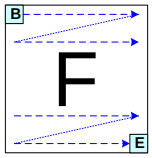
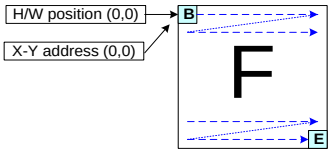
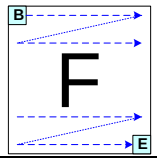
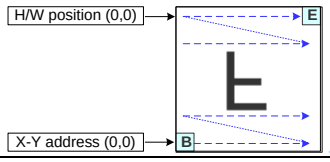
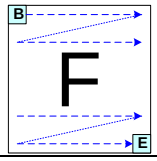
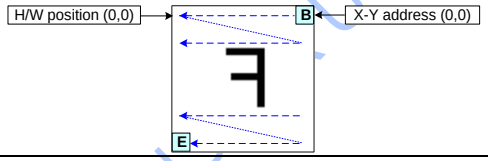
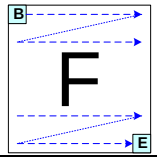
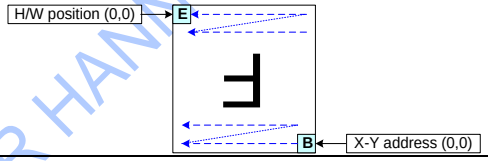
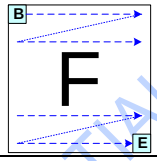
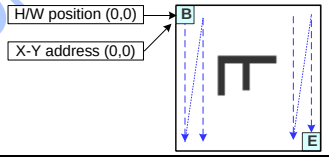
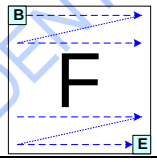
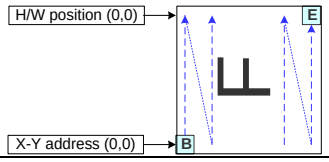
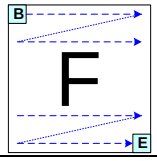
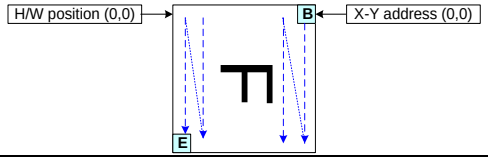
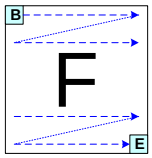
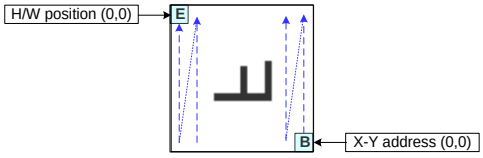
For example the whole display contents will be written, the window is defined by the following values: XS=20 (14h) YS=0 (0h) and XE=39 (27h), YE=159 (9Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET and MADCTL”, define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 7.4 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

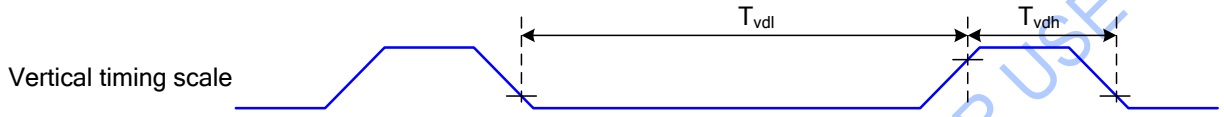
Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

7.5 Tearing Effect

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.5.1 Tearing effect line modes

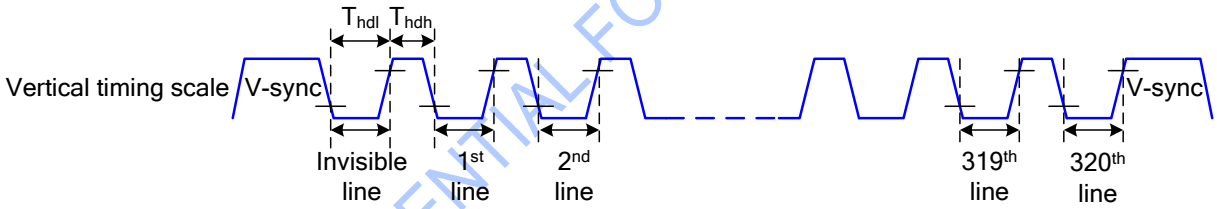
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

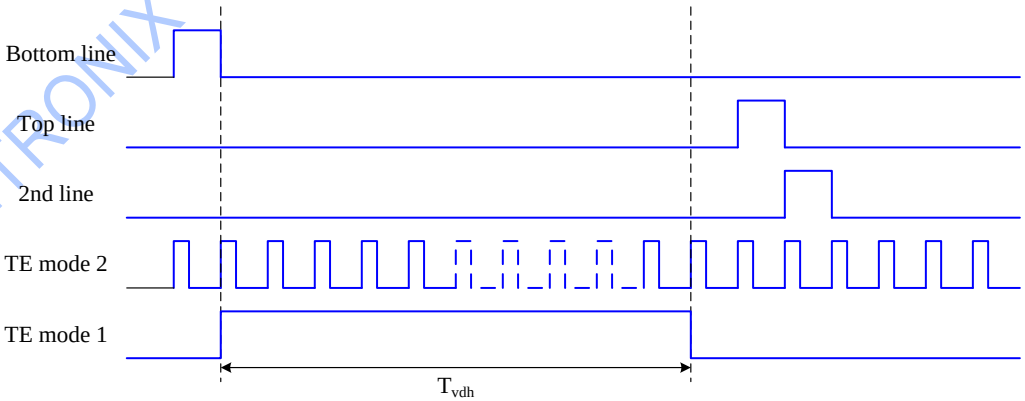
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

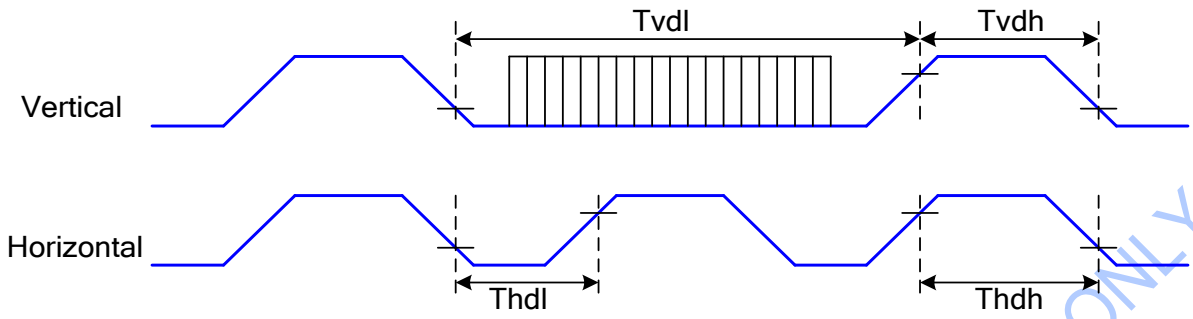
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

7.5.2 Tearing effect line timings

The Tearing Effect signal is described below:



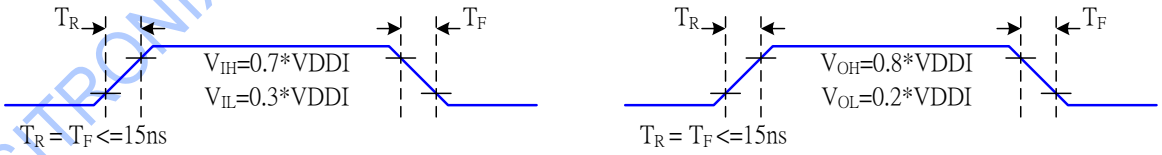
Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	30	-	ms	
tvdh	Vertical Timing High Duration	1.2	-	ms	
thdl	Horizontal Timing Low Duration	31.2	-	µs	
thdh	Horizontal Timing Low Duration	31.2	-	µs	

AC characteristics of Tearing Effect Signal HPM Mode (Frame Rate = 32 Hz, Ta=25°C)

Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	990.5	-	ms	
tvdh	Vertical Timing High Duration	9.5	-	ms	
thdl	Horizontal Timing Low Duration	250	-	µs	
thdh	Horizontal Timing Low Duration	250	-	µs	

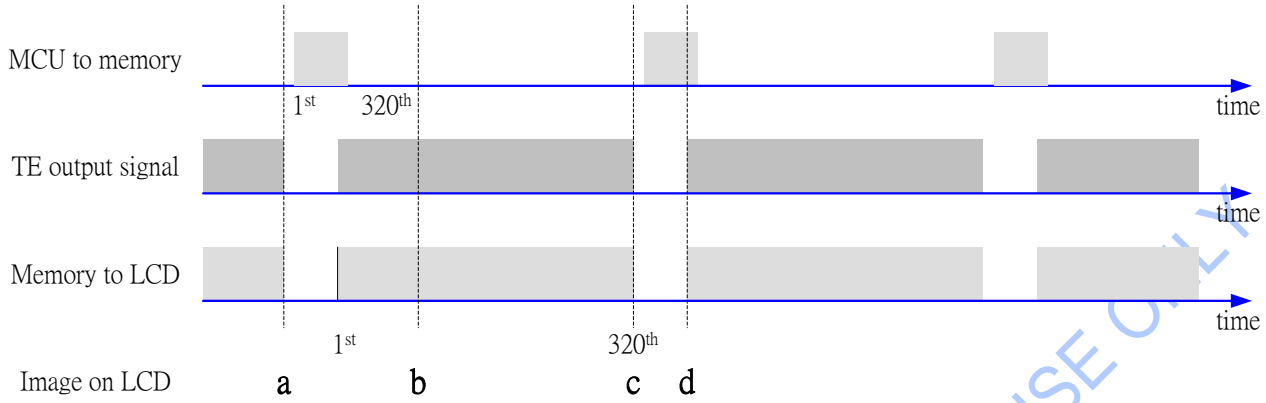
AC characteristics of Tearing Effect Signal LPM Mode (Frame Rate = 1 Hz, Ta=25°C)

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

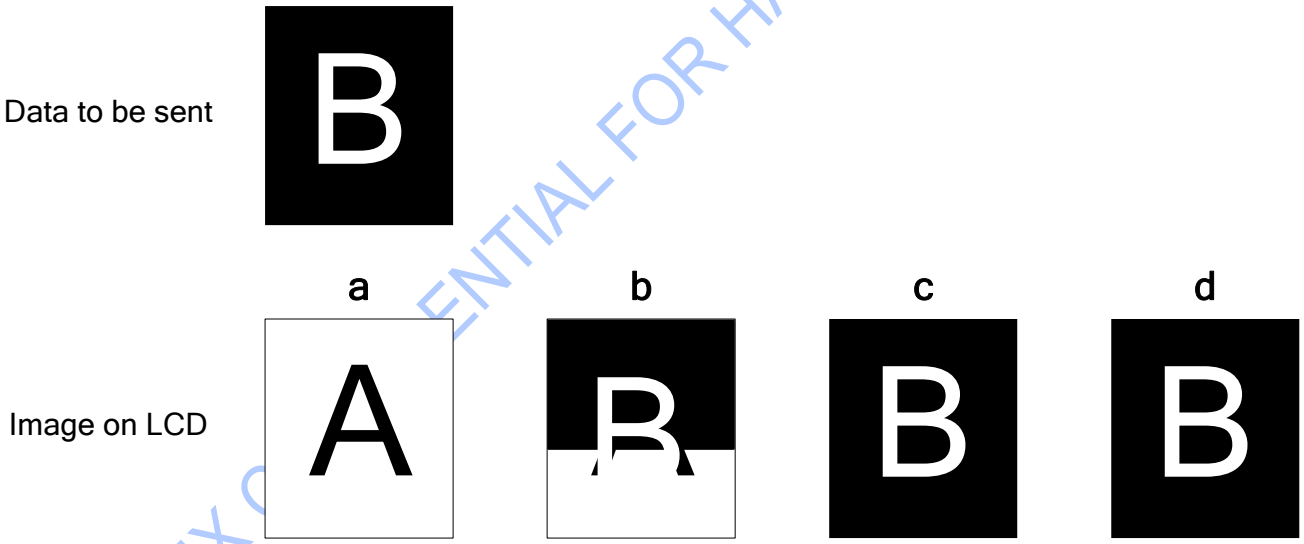


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

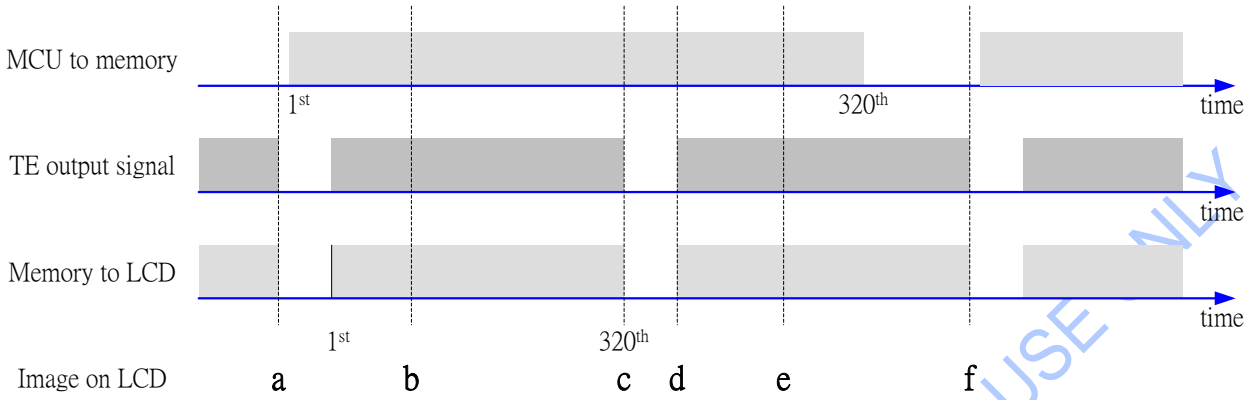
7.5.3 Example 1: MPU Write is faster than panel read



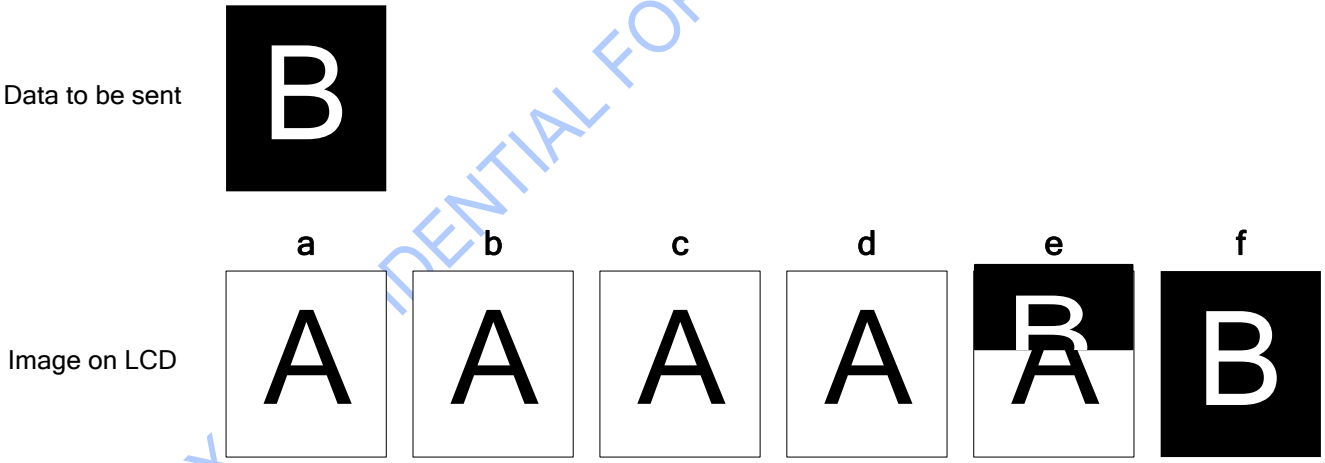
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



7.5.4 Example 2: MPU write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



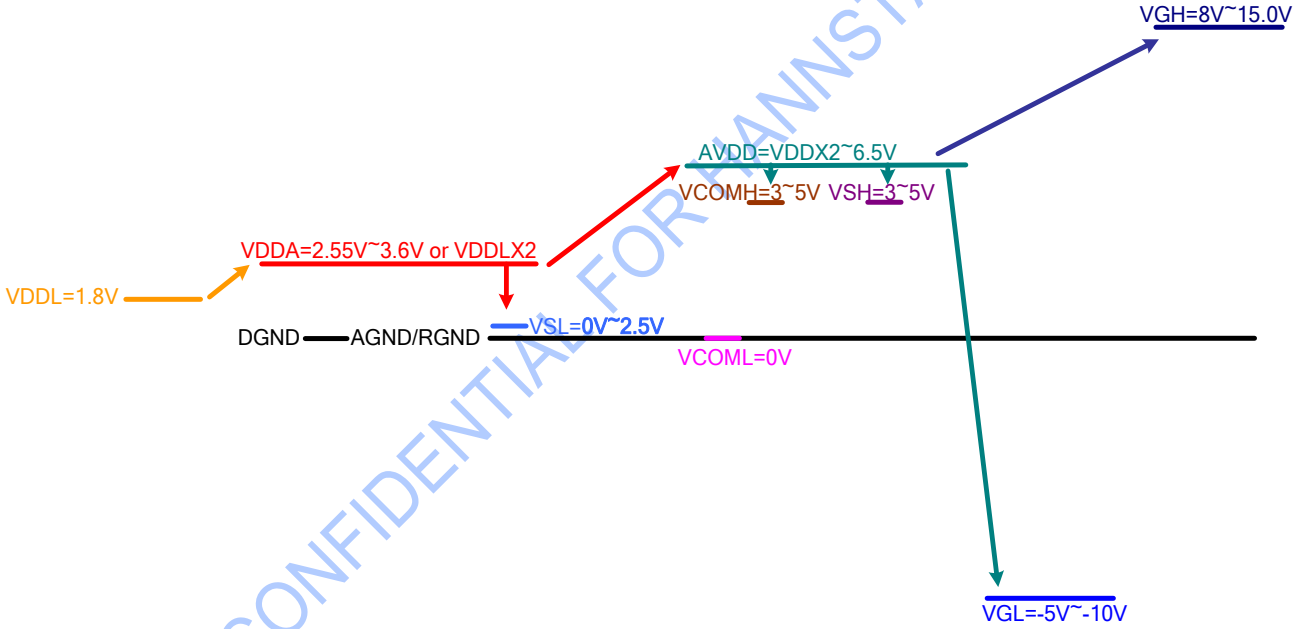
7.6 Oscillation Circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, connect CLS to VDDI; when the external oscillator is used, connect CLS to VSS and input external clock to CL pin. This oscillator signal is used by the voltage booster and display timing generation circuit.

7.7 Reset

Setting RSTB pin to “L” (hardware reset) can initialize internal function. Generally, VDDI is not stable at the time that the system power is just turned ON. The hardware reset or software reset is required to initialize internal registers after VDDI is stable. Initialization by RSTB pin or command SWRESET is essential before operating.

7.8 Power System



7.9 Power ON/OFF Sequence

VDDI and VDDA can be applied in any order.

VDDA and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down minimum 120msec after RSTB has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDDA can be powered down minimum 0msec after RSTB has been released.

CSB can be applied at any timing or can be permanently grounded. RSTB has priority over CSB.

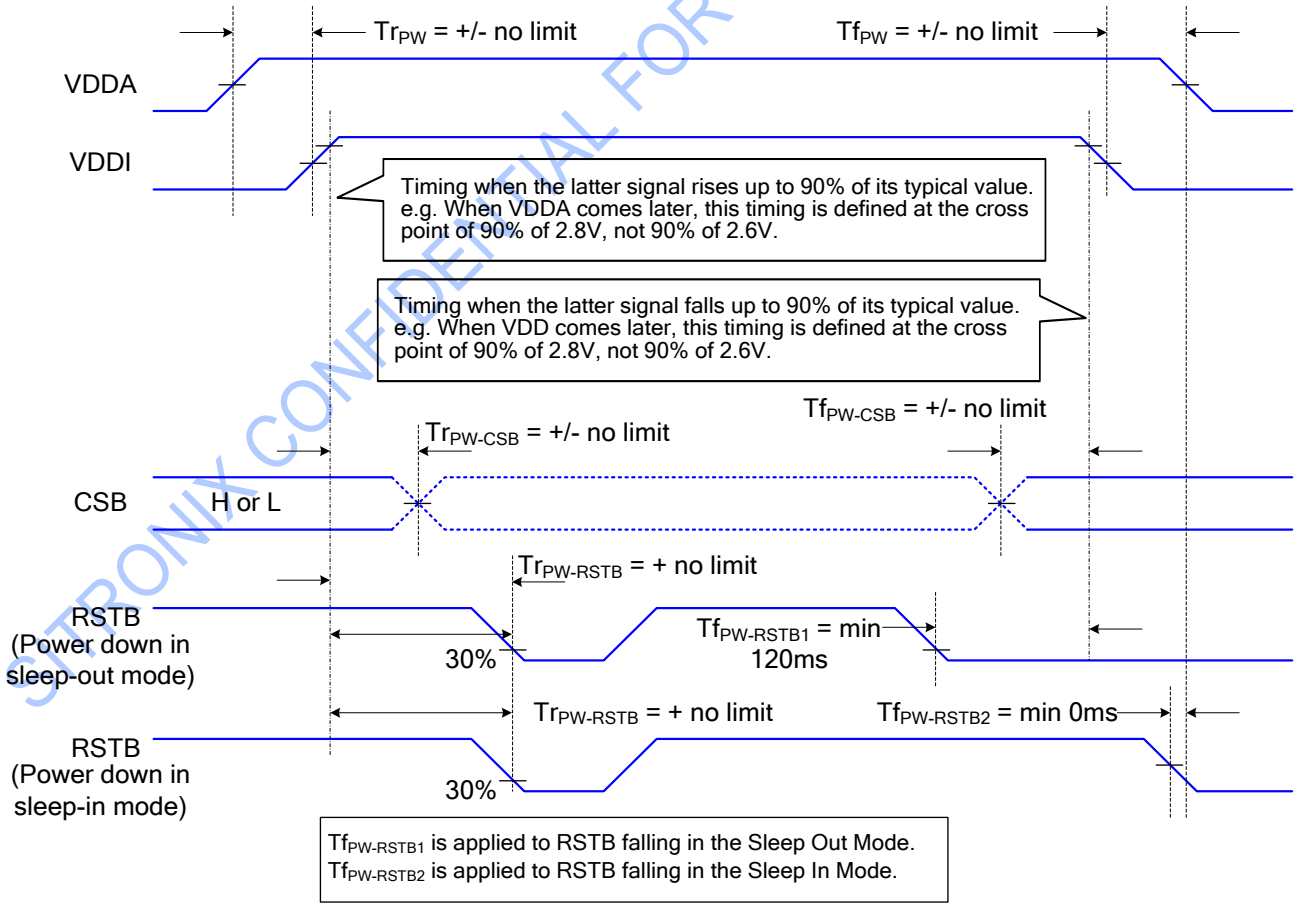
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RSTB line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RSTB) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



8 COMMAND

8.1 Command Table1

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1. NOP	0	↑	1	0	0	0	0	0	0	0	0	(00h)	No operation
2.SWRESET	0	↑	1	0	0	0	0	0	0	0	1	(01h)	Software reset
3.RDDID	0	↑	1	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
4.RDDST	0	↑	1	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	↑	BSTON	MY	MX	MV	ML	GS	DO	0		Display status1
	1	1	↑	0	XDE	0	BPS	PMS	PTLON	SLOUT	NORON		Display status2
	1	1	↑	VSON	0	INVON	0	0	DISON	TEON	0		Display status3
5.SLPIN	0	↑	1	0	0	0	1	0	0	0	0	(10h)	Sleep in
6.SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	(11h)	Sleep out
7.PTLON	0	↑	1	0	0	0	1	0	0	1	0	(12h)	Partial on (240 duty set)
8.PTLOFF	0	↑	1	0	0	0	1	0	0	1	1	(13h)	Partial off (320 duty set)
9.INVOFF	0	↑	1	0	0	1	0	0	0	0	0	(20h)	Display inversion off
10.INVON	0	↑	1	0	0	1	0	0	0	0	1	(21h)	Display inversion on
11.DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	(28h)	Display off
12.DISPON	0	↑	1	0	0	1	0	1	0	0	1	(29h)	Display on
13.CASET	0	↑	1	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	0	0	XS5	XS4	XS3	XS2	XS1	XS0		X address start: 14h≦ XS≦ X
	1	↑	1	0	0	XE5	XE4	XE3	XE2	XE1	XE0		X address end S≦ XE≦ X
14.RASET	0	↑	1	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		Y address start: 0≦ YS≦ Y
	1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		Y address end: S≦ YE≦ Y
15.RAMWR	0	↑	1	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
16.RAMRD	0	↑	1	0	0	1	0	1	1	1	0	(2Eh)	Memory read
	1	1	↑	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
17.TEOFF	0	↑	1	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
18.TEON	0	↑	1	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on/off
	1	↑	1	0	0	0	0	0	0	0	TEM		
19.MADCTL	0	↑	1	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	MY	MX	MV	ML	DO	GS	0	0		
20.VSCSAD	0	↑	1	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	1	-	-	-	-	-	-	-	VSP8		
	1	↑	1	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
21.HPM	0	↑	1	0	0	1	1	1	0	0	0	(38h)	High power mode
22.LPM	0	↑	1	0	0	1	1	1	0	0	1	(39h)	Low power mode
23.DTFORM	0	↑	1	0	1	0	0	0	1	0	0	(3Ah)	Data format select
	1	↑	1	0	0	0	XDE	0	0	0	BPS		
24.RAMWRC	0	↑	1	0	0	1	1	1	1	0	0	(3Ch)	Write memory continue
	1	↑	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
25.RAMRD	0	↑	1	0	0	1	1	1	1	1	0	(3Eh)	Memory read
	1	1	↑	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
	1	1	↑	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
26.TESCAN	0	↑	1	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	1	-	-	-	-	-	-	-	N8		
	1	↑	1	N7	N6	N5	N4	N3	N2	N1	N0		
27.RDID1	0	↑	1	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
28.RDID2	0	↑	1	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
29.RDID3	0	↑	1	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

"-": Don't care

8.1.1 NOP (00h)

00H	NOP (No Operation)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter											
Description	This command is empty command.											

8.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter-											
Description	-The display module performs a software reset, registers are written with their SW reset default values. -Frame memory contents are unaffected by this command.											
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command. Software reset command cannot be sent during sleep out sequence.											

8.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	0	0	0	0	0	1	0	0	(04h)
1st parameter	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
2nd parameter	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
3rd parameter	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	-This read byte returns 24-bit display identification information. -The 1st parameter (ID17 to ID10): LCD module's manufacturer ID. -The 2nd parameter (ID26 to ID20): LCD module/driver version ID -The 3rd parameter (ID37 to UD30): LCD module/driver ID. -Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.											

8.1.4 RDDST (09h): Read Display Status

09H	RDDST(Read Display Status)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	0	0	0	0	0	1	0	0	(09h)
1st parameter	1	1	↑	BSTON	MY	MX	MV	ML	GS	DO	0	
2nd parameter	1	1	↑	0	XDE	0	BPS	PMS	PTLON	SLOUT	NORON	
3rd parameter	1	1	↑	VSON	0	INVON	0	0	DISON	TEON	0	

Description

- This command indicates the current status of the display as described in the table below

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, (when ANAINI (D1h) D0='1') '0' =Booster off, (when ANAINI (D1h) D0='0')
MY	Row Address Order	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='0')
MV	Row/Column Exchange	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0'
ML	Scan Address Order	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
DO	Data Order	'0' =Left to right (When MADCTL (36h) D3='1') '1' = Right to left (When MADCTL (36h) D3='0', using in MX=1)
GS	Gate Scan Order	'0' = Data refresh Top to Bottom (when MADCTL (36h) D2='0') '1' = Data refresh Bottom to Top (when MADCTL (36h) D2='1')
XDE	Data Up Down Switch	'0' = Switch OFF (when COLMOD (3Ah) D4='0') '1' = Switch ON(when COLMOD (3Ah) D4='1', Using with MY=1)
BPS	Bytes Per Pixel Select	'0' = 4 writes operations for 24-bit data (when COLMOD (3Ah) D0='0') '1' = 3 writes operations for 24-bit data (when COLMOD (3Ah) D0='1')
PMS	Power Mode Select	'0' = High Power Mode, '1' = Low Power Mode
PTLON	Partial Mode ON/OFF	'0' = OFF, '1' = ON
SLPOUT	Sleep In/Out	'0' = In, '1' = Out
NORON	Display Normal Mode On/Off	'0' = Scroll or Partial ON, '1' = Normal,
VSON	Scroll Mode On/Off	'0' = Off, '1' = On

INVON	Inversion Status	‘0’ = Normal, ‘1’ = Inverse
DISON	Display On/Off	‘1’ = On, “0” = Off
TEON	Tearing effect line on/off	‘1’ = On, “0” = Off

8.1.5 SLPIN (10h): Sleep in

10H	SLPIN (Sleep In)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	↑	1	0	0	0	1	0	0	0	0	(10h)
parameter	No Parameter											
Description	-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped. -MCU interface and memory are still working and the memory keeps its contents.											
Restriction	-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending sleep in command.											

8.1.6 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	(11h)
parameter	No Parameter											
Description	-This command turn off sleep mode. -In this mode the DC/DC converter is enable, internal display oscillator is started, and panel scanning is started.											
Restriction	-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.											

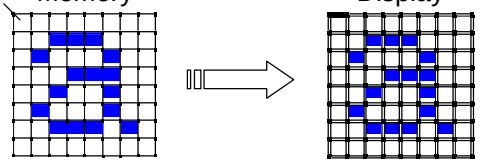
8.1.7 PTLON (12h): Partial On

12H	PTLON (Partial On)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	0	0	0	1	0	0	1	0	(12h)
parameter	No Parameter											
Description	-This command turns on Partial mode. When partial on, display window become 240duty. -To leave Partial mode, the Partial off command (13h) should be written.											

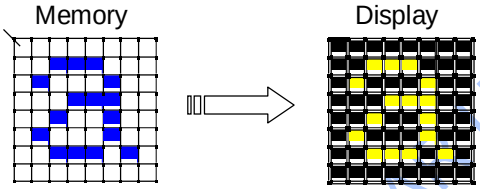
8.1.8 PTLOFF (13h): Partial Off

13H	PTLOFF (Partial Off)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	0	0	0	1	0	0	1	1	(13h)
parameter	No Parameter											
Description	-This command turns the display to partial off mode. When partial off, display window become 320duty. -Exit from NORON by the partial mode on command.											

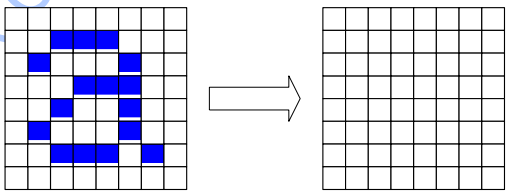
8.1.9 INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	0	↑	1	0	0	1	0	0	0	0	0	(20h)
parameter	No Parameter											
Description	-This command is used to recover from display inversion mode. (Example) Top-Left (0,0) Memory Display 											

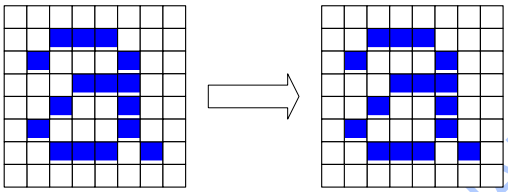
8.1.10 INVON (21h): Display Inversion On

21H	INVON (Display Inversion On)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	0	0	1	0	0	0	0	1	(21h)
parameter	No Parameter											
Description	-This command is used to recover from display inversion mode. (Example) Top-Left (0,0) Memory Display 											

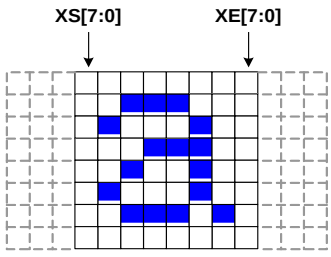
8.1.11 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	(28h)
parameter	No Parameter											
Description	- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29h) **(Example)** **Memory** **Display** 											

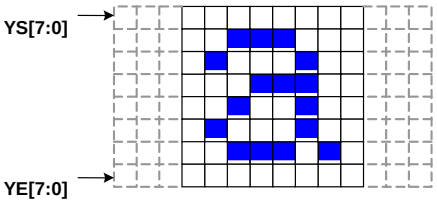
8.1.12 DISPON (29h): Display On

29H	DISPON (Display On)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPON	0	↑	1	0	0	1	0	1	0	0	1	(29h)
parameter	No Parameter											
Description	- This command is used to recover from DISPLAY OFF mode. - Output from the Frame Memory is enabled. - This command makes no change of contents of frame memory. - This command does not change any other status. **(Example)** **Memory** → **Display** 											

8.1.13 CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	↑	1	0	0	1	0	1	0	1	0	(2Ah)
1st parameter	1	↑	1	0	0	XS5	XS4	XS3	XS2	XS1	XS0	
2th parameter	1	↑	1	0	0	XE5	XE4	XE3	XE2	XE1	XE0	
Description	-The value of XS [5:0] and XE [5:0] are referred when RAMWR command comes. -Each value represents one column line in the Frame Memory. 											
Restriction	XS [5:0] always must be equal to or less than XE [5:0] When XS [5:0] or XE [5:0] is greater than maximum address like below, data of out of range will be ignored. (Parameter range: 20 (14h) < XS [5:0] < XE [5:0] < 59 (3Bh)											

8.1.14RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET	0	↑	1	0	0	1	0	1	0	1	1	(2Bh)
1nd parameter	1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
2th parameter	1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
Description	-This command is used to defined area of frame memory where MCU can access. -The value of YS [7:0] and YE [7:0] are referred when RAMWR command comes. -Each value represents one page line in the Frame Memory.  											
Restriction	YS [7:0] always must be equal to or less than YE [15:0] When YS [7:0] or YE [7:0] is greater than maximum address like below, data of out of range will be ignored.(Parameter range: 0 < YS [7:0] < YE [7:0] < 159 (9Fh)											

8.1.15RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	0	0	1	0	1	1	0	0	(2Ch)
1st parameter	1	↑	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
…	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
N parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	-This command is used to transfer data from MCU to frame memory. -When this command is accepted, the column register and the page register are reset to the start column/start page positions. -The start column/start page positions are different in accordance with MADCTL setting. -Sending any other command can stop frame write.											

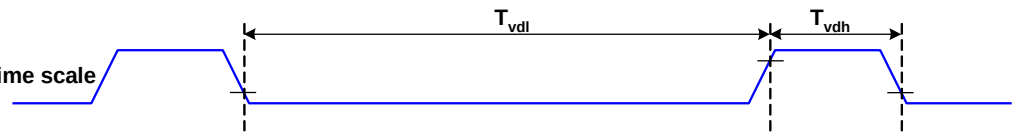
8.1.16 RAMRD (2Eh): Memory Read

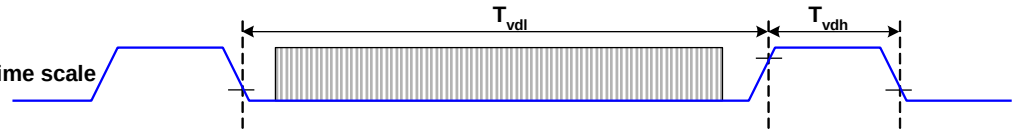
2EH	RAMRD (Memory Read)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMRD	0	↑	1	0	0	1	0	1	1	1	0	(2Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	
:	1	1	↑	:	:	:	:	:	:	:	:	
(N+1)th parameter	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	
Description	-This command is used to transfer data from frame memory to MCU. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTL setting. -Then D[7:0] is read back from the frame memory and the column register and the row register incremented -Frame Read can be cancelled by sending any other command.											

8.1.17 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	0	0	1	1	0	1	0	0	(34h)
parameter	No Parameter											
Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.											

8.1.18 TEON (35h): Tearing Effect Line On

35H	TEON (Tearing Effect Line On)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	0	0	1	1	0	1	0	1	(35h)
parameter	1	↑	1	0	0	0	0	0	0	0	TEM	
Description	-This command is used to turn ON the Tearing Effect output signal from the TE signal line. -This output is not affected by changing MADCTL bit ML. -The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line: -When TEM ='0': The Tearing Effect output line consists of V-Blanking information only **Vertical time scale** 											

	-When TEM ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information  Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

8.1.19 MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	↑	1	0	0	1	1	0	1	1	0	(36h)
parameter	1	↑	1	MY	MX	MV	ML	DO	GS	0	0	

Description

-This command defines read/ write scanning direction of frame memory.

Bit	NAME	DESCRIPTION
D7	MY	Page Address Order
D6	MX	Column Address Order
D5	MV	Page/Column Order
D4	ML	Scan Address Order
D3	DO	Data Output Order
D2	GS	Gate Scan Order

-Bit Assignment

Bit D7- Page Address Order (MY)

"0" = Top to Bottom (When MADCTL D7="0").

"1" = Bottom to Top (When MADCTL D7="1").

Bit D6- Column Address Order (MX)

"0" = Left to Right (When MADCTL D6="0").

"1" = Right to Left (When MADCTL D6="1").

Bit D5- Page/Column Order (MV)

"0" = Column Direction Mode (When MADCTL D5="0").

"1" = Page Direction Mode (When MADCTL D5="1")

Note: Bits D7 to D5, please refer to section 7.4 Address Control

Bit D4- Line Address Order (ML)

"0" = LCD Refresh Top to Bottom (When MADCTL D4="0")

"1" = LCD Refresh Bottom to Top (When MADCTL D4="1")

Bit D3- Data Order (DO)

"0" = Left to Right (When MADCTL D3="0")

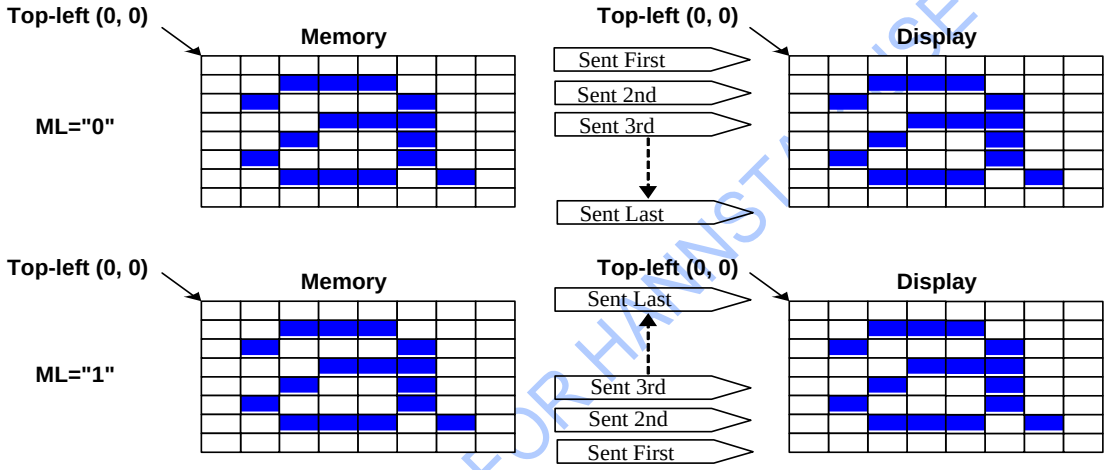
"1" = Right to Left (When MADCTL D3="1", using in MX=1)

Bit D2- Gate Scan Order (GS)

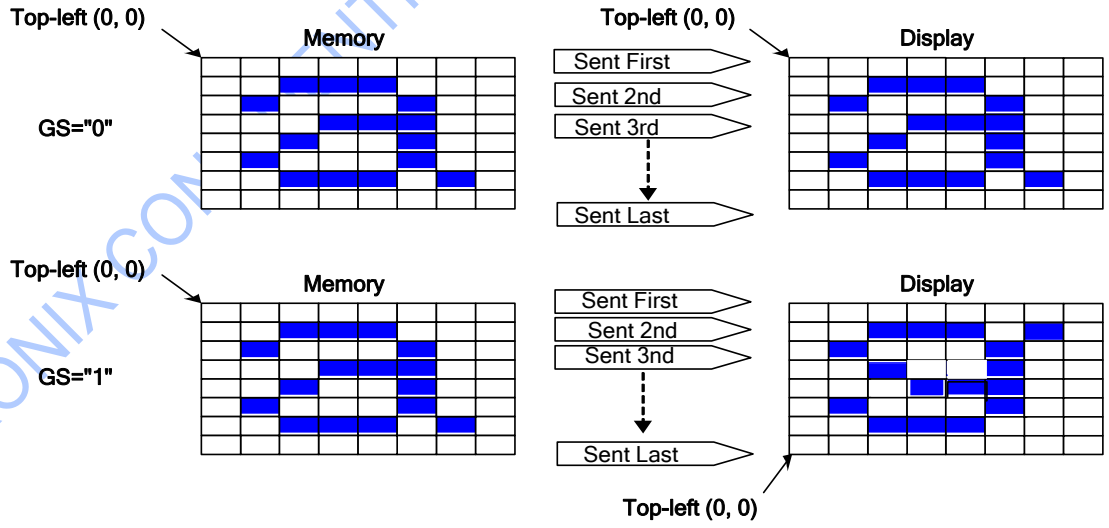
"0" =Data refresh Top to Bottom (When MADCTL D2="0")

"0" =Data refresh Bottom to Top (When MADCTL D2="1")

Line Address Order (ML)



Gate Scan Order (GS)



8.1.20 VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	RASET (Row Address Set)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCSAD	0	↑	1	0	0	1	1	0	1	1	1	(37h)
1st parameter	1	↑	1	-	-	-	-	-	-	-	VSP8	
2ND parameter	1	↑	1	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	

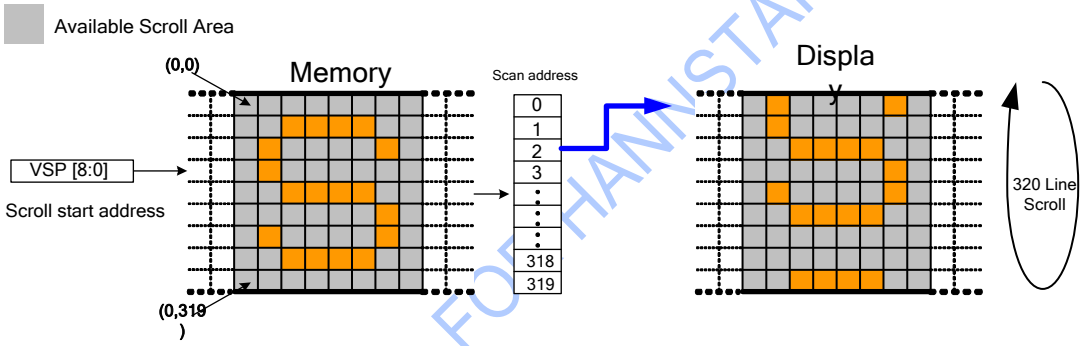
Description

- The Vertical Scrolling Start Address command has two parameters which describe which line in the Frame Memory will be written as the first line after the last line on the display as illustrated below: .

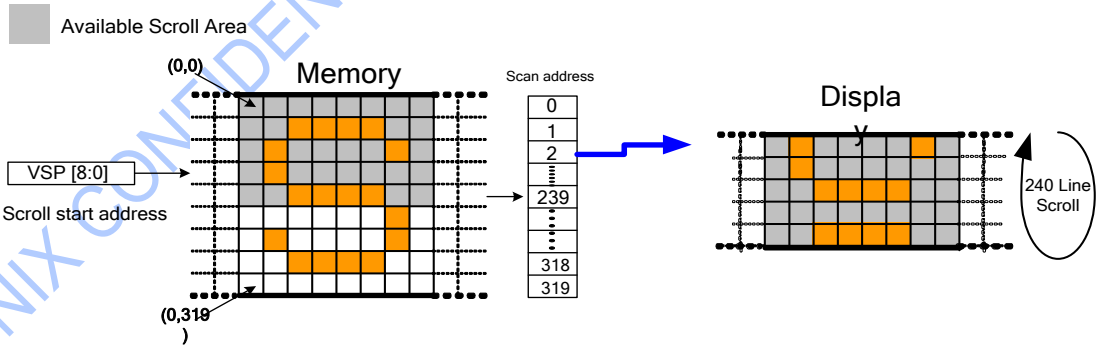
When ML=0

Example:

When partial off (320 Duty) and VSP = '2'



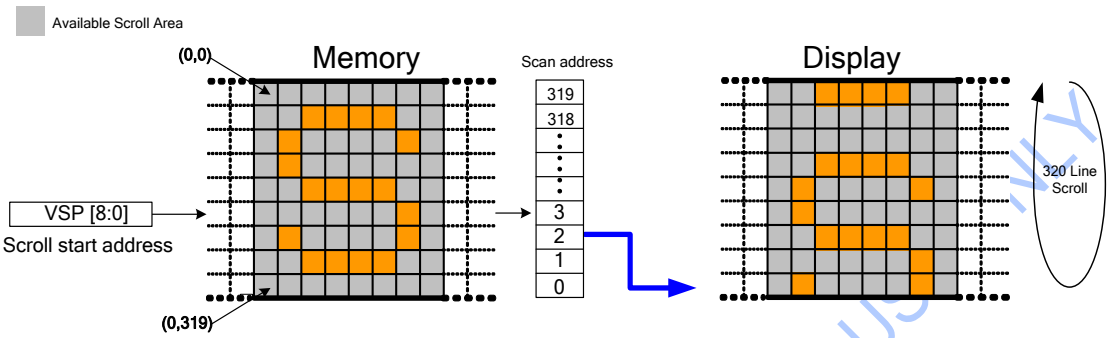
When partial on (240 Duty) and VSP = '2'



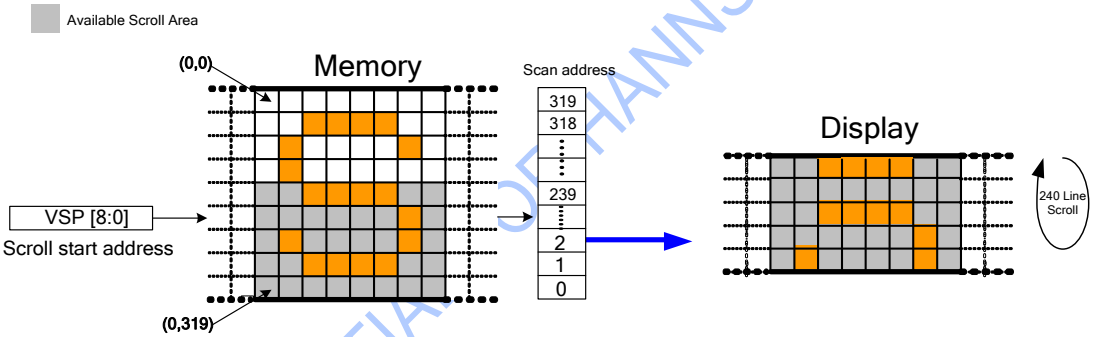
When ML=1

Example:

When partial off and VSP = '2'



When partial on and VSP = '2'



8.1.21 HPM (38h): High Power Mode ON

38H	HPM (High Power Mode ON)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
HPM	0	↑	1	0	0	1	1	1	0	0	0	(38h)
parameter	No Parameter											
Description	-This command is used to switch display drive mode to high power mode. In HPM, IC drivers LCD with frame rate (16 or 32Hz) that set by **FRCTRL (0xB2h)** command. Default setting of IC is HPM.											

8.1.22 LPM (39h): Low Power Mode ON

39H	LPM (Low Power Mode ON)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
LPM	0	↑	1	0	0	1	1	1	0	0	1	(39h)
parameter	No Parameter											
Description	-This command is used to switch display drive mode to low power mode. In LPM, IC drivers LCD with frame rate (0.25 to 8Hz) that set by **FRCTRL (0xB2h)** command.											

8.1.23 DTFORM (3Ah): Data Format Select

3AH	DTFORM (Data Format Select)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DTFORM	0	↑	1	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	↑	1	0	0	0	XDE	0	0	0	BPS	

Description

-This command defines data format select.

Bit	NAME	DESCRIPTION
D4	XDE	Data Up Down Switch
D0	BPS	Bytes Per Pixel Select

Bit D4- Data Up Down Switch (XDE)

"0" = Switch OFF

"1" = Switch ON (Using with MY=1)

Bit D0- Bytes Per Pixel Select (BPS)

"0" = 4 write operations for 24-bit data

"1" = 3 write operations for 24-bit data

8.1.24 WRMEMC (3Ch): Write Memory Continue

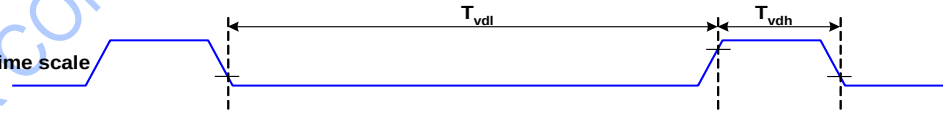
3CH	WRMEMC (Write Memory Continue)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRMEMC	0	↑	1	0	0	1	1	1	1	0	0	(3Ch)
1ST parameter	1	↑	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
⋮	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
Nth parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or memory write command. -If MV=0: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored. If MV=1: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored.											

8.1.25 RDMEMC (3Eh): Read Memory Continue

3EH	RDMEMC (Read Memory Continue)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDMEMC	0	↑	1	0	0	1	1	1	1	1	0	(3Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
:	1	1	↑	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
Nth parameter	1	1	↑	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous read memory continue or memory read command.											

	-If MV=0: Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are read from the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If MV=1: Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are read from the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command.

8.1.26 TESCAN (44h): Set Tear Scanline

44H	TESCAN (Set Tear Scanline)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TESCAN	0	↑	1	0	1	0	0	0	1	0	0	(44h)
1st Parameter	1	↑	1	-	-	-	-	-	-	-	N8	
2nd parameter	1	↑	1	N7	N6	N5	N4	N3	N2	N1	N0	
Description	-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV. -The tearing effect line on has one parameter that describes the tearing effect output line mode. -The tearing effect output line consist of V-blanking information only. **Vertical time scale**  Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0. The tearing effect output line shall be active low when the display module is in sleep mode											

8.1.27 RDID1 (DAh): Read ID1

DAH	RDID1 (Read ID1)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	1	1	0	1	1	0	1	0	(DAh)
parameter	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
Description	-This read byte is used to track the LCD module IC version.											

8.1.28 RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	1	1	0	1	1	0	1	1	(DBh)
parameter	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
Description	-This read byte is used to track the LCD module/driver IC version.											

8.1.29 RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	0	↑	1	1	1	0	1	1	1	0	0	(DCh)
parameter	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	-This read byte identifies the LCD module/driver.											

8.2 Command Table2

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
1.GTCON	0	↑	1	0	1	1	1	0	0	1	1	(73h)	Gate Timing Control
	1	↑	1	0	0	DEON	DEMODE	GAB[3]	GAB[2]	GAB[1]	GAB[0]		
	1	↑	1	0	0	CLKDIV[1]	CLKDIV[0]	FDEPA[3]	FDEPA[2]	FDEPA[1]	FDEPA[0]		
	1	↑	1	DEPWA[7]	DEPWA[6]	DEPWA[5]	DEPWA[4]	DEPWA[3]	DEPWA[2]	DEPWA[1]	DEPWA[0]		
	1	↑	1	DENUM[3]	DENUM[2]	DENUM[1]	DENUM[0]	DEINT[3]	DEINT[2]	DEINT[1]	DEINT[0]		
	1	↑	1	DEPWA[7]	DEPWA[6]	DEPWA[5]	DEPWA[4]	DEPWA[3]	DEPWA[2]	DEPWA[1]	DEPWA[0]		
	1	↑	1	DENUM[3]	DENUM[2]	DENUM[1]	DENUM[0]	DEINT[3]	DEINT[2]	DEINT[1]	DEINT[0]		
2.DUTYSET	0	↑	1	1	0	1	1	0	0	0	0	(B0h)	Duty Setting
	1	↑	1	0	DT[6]	DT[5]	DT[4]	DT[3]	DT[2]	DT[1]	DT[0]		
3.FSTCOM	0	↑	1	1	0	1	1	0	0	0	1	(B1h)	First Gate Setting
	1	↑	1	0	0	0	0	0	0	0	FTC[8]		
	1	↑	1	FTC[7]	FTC[6]	FTC[5]	FTC[4]	FTC [3]	FTC [2]	FTC [1]	FTC [0]		
4.FRCTRL	0	↑	1	1	0	1	1	0	0	1	0	(B2h)	FR Control
	1	↑	1	0	0	0	0	0	0	0	HFR		
	1	↑	1	0	0	0	0	0	LFR[2]	LFR[1]	LFR[0]		
5.VCOMEQ	0	↑	1	1	0	1	1	0	0	1	1	(B3h)	VCOM EQ Enable
	1	↑	1	COMEQ	0	0	1	0	1	0	0		
6.GATEUPEQ	0	↑	1	1	0	1	1	0	1	0	0	(B4h)	Update Period Gate EQ Control
	1	↑	1	FGS	GEQEN	1	0	0	1	0	1		
	1	↑	1	0	1	1	0	0	1	1	0		
	1	↑	1	GPCHPU4[1:0]		GPCHPU3[1:0]		GPCHPU2[1:0]		0	1		
	1	↑	1	GPCHP87[1:0]		GPCHPU7[1:0]		GPCHPU6[1:0]		GPCHPU5[1:0]			
	1	↑	1	GPCHPU12[1:0]		GPCHPU11[1:0]		GPCHPU10[1:0]		GPCHPU9[1:0]			
	1	↑	1	0	1	GPCHPU15[1:0]		GPCHPU14[1:0]		GPCHPU13[1:0]			
	1	↑	1	GPCLPU4[1:0]		GPCLPU3[1:0]		GPCLPU2[1:0]		0	1		
	1	↑	1	GPCLPU8[1:0]		GPCLPU7[1:0]		GPCLPU6[1:0]		GPCLPU5[1:0]			
	1	↑	1	GPCLPU12[1:0]		GPCLPU11[1:0]		GPCLPU10[1:0]		GPCLPU9[1:0]			
	1	↑	1	0	1	GPCLPU15[1:0]		GPCLPU14[1:0]		GPCLPU13[1:0]			

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
7.GATEDSEQ	0	↑	1	1	0	1	1	0	1	0	1	(B5h)	Destress Period Gate EQ Control
	1	↑	1	0	0	0	0	0	0	1	0		
	1	↑	1	0	0	0	0	0	1	0	0		
	1	↑	1	GPCDE4[1:0]		GPCDE3[1:0]		GPCDE2[1:0]		0	1		
	1	↑	1	GPCDE8[1:0]		GPCDE7[1:0]		GPCDE6[1:0]		GPCDE5[1:0]			
	1	↑	1	GPCDE12[1:0]		GPCDE11[1:0]		GPCDE10[1:0]		GPCDE9[1:0]			
	1	↑	1	0	1	GPCDE15[1:0]		GPCDE14[1:0]		GPCDE13[1:0]			
8.PNLSET	0	↑	1	1	0	1	1	1	0	0	0	(B8h)	Panel Setting
	0	↑	1	0	0	0	0	DPSCN[1]	DPSCN[0]	LAY[1]	LAY[0]		
9.SOCSET	0	↑	1	1	0	1	1	1	0	0	1	(B9h)	Source Setting
	0	↑	1	CLRAM[1:0]		GAMA	0	0	0	1	1		
10.CLRAM	0	↑	1	1	0	1	1	1	0	1	CLR	(BAh/BBh)	CLR RAM Control
11.GCTRL	0	↑	1	1	1	0	0	0	0	0	0	(C0h)	Gate Control
	1	↑	1	VGHS3	VGHS2	VGHS1	VGHS0	VGLS3	VGLS2	VGLS1	VGLS0		
12.VSHCTRL	0	↑	1	1	1	0	0	0	0	0	1	(C1h)	Source High Voltage Control
	1	↑	1	0	0	VSHRH5	VSHRH4	VSHRH3	VSHRH2	VSHRH1	VSHRH0		
	1	↑	1	0	0	VSHTH5	VSHTH4	VSHTH3	VSHTH2	VSHTH1	VSHTH0		
	1	↑	1	0	0	VSHRL5	VSHRL4	VSHRL3	VSHRL2	VSHRL1	VSHRL0		
	1	↑	1	0	0	VSHTL5	VSHTL4	VSHTL3	VSHTL2	VSHTL1	VSHTL0		
	1	↑	1	0	0	VSI5	VSI4	VSI3	VSI2	VSI1	VSI0		
	1	↑	1	0	0	VSK5	VSK4	VSK3	VSK2	VSK1	VSK0		
13.VSLCTRL	0	↑	1	1	1	0	0	0	0	1	0	(C2h)	Source Low Voltage Control
	1	↑	1	0	0	VSLRH5	VSLRH4	VSLRH3	VSLRH2	VSLRH1	VSLRH0		
	1	↑	1	0	0	VSLTH5	VSLTH4	VSLTH3	VSLTH2	VSLTH1	VSLTH0		
	1	↑	1	0	0	VSLRL5	VSLRL4	VSLRL3	VSLRL2	VSLRL1	VSLRL0		
	1	↑	1	0	0	VSLTL5	VSLTL4	VSLTL3	VSLTL2	VSLTL1	VSLTL0		
14.OSCEN	0	↑	1	1	1	0	0	0	1	1	1	(C7h)	OSC Enable
	1	↑	1	OSCEN	0	1	0	0	1	1	0		
	1	↑	1	1	1	1	0	1	0	0	1		

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
15.VCOMH CTRL	0	↑	1	1	1	0	0	1	0	1	1	(CBh)	VCOMH Control
	1	↑	1	0	0	VCOMH[5]	VCOMH[4]	VCOMH[3]	VCOMH[2]	VCOMH[1]	VCOMH[0]		
16.ID1SET	0	↑	1	1	1	0	0	1	1	0	0	(CCh)	ID1 Set
	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
17.ID2SET	0	↑	1	1	1	0	0	1	1	0	0	(CDh)	ID2 Set
	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
18.ID3SET	0	↑	1	1	1	0	0	1	1	0	0	(CEh)	ID3 Set
	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
19.BSTEN	0	↑	1	1	1	0	1	0	0	0	1	(D1h)	Booster Enable
	1	↑	1	0	0	0	0	0	0	0	BSTEN		
20.VSHLSEL	0	↑	1	1	1	0	1	0	1	1	0	(D6h)	Source Voltage Select
	1	↑	1	0	0	0	0	0	0	VSHLSEL[1:0]			
21. NVLOADCTRL	0	↑	1	1	1	0	1	0	1	1	1	(D7h)	NV Load Ctrl
	1	↑	1	0	1	1	0	1	VS_EN	ID_EN	0		
22.DBSPISET	0	↑	1	1	1	1	0	0	1	0	0	(E4h)	4SPI Input Select
	1	↑	1	0	0	0	DB4SPI	0	0	1	0		
23.NVMRD	0	↑	1	1	1	1	0	1	0	0	1	(E9h)	OTP Data Read
	1	1	↑	DO[7]	DO[6]	DO[5]	DO[4]	DO[3]	DO[2]	DO[1]	DO[0]		
24. NVMLOADEN	0	↑	1	1	1	1	0	1	0	1	1	(EBh)	NV Load Enable
	1	↑	1	0	0	0	0	0	0	XARD	0		
25.EXTBCTRL	0	↑	1	1	1	1	0	1	1	0	0	(ECh)	EXTB Control
	1	↑	1	EXTB_CTRL [7:0]									
26.NVM CTRL1	0	↑	1	1	1	1	1	1	0	0	0	(F8h)	NVM WR/RD Control
	1	↑	1	0	1	0	1	1	0	1	0	(5Ah)	
	1	↑	1	0	1	1	0	1	0	0	1	(69h)	
	1	↑	1	1	1	1	0	1	1	1	0	(EEh)	
	1	↑	1	0	0	0	0	0	PROG	RD	0		

Instruction	A0	R/W	ERD	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
27.NVM CTRL2	0	↑	1	1	1	1	1	1	0	1	0	(FAh)	NVM Program Setting
	1	↑	1	0	0	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]		
	1	↑	1	PIN[7]	PIN[6]	PIN[5]	PIN[4]	PIN[3]	PIN[2]	PIN[1]	PIN[0]		
28.NVM RDEN	0	↑	1	1	1	1	1	1	0	1	1	(FBh)	Enable NVM Read
	1	↑	1	0	1	0	0	1	0	1	0	(4Ah)	
	1	↑	1	1	0	1	0	0	1	0	1	(A5h)	
29.NVPROM	0	↑	1	1	1	1	1	1	0	1	1	(FCh)	Enable NVM Program
	1	↑	1	0	0	1	0	1	0	0	1	(29h)	
	1	↑	1	1	0	1	0	0	1	0	1	(A5h)	

8.2.1 GTCON (73h): Gate Timing Control

71H	GTCON (Gate Timing Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GTCON	0	↑	1	0	1	1	1	0	0	0	1	(73h)
1st Parameter	1	↑	1	0	0	DEON	DEMODE	GAB[3]	GAB[2]	GAB[1]	GAB[0]	
2nd parameter	1	↑	1	0	0	CLKDIV[1]	CLKDIV[0]	FDEPA[3]	FDEPA[2]	FDEPA[1]	FDEPA[0]	
3rd parameter	1	↑	1	DEPWA[7]	DEPWA[6]	DEPWA[5]	DEPWA[4]	DEPWA[3]	DEPWA[2]	DEPWA[1]	DEPWA[0]	
4th parameter	1	↑	1	DENUM[3]	DENUM[2]	DENUM[1]	DENUM[0]	DEINT[3]	DEINT[2]	DEINT[1]	DEINT[0]	

Description

-This command is used to set gate timing during destress period in low power mode. The frame period is composed of display update period and destress period.

DEON: Destress ON/OFF. “0”=>OFF ; “1”=>ON

DEMODE: Destress Mode. “0”=>DC Mode ; “1”=>AC Mode.

GAB[3:0]: GA and GB Frame Interval. GAB is set within the rage of 0 to 15 frames.

CLKDIV[1:0]: Destress CLK Divide

CLKDIV [1:0]	Destress CLK Divide
00	Divide by 1
01	Divide by 2
10	Divide by 4
11	Divide by 8

FDFPA[3:0]: First Destress Pulse to Data Upload End. Must be set within the rage of 0 to 15 (1 to 16 gate).

DEPWA[7:0]: Destress Pulse Width. Must be set within the rage of 0 to 255.

DENUM[3:0]: Destress Pulse Number. Must be set within the rage of 0 to 15.

DEINT[3:0]: Destress Pulse Interval Must be set within the rage of 1 to 15.

8.2.2 DUTYSET (B0h): Duty Setting

B0H	DUTYSET (Duty Setting)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DUTYSET	0	↑	1	1	0	1	1	0	0	0	0	(B0h)
1st Parameter	1	↑	1	0	DT[6]	DT[5]	DT[4]	DT[3]	DT[2]	DT[1]	DT[0]	

Description

DT[6:0] specifies the duty of the module in 4-line basis.

This command must be selected before sleep-out. Do not change this command while the display is turned on.

The relationship between the parameter DT [6:0] and the number of display lines is shown below.

DT[6]	DT[5]	DT[4]	DT[3]	DT[2]	DT[1]	DT[0]	Duty of Module
0	0	0	0	0	0	1	1/4
0	0	0	0	0	1	0	1/8
0	0	0	0	0	1	1	1/12
:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	1/312
1	0	0	1	1	1	1	1/316
1	0	1	0	0	0	0	1/320

8.2.3 FSTCOM (B1h): First Gate Setting

B1H	FSTCOM (First Gate Setting)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FSTCOM	0	↑	1	1	0	1	1	0	0	0	1	(B1h)
1st Parameter	1	↑	1	0	0	0	0	0	0	0	FTC[8]	
2nd parameter	1	↑	1	FTC[7]	FTC[6]	FTC[5]	FTC[4]	FTC[3]	FTC[2]	FTC[1]	FTC[0]	

Description

FST[8:0] specifies "the first output gate number – 1 " that mapping to the RAM page address 0.

For detail setting value, please see the table as below.

FST8	FST7	FST6	FST5	FST4	FST3	FST2	FST1	FST0	Line address
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320

Example:

If FST[8:0]=8h, Gate 9 would output the data of RAM page address 0.

8.2.4 FRCTRL (B2h): Frame Rate Control

B2H	FRCTRL (Frame Rate Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRCTRL	0	↑	1	1	0	1	1	0	0	1	0	(B2h)
1st Parameter	1	↑	1	0	0	0	0	0	0	0	HFR	
2nd parameter	1	↑	1	0	0	0	0	0	LFR[2]	LFR[1]	LFR[0]	

Description

Frame rate control in high power mode (HPM).

HFR	Frame rate (Hz)
0	16
1	32

Frame rate control in low power mode (LPM).

LFR [2:0]	Frame rate (Hz)
0h	0.25
1h	0.5
2h	1
3h	2
4h	4
5h	8

8.2.5 VCOMEQ (B3h): VCOM EQ Enable

B3H	VCOMEQEN (VCOM EQ Enable)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCOMEQ	0	↑	1	1	0	1	1	0	0	1	1	(B3h)
1st Parameter	1	↑	1	COMEQEN	0	0	1	0	1	0	0	

Description

COMEQEN:

"0": Disable VCOM EQ.

"1": Enable VCOM EQ.

8.2.6 GATEUPDEQ (B4h): Update Period Gate EQ Control

B4H	GATEUPDEQ (Update Period Gate EQ Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GATEUPDEQ	0	↑	1	1	0	1	1	0	1	0	0	(B4h)
1st Parameter	1	↑	1	FGS	GEQEN	1	0	0	1	0	1	
2nd parameter	1	↑	1	0	1	1	0	0	1	1	0	
3rd parameter	1	↑	1	GPCHPU4[1:0]		GPCHPU3[1:0]		GPCHPU2[1:0]		0	1	
4th parameter	1	↑	1	GPCHPU8[1:0]		GPCHPU7[1:0]		GPCHPU6[1:0]		GPCHPU5[1:0]		
5th parameter	1	↑	1	GPCHPU12[1:0]		GPCHPU11[1:0]		GPCHPU10[1:0]		GPCHPU9[1:0]		
6th parameter	1	↑	1	0	1	GPCHPU15[1:0]		GPCHPU14[1:0]		GPCHPU13[1:0]		
7rd parameter	1	↑	1	GPCLPU4[1:0]		GPCLPU3[1:0]		GPCLPU2[1:0]		0	1	
8th parameter	1	↑	1	GPCLPU8[1:0]		GPCLPU7[1:0]		GPCLPU6[1:0]		GPCLPU5[1:0]		
9th parameter	1	↑	1	GPCLPU12[1:0]		GPCLPU11[1:0]		GPCLPU10[1:0]		GPCLPU9[1:0]		
10th parameter	1	↑	1	0	1	GPCLPU15[1:0]		GPCLPU14[1:0]		GPCLPU13[1:0]		

Description

-This command is used to set gate EQ waveform in update period.

FGS: First Output Gate Select

FGS	First Output Gate
0	Right
1	Left

GEQEN: Gate EQ Enable

GEQEN	Gate EQ Enable
0	Disable
1	Enable

GPCHPUx/ GPCLPUx :

Gate EQ of update period includes 16 PWMs to achieve. PWM1 and PWM16 must be fixed in VGL voltage.

GPCHPU2~ GPCHPU15: Gate EQ Control in HPM at 2~15 PWM

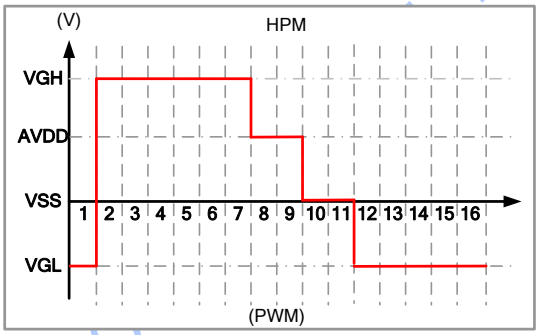
GPCLPU2~ GPCLPU15: Gate EQ Control in LPM. at 2~15 PWM

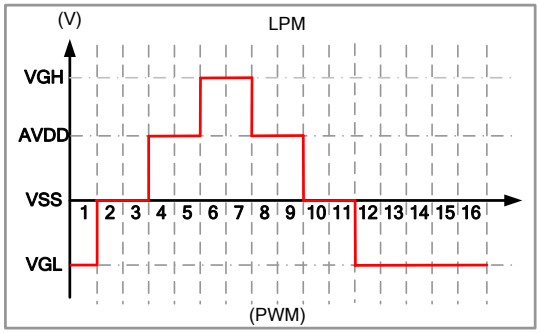
GPCHPUx /GPCLPUx [1:0]	Gate EQ Voltage
00	VSS
01	VGL
10	AVDD
11	VGH

Default Update EQ Setting .

HPM PWM	Default Parameter	Voltage	LPM PWM	Default Parameter	Voltage
GPCHPU2	11	VGH	**GPCLPU2**	00	VSS
GPCHPU3	11	VGH	**GPCLPU3**	00	VSS
GPCHPU4	11	VGH	**GPCLPU4**	10	AVDD
GPCHPU5	11	VGH	**GPCLPU5**	10	AVDD
GPCHPU6	11	VGH	**GPCLPU6**	11	VGH
GPCHPU7	11	VGH	**GPCLPU7**	11	VGH
GPCHPU8	10	AVDD	**GPCLPU8**	10	AVDD
GPCHPU9	10	AVDD	**GPCLPU9**	10	AVDD
GPCHPU10	00	VSS	**GPCLPU10**	00	VSS
GPCHPU11	00	VSS	**GPCLPU11**	00	VSS
GPCHPU12	01	VGL	**GPCLPU12**	01	VGL
GPCHPU13	01	VGL	**GPCLPU13**	01	VGL
GPCHPU14	01	VGL	**GPCLPU14**	01	VGL
GPCHPU15	01	VGL	**GPCLPU15**	01	VGL

Default Update EQ Waveform as below





8.2.7 GATEDSEQ (B5h): Destress Period Gate EQ Control

B5H	GATEDSEQ (Destress Period Gate EQ Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GATEDSEQ	0	↑	1	1	0	1	1	0	1	0	1	(B5h)
1st Parameter	1	↑	1	0	0	0	0	0	0	1	0	
2nd parameter	1	↑	1	0	0	0	0	0	1	0	0	
3rd parameter	1	↑	1	GPCDE4[1:0]		GPCDE3[1:0]		GPCDE2[1:0]		GPCDE1[1:0]		
4th parameter	1	↑	1	GPCDE8[1:0]		GPCDE7[1:0]		GPCDE6[1:0]		GPCDE5[1:0]		
5th parameter	1	↑	1	GPCDE12[1:0]		GPCDE11[1:0]		GPCDE510[1:0]		GPCDE9[1:0]		
6th parameter	1	↑	1	GPCDE16[1:0]		GPCDE15[1:0]		GPCDE514[1:0]		GPCDE13[1:0]		

Description

-This command is used to set gate EQ waveform in destress period.

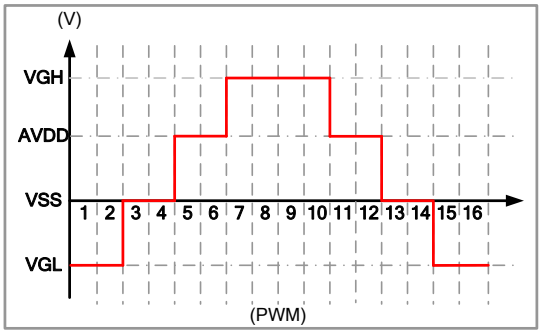
GPCDEx: Gate EQ of destress period includes 16 PWMs to achieve. PWM1 and PWM16 must be fixed in VGL voltage.

GPCDE2~ GPCDE15: Gate EQ control in destress period at 2~15 PWM

GPCDEx [1:0]	Gate EQ Voltage
00	VSS
01	VGL
10	AVDD
11	VGH

Default Destress EQ Setting .

PWM	Default Parameter	Voltage
GPCDE2	01	VGL
GPCDE3	00	VSS
GPCDE4	00	VSS
GPCDE5	10	AVDD
GPCDE6	10	AVDD
GPCDE7	11	VGH
GPCDE8	11	VGH
GPCDE9	11	VGH
GPCDE10	11	VGH
GPCDE11	10	AVDD
GPCDE12	10	AVDD
GPCDE13	00	VSS
GPCDE14	00	VSS
GPCDE15	01	VGL

	Default Destress EQ Waveform as below 

8.2.8 PNLSET (B8h): Panel Setting

B8H	PNLSET (Panel Setting)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PNLSET	0	↑	1	1	0	1	1	1	0	0	0	(B8h)
Parameter	1	↑	1	0	0	0	0	DPSCN[1]	DPSCN[0]	LAY[1]	LAY[0]	

Description

-This command is used to set the gate scan and panel layout.

DPSCN[1:0]: Display Gate Scan Mode Select

DPSCN [1:0]	Gate Scan Mode
00	Two Line Interval
01	One Line Interval
10	Frame interval

LAY[1:0]: Panel Layout Select

LAY [1:0]	Panel Layout
00	Two Line Interlace
01	One Line Interlace
10	Non Interlace

8.2.9 SOCSET (B9h): Source Setting

B9H	SOCSET (Source Setting)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SOCSET	0	↑	1	1	0	1	1	1	0	0	1	(B9h)
Parameter	1	↑	1	CLRAM[1]	CLRAM[0]	1	0	0	0	1	1	
Description	-This command is used to control gamma mode and inversion - CLRAM[1:0] : Clear RAM ON/OFF **CLRAM [1:0]** / **Clear RAM** 00 / OFF 11 / ON -GAMA : Gamma Mode Setting "0" = 4GS "1" = Mono (Default)											

8.2.10 CLRAM (BAh/BBh): Enable Clear RAM

BAH/BBH	CLRAM (Enable Clear RAM)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CLRAM	0	↑	1	1	0	1	1	1	0	1	CLR	(BAh/BBh)
parameter	No Parameter											
Description	-This command is used to enable clear RAM mode. CLR=0 ; Enable Clear RAM CLR=1 ; Disable Clear RAM											

8.2.11 GCTRL (C0h): Gate Voltage Control

C0H	GCTRL (Gate Voltage Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GCTRL	0	↑	1	1	1	0	0	0	0	0	0	(C0h)
Parameter	1	↑	1	VGHS3	VGHS2	VGHS1	VGHS0	VGLS3	VGLS2	VGLS1	VGLS0	

Description

VGHS[3:0]: VGH Setting.

VGHS[3:0]	VGH (V)
00h	8.0
01h	8.5
02h	9.0
03h	9.5
04h	10.0
05h	10.5
06h	11.0
07h	11.5
08h	12.0
09h	12.5
0Ah	13.0
0Bh	13.5
0Ch	14.0
0Dh	14.5
0Eh	15.0

VGLS[3:0]: VGL Setting.

VGLS[3:0]	VGL (V)
00h	-5.0
01h	-5.5
02h	-6.0
03h	-6.5
04h	-7.0
05h	-7.5
06h	-8.0
07h	-8.5
08h	-9.0
09h	-9.5
0Ah	-10.0

8.2.12 SCTRL1 (C1h): Source Voltage Control 1

C1H	SCTRL1 (Source Voltage Control 1)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SCTRL1	0	↑	1	1	1	0	0	0	0	0	1	(C1h)
1st Parameter	1	↑	1	0	0	VSHRH5	VSHRH4	VSHRH3	VSHRH2	VSHRH1	VSHRH0	
2nd parameter	1	↑	1	0	0	VSHTH5	VSHTH4	VSHTH3	VSHTH2	VSHTH1	VSHTH0	
3rd parameter	1	↑	1	0	0	VSHRL5	VSHRL4	VSHRL3	VSHRL2	VSHRL1	VSHRL0	
4th parameter	1	↑	1	0	0	VSHTL5	VSHTL4	VSHTL3	VSHTL2	VSHTL1	VSHTL0	
5th parameter	1	↑	1	0	0	VSI5	VSI4	VSI3	VSI2	VSI1	VSI0	
6th parameter	1	↑	1	0	0	VSK5	VSK4	VSK3	VSK2	VSK1	VSK0	

Description

-This command is used to set source voltage in different mode.

VSHRH[5:0] : Source High Voltage in HPM at Reflective mode

VSHTH[5:0] : Source High Voltage in HPM at Transmissive mode

VSHRL[5:0] : Source High Voltage in LPM at Reflective mode

VSHTL[5:0] : Source High Voltage in LPM at Transmissive mode

VSHxx[5:0]

VSHxx[5:0]	VSHxx (V)	VSHxx[5:0]	VSHxx (V)
00h	3.00	15h	4.05
01h	3.05	16h	4.10
02h	3.10	17h	4.15
03h	3.15	18h	4.20
04h	3.20	19h	4.25
05h	3.25	1Ah	4.30
06h	3.30	1Bh	4.35
07h	3.35	1Ch	4.40
08h	3.40	1Dh	4.45
09h	3.45	1Eh	4.50
0Ah	3.50	1Fh	4.55
0Bh	3.55	20h	4.60
0Ch	3.60	21h	4.65
0Dh	3.65	22h	4.70
0Eh	3.70	23h	4.75
0Fh	3.75	24h	4.80
10h	3.80	25h	4.85
11h	3.85	26h	4.90
12h	3.90	27h	4.95
13h	3.95	28h	5.00
14h	4.00		

VSI [5:0] : Gamma1 Voltage

VSI[5:0]	VSI (V)	VSI[5:0]	VSI (V)
00h	2.50	15h	3.55
01h	2.55	16h	3.60
02h	2.60	17h	3.65
03h	2.65	18h	3.70
04h	2.70	19h	3.75
05h	2.75	1Ah	3.80
06h	2.80	1Bh	3.85
07h	2.85	1Ch	3.90
08h	2.90	1Dh	3.95
09h	2.95	1Eh	4.00
0Ah	3.00	1Fh	4.05
0Bh	3.05	20h	4.10
0Ch	3.10	21h	4.15
0Dh	3.15	22h	4.20
0Eh	3.20	23h	4.25
0Fh	3.25	24h	4.30
10h	3.30	25h	4.35
11h	3.35	26h	4.40
12h	3.40	27h	4.45
13h	3.45	28h	4.50
14h	3.50		

VSK [5:0] : Gamma2 Voltage

VSI[5:0]	VSI (V)	VSI[5:0]	VSI (V)
00h	1.50	15h	2.55
01h	1.55	16h	2.60
02h	1.60	17h	2.65
03h	1.65	18h	2.70
04h	1.70	19h	2.75
05h	1.75	1Ah	2.80
06h	1.80	1Bh	2.85
07h	1.85	1Ch	2.90
08h	1.90	1Dh	2.95
09h	1.95	1Eh	3.00
0Ah	2.00	1Fh	3.05
0Bh	2.05	20h	3.10
0Ch	2.10	21h	3.15
0Dh	2.15	22h	3.20
0Eh	2.20	23h	3.25
0Fh	2.25	24h	3.30
10h	2.30	25h	3.35
11h	2.35	26h	3.40
12h	2.40	27h	3.45
13h	2.45	28h	3.50
14h	2.50		

8.2.13 SCTRL2 (C2h): Source Voltage Control2

C2H	SCTRL2 (Source Voltage Control 2)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SCTRL2	0	↑	1	1	1	0	0	0	0	1	0	(C2h)
1st Parameter	1	↑	1	0	0	VSLRH5	VSLRH4	VSLRH3	VSLRH2	VSLRH1	VSLRH0	
2nd parameter	1	↑	1	0	0	VSLTH5	VSLTH4	VSLTH3	VSLTH2	VSLTH1	VSLTH0	
3rd parameter	1	↑	1	0	0	VSLRL5	VSLRL4	VSLRL3	VSLRL2	VSLRL1	VSLRL0	
4th parameter	1	↑	1	0	0	VSLTL5	VSLTL4	VSLTL3	VSLTL2	VSLTL1	VSLTL0	

Description

-This command is used to set source voltage in different mode.

VSLRH[5:0] : Source Low Voltage in HPM at Reflective mode

VSLTH[5:0] : Source Low Voltage in HPM at Transmissive mode

VSLRL[5:0] : Source Low Voltage in LPM at Reflective mode

VSLTL[5:0] : Source Low Voltage in LPM at Transmissive mode

VSLxx[5:0]	VSLxx (V)	VSLxx[5:0]	VSLxx (V)
00h	0.00	1Ah	1.30
01h	0.05	1Bh	1.35
02h	0.10	1Ch	1.40
03h	0.15	1Dh	1.45
04h	0.20	1Eh	1.50
05h	0.25	1Fh	1.55
06h	0.30	20h	1.60
07h	0.35	21h	1.65
08h	0.40	22h	1.70
09h	0.45	23h	1.75
0Ah	0.50	24h	1.80
0Bh	0.55	25h	1.85
0Ch	0.60	26h	1.90
0Dh	0.65	27h	1.95
0Eh	0.70	28h	2.00
0Fh	0.75	29h	2.05
10h	0.80	2Ah	2.10
11h	0.85	2Bh	2.15
12h	0.90	2Ch	2.20
13h	0.95	2Dh	2.25
14h	1.00	2Eh	2.30
15h	1.05	2Fh	2.35
16h	1.10	30h	2.40
17h	1.15	31h	2.45
18h	1.20	32h	2.50
19h	1.25		

8.2.14 OSCEN (C7h): OSC Enable

C7H	OSCEN (OSC Enable)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
OSCEN	0	↑	1	1	1	0	0	0	1	1	1	(C7h)
Parameter	1	↑	1	OSCEN	0	1	0	0	1	1	0	
Parameter	1	↑	1	1	1	1	0	1	0	0	1	
Description	**OSCEN:** "0": Disable OSC "1": Enable OSC											

8.2.15 VCOMCTRL (CBh): VCOMH Voltage Setting

CBH	VCOMCTRL (VCOM Voltage Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCOMCTRL	0	↑	1	1	1	0	0	1	0	1	1	(CBh)
Parameter	1	↑	1	0	0	VCOMH[5]	VCOMH[4]	VCOMH[3]	VCOMH[2]	VCOMH[1]	VCOMH[0]	

Description

VCOMH[5:0]

VCOMH[5:0]	VCOMH (V)	VCOMH[5:0]	VCOMH (V)	VCOMH[5:0]	VCOMH (V)
00h	3.00	0Eh	3.70	1Ch	4.40
01h	3.05	0Fh	3.75	1Dh	4.45
02h	3.10	10h	3.80	1Eh	4.50
03h	3.15	11h	3.85	1Fh	4.55
04h	3.20	12h	3.90	20h	4.60
05h	3.25	13h	3.95	21h	4.65
06h	3.30	14h	4.00	22h	4.70
07h	3.35	15h	4.05	23h	4.75
08h	3.40	16h	4.10	24h	4.80
09h	3.45	17h	4.15	25h	4.85
0Ah	3.50	18h	4.20	26h	4.90
0Bh	3.55	19h	4.25	27h	4.95
0Ch	3.60	1Ah	4.30	28h	5.00
0Dh	3.65	1Bh	4.35		

8.2.16 ID1SET (CCh): ID1 Setting

CCH	ID1SET (ID1 Code Setting)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ID1SET	0	↑	1	1	1	0	0	1	1	0	0	(CCh)
Parameter	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
Description	**ID1[7:0]:** ID1 Setting.											

8.2.17 ID2SET (CDh): ID2 Setting

CDH	ID2SET (ID2 Code Setting)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ID2SET	0	↑	1	1	1	0	0	1	1	0	0	(CDh)
Parameter	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
Description	**ID2[7:0]:** ID1 Setting.											

8.2.18 ID3SET (CEh): ID3 Setting

CEH	ID3SET (ID3 Code Setting)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ID3SET	0	↑	1	1	1	0	0	1	1	1	0	(CEh)
Parameter	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	**ID3[7:0]:** ID1 Setting.											

8.2.19 BSTEN (D1h): Booster Enable

D1H	BSTEN (Booster Enable)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BSTEN	0	↑	1	1	1	0	1	0	0	0	1	(D1h)
Parameter	1	↑	1	0	0	0	0	0	0	0	BSTEN	
Description	**BSTEN:** "0": Disable Booster "1": Enable Booster											

8.2.20 VSHLSEL(D6h): Source Voltage Select

D6H	VSHLSEL (Source Voltage Select)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BSTEN	0	↑	1	1	1	0	1	0	1	1	0	(D6h)
Parameter	1	↑	1	0	0	0	0	0	0	VSHLSEL[1:0]		

Description

VSHLSEL[1:0]

VSHRH/VSLRH : Source High/Low Voltage in HPM at Reflective mode

VSHTH/VSLTH : Source High/Low Voltage in HPM at Transmissive mode

VSHRL/VSLRL: Source High/Low Voltage in LPM at Reflective mode

VSHTL/VSLTL : Source High/Low Voltage in LPM at Transmissive mode

VSHLSEL [1:0]	Source Voltage
00	VSHRH/VSLRH
01	VSHTH/VSLTH
10	VSHRL/VSLRL
11	VSHTL/VSLTL

8.2.21 NVMLOADCTRL(D7h): NVM Load Control

D7H	NVMLOADCTRL (NVM Load Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMLOADCTRL	0	↑	1	1	1	0	1	0	1	1	1	(D7h)
Parameter	1	↑	1	0	1	1	0	1	VS_EN	ID_EN	0	

Description

-This command is used to control the items load by NVM.

Bit	NVM Load Item	Value
VS_EN	Source High/Low Voltage	'1' =Disable Source High/Low Voltage Load '0' = Enable Source High/Low Voltage Load
ID_EN	ID1/ID2/ID3	'1' =Disable ID1/ID/ID3 Load '0' = Enable ID1/ID/ID3 Load

8.2.22 DBSPISET (E4h): 4SPI Input Data select

E4H	DBSPISET (4SPI Input Data select)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DBSPISET	0	↑	1	1	1	1	0	0	1	0	0	(E4h)
Parameter	1	↑	1	0	0	DB4SPI	0	0	0	1	0	
Description	**DB4SPI:** "0": Singel Data Lane (SDA) "1": Two Data Lane (Lane1: „SDA" ; Lane2: „RWR")											

8.2.23 NVMRD (E9h): NVM Data Read

E9H	NVMRD (NVM Data Read)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMRD	0	↑	1	1	1	1	0	1	0	0	1	(E9h)
Parameter	1	↑	1	DO[7]	DO[6]	DO[5]	DO[4]	DO[3]	DO[2]	DO[1]	DO[0]	
Description	-This command is used to read register that load from NVM.											

8.2.24 NVMLOADEN (EBh): NVM Load Enable

EBH	NVMLOADEN (NVM Load Enable)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMLOADEN	0	↑	1	1	1	1	0	1	0	1	1	(EBh)
Parameter	1	↑	1	0	0	0	0	0	0	XARD	0	
Description	**XARD:** "0": NVM load will be trigger by sleep Out. "1": NVM load will not be trigger by sleep Out.											

8.2.25 EXTBCTRL (ECh): EXTB Control

ECH	EXTBCTRL (EXTB Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EXTBCTRL	0	↑	1	1	1	1	0	1	1	0	0	(ECh)
Parameter	1	↑	1	EXTB_CTRL[7:0]								
Description	**EXTB_CTRL[7:0]:** "5Ah": EXTB=H (VDD) "A5h": EXTB=L (VSS)											

8.2.26 NVMCTRL1 (F8h): NVM WR/RD Control

F8H	NVMCTRL1 (NVM WR/RD Control)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMCTRL1	0	↑	1	1	1	1	1	1	0	0	0	(F8h)
Parameter	1	↑	1	0	1	0	1	1	0	1	0	(5Ah)
Parameter	1	↑	1	0	1	1	0	1	0	0	1	(69h)
Parameter	1	↑	1	1	1	1	0	1	1	1	0	(EEh)
Parameter	1	↑	1	0	0	0	0	0	PROG	RD	0	
Description	-NVM WR/RD mode select											

Bit	Value
PROG	'1' =Enable Program Mode '0' =Disable Program Mode
RD	'1' = Enable Read Mode '0' = Disable Read Mode

8.2.27 NVMCTRL2(FAh): NVM Program Setting

FAH	NVMCTRL2 (NVM Program Setting)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMCTRL2	0	↑	1	1	1	1	1	1	0	1	0	(FAh)
Parameter	1	↑	1	0	0	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]	
Parameter	1	↑	1	PIN[7]	PIN[6]	PIN[5]	PIN[4]	PIN[3]	PIN[2]	PIN[1]	PIN[0]	
Description	-NVM program register address and data setting.											

8.2.28 NVMRDEN(FBh): NVM Read Enable

FBH	NVMRDEN (NVM Read Enable)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMCTRL2	0	↑	1	1	1	1	1	1	0	1	1	(FBh)
Parameter	1	↑	1	0	1	0	0	1	0	1	0	(4Ah)
Parameter	1	↑	1	1	0	1	0	0	1	0	1	(A5h)
Description	-Enable NVM read mode.											

8.2.29 NVMPROM(FCh): NVM Program Enable

FCH	NVMPROM (NVM Program Enable)											
Inst / Para	D/CX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMCTRL2	0	↑	1	1	1	1	1	1	1	0	0	(FCh)
Parameter	1	↑	1	0	0	1	0	1	0	0	1	(29h)
Parameter	1	↑	1	1	0	1	0	0	1	0	1	(A5h)
Description	-Enable NVM program mode.											

9 ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
I/O Power Supply Voltage	VDDI	- 0.3 ~ +4.0	V
Analog Power Supply Voltage	VDDA	- 0.3 ~ +4.0	V
Reference Power Supply Voltage	VDDR	- 0.3 ~ +4.0	V
LCD Driver Supply Voltage	VMV	- 0.3 ~ +4.0	V
	AVDD	- 0.3 ~ +6.5V	V
	VCOMH-VCOML	-0.3 ~ +5.5	V
	VSH-VSL	-0.3 ~ +5.5	V
	VGH-VGL	-0.3 ~ +25.5	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +70	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Table 1 Maximum Ratings

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

10 DC CHARACTERISTICS

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
Analog Power Supply	VDDA\VDDR	Analog Power	2.55		3.6	V	
Digital Power Supply	VDDI	I/O Supply Voltage	1.65		3.6	V	
Gate Driver High Voltage	VGH		8		13.5	V	Note 2
Gate Driver Low Voltage	VGL		-10		-5	V	
Gate Driver Supply Voltage		| VGH-VGL |	13		23.5	V	Note 3
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM amplitude	VCOM		0		5	V	
Source Driver							
Source Driver High Voltage	VSH		3		5	V	
Source Driver High Voltage	VSL		0		2.5	V	

Table 2 Basic DC Characteristics

Notes:

1. TA= -30 to 70℃ (to +85℃ no damage).

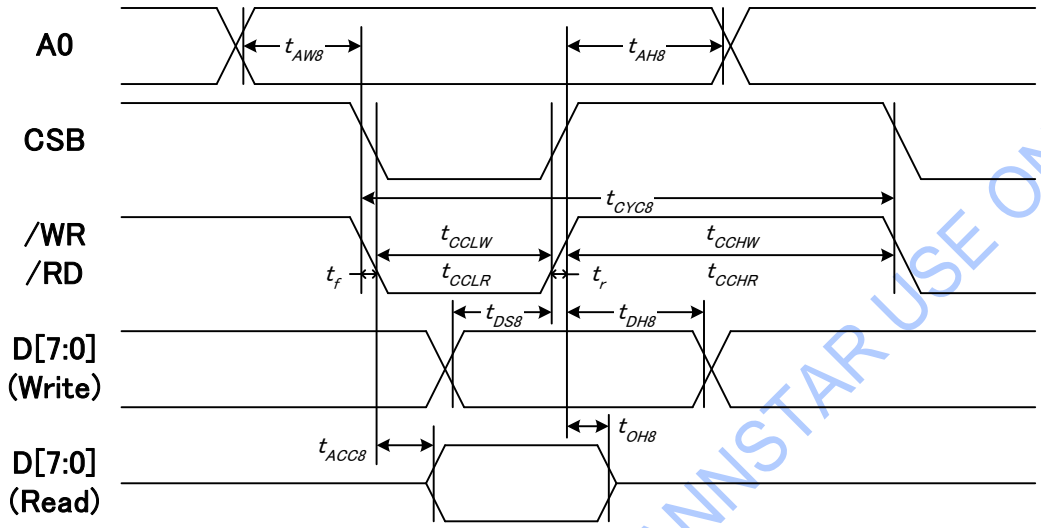
2. When evaluating the maximum and minimum of VGH, VDD=2.8V.

3. The maximum value of \|VGH-VGL\| can not over 24V.

11 AC CHARACTERISTICS

11.1 Interface Timing

11.1.1 System Bus Timing for Parallel 8080 MCU Interface



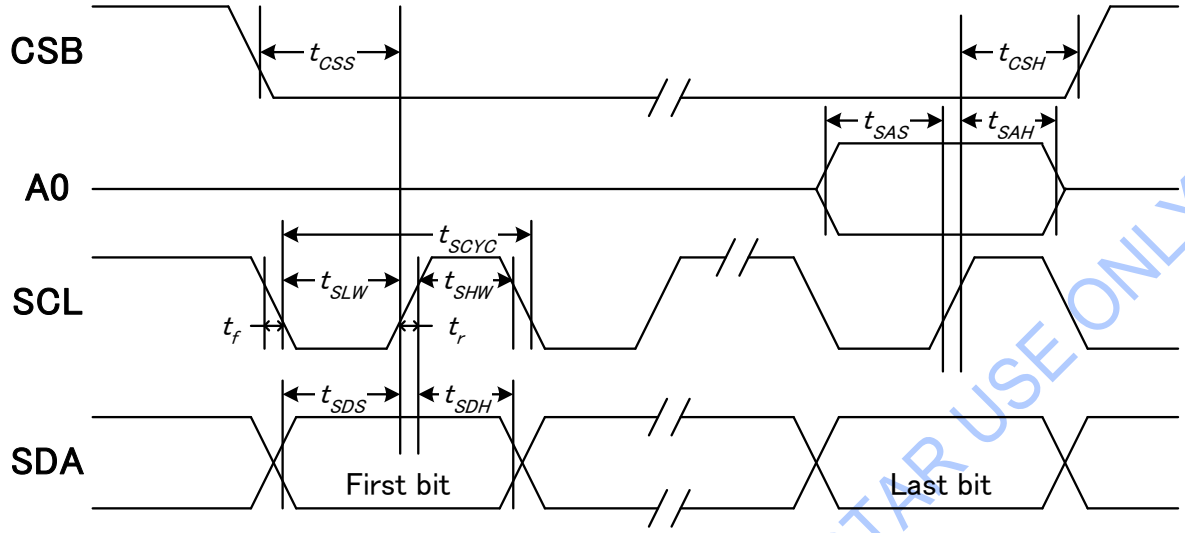
VDDI = 1.8~3.3V, Ta = 25˚C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		20	—	ns
Address hold time		tAH8		0	—	
System cycle time (WRITE)	/WR	tCYC8		160	—	
/WR L pulse width (WRITE)		tCCLW		70	—	
/WR H pulse width (WRITE)		tCCHW		70	—	
System cycle time (READ)	RD	tCYC8		400	—	
/RD L pulse width (READ)		tCCLR		180		
/RD H pulse width (READ)		tCCHR		180		
WRITE Data setup time	D[7:0]	tDS8		15	—	
WRITE Data hold time		tDH8		15	—	
READ access time		tACC8	CL = 30 pF	—	100	
READ Output disable time		tOH8	CL = 30 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDDI as the reference.

11.1.2 System Bus Timing for 4SPI MCU Interface



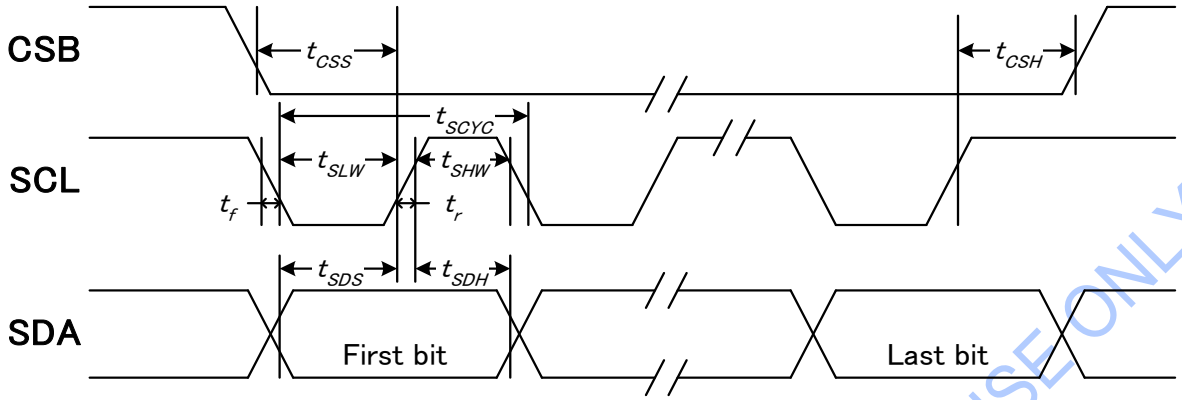
VDDI = 1.8~3.3V, Ta = 25˚C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		30	—	ns
SCLK “H” pulse width		tSHW		15	—	
SCLK “L” pulse width		tSLW		15	—	
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		10	—	
Data setup time	SDA	tSDS		10	—	
Data hold time		tSDH		10	—	
CSB-SCLK time	CSB	tCSS		10	—	
CSB-SCLK time		tCSH		10	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

11.1.3System Bus Timing for 3SPI MCU Interface



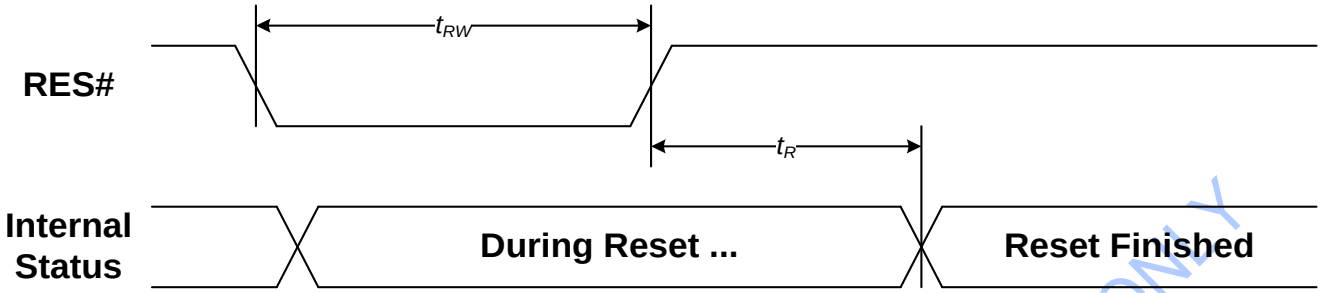
VDDI = 1.8~3.3V, Ta = 25˚C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		30	—	ns
SCLK “H” pulse width		tSHW		15	—	
SCLK “L” pulse width		tSLW		15	—	
Data setup time	SDA	tSDS		10	—	
Data hold time		tSDH		10	—	
CSB-SCLK time	CSB	tCSS		10	—	
CSB-SCLK time		tCSH		10	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

11.1.4 Reset Timing



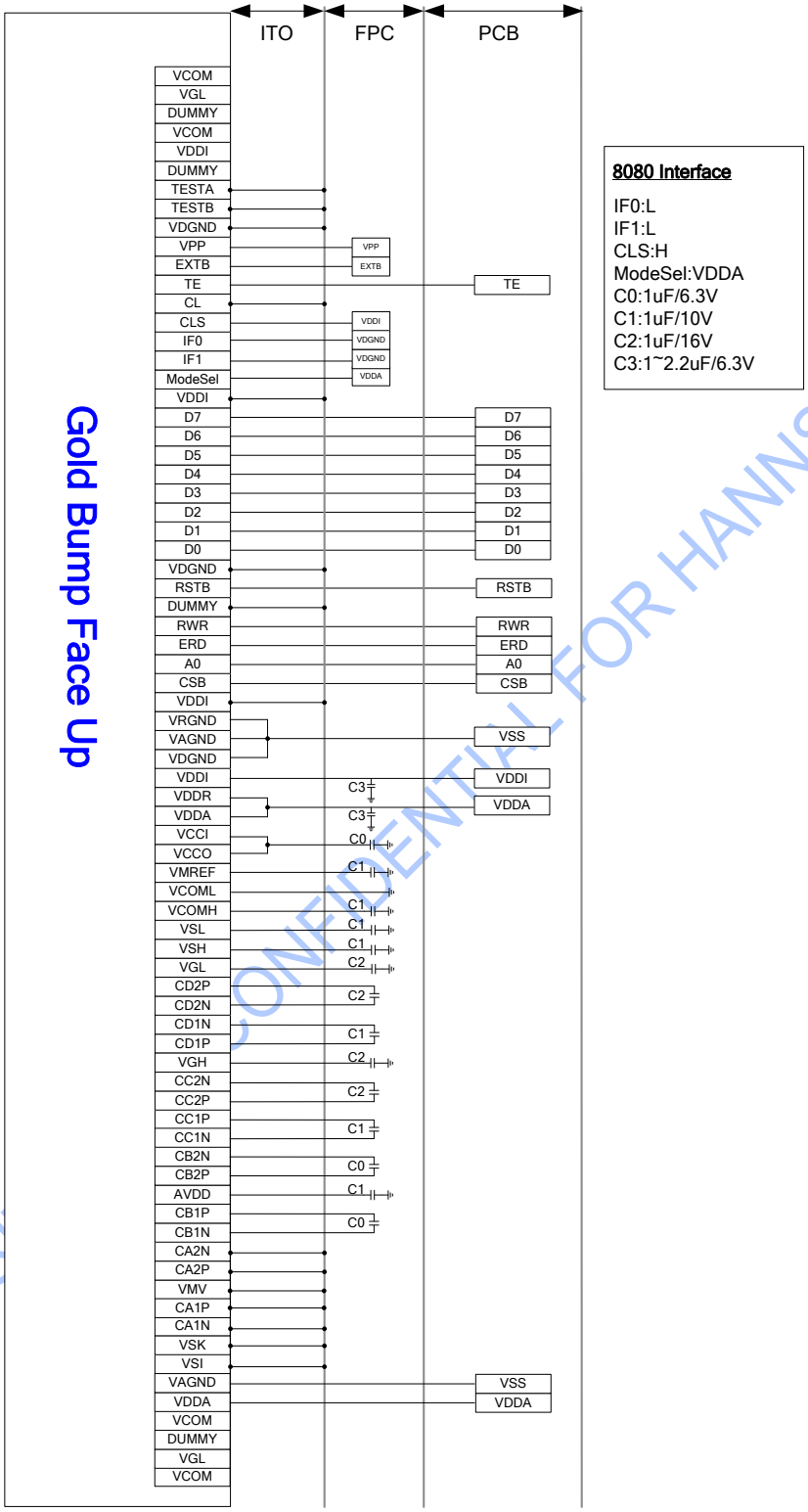
VDDI = 1.8~3.3V, Ta = 25˚C

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1	ms
Reset “L” pulse width	tRW		1	—	ms

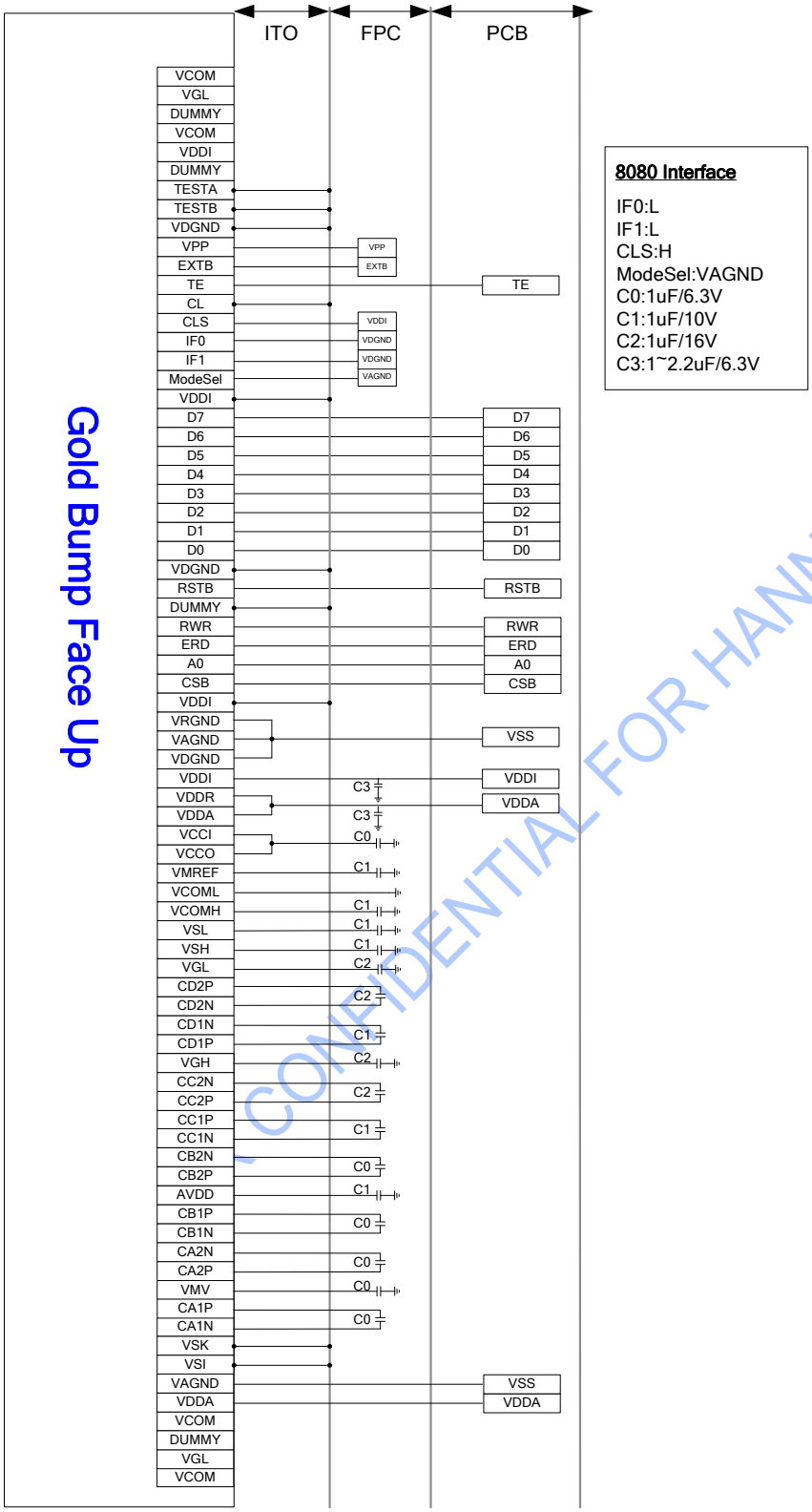
12 APPLICATION NOTE

12.1 Parallel 8080 Interface

12.1.1 VDDA=3.3V

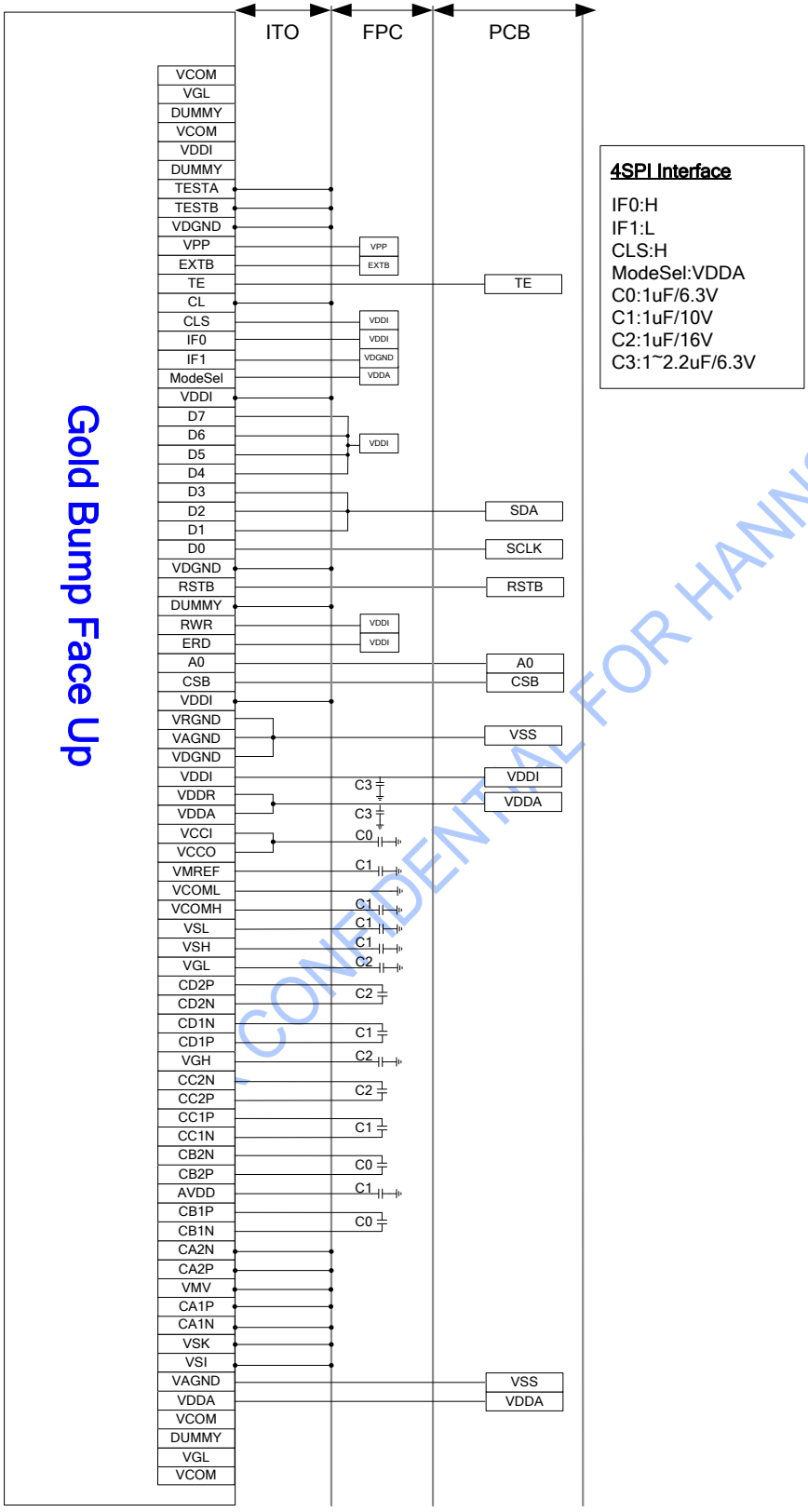


12.1.2 VDDI=VDDA=1.8V

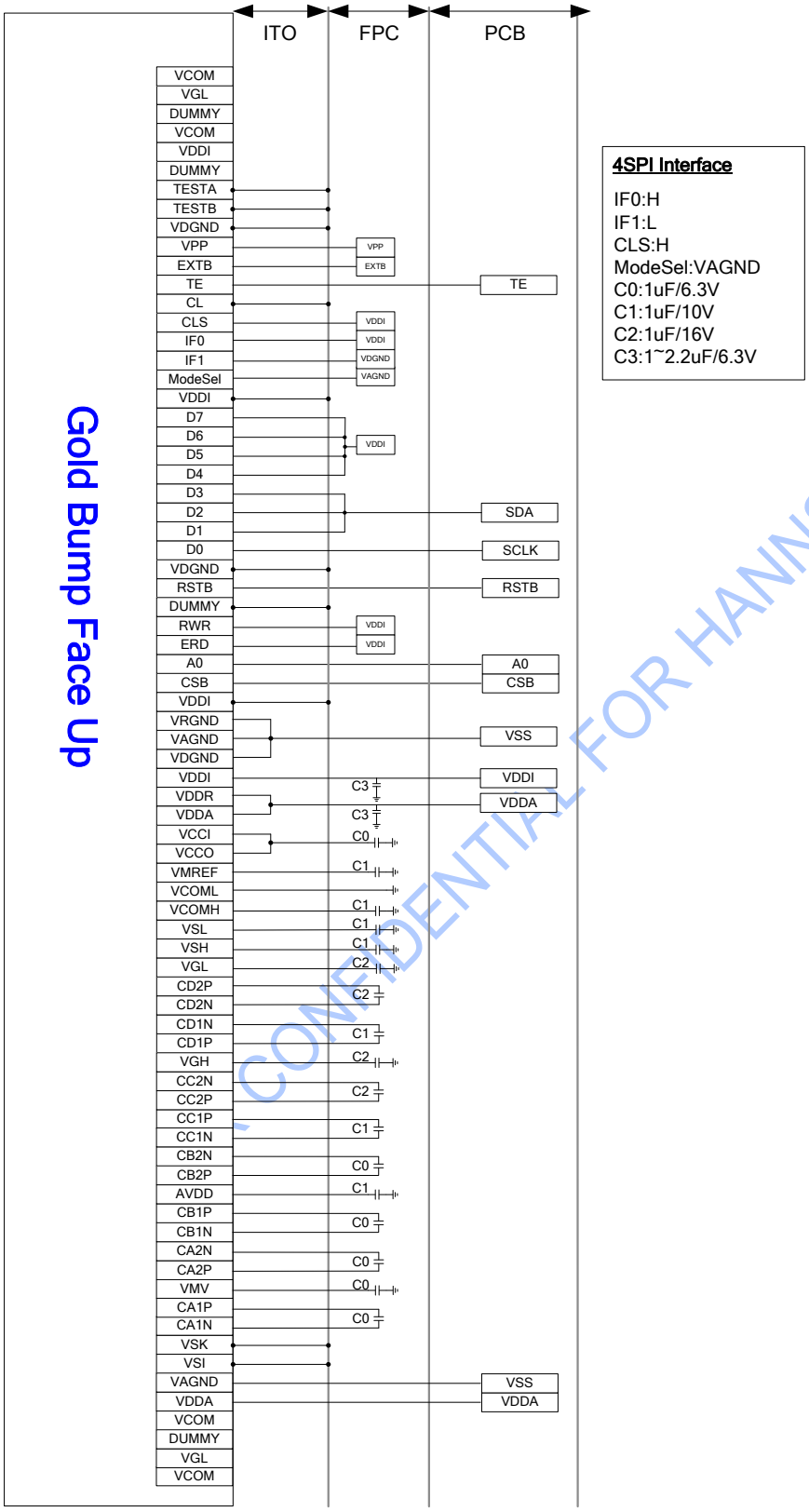


12.2 4-line SPI Interface

12.2.1 VDDA=3.3V

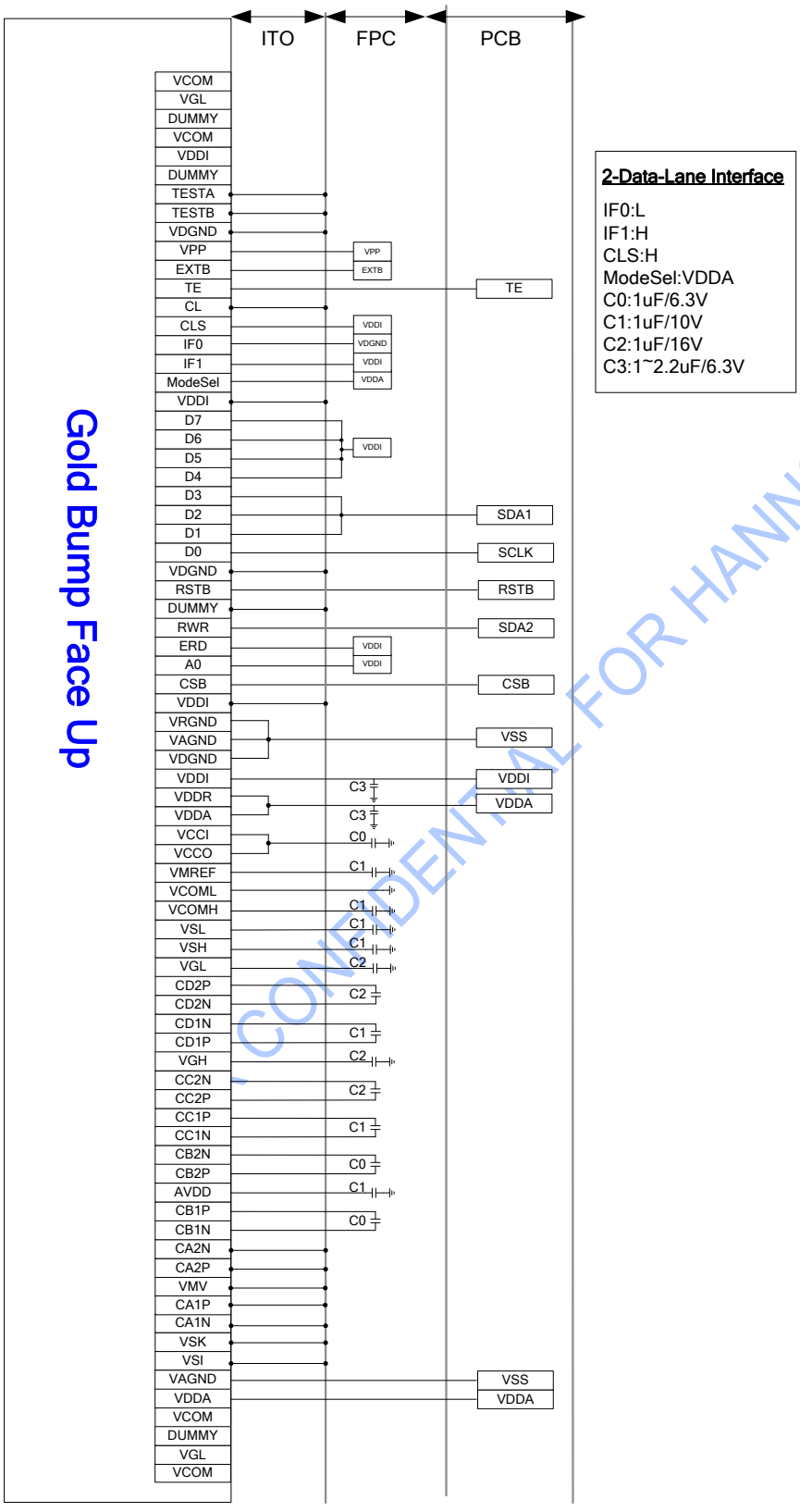


12.2.2 VDDI=VDDA=1.8V

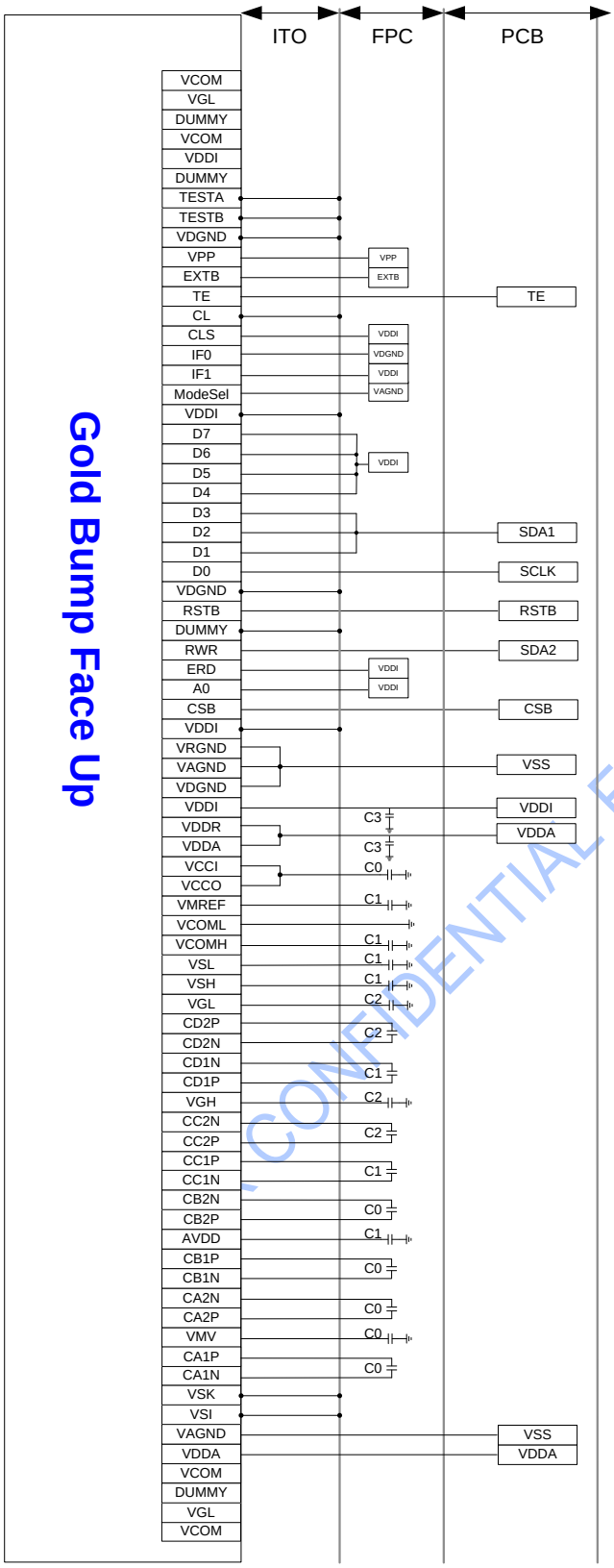


12.3 2-Data-Lane Serial Interface

12.3.1 VDDA=3.3V

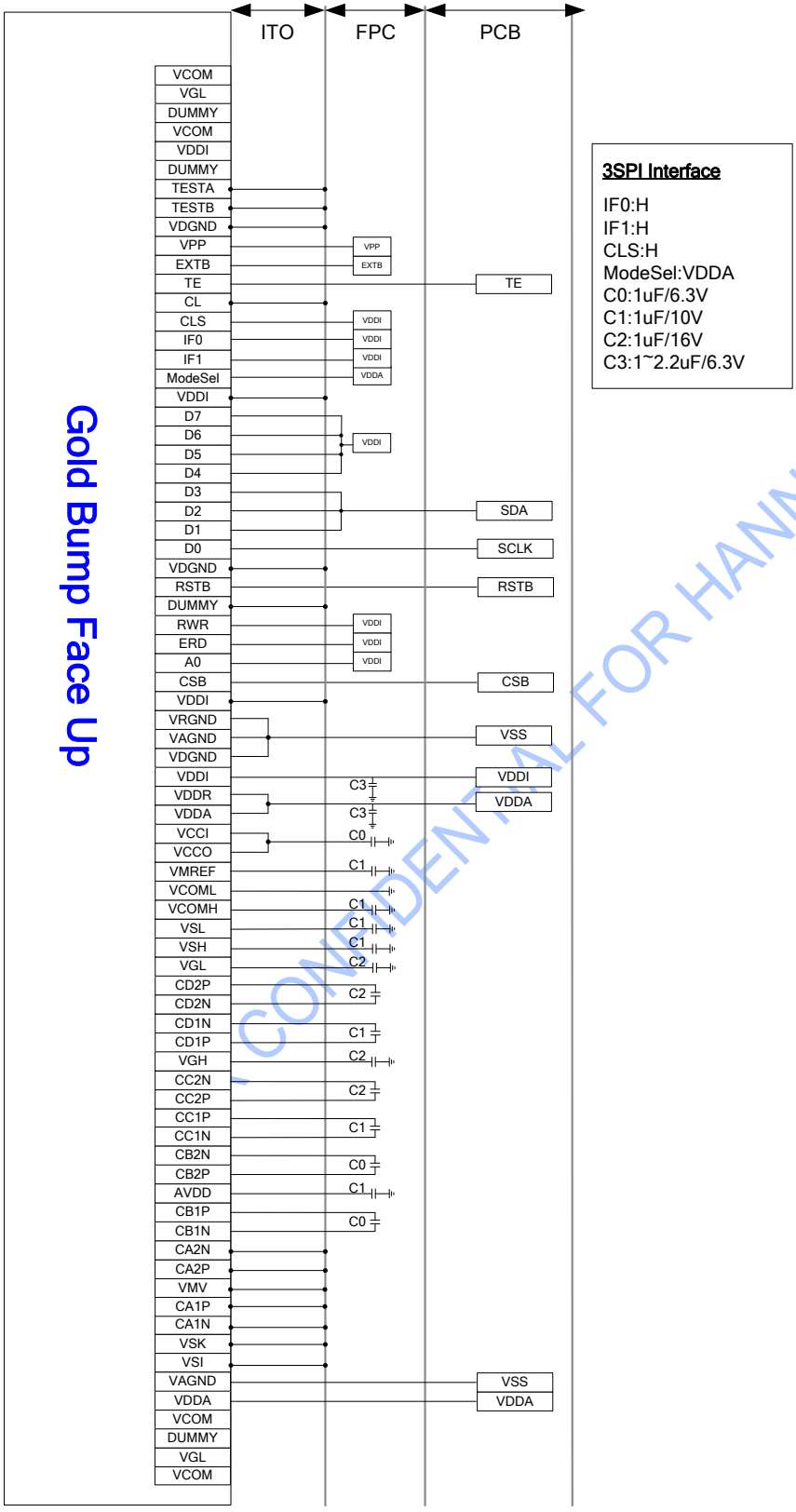


12.3.2 VDDI=VDDA=1.8V

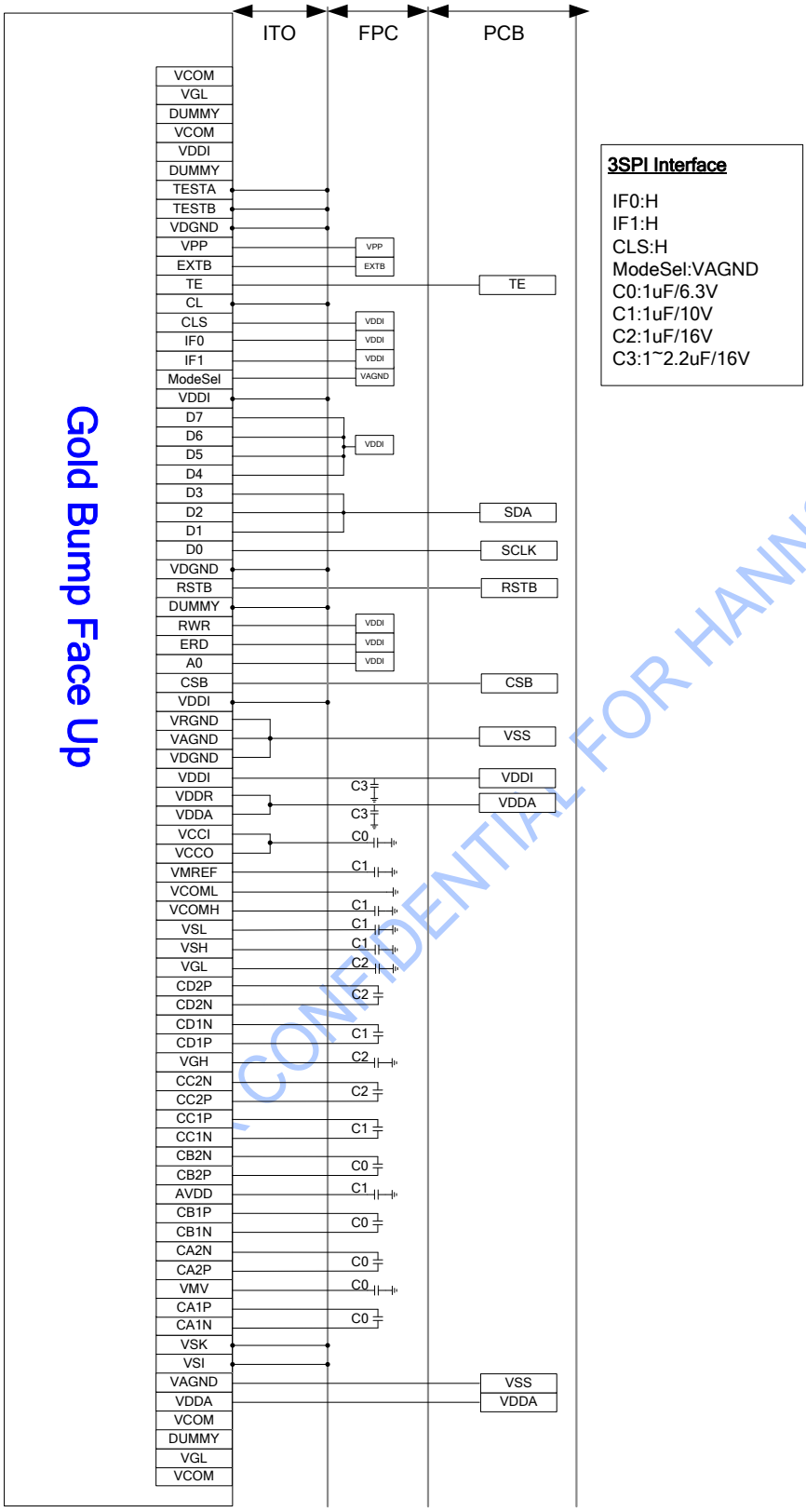


12.4 3-line SPI Interface

12.4.1 VDDA=3.3V



12.4.2 VDDI=VDDA=1.8V



13 REVISION HISTORY

Version	Date	Description
V0.0	2018/02	● Preliminary.