**Description of the pipelineRegister circuit files for Labs 8 –Pipeline CPU**

The pipeline registers are designated by a number indicating which stages they bridge and a

descriptor indicating the information stored at that stage.

* 1 indicates the IF/ID register
* 2 indicates the ID/EX registers
* 3 indicates the EX/Mem registers
* 4 indicate the Mem/WB registers
* PC indicates the address information needed to compute branch and jump PC addresses
* Ctrl indicate control lines
* DP indicates the main data-path
* ALUCtrl indicates the ALU control bits going to the ALU
* Rd indicates the destination register for write-back
  + Rt is the register to use for write-back.

The initial file is pipelineRegisters.circ. It includes the following completed pipeline

registers which are used in PiplineARM-CPU1-start.circ:

PipeReg1 (only one pipeline register needed here for PC and Instruction)

PipeReg2PC (stores PC)

PipeReg2Ctrl (stores all control values)

PipeReg2DP (stores data path values from A-reg, B-reg, and extended immediate)

PipeReg2ALUCtrl/Rd (ALU control bits and possible destination register rd)

You need to complete this file by determining what pipeline registers will be needed between the EX and MEM stages, labeled PipeReg3x, and what pipeline registers will be needed between the MEM and WB stages, labeled PipeReg4x, where the x is replaced by an appropriate designation.

PipeReg3DP (Stores result and zero bit of ALU and data paths of B-reg)

PipeReg3Rt (Stores destination register Rt)

PipeReg3BAddress (Store the branch address)

PipeReg3Ctrl (Stores all control values excluding ALUsrc)

PipeReg4Rt (Stores destination register Rt)

PipeReg4DP (Stores either data from memory or result from ALU)

PipeReg4RegCtrl (Stores control bits for MemToReg and RegWrite to determine what to write back)