Uncond Cond

Branch Branch MemToReg MemRead  MemWrite ALUSrc  RegWrite Reg2Loc ALU control bits

**add**

**sub**

**and**

**or**

**ldur**

**stur**

**cbz**

**b**

(ALU has four ontrol bits)

Instruction Opcode

R-type

add 100 0101 1000

sub 110 0101 1000

and 100 0101 0000

or 101 0101 0000

Load/Store

ldur 111 1100 0010

stur 111 1100 0000

Conditional Branch

cbz 101 1010 0xxx

Unconditional Branch

b 000 101x xxxx

Note: for this instruction set, bit 28 in the opcode (fourth from left) determines the value of Reg2Loc control.