Uncond Cond

Branch Branch MemToReg MemRead  MemWrite ALUSrc  RegWrite Reg2Loc ALU control bits

**add 0 0 0 0 0 0 1 0 0010**

**sub 0 0 0 0 0 0 1 0 0110**

**and 0 0 0 0 0 0 1 0 0000**

**or 0 0 0 0 0 0 1 0 0001**

**ldur 0 0 1 1 0 1 1 X 0010**

**stur 0 0 X 0 1 1 0 1 0010**

**cbz 0 1 0 0 0 0 0 1 0011**

**b 1 0 0 0 0 X 0 X XXXX**

(ALU has four ontrol bits)

Instruction Opcode

R-type

add 100 0101 1000

sub 110 0101 1000

and 100 0101 0000

or 101 0101 0000

Load/Store

ldur 111 1100 0010

stur 111 1100 0000

Conditional Branch

cbz 101 1010 0xxx

Unconditional Branch

b 000 101x xxxx

Note: for this instruction set, bit 28 in the opcode (fourth from left) determines the value of Reg2Loc control.