## funct7

0000000	rs2	rs1	000	rd	0110011	R add
00000	rs2	rs1	000	rd	0110011	R sub
0000000	rs2	rs1	001	rd	0110011	R sll
0000000	rs2	rs1	010	rd	0110011	R slt
0000000	rs2	rs1	011	rd	0110011	Rsltu
0000000	rs2	rs1	100	rd	0110011	R xor
0000000	rs2	rs1	101	rd	0110011	R srl
d100000	rs2	rs1	101	rd	0110011	R sra
0000000	rs2	rs1	110	rd	0110011	R or
0000000	rs2	rs1	111	rd	0110011	R and
						· -
0000000	shamt	rs1	001	rd	0010011	I slli
0000000	shamt	rs1	101	rd	0010011	I srli
( <mark>1</mark> )00000	shamt	rs1	101	rd	0010011	I srai

31		5 24 2		20	19	15 14	12 1	1 8	7	6 0	<b>\</b>
	funct7	I	s2		rs1	funct	3	ro	i	opcode	R-type
	imm[1	1.01			no 1	funct	2			anaada	T tumo
	imm[1	1.0]			rs1	Tunct	3	ro		opcode	I-type
in	nm[11:5]	r	s2		rs1	funct	3	imm[	4:0]	opcode	S-type
imm[12]	imm[10:5]	r	s2		rs1	funct	3 i	imm[4:1]	imm[11]	opcode	B-type
	[21.12]									1	
imm[31:12] rd							opcode	U-type			
imm[20]	imm[20] imm[10:1] imm[11]			imm[19:12]		Т	rd		opcode	J-type	

## 指令包含两类信息:

1.身份信息: opcode、funct3、funct7 → CU

2.参数信息: rs1 、 rs2 、 rd → REGFILES

imm12  $\downarrow$  imm20  $\rightarrow$  ALU

## 立即数相关指令

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imm[11:0]	rs1	000	rd	0010011	I addi	
imm[11:0]	rs1	010	rd	0010011	I slti	
imm[11:0]	rs1	011	rd	0010011	I sltiu	
imm[11:0]		rs1	100	rd	0010011	I xori
imm[11:0]		rs1	110	rd	0010011	I ori
imm[11:0]		rs1	111	rd	0010011	I andi
						1
0000000	shamt	rs1	001	rd	0010011	I slli
0000000	shamt	rs1	101	rd	0010011	I srli
0100000 shamt		rs1	101	rd	0010011	I srai
			:			-
imm[11:0]	rs1	010	rd	0000011	I lw	

```
begin
          case (opcode)
               7' b0110011: //r
               begin
                   regWe=1'b1;
                   pcSourceCode=2'b00;
                   memWe=1'b0:
                   bIsImm=1'b0:
                   bIs20bImm=1'b0;
                   regDataIsFromMem=1'b0;
                   regDataIsFromPC4=1'b0;
                   case (funct3)
                   3' b000:
                        begin
                             if (funct7==0) alu0pCode=4'b0000; //add
                             else alu0pCode=4'b0001;//sub
                        end
                     3' b111: a1u0pCode=4' b0010; //and
56
                     3'b110: a1u0pCode=4'b0011; //or
57
                     3'b100: alu0pCode=4'b0100; //xor
58
                     3'b001: alu0pCode=4'b0101; //s11
59 :
                     3'b101:
60 Ö
61 🖨
                         begin
                             if(funct7==0) alu0pCode=4'b0110;//sr1
62 ⊜
                             else alu0pCode=4'b0111; //sra
63 <u>\( \text{\text{o}} \)</u>
64 🖒
                         end
                     endcase
65 🖨
66 ⊝
                 end
                 7' b0010011://i
67 🖨
68 🖨
                 begin
                     regWe=1'b1;
69 :
70
                     pcSourceCode=2'b00;
                     memWe=1'b0;
71
                     bIsImm=1'b1:
72
                     bIs20bImm=1'b0;
73
```

```
73
                      bIs20bImm=1'b0:
 74
                      regDataIsFromMem=1'b0;
                      regDataIsFromPC4=1'b0;
 75
 76 🖨
                      case (funct3)
                          3'b000:a1u0pCode=4'b0000; //addi
 77
                          3' b111:a1u0pCode=4' b0010; //andi
 78
                          3'b110:a1u0pCode=4'b0011; // ori
 79
                          3'b100:a1u0pCode=4'b0100; // xori
 80
                          3'b001:alu0pCode=4'b0101; // s11i
 81
                          3'b101:
 82 <del>=</del>
                             begin
 83 🖨
                                  if(funct7==0) alu0pCode=4'b0110; // sr1i
 84 
\dot{\ominus}
                                  else alu0pCode=4'b0111; //srai
 85 🖨
 86 🖨
                              end
 87 🖨
                      endcase
 88 🖨
                  end
 89 🖨
                  7' b0000011: //1w
 90 🖨
                 begin
 91 :
                        regWe=1'b1;
 92
                        pcSourceCode=2'b00;
                        memWe=1'b0:
 93
 94
                        bIsImm=1'b1;
                        bIs20bImm=1'b0;
 95
 96
                        regDataIsFromMem=1'b1;
                        regDataIsFromPC4=1'b0;
 97
 98
                        alu0pCode=4'b1000; //1w
 99 🖨
                   end
                   7'b0100011://sw
100 🗇
101 🗇
                        begin
                            regWe=1'b0;
102
                            pcSourceCode=2' b00;
103
104
                            memWe=1'b1;
                            bIsImm=1'b1:
105
106
                            bIs20bImm=1'b0;
                            regDataIsFromMem=1'b0;
107
                            regDataIsFromPC4=1'b0;
108
                            alu0pCode=4'b0000; //sw
109
```

```
alu0pCode=4' b0000; //sw
109
                      end
110 🖨
                  7' b0110111://lui
111 Ö
112€
                      begin
113
                          regWe=1'b1;
                           pcSourceCode=2'b00;
114
115
                           memWe=1'b0:
                           bIsImm=1'b1;
116
                           bIs20bImm=1'b1:
117
                           regDataIsFromMem=1'b0;
118
                           regDataIsFromPC4=1'b0;
119
                           alu0pCode=4' b1010; //lui
120
121 🖒
                      end
                  7' b1100011://b
122 🖨
                      begin
123 ⊕
                          regWe=1'b0:
124
125
                           pcSourceCode=condition?2'b01:2'b00;
                           memWe=1'b0:
126
                           bIsImm=1'b0:
127
                            bIsImm=1'b0;
 127
 128
                            bIs20bImm=1'b0:
 129
                            regDataIsFromMem=1'b0;
                            regDataIsFromPC4=1'b0;
 130
                            case (funct3)
 131 ⊖
 132
                                3' b000:alu0pCode=4' b1011; //beq
                                3' b100:a1u0pCode=4' b1100; //b1t
 133
                                3' b110:a1u0pCode=4' b1101; //b1tu
 134
                            endcase
 135 🖨
 136 白
                        end
 137 ⊜
                   7' b1101111:
 138 ⊖
                       begin
                            regWe=1'b1:
 139
 140
                            pcSourceCode=2'b10;
                            memWe=1'b0:
 141
                            bIsImm=1'b1:
 142
                            bIs20bImm=1'b1;
 143
                            regDataIsFromMem=1'b0;
 144
```

```
144
                        regDataIsFromMem=1'b0;
                        regDataIsFromPC4=1'b1;
145
                        alu0pCode=4'b1110; //ja1
146
                    end
147 🖨
148 ⊖
            endcase
149 🖨
        end
         assign pcSourceCode=2'b00;
150 ⊝ //
151 //
         assign regWe=1'b1;
         assign memWe=1'b0;
152 //
         assign bIsImm=1'b1;
153 //
         assign bIs20bImm=1'b0;
154 //
155 : //
         assign regDataIsFromMem=1'b0;
         assign regDataIsFromPC4=1'b0;
156 //
         assign alu0pCode=4'b0011;
157台 //
158
159
160  endmodule
```