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No.

Date. / /

HW 8.

1. (1) F.

(2) F

(3) F.

(4) F

(5) T

2. Final TLB

| VPN | PPN | Valid | Dirty | LRU |
|---|---|---|---|---|
| 0x01 | 0x11 | 1 | 1 | 5 |
| 0x23 | 0x17 | 1 | 1 | 4 |
| 0x10 | 0x13 | 1 | 1 | 6 |
| 0x20 | 0x12 | 1 | 1 | 1 |
| 0x13 | 0x18 | 1 | 1 | 2 |
| 0x11 | 0x14 | 1 | 0 | 3 |
| 0xAC | 0x15 | 1 | 1 | 7 |
| 0x34 | 0x19 | 1 | 1 | 0 |

3. VA: 0xD180B → PA: 0x5180B

(a) Final TLB

| VPN | PPN |
|---|---|
| 0x8 | 0x5 |
| 0x1 | 0x5 |
| | |
| | |

(b) VA: 0x987DA → PA: 0x487DA.

Final TLB

| VPN | PPN |
|---|---|
| 0x8 | 0x1 |
| 0x2 | 0x1 |
| 0x9 | 0x4 |
| | |

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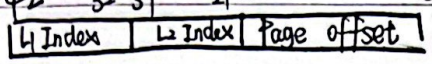
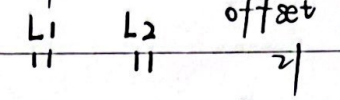



maps to a 2MB page.

(a)




L1 entry num ↓ L2 entry num ↓ L3 entry num ↓

(b) ① $PTO_{4KB} = \frac{2^{11} \times 8 + 2^{11} \times 8 + 2^{9} \times 8 \times 2}{768 \times 2^{12}} = \frac{1}{384} \approx 1.3\%$

∵ L3 has $2^9$ entry. but we need 768 pages

∴ we need two L3 PT

② $PTO_{2MB} = \frac{2^{11} \times 8 + 2^{11} \times 8}{2 \times 2^{21}} = \frac{1}{128} = 7.8125 \times 10^{-3} \approx 0.8\%$

(c) ① $PFO_{4KB} = \frac{0}{768 \times 2^{12}} = 0$

② $PFO_{2MB} = \frac{1MB}{(2 \times 2MB - 1MB)} = \frac{1}{3} = 33.3\%$

(d)

| | Data TLB misses | per miss reference |
|---|---|---|
| 4KB | 768 | 3 |
| 2MB | 2 | 2 |

this is a basic (knowledge) concept. all we need to know is the num of levels in the different mappings.

this is because the memory is continuous and the replacement policy is FIFO

we will must access every page we have allocated

so the number is the num of pages.

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I. (a) ① $2^8 = 256$ Byte : page size

(a)

② PPN 16-8=8 bits

③ Page offset 8 bits (copy from VM address offset)

(b) (b)

condition analysis . size of page is $2^8 = 256$ Byte

But every step add (512) $\Rightarrow 512 \times 4 = 2048$ Byte $= 2^{11}$

physical addr 0x1FFe <map> virtual addr 0x06000

TLB has 16 entries, and we just focus on the steady stage

(1)(1) TLB direct-mapped

① Misses from TLB : 24

② total memory accesses : ~~8~~ $24 \times 4 = 96$ 16

reason because 16 TLB entries and direct-mapped ∴ ① 4 bit index

| | | |
|---|---|---|
| +0 | 0000 | 0000 0000 |
| +512 | 0010 | |
| +1024 | 0100 | |
| +1536 | 0110 | |
| +2048 | 1000 | |

→ same set ∴ replace four times

→ same set when steady.

eg +512, TLB corresponding index is +1536;
+1024, actually is +2048
+1536, actually is +512
+2048, actually is +1024

(2)(2) TLB fully-associative (LRU)

① Misses from TLB : 0

② Total memory accesses : 4 = 4X1

reason because fully-associative, so we don't need to care when it is in the steady stage.

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