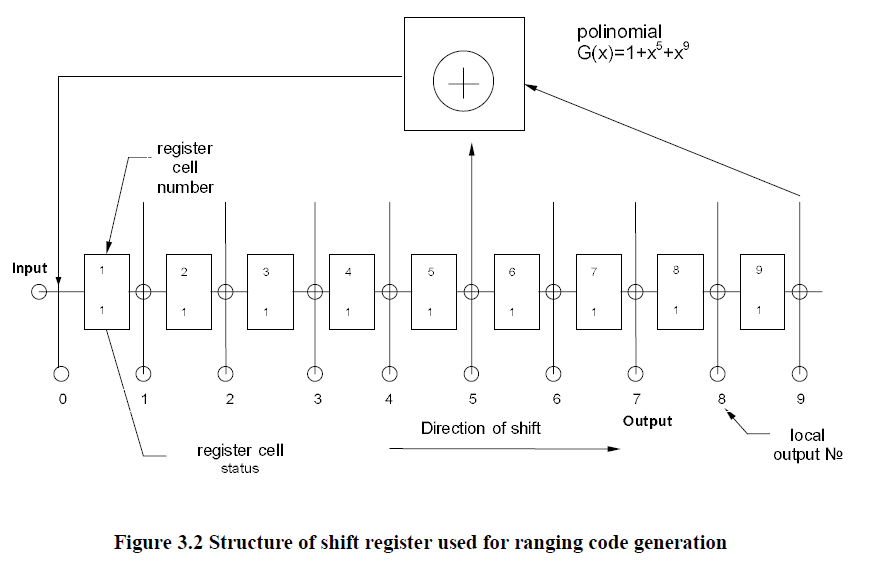
T1

a)



9-stage shift register

Step0: at beginning of each period (1ms), the 9-bit sequence is set to 1

Step1: 5th+9th🡪1st , 7th output 011111111 output: 1

Step2: 5th+9th🡪1st, 7th output 001111111 output: 1

….

Step511: 5th+9th🡪1st, 7th output PRN length: 511

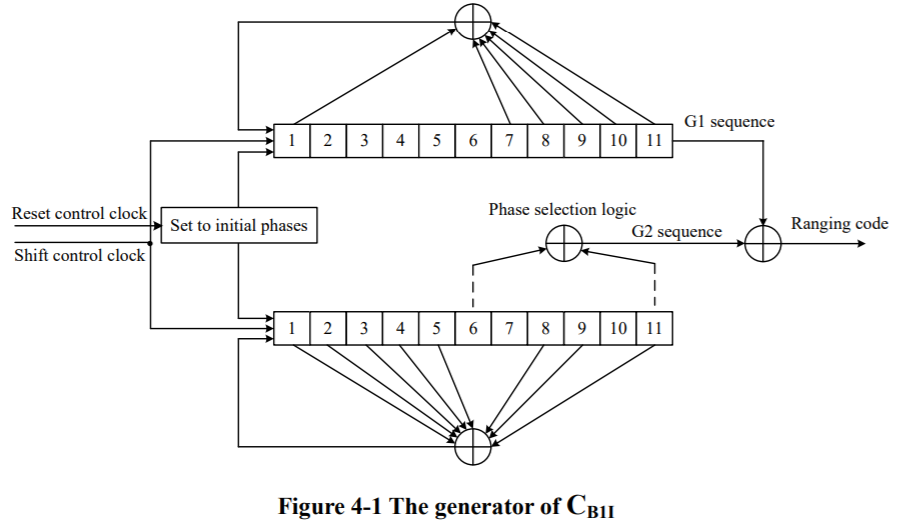
Reset,

Step512: 5th+9th🡪1st , 7th output 011111111 output: 1

b)

T2

a)



G1 calculation🡪output value G1

G2 calculation🡪output value G2

G1+G2🡪output ranging code

b)