CS 250: Computer Architecture

Final Exam Sample Problems

1. (10 questions) True or False? Indicate by entering a 'T' (if true) or 'F' (if false) in the appropriate brackets before each question (grading: +2 for each correct answer, 0 for incorrect or no answer). Examples are:

(1) [ ] Pipelining does not shorten the execution time of a single instruction. Instead, its goal is to shorten the execution time of a sequence of instructions.

(2) [ ] Spatial locality means that if a data item is accessed, the item is likely to be accessed again soon.

(3) [ ] To implement a 64KB cache, the cache miss rate using the *fully associative* design tends to be higher than the cache miss rate using the *direct mapped* design.

(4) [ ] TLB lookup doesn't require main memory access whereas page table lookup does.

(5) [ ] To access data on a hard disk, the amount of time to move the disk head to the right track is called the rotational latency.

2. (5 questions) Multiple choices. For each question, there is one and only one correct answer. Enter your answer in the appropriate brackets after each question (grading: +2 for each correct answer, 0 for incorrect or no answer). Examples are:

(1) To implement an 8-way set associative cache, how many comparators do we need to locate the right cache block?

A. *Two*
B. *Three*
C. *Eight*
D. *The same as the total number of cache blocks*
[ ]

(2) A direct mapped cache has 16 blocks and each block has 32 bytes. In a 32-bit memory address (assuming byte addresses), which bits will be used as tag?

A. Bits [31-9]
B. Bits [31-5]
C. Bits [4 - 0]
D. Bits [8 - 5]
[ ]

(3) Imagine an interactive video game application running in PlayStation 2 (which by the way uses MIPS CPU!), which of the following I/O mechanism(s) is involved in its execution?

A. Polling
B. Interrupt
C. DMA
D. Both B and C
[ ]

3. (10 questions) Short Q&A. Answer each question in at most four sentences. Examples are:

(1) How many pipeline registers are there in the 5-stage MIPS processor? You *don't* have to explain your answer.

(2) Describe a scenario that reflects spatial locality in *programs* and a scenario that reflects spatial locality in *data*.

(3) (2 points) Name one advantage and one disadvantage of the fully associative cache in comparison with the direct-mapped cache.

(4) (2 points) Describe a specific scenario where executing one MIPS instruction will result in *three* main memory accesses.

(5) (2 point) What is the main purpose of the TLB?

4. MIPS pipelined processor Similar to the in-class exercise problem on forwarding (http://www.cs.purdue.edu/homes/dxu/cs250/notes/Forwarding_exercise_solution.pdf), you will be given a MIPS instruction sequence. First, you will be asked to identify all the hazards in the code; Second, you will show the execution of the instruction sequence using the time chart (like the one in the exercise problem); Finally, you will be asked to identify the specific forwarding paths for resolving the hazards in the pipelined processor diagram.

Please re-visit the exercise problem (available on the lecture notes web page). No new sample problem will be given.

5. Direct-mapped cache Consider a 32KB (2^{15} bytes), direct mapped cache with a block size of 16 (2^4) bytes. The memory address (byte address) is 32-bit wide.

(1) Show the partition of the 32-bit address for cache access, i.e. which bits are for block offset, block index, and tag, respectively.

(2) Consider the following memory (byte) addresses. Can their contents be stored in the cache at the *same* time? Briefly explain your answer.

Address 1: 0000 0000 1111 1110 1001 0000 0000 0010
Address 2: 0000 0000 1100 1010 1001 0000 0000 0000

6. Set associative cache Consider a 2-way set associative cache with 8 one-word blocks. The cache is initially empty. The computer system uses *word addresses* instead of byte addresses (i.e. a word is the minimum unit of memory access).

Assume that each word stored in the main memory has the same value as its address. For example, the word at address 2011 has a value of 2011. Consider a sequence of memory references to the following word addresses:

6, 14, 16, 20, 14, 18, 20, 6, 4

(1) Suppose that the cache block replacement policy is LRU. In the table below, show the content of the cache *after* each memory reference. The first two rows have been filled in as an example. "—" indicates empty.

Address	Hit or Miss	Contents of Cache AFTER each Reference							
		Set 0		Set 1		Set 2		Set 3	
		block	block	block	block	block	block	block	block
6	Miss	—	—	—	—	6	—	—	—
14	Miss	—	—	—	—	6	14	—	—
16	Miss	16	—	—	—	6	14	—	—
20									
14									
18									
20									
6									
4									

(2) I will describe a new cache replace policy different from LRU. You will be asked to repeat Question **(1)** but under my new policy.

The new policy will be an interesting one.

7. Virtual memory using paging You will be given the parameters of a paging-based memory system (e.g., page size, virtual address length, physical memory size) as well as some entries in a page table. You will then be asked to translate a virtual address into a physical address (similar to **Quiz 4**). Next I will show you the content of the TLB and give you a number of virtual addresses. You are supposed to decide if each of the virtual addresses will result in a TLB hit or TLB miss. Finally, you will work on a (hopefully fun) problem that combines page table lookup, TLB lookup, and cache lookup.

Please re-visit Quiz 4. No new sample problem will be given.

8. Disk I/O You will be given parameters of a disk (e.g., number of sectors per track, number of bytes per sector, rotational rate, average seek time, and disk controller overhead). You will then be asked to compute the total time to read a certain amount of data from the disk.

Please study the relevant lecture notes. This is supposed to be a very easy problem.