Lecture Summary – Module 1

Switching Algebra and CMOS Logic Gates

Learning Outcome: ***an ability to analyze and design CMOS logic gates***

Learning Objectives:

1-1. convert numbers from one base (radix) to another: 2, 10, 16

1-2. define a binary variable

1-3. identify the theorems and postulates of switching algebra

1-4. describe the principle of duality

1-5. describe how to form a complement function

1-6. prove the equivalence of two Boolean expressions using perfect induction

1-7. describe the function and utility of basic electronic components (resistors, capacitors, diodes, MOSFETs)

1-8. define the switching threshold of a logic gate and identify the voltage ranges typically associated with a "logic high" and a "logic low"

1-9. define assertion level and describe the difference between a positive logic convention and a negative logic convention

1-10. describe the operation of basic logic gates (NOT, NAND, NOR) constructed using N- and P-channel MOSFETs and draw their circuit diagrams

1-11. define "fighting" among gate outputs wired together and describe its consequence

1-12. define logic gate fan-in and describe the basis for its practical limit

1-13. identify key information contained in a logic device data sheet

1-14. calculate the DC noise immunity margin of a logic circuit and describe the consequence of an insufficient margin

1-15. describe the consequences of a "non-ideal" voltage applied to a logic gate input

1-16. describe how unused ("spare") CMOS inputs should be terminated

1-17. describe the relationship between logic gate output voltage swing and current sourcing/sinking capability

1-18. describe the difference between "DC loads" and "CMOS loads"

1-19. calculate V_{OL} and V_{OH} of a logic gate based on the "on" resistance of the active device and the amount of current sourced/sunk by the gate output

1-20. calculate logic gate fan-out and identify a practical lower limit

1-21. calculate the value of current limiting resistor needed for driving an LED

1-22. describe the deleterious effects associated with loading a gate output beyond its rated specifications

1-23. define propagation delay and list the factors that contribute to it

1-24. define transition time and list the factors that contribute to it

1-25. estimate the transition time of a CMOS gate output based on the "on" resistance of the active device and the capacitive load

1-26. describe ways in which load capacitance can be minimized

1-27. identify sources of dynamic power dissipation

1-28. plot power dissipation of CMOS logic circuits as a function of operating frequency

1-29. plot power dissipation of CMOS logic circuits as a function of power supply voltage

1-30. describe the function and utility of decoupling capacitors

1-31. define hysteresis and describe the operation of Schmitt-trigger inputs

1-32. describe the operation and utility of a transmission gate

1-33. define high-impedance state and describe the operation of a tri-state buffer

1-34. define open drain as it applies to a CMOS logic gate output and calculate the value of pull-up resistor needed

1-35. describe how to create "wired logic" functions using open drain logic gates

1-36. calculate the value of pull-up resistor needed for an open drain logic gate

Lecture Summary – Module 1-A

Number Systems

Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 25-34

- **overview**
  - o **d_n – digits of base R number**
  - o **c_n – converted corresponding digits in base 10**
  - o **dealing with *unsigned* numbers only at this point → leading zeroes don't matter**
  - o **table of correspondence**

N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{16}
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1
10	2	2	2	2	2	2	2	2	2
11	10	3	3	3	3	3	3	3	3
100	11	10	4	4	4	4	4	4	4
101	12	11	10	5	5	5	5	5	5
110	20	12	11	10	6	6	6	6	6
111	21	13	12	11	10	7	7	7	7
1000	22	20	13	12	11	10	8	8	8
1001	100	21	14	13	12	11	10	9	9
1010	101	22	20	14	13	12	11	10	A
1011	102	23	21	15	14	13	12	11	B
1100	110	30	22	20	15	14	13	12	C
1101	111	31	23	21	16	15	14	13	D
1110	112	32	24	22	20	16	15	14	E
1111	120	33	30	23	21	17	16	15	F
10000	121	100	31	24	22	20	17	16	10

- **integer conversion: base R to base 10**
  - o **method: iterative multiply and add**
  - o **based on nested expression of a number**

$$(d_3d_2d_1d_0)_R = (N)_{10}$$
$$= c_3 x R^3 + c_2 x R^2 + c_1 x R^1 + c_0 x R^0$$
$$= (((c_3 \times R + c_2) \times R + c_1) \times R + c_0)$$

<u>Example</u>: Convert $(4352)_8$ to base 10

$4 \times 8 + 3 = 35$

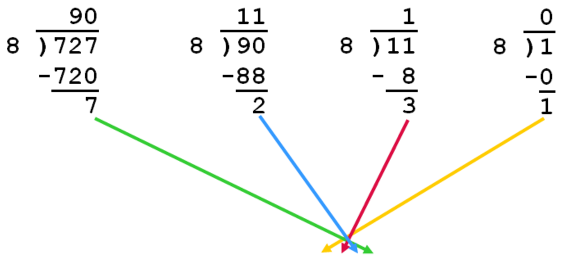
$35 \times 8 + 5 = 285$

$285 \times 8 + 2 = 2282$

Therefore, $(4352)_8 = (2282)_{10}$

- **integer conversion: base 10 to base R**
  - o **method: iterative division**
  - o **remainders become digits of converted number**
  - o **quotient of zero indicates conversion is complete**

<u>Example</u>: Convert $(727)_{10}$ to base 8



```
    90          11          1         0
8 )727      8 )90       8 )11     8 )1
  -720        -88       -  8       -0
     7          2          3        1
```

Therefore, $(727)_{10} = (1327)_8$

- **short cut for conversion among powers of 2 (from base "A" to base "B")**
  - **method: size $\log_2 R$ groupings**
  - **write an n-digit binary number for each base A digit in the original number, where n = $\log_2 A$**
  - **starting at the least significant position, form m-digit groups, where m = $\log_2 B$**

Example: Convert $(136)_8$ to base 2 and base 16

```
   1        3          6
  001      011        110
    0101         1110
      5            E
```

Therefore, $(136)_8 = (\underline{\ 1011110\ })_2 = (\underline{\ 5E\ })_{16}$

Exercise: Convert $(110101)_2$ to bases 8 and 16

```
     6      5
    110    101
      110101
   0011    0101
     3       5
```

Therefore, $(110101)_2 = (\underline{\ 65\ })_8 = (\underline{\ 35\ })_{16}$

Lecture Summary – Module 1-B
Switching Algebra

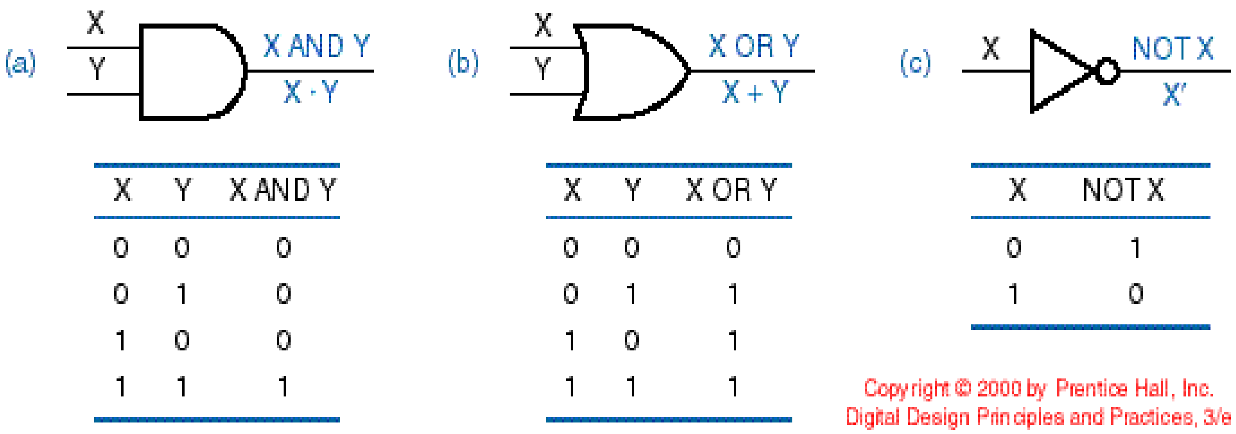
Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 183-199

- **overview**
  - **formal analysis techniques for digital circuits are based on a two-valued algebraic system called *Boolean algebra* (named after George Boole, who invented it in 1854); Claude Shannon (1938) showed how to adapt Boolean algebra to analyze and describe the behavior of circuits built from relays**
  - **definition: the *axioms* (or *postulates*) of a mathematical system are a minimal set of basic definitions that we assume to be true, from which all other information about the system can be derived**
  - **notation: a *prime* (′) will be used to denote an inverter's function (i.e., the *complement* of a logic signal) – note that *prime* is an *algebraic operator*, that X′ is an *expression*, and that Y=X′ is an *equation***
  - **definition: a *binary variable*, X, is a two-valued quantity such that:**
    - **if $X \neq 1$, then $X = 0$**
    - **if $X \neq 0$, then $X = 1$**
  - **definition: the function of a 2-input AND gate is called *logical multiplication* and is symbolized by a *multiplication dot* (·)**
  - **definition: the function of a 2-input OR gate is called *logical addition* and is symbolized algebraically by a *plus sign* (+)**
  - **convention: Multiplication (AND) has *implied precedence* over addition (OR)**
  - **five axioms completely define switching algebra (note that the second axiom in each pair is referred to as the *dual* of the first one)**

➢ **(A1) $X = 0$ if $X \neq 1$**	➢ **(A1^D) $X = 1$ if $X \neq 0$**
➢ **(A2) if $X = 0$, then $X' = 1$**	➢ **(A2^D) if $X = 1$, then $X' = 0$**
➢ **(A3) $0 \cdot 0 = 0$**	➢ **(A3^D) $1 + 1 = 1$**
➢ **(A4) $1 \cdot 1 = 1$**	➢ **(A4^D) $0 + 0 = 0$**
➢ **(A5) $0 \cdot 1 = 1 \cdot 0 = 0$**	➢ **(A5^D) $1 + 0 = 0 + 1 = 1$**

- **duality**
  - **definition: the *dual* of an expression is formed through the simultaneous interchange of the operators "·" and "+" and the elements "0" and "1"**
  - **important principle: if two Boolean expressions can be proven to be equivalent using a given sequence of axioms or theorems, then the *dual expressions* may be proven to be equivalent by simply applying the sequence of *dual* axioms or theorems**

- **basic logic gates (“Boolean’s Big Three”)**
  - **AND – produces a 1 output iff all its inputs are 1**
  - **OR – produces a 1 output if one or more of its inputs are 1**
  - **NOT (inverter) – produces an output value that is the opposite of its input value**



X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

X	NOT X
0	1
1	0

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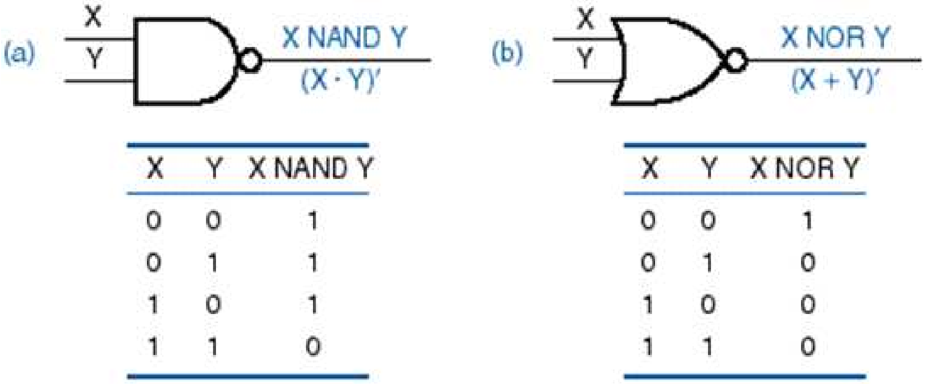
Digital Design Principles and Practices, 3/e

- **other basic gates (more commonly used)**
  - **NAND (“Not AND”) – produces the opposite of an AND gate’s output**
  - **NOR (“Not OR”) – produces the opposite of an OR gate’s output**



X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0

X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0

NAND and NOR gates are easier to make (require fewer transistors) than AND gates and OR gates

- **logical completeness: “anything digital” can be built using solely AND, OR, and NOT gates -or- solely using NAND gates -or- solely using NOR gates**

- **theorems**
  - **<u>definition</u>: switching algebra *theorems* are statements, known always to be true, that allow manipulation of algebraic expressions**
  - **<u>definition</u>: a technique called *perfect induction* can be used to prove switching algebra theorems ("perfect" implies the use of *all possible combinations* of the values of the variables – thus, it is an *exhaustive* type of proof)**
  - **single-variable theorems**
    - **(T1) $X + 0 = X$ (T1^D) $X \cdot 1 = X$ *Identities***
    - **(T2) $X + 1 = 1$ (T2^D) $X \cdot 0 = 0$ *Null elements***
    - **(T3) $X + X = X$ (T3^D) $X \cdot X = X$ *Idempotency***
    - **(T4) $(X')' = X$ *Involution***
    - **(T5) $X + X' = 1$ (T5^D) $X \cdot X' = 0$ *Complements***
  - **two- and three-variable theorems**
    - **(T6) $X + Y = Y + X$ *Commutivity***

      (T6^D) $X \cdot Y = Y \cdot X$
    - **(T7) $(X + Y) + Z = X + (Y + Z)$ *Associativity***

      (T7^D) $(X \cdot Y) \cdot Z = X \cdot (Y \cdot Z)$
    - **(T8) $X \cdot Y + X \cdot Z = X \cdot (Y + Z)$ *Distributivity***

      (T8^D) $(X + Y) \cdot (X + Z) = X + Y \cdot Z$
    - **(T9) $X + X \cdot Y = X$ *Covering***

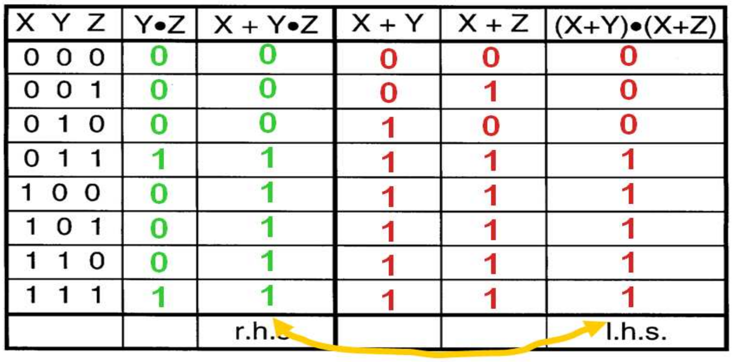
      (T9^D) $X \cdot (X + Y) = X$
    - **(T10) $X \cdot Y + X \cdot Y' = X$ *Combining***

      (T10^D) $(X + Y) \cdot (X + Y') = X$
    - **(T11) $X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z$ *Consensus***

      (T11^D) $(X + Y) \cdot (X' + Z) \cdot (Y + Z) = (X + Y) \cdot (X' + Z)$

<u>Note</u>: In all theorems, it is possible to replace each variable with an arbitrary logic expression

- **<u>example</u>: proof of T8^D using perfect induction**



X Y Z	Y•Z	X + Y•Z	X + Y	X + Z	(X+Y)•(X+Z)
0 0 0	0	0	0	0	0
0 0 1	0	0	0	1	0
0 1 0	0	0	1	0	0
0 1 1	1	1	1	1	1
1 0 0	0	1	1	1	1
1 0 1	0	1	1	1	1
1 1 0	0	1	1	1	1
1 1 1	1	1	1	1	1
		r.h.s.			l.h.s.

- **example: proof of T9 using other theorems**

$$\text{(T9)}\quad X + X \cdot Y = X \cdot 1 + X \cdot Y \qquad (\text{T1}^D)$$
$$= X \cdot (1 + Y) \qquad \text{(T8)}$$
$$= X \cdot 1 \qquad \text{(T2)}$$
$$= X \qquad (\text{T1}^D)$$

- **example: verify the following equivalence relationship**

$$X\cdot Y + Y\cdot Z + X'\cdot Z = X\cdot Y + Y\cdot Z\cdot(X + X') + X'\cdot Z$$
$$= X\cdot Y + X\cdot Y\cdot Z + X'\cdot Y\cdot Z + X'\cdot Z$$
$$= X\cdot Y\cdot(1 + Z) + X'\cdot Z\cdot(Y + 1)$$
$$= X\cdot Y + X'\cdot Z$$

main "tricks":
- multiply by (X + X′)
- factor out common terms

- **n-variable theorems**
  - **(T12)** $X + X + \ldots + X = X$ *Generalized Idempotency*

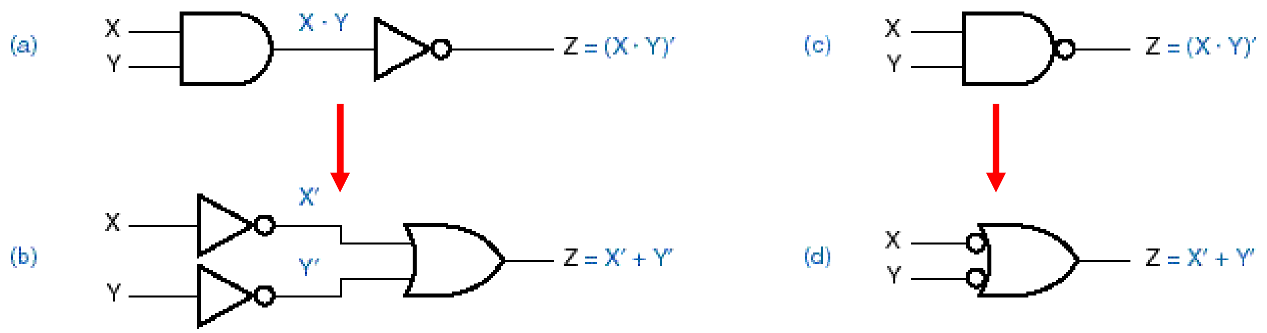
    (T12^D) $X \cdot X \cdot \ldots \cdot X = X$
  - **(T13)** $(X1 \cdot X2 \cdot \ldots \cdot Xn)' = X1' + X2' + \ldots + Xn'$ *DeMorgan's Law*

    (T13^D) $(X1 + X2 + \ldots + Xn)' = X1' \cdot X2' \cdot \ldots \cdot Xn'$
  - **(T14)** $[F(X1,X2, \ldots ,Xn)]' = F^D(X1',X2', \ldots , Xn')$ *Generalized DeMorgan's Law*

- **equivalent circuits based on DeMorgan's law (T13)**

$$\boxed{(X \cdot Y)' = X' + Y'}$$

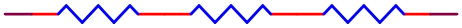
observation: a *logically equivalent circuit* can be formed by taking the *dual* of the operator(s) and *complementing* all the inputs and outputs

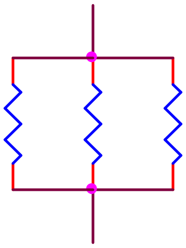


Lecture Summary – Module 1-C
Basic Electronic Components and Concepts

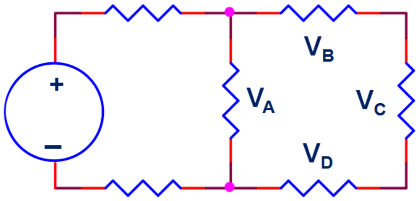
Reference: *DDPP* supplement "Appendix B: Electrical Circuits Review" (link on References page)

- **voltage – difference in electrical potential, expressed in *volts***
- **current – the flow of charge in a conductor between two points having a difference in potential, expressed in *amperes* (amps)**
- **resistor – a device that limits the amount of current flowing through a circuit, measured in *ohms* (Ω)**

  - **resistance is also referred to as *impedance* (inverse of impedance is *admittance*)**
  - **fundamental relationship: the voltage drop (V_R) across a resistor is equal to the product of the current flowing through it (I_R) and the value of the resistance (R)**
  - ***Ohm's Law*** **$V = I \times R$**
  - **resistors in series: $R_T = R_1 + R_2 + R_3$** 
  - **resistors in parallel: $1/R_T = 1/R_1 + 1/R_2 + 1/R_3$**

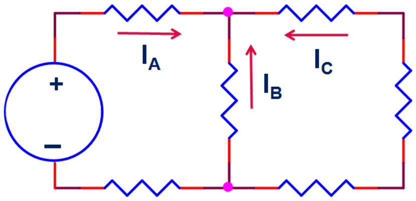


- **Kirchhoff's Voltage Law (KVL) – voltage around a loop sums to zero (based on conservation of energy)**



$V_A + V_B + V_C + V_D = 0$

- **Kirchhoff's Current Law (KCL) – sum of currents at any node is zero (based on conservation of electric charge)**

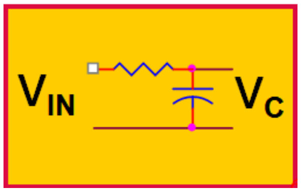


$I_A + I_B + I_C = 0$

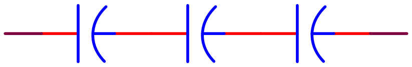
- **power – amount of energy, expressed in *watts*, typically calculated as the product of the *voltage* drop across a device and the *current* flowing through it**
  - **$P = V \times I$**
  - **$P = V^2 / R$**
  - **$P = I^2 \times R$**

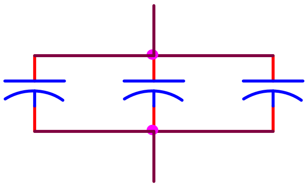
based on Ohm's law substitutions:
$I = V / R$
$V = I \times R$

- **capacitor – a device that stores an electric charge, measured in *farads* (F)**

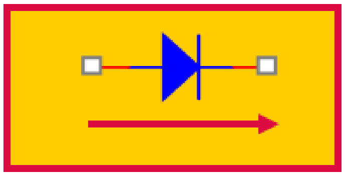


  - **a resistor-capacitor (RC) network charges and discharges exponentially**
  - **the voltage across a capacitor cannot change instantaneously**
  - **the product of R and C is called the *RC time constant***
  - **$V_C = V_{IN} \times (1 - e^{-t/RC})$**
  - **capacitors in series: $1/C_T = 1/C_1 + 1/C_2 + 1/C_3$**
  - **capacitors in parallel: $C_T = C_1 + C_2 + C_3$**

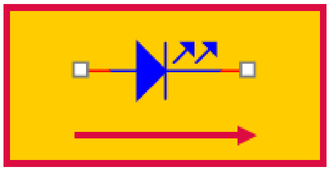




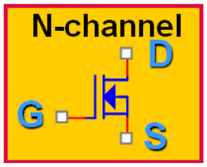
- **diode – a device that restricts the flow of current to a single direction (from its *anode* to its *cathode*)**
  - **a diode through which current is flowing (because the voltage at the anode is greater than at the cathode) is *forward biased***
  - **if current is not flowing through a diode (because the voltage at the cathode is greater than at the anode), the diode is *reverse biased***

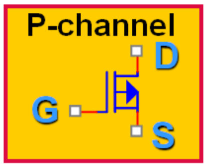


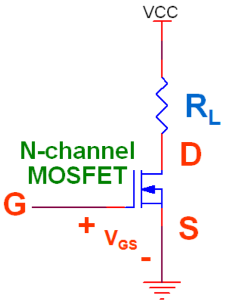
- **light emitting diode (LED) – a diode that emits visible (red/yellow/green/blue/white) or invisible (infrared) light when forwarded biased**
  - **the brightness of an LED is proportional to the amount of current flowing through it (called the *forward current*)**
  - **a *resistor* is placed in series with an LED to limit the amount of current flowing through it**
  - **the voltage drop across an LED when it is forward biased is called the *forward voltage***



- **field effect transistor (FET) – a 3-terminal device (G-gate, S-source, D-drain) that provides a voltage-controlled *impedance***
  - **N-channel: *high* potential on G (gate) relative to S (source) causes transistor to turn on (low impedance between S and D terminals)**
  - **P-channel: *low* potential on G (gate) relative to S (source) causes transistor to turn on**
  - **can be used as a voltage-controlled switch**







Voltage-controlled resistance:

increase V_{GS} → decrease R_{DS}

Note: normally, $V_{GS} \geq 0$

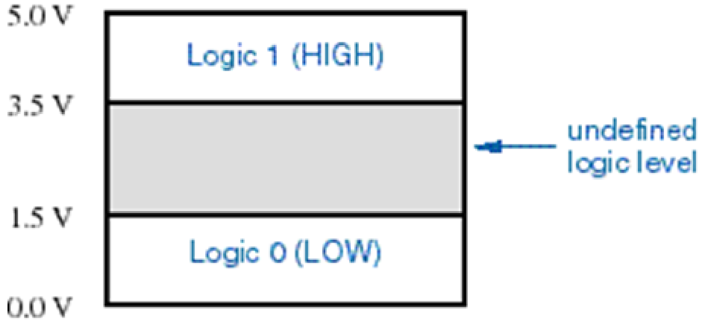
As R_{DS} decreases, power delivered to load (R_L) increases

Lecture Summary – Module 1-D

Logic Signals and CMOS Logic Circuits

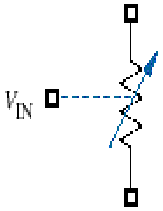
Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 79-96, 141-148

- **overview**
  - **a logic value, 0 or 1, is often referred to as a *binary digit* or *bit***
  - **"LOW" and "HIGH" are often used in place of "0" and "1" to refer to *logic signals***
    - **LOW - a signal in the range of "lower" voltages (e.g., 0 - 1.5 volts for 5V CMOS logic), which is interpreted as a logic 0**
    - **HIGH - a signal in the range of "higher" voltages (e.g., 3.5 - 5.0 volts for 5V CMOS logic), which is interpreted as a logic 1**
  - **the *assignment* of 0 and 1 to LOW and HIGH, respectively, is referred to as a *positive logic convention* (or simply "positive logic")**
    - **a positive logic signal that is *asserted* is in the HIGH state, and is therefore referred to as an "active high" signal**
    - **a positive logic signal that is *negated* is in the LOW state**
  - **the *opposite assignment* (1 to LOW and 0 to HIGH) is referred to as a *negative logic convention* (or "negative logic")**
    - **a negative logic signal that is *asserted* is in the LOW state, and is therefore referred to as an "active low" signal**
    - **a negative logic signal that is *negated* is in the HIGH state**
- **logic families**
  - **complementary metal oxide semiconductor (CMOS) logic is both the most capable and the easiest to understand commercial digital logic technology, and accounts for the vast majority of the worldwide integrated circuit (IC) market**
  - **5-volt CMOS logic levels (other operating voltage ranges proportioned accordingly)**

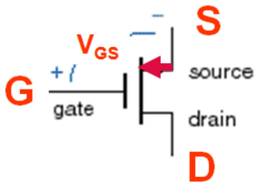


indeterminate region - ***undefined input yields undefined output***

- **MOS field effect transistor (MOSFET)**
  - **modeled as a 3-terminal device that acts like a voltage-controlled resistance**

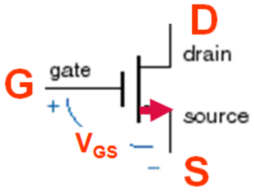


  - **in digital logic applications, MOSFETs are operated so that their resistance is either *very high* (transistor is "off") or *very low* (transistor is "on")**
  - **P-channel MOS (PMOS)**



Voltage-controlled resistance:
decrease V_{GS} → decrease R_{DS}
(current flows from S terminal to D)
Note: normally, $V_{GS} \le 0$

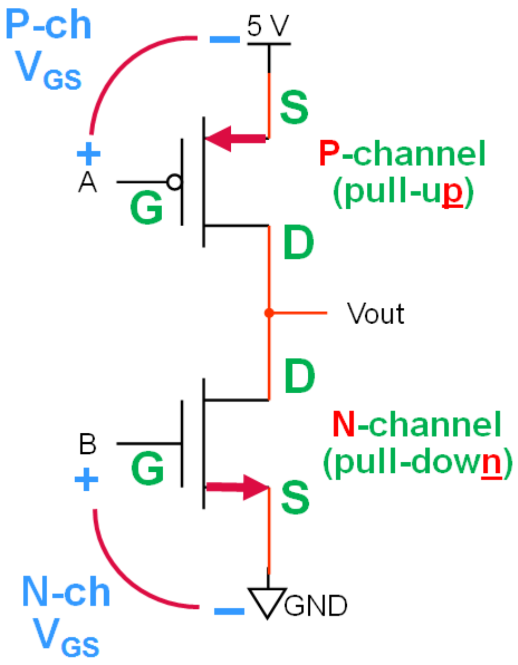
  - **N-channel MOS (NMOS)**



Voltage-controlled resistance:
increase V_{GS} → decrease R_{DS}
(current flows from D terminal to S)
Note: normally, $V_{GS} \ge 0$

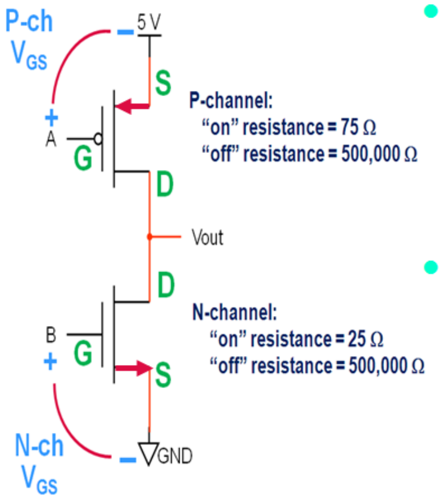
current only flows through the resistance *one way*

  - **basic CMOS logic circuit**



- The S terminal of the P-ch MOSFET is connected to 5 V
- The S terminal of the N-ch MOSFET is connected to GND
- The D terminals of both MOSFETs are connected to the output (Vout)
- The direction of current flow in the P-ch device is from the S terminal to the D terminal ("sources" current)
- The direction of current flow in the N-ch device is from the D terminal to the S terminal ("sinks" current)
- A high voltage on the G terminal of the N-ch MOSFET (relative to GND) turns it on
- A low voltage on the G terminal of the P-ch MOSFET (relative to 5 V) turns it on

- **example: inverter operation (very low power dissipation, very low voltage drop across "on" device under "no load" conditions)**



- **Calculate V_{out} for the case A=B=0V**

  P-ch device is "on" (R_{DS} = 75 Ω)

  N-ch device is "off" (R_{DS} = 500,000 Ω)

  V_{out} = 5 x (500,000 / 500,075) ≈ 4.999 V

  $P_{dissipation}$ = 5^2 / 500,075 ≈ 0.05 mW

- **Calculate V_{out} for the case A=B=5V**

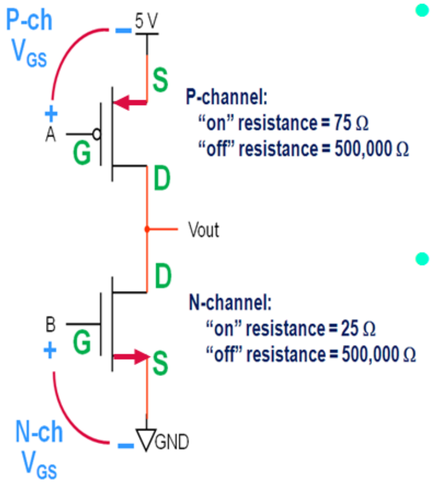
  P-ch device is "off" (R_{DS} = 500,000 Ω)

  N-ch device is "on" (R_{DS} = 25 Ω)

  V_{out} = 5 x (25 / 500,025) ≈ 0.00025 V

  $P_{dissipation}$ = 5^2 / 500,025 ≈ 0.05 mW

- **example: "non-inverter" operation (Q: what would you call each of these cases?)**



- **Calculate V_{out} for the case A=0, B=5 V**

  P-ch device is "on" (R_{DS} = 75 Ω)

  N-ch device is "on" (R_{DS} = 25 Ω)

  V_{out} = 5 x (25 / 100) = 1.25 V

  $P_{dissipation}$ = 5^2 / 100 = 250 mW

- **Calculate V_{out} for the case A=5V, B=0**

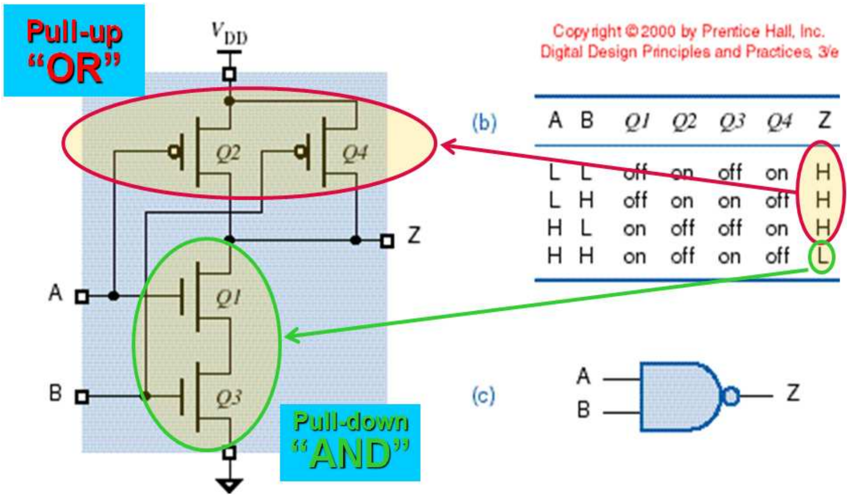
  P-ch device is "off" (R_{DS} = 500,000 Ω)

  N-ch device is "off" (R_{DS} = 500,000 Ω)

  V_{out} = 5 x (500,000 / 1,000,000) = 2.5 V

  $P_{dissipation}$ = 5^2 / 1,000,000 = 0.025 mW

- **basic CMOS NAND gate**



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A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

more input combinations pull output high than low → P-channel pull-ups in *parallel* ("OR"), N-channel pull-downs in *series* ("AND")

- **fighting!**

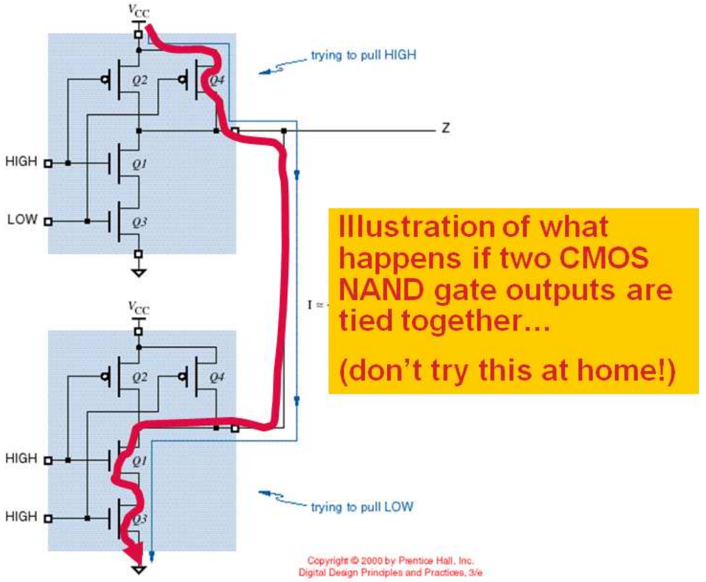

Illustration of what happens if two CMOS NAND gate outputs are tied together…

(don't try this at home!)

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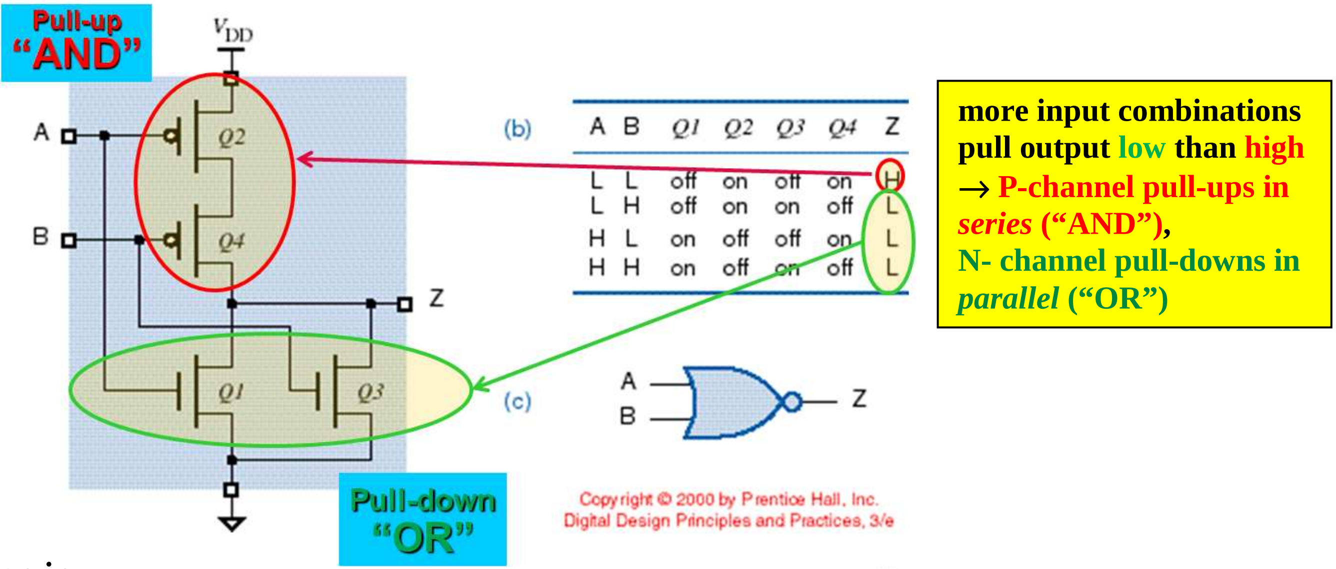
- **basic CMOS NOR gate**



A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

more input combinations pull output low than high → P-channel pull-ups in *series* ("AND"), N- channel pull-downs in *parallel* ("OR")

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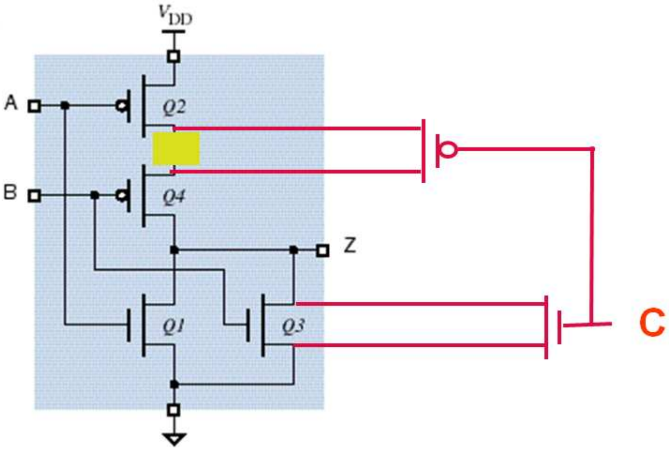
- **fan-in**
  - **definition: the number of inputs a gate can have in a particular logic family is called the logic family's *fan-in***
  - **CMOS gates with more than two inputs can be obtained by extending the "series-parallel" circuit designs (e.g., for NAND and NOR gates) illustrated previously**
  - **in practice, the additive "on" resistance of series transistors limits the fan-in of CMOS gates to a relatively small number**
  - **example: expand fan-in of 2-input NOR gate to 3 inputs**



method:

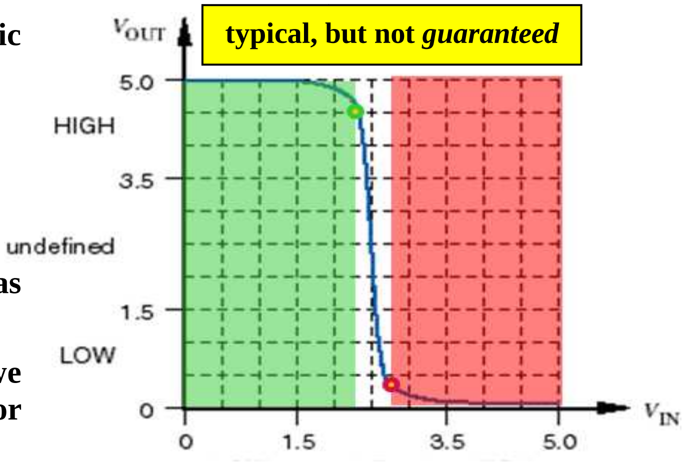
- **expand serial chain**
- **expand parallel train**

Lecture Summary – Module 1-E

Logic Levels and Noise Margins

Reference: *Digital Design Principles and Practices* (4^{th} Ed.), pp. 96-103

- **overview**
  - **<u>objective:</u> to be able to design *real* circuits using CMOS or other logic families design margins**
    - **need to ensure that the "*digital abstraction*" is valid for a given circuit**
    - **need to provide adequate engineering *design margins* to ensure that a circuit will work properly under a variety of conditions**
    - **need to be able to read and understand data sheets and specifications, in order to create reliable and robust real-world circuits and systems**
  - **noise**
    - **the main reason for providing engineering design margins is to ensure proper operation in the presence of *noise***
    - **examples of noise sources:**
      - **cosmic rays**
      - **magnetic fields generated by machinery**
      - **power supply disturbances**
      - **the "*switching action*" of the logic circuits themselves**
  - **CMOS inverter input/output transfer characteristic**
  - **factors that cause the transfer characteristic to vary**
    - **power supply voltage**
    - **temperature**
    - **output loading**
    - **conditions under which a device was fabricated**
  - **sound engineering practice dictates that we use more "*conservative*" specifications for LOW and HIGH**



typical, but not *guaranteed*

- **input/output voltage definitions**
  - **V_{OHmin} - the minimum output voltage in the HIGH state**
  - **V_{IHmin} - the minimum input voltage guaranteed to be recognized as a HIGH**
  - **V_{ILmax} - the maximum input voltage guaranteed to be recognized as a LOW**
  - **V_{OLmax} - the maximum output voltage in the LOW state**

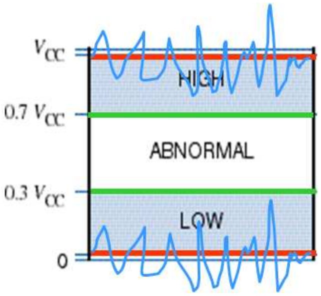
- **DC noise margin**
  - **definition: a measure of how much noise it takes to *corrupt* a worst-case output voltage into a value that may not be recognized properly by an input**
  - **calculation of DC noise margin (or the "noise immunity margin")**
  - **HC family (5-volt) CMOS data sheet**

– V_{OHmin} Vcc – 0.1v

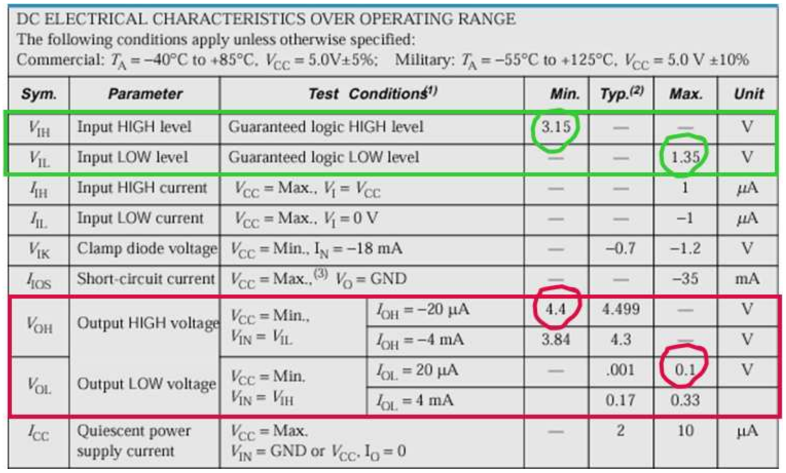
– V_{IHmin} 70% of Vcc

– V_{ILmax} 30% of Vcc

– V_{OLmax} GND + 0.1v



DCNM = min (V_{OHmin} – V_{IHmin}, V_{ILmax} – V_{OLmax})



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE
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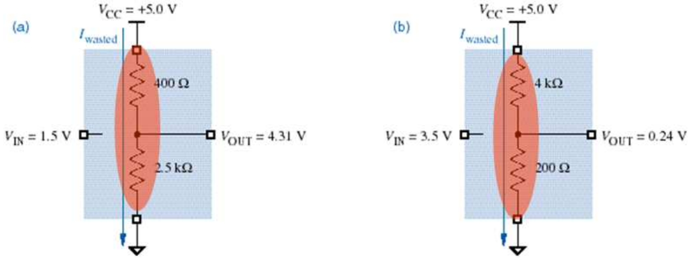
Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	µA
I_{IL}	Input LOW current	V_{CC} = Max., V_I = 0 V		—	—	–1	µA
V_{IK}	Clamp diode voltage	V_{CC} = Min., I_N = –18 mA		—	–0.7	–1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	–35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	I_{OH} = –20 µA	4.4	4.499	—	V
			I_{OH} = –4 mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	I_{OL} = 20 µA	—	.001	0.1	V
			I_{OL} = 4 mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, I_O = 0		—	2	10	µA

For HC family (5-volt) CMOS:

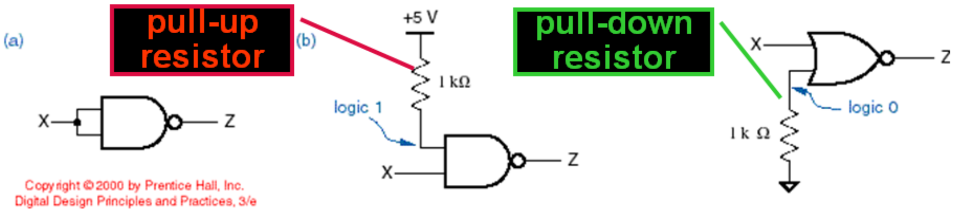
DCNM = min (4.4 – 3.15, 1.35 – 0.1) = 1.25 v

Q: Is a DCNM of 1.25 V "good" or "bad"?

- **other gate input considerations**
  - **if the inputs to a CMOS circuit are not close to the Vcc / GND rails, the "on" transistor may not be *fully on* and the "off" transistor may not be *fully off* – causing power dissipation of the device to *increase***



  - **unused ("spare") CMOS inputs should *never* be left unconnected ("floating") – a small amount of circuit noise can temporarily make a floating input look HIGH (solution: tie unused inputs high or low using a pull-up or pull-down resistor, respectively)**



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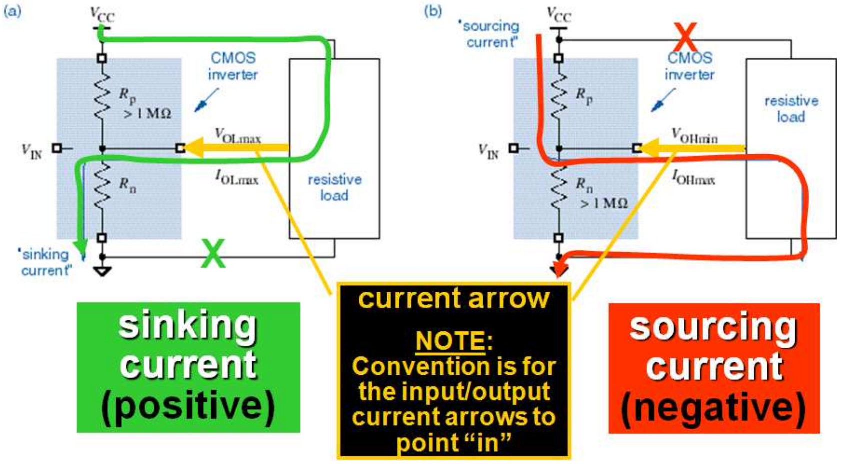
  - **CMOS device inputs are subject to damage from electrostatic discharge (ESD) – touch a source of earth ground before handling static sensitive devices or circuit boards that contain them**

Lecture Summary – Module 1-F
Current Sourcing and Sinking

Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 103-114

- **sourcing and sinking current**
  - **CMOS gate inputs have a very high impedance and consume *very little current* (about 1 microamp) from the circuits that drive them**
    - **I_{IL} - maximum current that flows into the input in the LOW state**
    - **I_{IH} - maximum current that flows into the input in the HIGH state**
  - **IC manufacturers specify a maximum load for the output in each state (HIGH or LOW) and guarantee a worst-case output voltage for that load**
    - **I_{OL} - maximum current that the output can "sink" in the LOW state while still maintaining an output voltage *no greater than* V_{OLmax}**
    - **I_{OH} - maximum current that the output can "source" in the HIGH state while still maintaining an output voltage *no less than* V_{OHmin}**
  - **sourcing/sinking sign convention**



sinking current (positive)

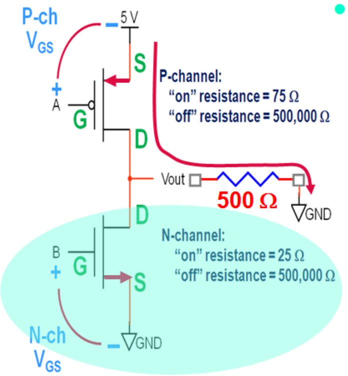
current arrow

NOTE: Convention is for the input/output current arrows to point "in"

sourcing current (negative)

- **"CMOS loads" vs. "DC loads"**
  - **often times gate outputs need to drive devices that require a non-trivial amount of current to operate – called a *resistive* load or *DC* load**
  - **when driving a resistive load, the output of a CMOS circuit is not nearly as *ideal* as described previously (the output voltage swing may significantly degrade)**
  - **in either output state, the CMOS output transistor that is "on" has a non-zero resistance, and a load connected to its output terminal will cause a voltage drop across this resistance**
  - **consequently, most CMOS devices have two sets of loading specifications:**
    - **"CMOS loads" – device output connected to other CMOS inputs, which require *very little current* to recognize a "high" input or "low" input**
    - **"DC loads" – device output connected to resistive loads (devices that consume significant current, typically several milliamps)**

- **example: inverter - current sourcing (DC load)**



- **Calculate V_{OH} and I_{OH} for A=B=0V**

Current SOURCING configuration

DC Load is 500 Ω resistor between V_{out} and GND

P-ch device is "on" (R_{DS} = 75 Ω)

N-ch device is "off" (R_{DS} = 500,000 Ω)

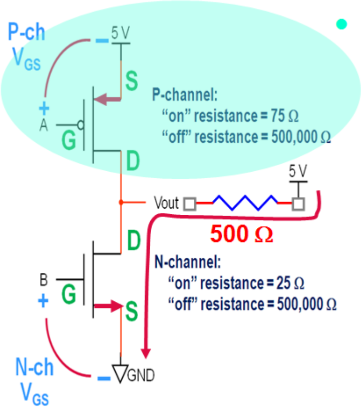
Load impedance is 500,000 Ω in parallel with 500 Ω ≈ 500 Ω

V_{OH} ≈ 5 x (500 / 575) ≈ 4.35 V

I_{OH} ≈ 5 / (75 + 500) ≈ 0.0087 A (8.7 mA)

In the current SOURCING configuration, the inverter output is active high ("asserted high"); the N-channel pull-down virtually "disappears"

- **example: inverter – current sinking (DC load)**



- **Calculate V_{OL} and I_{OL} for A=B=5V**

Current SINKING configuration

DC Load is 500 Ω resistor between 5 V supply and V_{out}

P-ch device is "off" (R_{DS} = 500,000 Ω)

N-ch device is "on" (R_{DS} = 25 Ω)

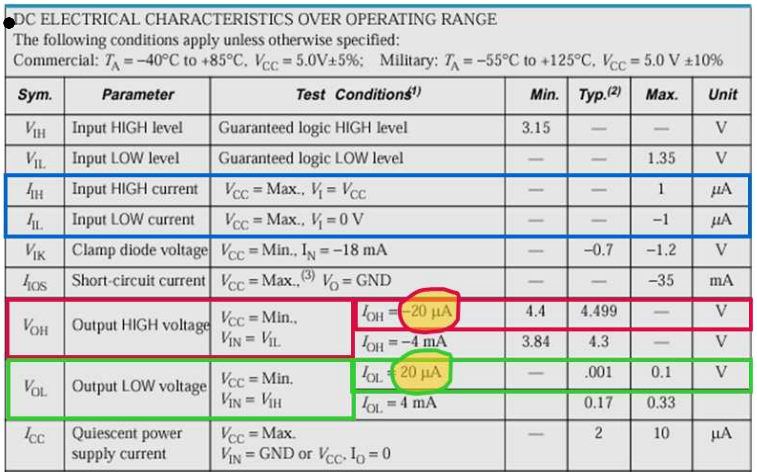
Load impedance is 500,000 Ω in parallel with 500 Ω ≈ 500 Ω

V_{OL} ≈ 5 x (25 / 525) ≈ 0.24 V

I_{OL} ≈ 5 / (25 + 500) ≈ 0.0095 A (9.5 mA)

In the current SINKING configuration, the inverter output is active low ("asserted low"); the P-channel pull-up virtually "disappears"

- **fan-out**
  - **<u>definition</u>: the number of gate inputs that a gate output can drive *without exceeding* its worst-case loading specifications**
  - **depends on characteristics of both the output device and the inputs being driven**
  - **must be examined for both the "sourcing" and "sinking" cases**
  - **limitations due to capacitive loading (impact on rise/fall times may be more of a limiting factor than fan-out or DCNM)**
  - **"practical" fan-out is the *minimum* of the HIGH- and LOW-state fan-outs**



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Sym.	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	µA
I_{IL}	Input LOW current	V_{CC} = Max., V_I = 0 V		—	—	–1	µA
V_{IK}	Clamp diode voltage	V_{CC} = Min., I_N = –18 mA		—	–0.7	–1.2	V
I_{OS}	Short-circuit current	V_{CC} = Max.,(3) V_O = GND		—	—	–35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	I_{OH} = –20 µA	4.4	4.499	—	V
			I_{OH} = –4 mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	I_{OL} = 20 µA	—	.001	0.1	V
			I_{OL} = 4 mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, I_O = 0		—	2	10	µA

Fan-out = min (I_{OHmax} / I_{IH}, I_{OLmax} / I_{IL})

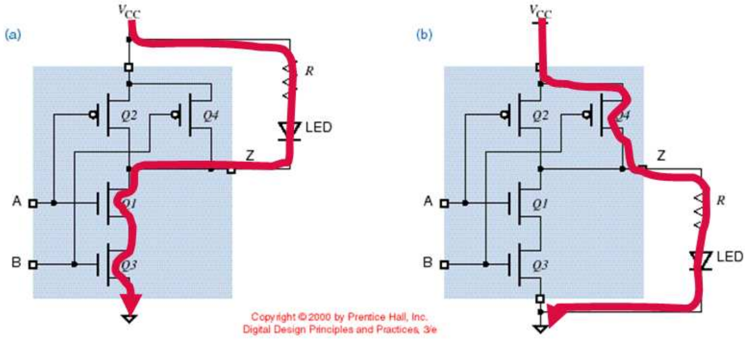
For HC family (5-volt) CMOS:

Fan-out = min (I_{OHmax} / I_{IH}, I_{OLmax} / I_{IL})
= min (0.02 mA / 0.001 mA,
-0.02 mA / -0.001 mA)
= 20

Q: Is a fan-out of 20 "good" or "bad"?

DC fan-out is considerably greater in this case if the output voltage swing is degraded … *but* DCNM is lower and signal transitions times are longer, causing speed degradation

- **driving LEDs**
  - **LEDS represent "DC loads" and can be interfaced to a CMOS gate output either by sinking current (LOW output) or sourcing current (HIGH output)**



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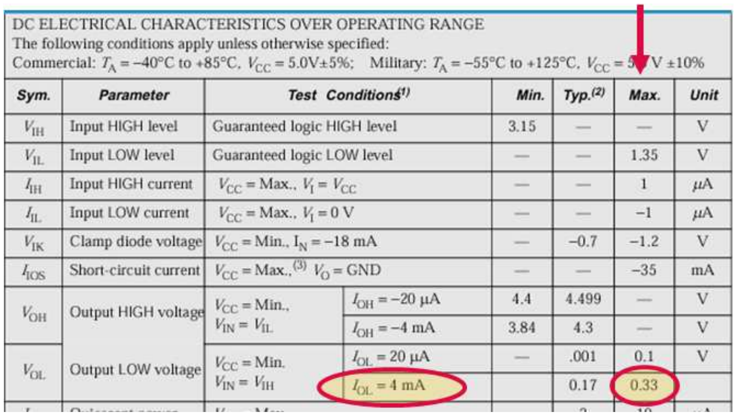
Q: Which method is generally preferred (and *why*)?

- **example: "worst case" souring and sinking analysis for driving an LED**
  - **sinking current**



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V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	−0.7	−1.2	V
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			$I_{OH} = -4$ mA	3.84	4.3	—	V
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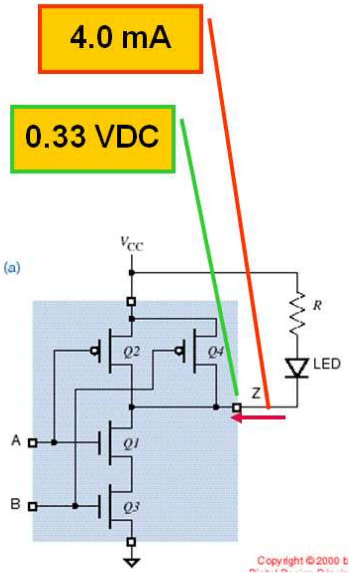
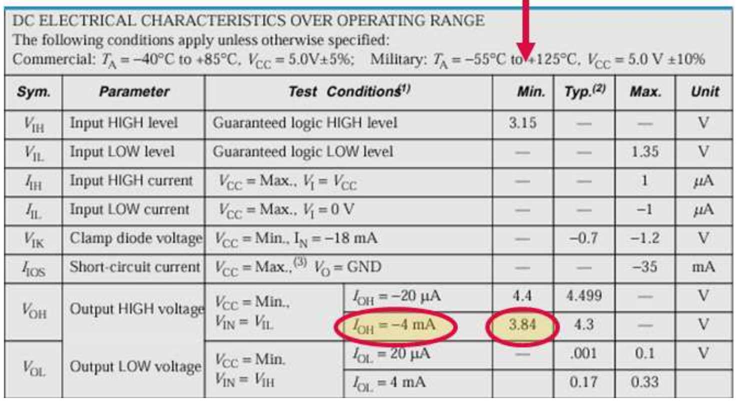
			$I_{OL} = 4$ mA		0.17	0.33	



$V_R = 5.0 - V_{LED} - V_{OL} = 5.0 - 1.9 - 0.33 = 2.77$ V
use "Max" value indicated for V_{OL} of 0.33 V
$R = V_R/I_{OL} = 2.77/0.004 = 693\ \Omega$
$P_R = R \times I_{OL}^2 = 693 \times (0.004)^2 = 11.1$ milliwatts

Can also calculate power dissipation of resistor using $V_R \times I_{OL}$ or $(V_R^2)/R$

  - **sourcing current**



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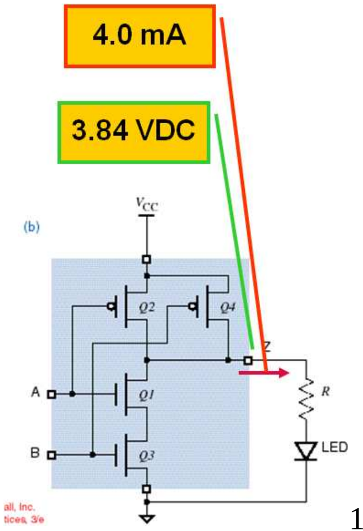
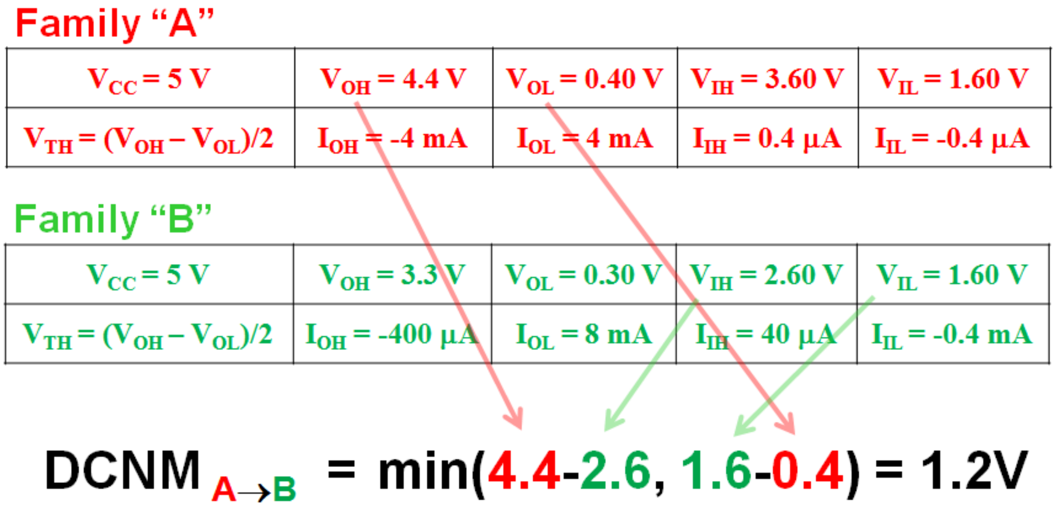


$V_R = V_{OH} - V_{LED} = 3.84 - 1.9 = 1.94$ V
use "Min" value indicated for V_{OH} of 3.84 V
$R = V_R/I_{OH} = 1.94/0.004 = 485\ \Omega$
$P_R = R \times I_{OH}^2 = 485 \times (0.004)^2 = 7.8$ milliwatts

- **effects of excessive loading**
  - **in the LOW state, the output voltage (V_{OL}) may increase beyond V_{OLmax}**
  - **in the HIGH state, the output voltage (V_OH) may fall below V_{OHmin}**
  - **output rise and fall times may increase beyond their specifications (details in next section)**
  - **the operating temperature of the device may increase, thereby *reducing* the *reliability* of the device and eventually causing device *failure***

- **<u>example</u>: a tale of two logic families**

  - **DCNM, A→B**



Family "A"

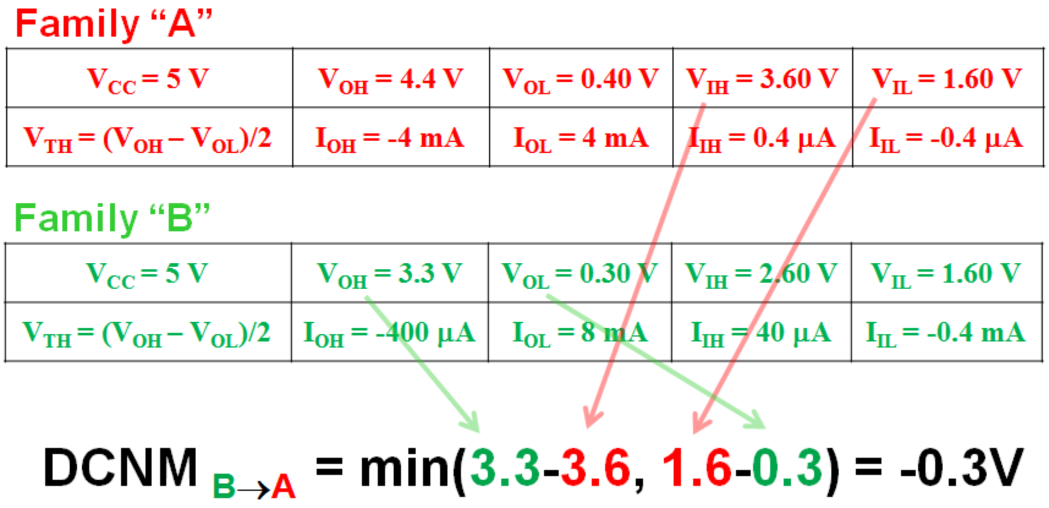
V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 µA	I_{IL} = -0.4 µA

Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 µA	I_{OL} = 8 mA	I_{IH} = 40 µA	I_{IL} = -0.4 mA

$$\text{DCNM}_{A\to B} = \min(4.4-2.6,\ 1.6-0.4) = 1.2\text{V}$$

  - **DCNM, B→A**



Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 µA	I_{IL} = -0.4 µA

Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 µA	I_{OL} = 8 mA	I_{IH} = 40 µA	I_{IL} = -0.4 mA

$$\text{DCNM}_{B\to A} = \min(3.3-3.6,\ 1.6-0.3) = -0.3\text{V}$$

  - **DCNM thought questions**
    - **What is the consequence of a <u>negative</u> DCNM?**
    - **What is the <u>minimum</u> DCNM required?**

- **<u>example</u>: a tale of two logic families, continued…**

  - **Fan-out, A→B**

Family “A”

$V_{CC} = 5$ V	$V_{OH} = 4.4$ V	$V_{OL} = 0.40$ V	$V_{IH} = 3.60$ V	$V_{IL} = 1.60$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -4$ mA	$I_{OL} = 4$ mA	$I_{IH} = 0.4$ μA	$I_{IL} = -0.4$ μA

Family “B”

$V_{CC} = 5$ V	$V_{OH} = 3.3$ V	$V_{OL} = 0.30$ V	$V_{IH} = 2.60$ V	$V_{IL} = 1.60$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -400$ μA	$I_{OL} = 8$ mA	$I_{IH} = 40$ μA	$I_{IL} = -0.4$ mA

$$\text{Fanout}_{A\to B} = \min(4 / 0.04,\ 4 / 0.4) = 10$$

CAUTION!! Current arrows for I_O and I_I point in *<u>opposite directions</u>*

  - **Fan-out, B→A**

Family “A”

$V_{CC} = 5$ V	$V_{OH} = 4.4$ V	$V_{OL} = 0.40$ V	$V_{IH} = 3.60$ V	$V_{IL} = 1.60$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -4$ mA	$I_{OL} = 4$ mA	$I_{IH} = 0.4$ μA	$I_{IL} = -0.4$ μA

Family “B”

$V_{CC} = 5$ V	$V_{OH} = 3.3$ V	$V_{OL} = 0.30$ V	$V_{IH} = 2.60$ V	$V_{IL} = 1.60$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -400$ μA	$I_{OL} = 8$ mA	$I_{IH} = 40$ μA	$I_{IL} = -0.4$ mA

$$\text{Fanout}_{B\to A} = \min(400/0.4,\ 8/0.0004) = 1000$$

CAUTION!! Current arrows for I_O and I_I point in *<u>opposite directions</u>*

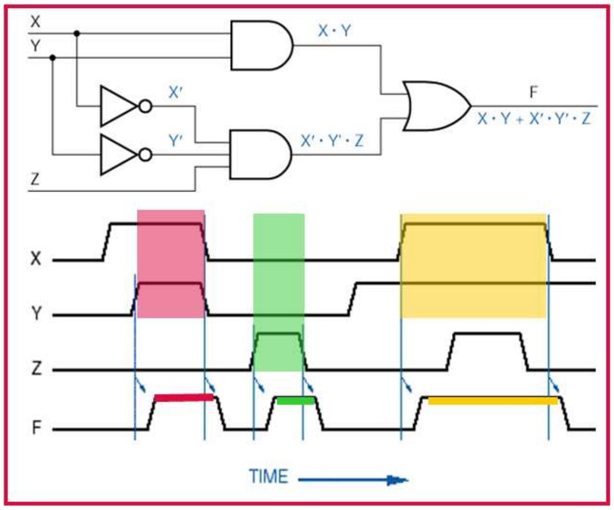
  - **Fan-out thought questions**
    - **Is it possible for the fan-out to be <u>negative</u>?**
    - **What is the <u>minimum</u> fan-out required?**

Lecture Summary – Module 1-G

Propagation Delay and Transition Time

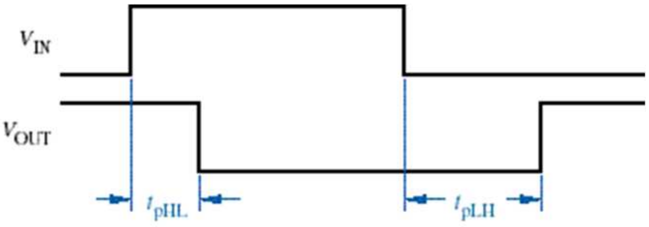
Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 114-128

- **overview**
  - **the *speed* and *power dissipation* of a CMOS device depend on the dynamic ("AC") characteristics of the device and its load**
  - **logic designers must carefully examine the effects of output loading and redesign where the loading is too high**
  - **speed (performance) depends on two characteristics:**
    - ***propagation delay***
    - ***transition time***
  - **logic gates require a certain amount of "think time" to produce a new output in response to changing inputs – referred to as the *propagation delay* of the gate**
  - **logic gate outputs can not change from a low voltage to a high voltage (or vice-versa) "instantaneously" – referred to as the *transition time* of the gate**
  - **a *timing diagram* can be used to show how a logic circuit responds to time-varying input signals**

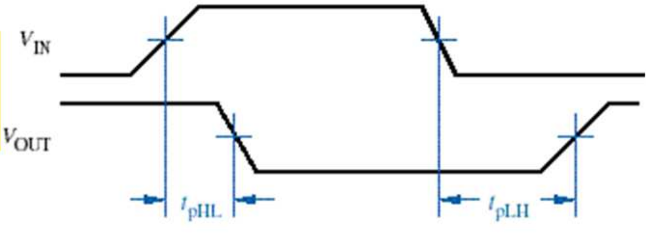


- **propagation delay**
  - **<u>definition</u>: the electrical path from a particular input signal of a logic element to its output signal is called a *signal path***
  - **<u>definition</u>: the amount of time it takes for a change in an input signal to cause a corresponding change in a gate's output signal is called the *propagation delay* (t_p)**
  - **the propagation delay for an output signal going from LOW-to-HIGH (t_{PLH}) may be different than the propagation delay of that signal going from HIGH-to-LOW (t_{PHL})**

Ignoring rise and fall times

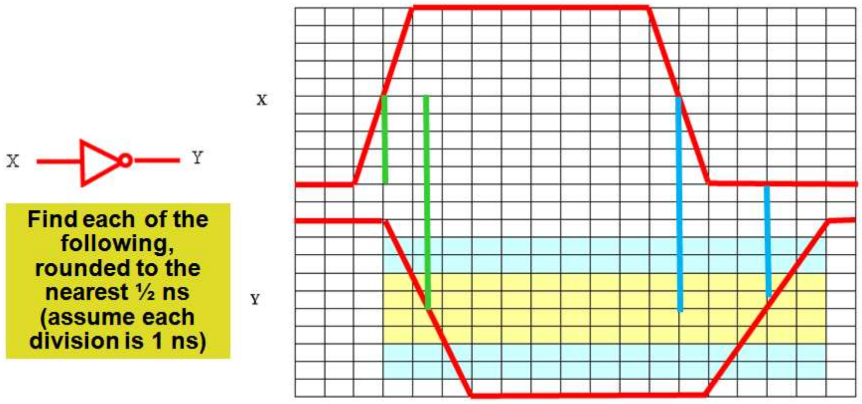


Measured at midpoints of transitions



The "name" used for the propagation delay (t_{PLH} vs. t_{PHL}) is based on what the gate <u>output</u> is doing

- **propagation delay, continued…**
  - **several factors lead to *non-zero* propagation delays in CMOS circuits:**
    - **the rate at which transistors change state is influenced both by semiconductor physics and the circuit environment (input signal transition time, input capacitance, and output loading)**
    - **multistage devices (e.g., non-inverting gates) may require several internal transistors to change state before the output can change state**
  - **<u>example</u>: propagation delay measurement**



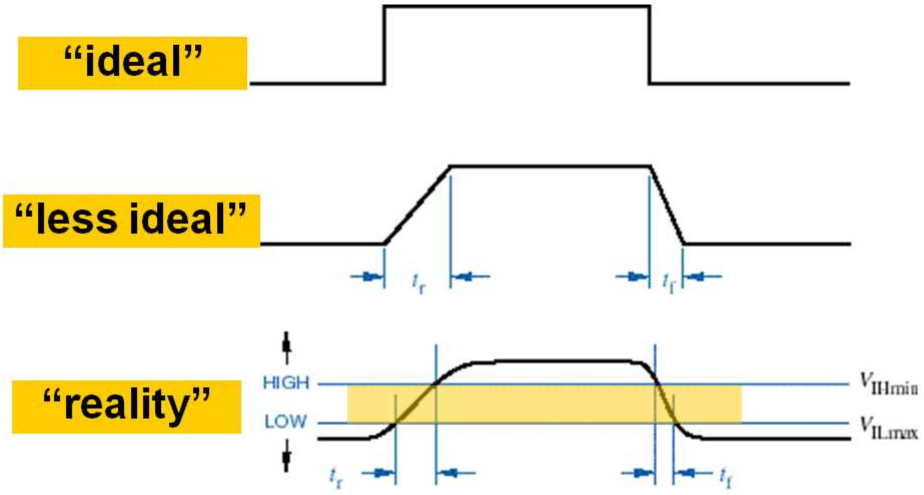
Find each of the following, rounded to the nearest ½ ns (assume each division is 1 ns)

The "name" used for the propagation delay (t_{PLH} vs. t_{PHL}) is based on what the gate <u>output</u> is doing

Rise propagation delay (t_{PLH}) = 3 ns

Fall propagation delay (t_{PHL}) = 1.5 ns

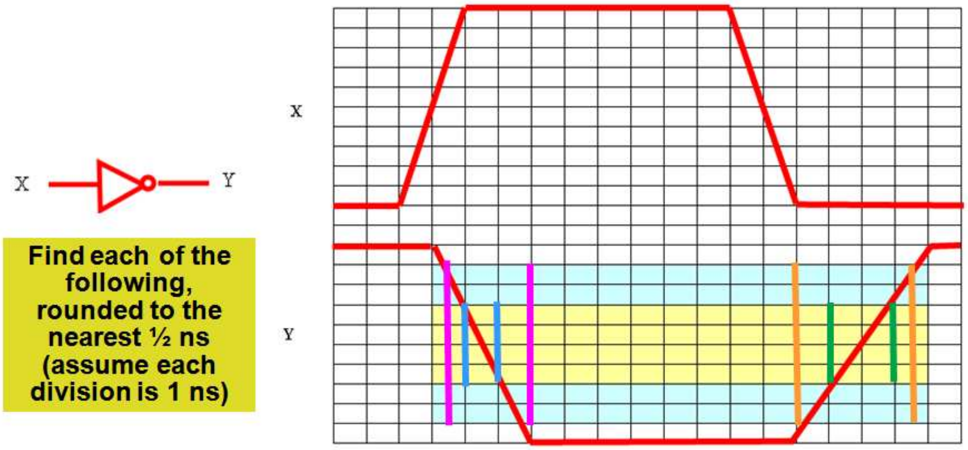
- **transition time**
  - **<u>definition</u>: the amount of time that the output of a logic circuit takes to change from one state to another**
    - **rise time (t_r or t_{TLH}): the time an output signal takes to transition from low-to-high**
    - **fall time (t_f or t_{THL}): the time an output signal takes to transition from high-to-low**
  - **gate outputs can *not* change state *instantaneously* (i.e., with a transition time of zero) because they need to *charge the stray capacitance* of the wires and other components they drive**



The "name" used for the transition time (t_{TLH} vs. t_{THL}) is based on what the gate <u>output</u> is doing

The rise and fall times are typically *not* equal in value

- **transition time, continued…**
  - **to avoid difficulties in defining the endpoints, transition times are normally measured one of two different ways:**
    - **at the boundaries of the valid logic levels (i.e., V_{IHmin} and V_{ILmax})**
    - **at the 10% and 90% points of the output waveform**
  - **using the "valid logic level" convention (above), the rise and fall times indicate how long it takes for an output signal to pass through the (undefined) *indeterminate region* between LOW and HIGH**
  - **<u>example</u>: transition time measurement / comparison of endpoints**



Find each of the following, rounded to the nearest ½ ns (assume each division is 1 ns)

The "name" used for the transition time (t_{TLH} vs. t_{THL}) is based on what the gate <u>output</u> is doing

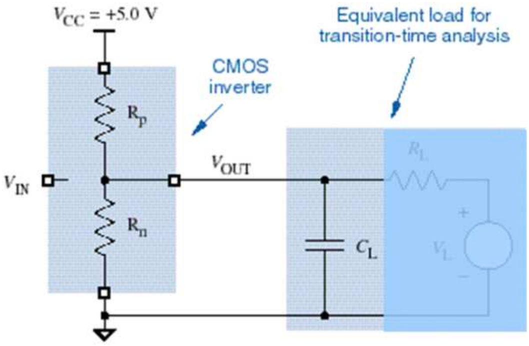
Rise time (t_{TLH}) based on Wakerly's (30%-70%) definition = 2 ns

Rise time (t_{TLH}) based on standard 10%-90% definition = 3.5 ns

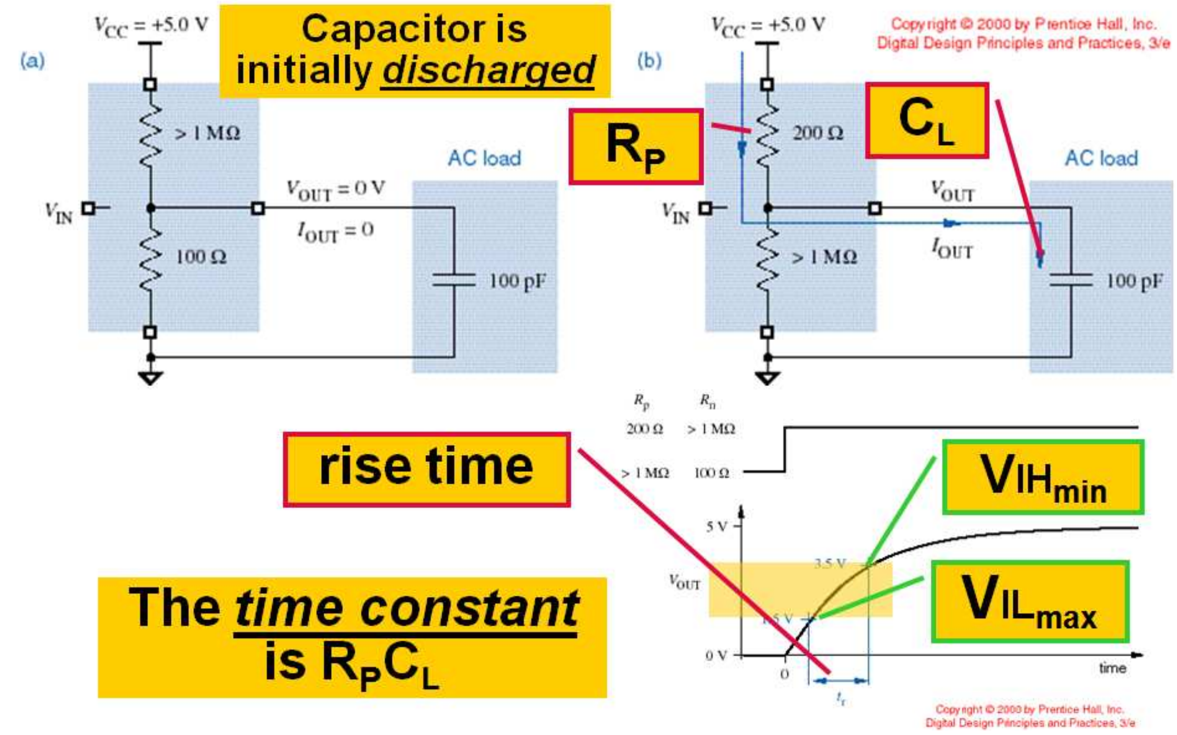
Fall time (t_{THL}) based on Wakerly's (70%-30%) definition = 1 ns

Fall time (t_{THL}) based on standard 90%-10% definition = 2.5 ns

-
  - **transition time factors**
    - **the transition times of a CMOS circuit depend mainly on two factors:**
      - ***the "on" transistor resistance***
      - ***the load capacitance***
    - ***stray capacitance* (called an "AC load") arises from at least three different sources:**
      - **output circuits – including transistors, internal wiring, and packaging**
      - **wiring that connects a gate output to other gate inputs**
      - **input circuits – including transistors, internal wiring, and packaging**
  - **equivalent circuit**
    - **a gate output's load can be modeled by an equivalent load circuit with three components:**
      - **R_L and V_L represent the DC load – they determine the steady state voltages and currents present and do not have much effect on transition times**
      - **C_L represents the AC (capacitive) load – it determines the voltages and currents present while the output is changing, as well as how long it takes to change from one state to another**



- **transition time, continued…**
  - o **model for low-to-high transition**



Capacitor is initially *discharged*

R_P

C_L

rise time

The *time constant* is R_PC_L

V_{IHmin}

V_{ILmax}

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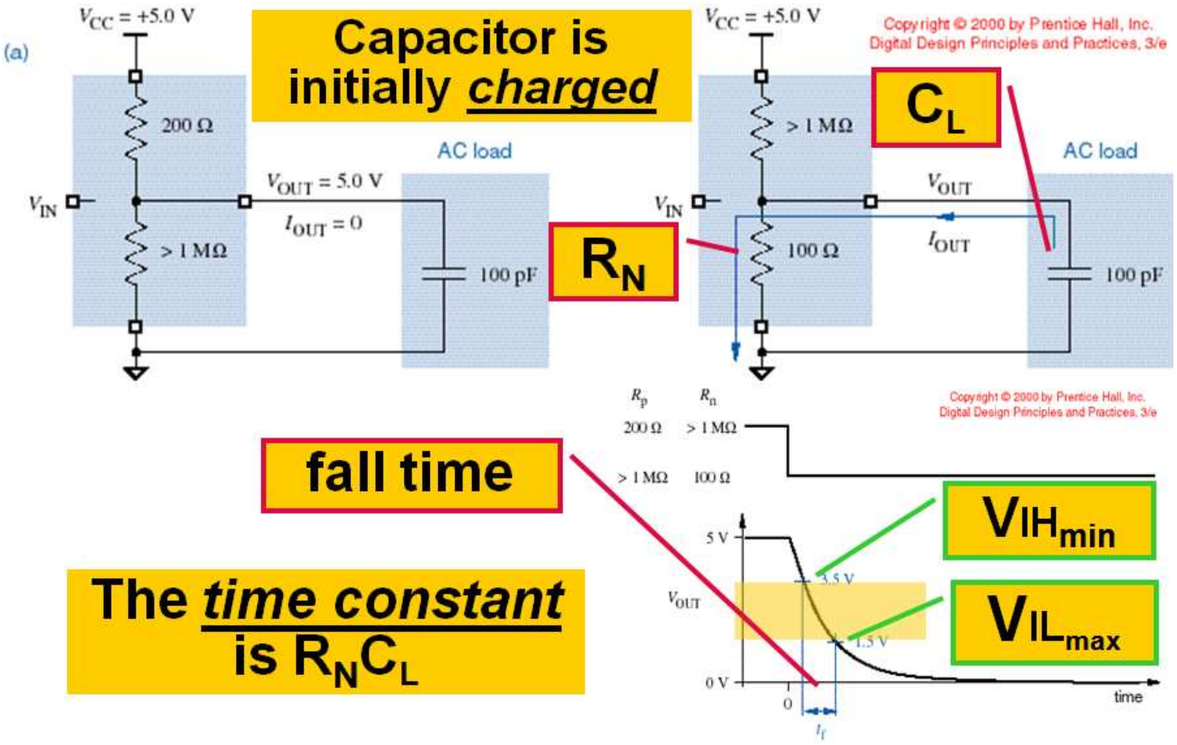
- o **model for high-to-low transition**



Capacitor is initially *charged*

C_L

R_N

fall time

The *time constant* is R_NC_L

V_{IHmin}

V_{ILmax}

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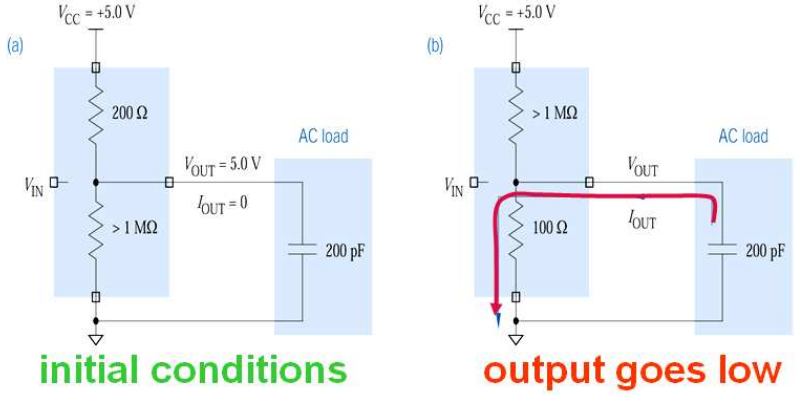
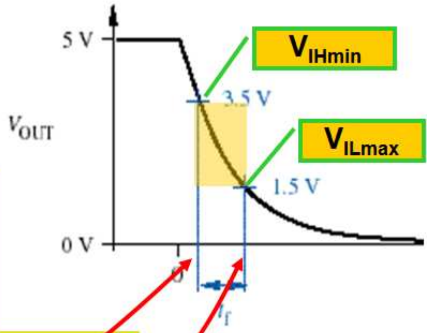
- **transition time, continued…**
  - **<u>example</u>: given that a CMOS inverter's P-channel MOSFET has an ON resistance of 200Ω, that its N-channel MOSFET has an ON resistance of 100Ω, and that the capacitive (or AC) load C_L = 200 pF, calculate the fall time**



***Calculated transition times are sensitive to the choice of logic levels* (i.e., V_{IHmin} and V_{ILmax})**



$t = -R_n * C_L * \ln(V_{out}/V_{DD})$

$= -100 * 200 * 10^{-12} * \ln(V_{out} / 5.0)$

$= -20 * 10^{-9} * \ln(V_{out} / 5.0)$

$t_{3.5} = -20 * 10^{-9} * \ln(3.5/5.0) = 7.13$ ns

$t_{1.5} = -20 * 10^{-9} * \ln(1.5/5.0) = 24.08$ ns

$t_{PHL} = t_f$ *(fall time)* = 24.08 – 7.13 = 16.95 ns

  - **transition time estimation ("rule of thumb") - in practical circuits, the transition time can be *estimated* using the RC time constant of the charging or discharging circuit**
  - **<u>example</u>: given that a CMOS inverter's P-channel MOSFET has an ON resistance of 200Ω, that its N-channel MOSFET has an ON resistance of 100Ω, and that the capacitive (or "A.C.") load C_L = 200 pF, *estimate* the fall time and rise time**

Fall time estimate:

$R_N \times C_L = 100 \times 200$ pF

$= 1 \times 10^2 \times 2 \times 10^{-10}$

$= 2 \times 10^{-8} = 20 \times 10^{-9}$

= 20 ns

Rise time estimate:

$R_P \times C_L = 200 \times 200$ pF

$= 2 \times 10^2 \times 2 \times 10^{-10}$

$= 4 \times 10^{-8} = 40 \times 10^{-9}$

= 40 ns

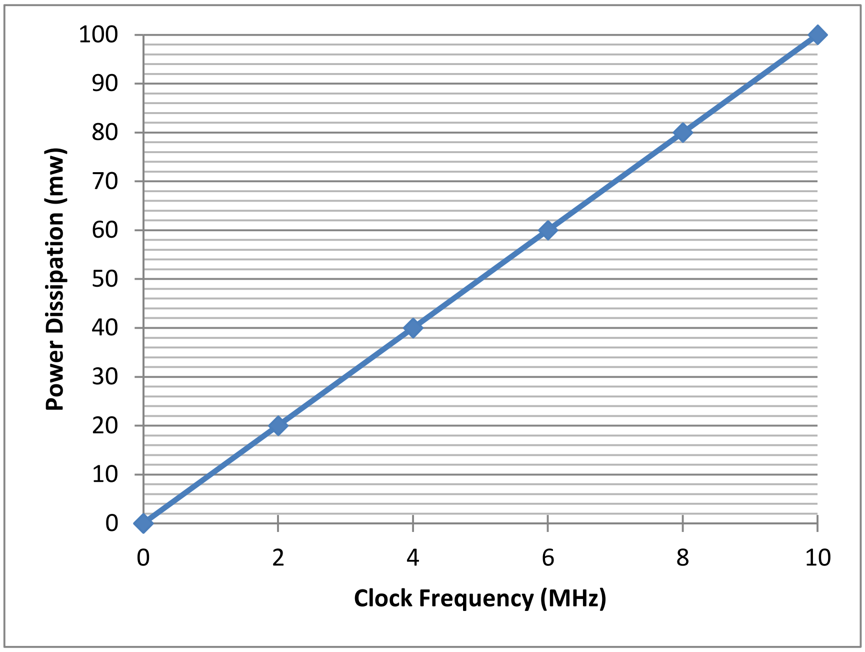
- **capacitive load – conclusions**
  - **an increase in load capacitance causes an increase in the RC time constant and a corresponding increase in the output transition (rise/fall) times**
  - **load capacitance must be *minimized* to obtain high circuit performance – this can be achieved by:**
    - **minimizing the number of inputs driven by a given signal**
    - **creating multiple copies of the signal (using "buffers")**
    - **careful *physical layout* of the circuit**

Lecture Summary – Module 1-H

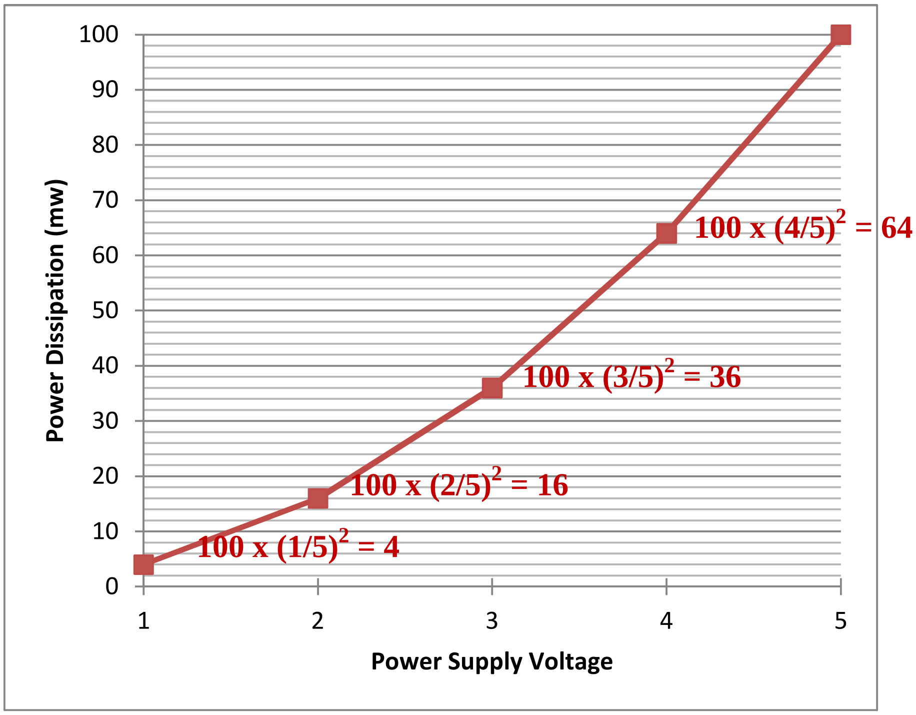
Power Consumption and Decoupling

Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 122-124

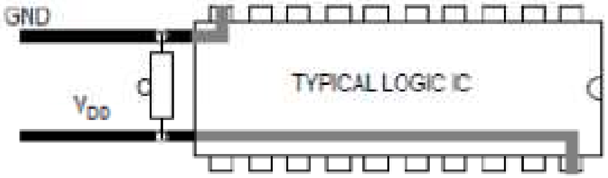
- **overview**
  - **<u>definition</u>: the power dissipation (consumption) of a CMOS circuit whose output is *not changing* is called *static (quiescent) power dissipation***
  - **most CMOS circuits have *very low* static power dissipation**
  - **CMOS circuits only dissipate a significant amount of power during *transitions* – this is called *dynamic power dissipation***
- **sources of dynamic power dissipation:**
  - **the partial "short-circuiting" of the CMOS output structure (e.g., when the input voltage is not close to one of the power supply rails) – called "P_T" (power due to output transitions)**
  - **the capacitive load on the output (power is dissipated in the "on" resistance of the active transistor to charge/discharge the capacitive load) – called "P_L" (power due to charging/discharging load)**
  - **total dynamic power dissipation (P_T + P_L) is proportional to the *square* of the power supply voltage times the transition frequency**
- **conclusions:**
  - **power dissipation increases *linearly* as the frequency of operation increases**
  - **reducing the power supply voltage results in a *quadratic* reduction of the power dissipation**
- **<u>example</u>: a microcontroller can operate over a frequency range of 0 Hz to 10 MHz, and dissipates 100 mW when operated at 10 MHz; plot its power dissipation over the specified frequency range**



- **<u>example</u>: a microcontroller can operate over a power supply range of 1 to 5 volts, and dissipates 100 mW when operated at 5 VDC; plot its power dissipation over the specified power supply range**



- **current spikes and decoupling**
  - **when a CMOS gate output changes state, the P- and N-channel transistors are both partially on simultaneously, causing a *current spike***
  - **current spikes often show up as *noise* on the power supply and ground connections**
  - ***decoupling capacitors* (between Vcc and GND) must be distributed throughout a printed circuit board (PCB) to serve as a source of instantaneous current during output transitions – *this helps mitigate noise and improve signal quality***
  - **decoupling capacitors should be located as *physically close* as possible to each IC**
  - **use 0.1 µF decoupling capacitors for system frequencies up to 15 MHz; above 15 MHz, use 0.01 µF decoupling capacitors**

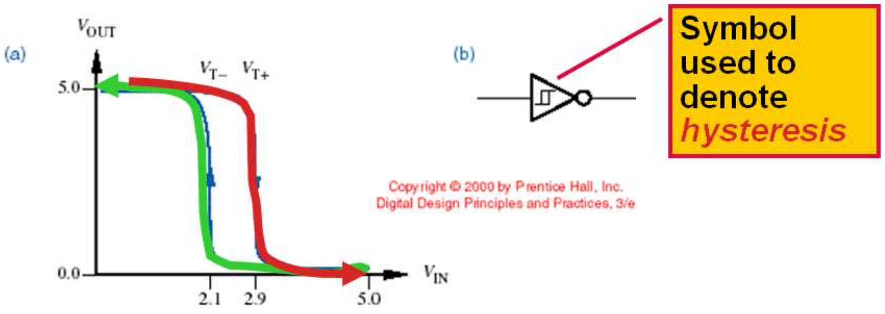


Lecture Summary – Module 1-I

Schmitt Triggers and Transmission Gates

Reference: *Digital Design Principles and Practices* (4^{th} Ed.), pp. 129-131

- **overview**
  - **the basic CMOS circuit has been "tailored" in many ways to produce gates for specific applications**
  - **this circuit tailoring has been motivated by the need for:**
    - **higher performance than can be achieved with "standard" NAND/NOR gates**
    - **"conditioning" noisy, slowly changing logic signals**
    - **allowing logic elements to communicate via buses**
- **Schmitt-trigger inputs**
  - **a *Schmitt trigger* is a special circuit that shifts the switching threshold depending on whether the input is changing from LOW-to-HIGH (V_{T+}) or from HIGH-to-LOW (V_{T-})**
  - **the difference between the two thresholds is called *hysteresis***



Symbol used to denote *hysteresis*

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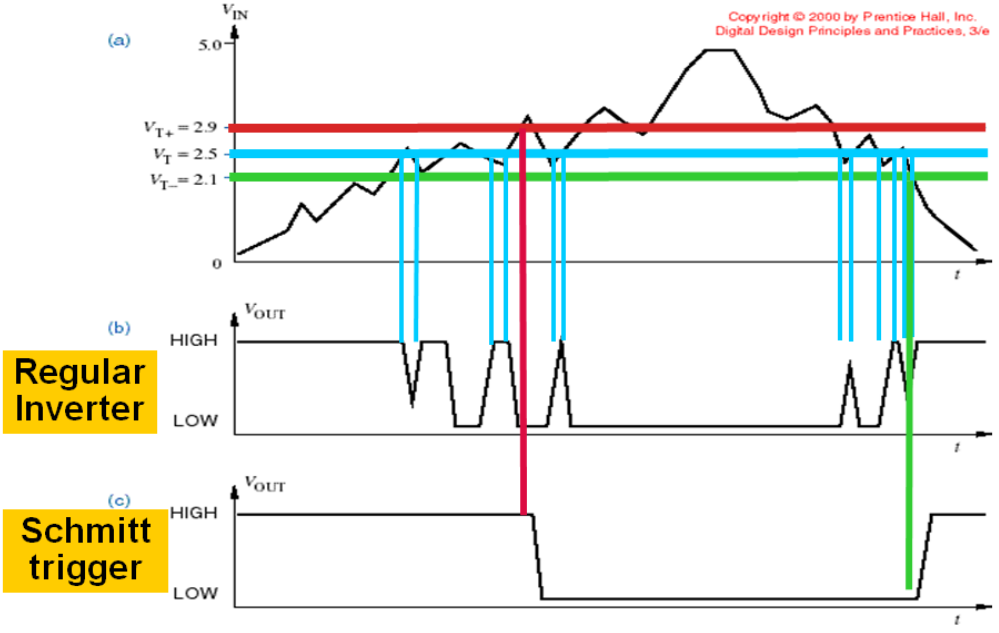
  - **comparison of Schmitt trigger with regular (single-threshold) inverter**



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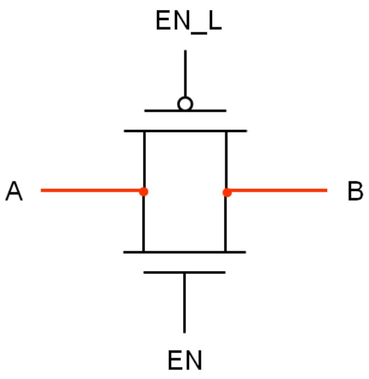
Regular Inverter

Schmitt trigger

- **Schmitt-trigger inputs, continued…**
  - **observations**
    - **Schmitt-trigger inputs have *better noise immunity* margin than ordinary gates for *noisy or slowly changing signals***
    - **"distorted" logic signals of this type typically occur in *physically long connections*, such as I/O buses and computer interface cables**
  - **"rule of foot" - logic-level signals can be sent reliably over a cable for only a *few feet***
- **transmission gates**
  - **the P- and N-channel transistor pair can be connected together to form a logic-controlled switch, called a *transmission gate***
  - **control signals EN_L and EN are at opposite levels**
  - **when EN is asserted, there is a low-impedance connection between A and B; when EN is negated, A and B are disconnected**



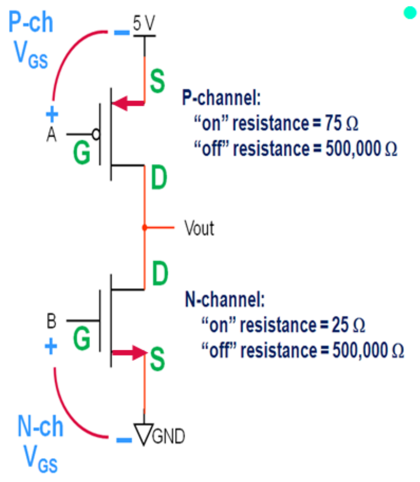
A high performance multiplexer (input selector switch) can be constructed using a pair of transmission gates and an inverter

Lecture Summary – Module 1-J

Three-State and Open-Drain Outputs

Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 132-136, 138-141

- **three-state ("tri-state") outputs**
  - **<u>definition</u>: a gate output that has a third "electrical state" is called a *three-state output* (or *tri-state output*)**
  - **this third electrical state is called the *high impedance*, *Hi-Z*, or *floating* state**
  - **in the high impedance state, the gate output effectively appears to be *disconnected* from the rest of the circuit**
  - **three-state devices have an extra input, typically called the *Output Enable* (OE), for enabling data to "flow through" the device (when asserted) or placing the output in the high impedance state (when negated)**
  - **revisit basic CMOS output circuit**



- Calculate V_{out} for the case A=5V, B=0

P-ch device is "off" (R_{DS} = 500,000 Ω)

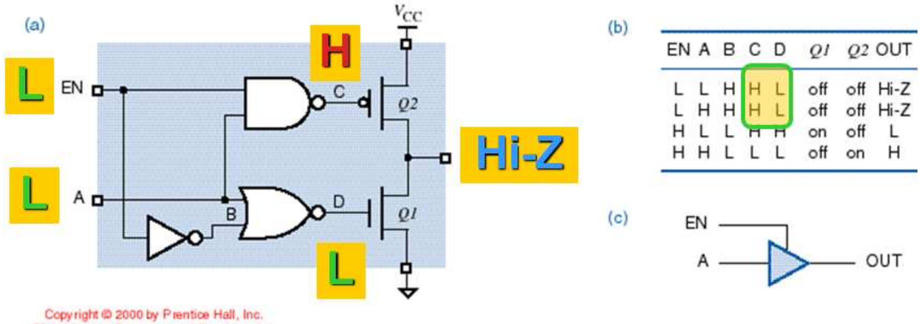
N-ch device is "off" (R_{DS} = 500,000 Ω)

V_{out} = 5 x (500,000 / 1,000,000) = 2.5 V

$P_{dissipation}$ = 5^2 / 1,000,000 = 0.025 mW

Here, Vout is effectively disconnected (in the "Hi-Z state") when A is high and B is low

Use OE (output enable) signal to force A high and B low when OE is negated



EN	A	B	C	D	Q1	Q2	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

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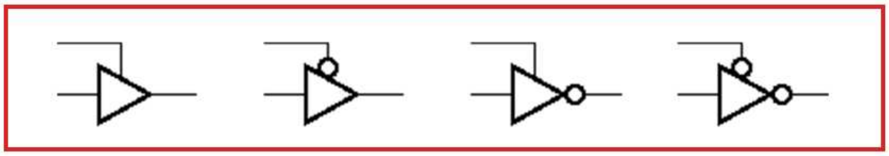
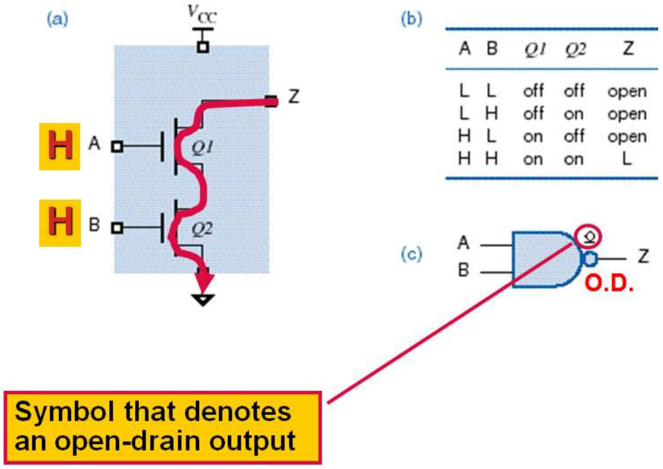


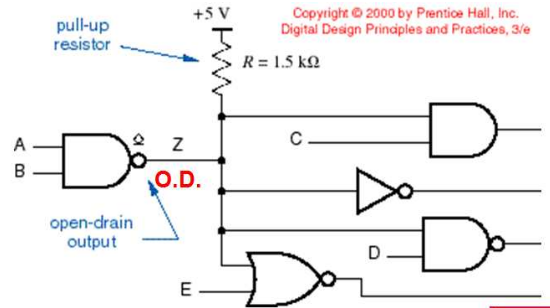
<u>Basic variations</u>: The buffer may be inverting or non-inverting, and the tri-state enable can either be active low or active high

- **three-state ("tri-state") outputs, continued…**
    - **applications**
        - **the most common use of tri-state buffers is to create *data buses* over which digital subsystems can (bi-directionally) send and receive data**
        - **<u>definition</u>: a *bus* is a collection of signals with a "common purpose" (e.g., sending the address of an item in memory, sending the data to be written to memory)**
        - **a *bus transceiver* contains pairs of tri-state buffers connected in opposite directions between each pair of pins, so that data can be transferred in *either direction***
    - **float delay**
        - **tri-state outputs are typically designed so that they *go into* the Hi-Z (high impedance) state faster than they *come out of* the Hi-Z state (i.e., t_{pLZ} and t_{pHZ} are both less than t_{pZL} and t_{pZH})**
        - **the time it takes to go from a "driven" state (valid logic level) to the Hi-Z "floating" state is called the *float delay***
        - **given this "rule", if one tri-state device is disabled and another tri-state device is enabled simultaneously, then the first device will get *off* the bus before the second one gets *on* – this helps prevent *fighting***
- **open-drain outputs**
    - **<u>definition</u>: a CMOS output structure that does <u>not</u> include a P-channel (pull-up) transistor is called an *open-drain output***
    - **an open-drain output is in one of two states: LOW or "open" (i.e., disconnected)**
    - **an *underscored diamond* (or "O.D.") is used to indicate that an output is open drain**
    - **an open-drain output requires an external pull-up resistor to *passively* pull it high in the "open" state (since the output structure does NOT include a P-channel active pull-up)**



A	B	Q1	Q2	Z
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L

Symbol that denotes an open-drain output



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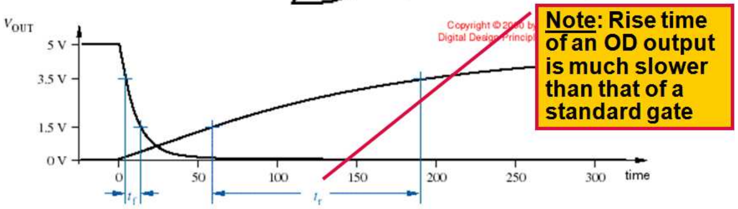
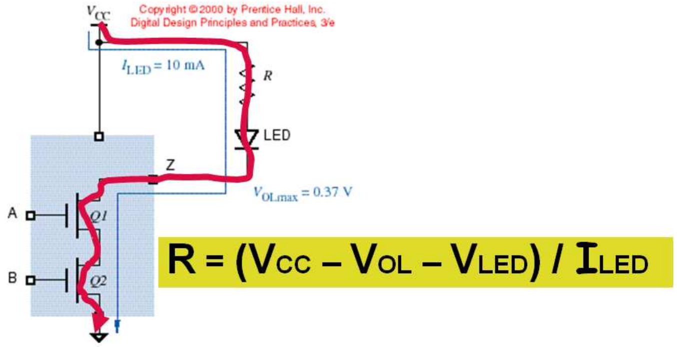


Note: Rise time of an OD output is much slower than that of a standard gate

- **open-drain outputs, continued…**
  - **application – driving LEDs** **(O.D. outputs can typically sink more current than conventional gates)**


V_{CC}
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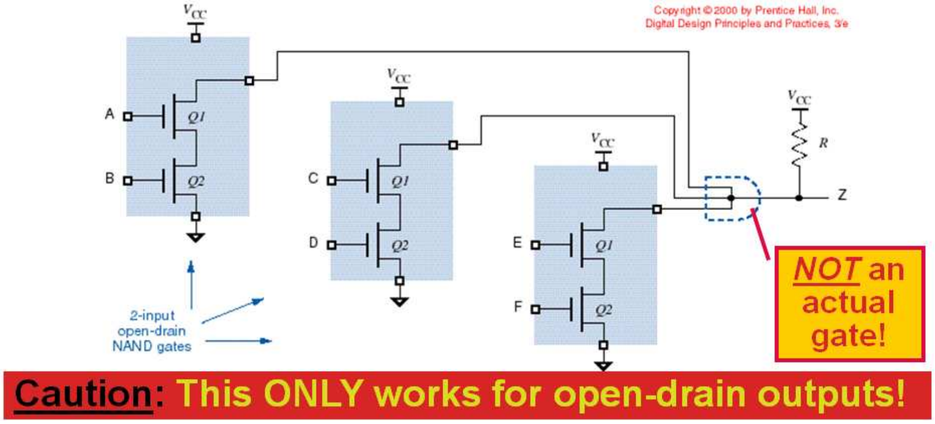
I_{LED} = 10 mA
R
LED
Z
V_{OLmax} = 0.37 V
A
B
Q1
Q2

$R = (V_{CC} – V_{OL} – V_{LED}) / I_{LED}$

  - **application - "wired" logic (<u>definition</u>: *wired logic* is performed if the outputs of several open-drain gates are tied together with a single pull-up resistor)**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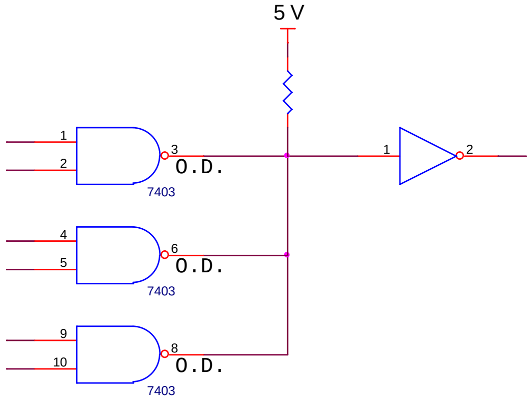
Digital Design Principles and Practices, 3/e
V_{CC}
A
B
C
D
E
F
Q1
Q2
R
Z
2-input
open-drain
NAND gates
NOT an actual gate!

Caution: This ONLY works for open-drain outputs!

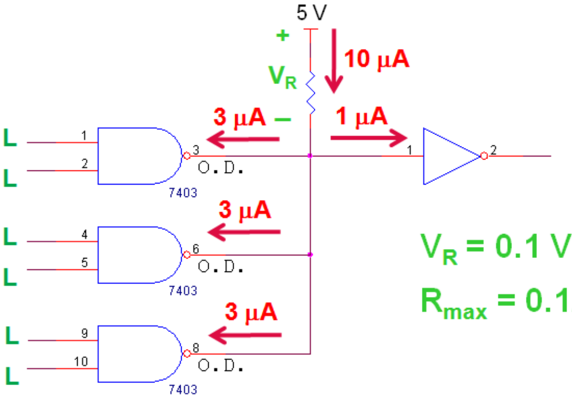
  - **pull-up resistor calculations**
    - **in open-drain applications, two calculations bracket the allowable values of the pull-up resistor R:**
      - **LOW - the sum of the current through R plus the LOW state input currents of the gate inputs driven *must not exceed* the I_{OLmax} of the active device**
      - **HIGH - the voltage drop across R in the HIGH state *must not reduce* the output voltage below the V_{IHmin} of the driven gate inputs**
  - **<u>example</u>: calculate a suitable value of pull-up resistor to use with the following circuit:**



Specifications (hypothetical data):

- **Off-state leakage current of O.D. NAND gate output: +3 μA**
- **I_{IH} and I_{IL} required by inverter input: ±1 μA**
- **V_{IH} desired for inverter input: 4.9 V**
- **$I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V**

- **open-drain outputs, continued…**
  - **pull-up resistor calculation example, continued…**
    - **solution, <u>maximum</u> R Value – based on V_{IH} desired**



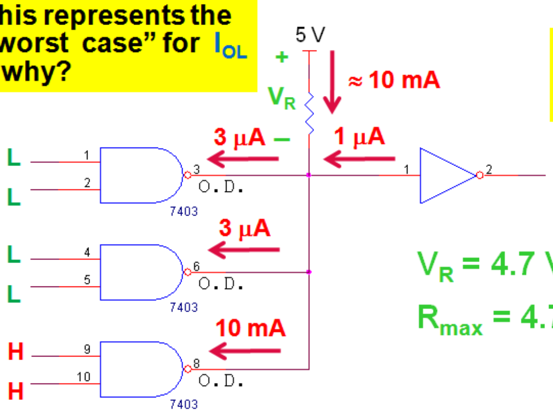
Conclusion – A pull-up resistor ranging from 470 Ω (R_{min}) to 10,000 Ω (R_{max}) will satisfy the specified constraints

$V_R = 0.1$ V $I_R = 10$ µA

$R_{max} = 0.1/0.00001 = 10{,}000\ \Omega$

- **solution, <u>minimum</u> R Value – based on $I_{OL\ max}$ of <u>one</u> gate**

This represents the "worst case" for I_{OL} – why?



Here, can safely ignore leakage and I_{IL} currents – why?

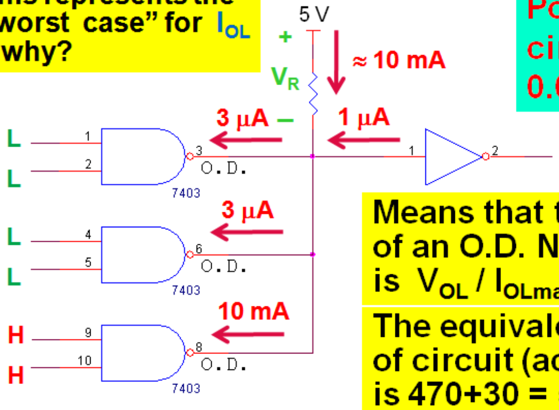
$V_R = 4.7$ V $I_R \approx 10$ mA

$R_{max} = 4.7/0.01 = 470\ \Omega$

NOTE: Picking R_{min} will minimize the rise time, while picking R_{max} will minimize the power dissipation

- **"prove" the "worst case" scenario (R = 470 Ω)**

This represents the "worst case" for I_{OL} – why?



Power dissipation of circuit is $I_R^2 \times R_{eq} = 0.01^2 \times 500 \approx 50$ mW

Means that the "on" resistance of an O.D. NAND gate used here is $V_{OL} / I_{OLmax} = 0.3/0.01 = 30\ \Omega$

The equivalent load impedance of circuit (across power supply) is 470+30 = 500 Ω

Specifications (hypothetical data):

- Off-state leakage current of O.D. NAND gate output: +3 µA
- I_{IH} and I_{IL} required by inverter input: ±1 µA
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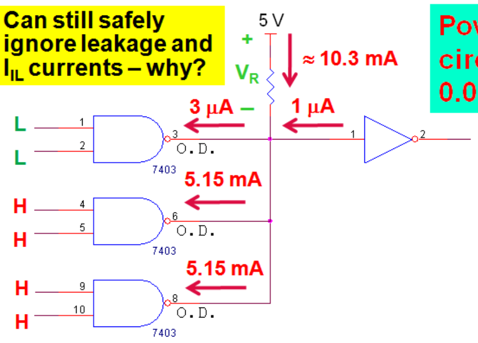
- $I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V

- **open-drain outputs, continued…**
  - **pull-up resistor calculation example, continued…**
    - **"proof", continued…**



Can still safely ignore leakage and I_{IL} currents – why?

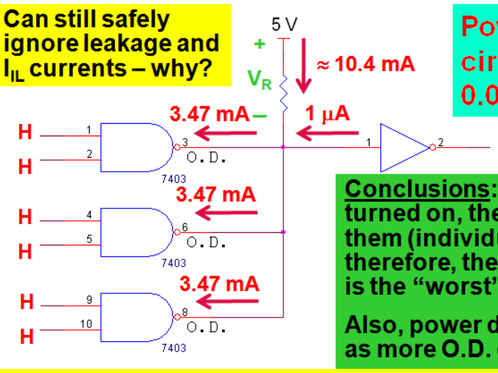
Power dissipation of circuit is I_R^2 x R_{eq} = 0.0103^2 x 485 ≈ 51.5 mW

Next, turn on <u>two</u> O.D. gates

The equivalent load impedance of circuit is 470+15 = 485 Ω (because have two 30 Ω "on" resistances in parallel)

I_R is now 5 / 485 = 0.0103 A = 10.3 mA, which is <u>split</u> between the two gates that are "on"

- **conclusions**



Can still safely ignore leakage and I_{IL} currents – why?

Power dissipation of circuit is I_R^2 x R_{eq} = 0.0104^2 x 480 ≈ 52 mW

<u>Conclusions</u>: As more O.D. gates are turned on, the amount of current each of them (individually) has to sink is <u>reduced</u>; therefore, the first case (single gate "on") is the "worst" one with respect to I_{OL}.

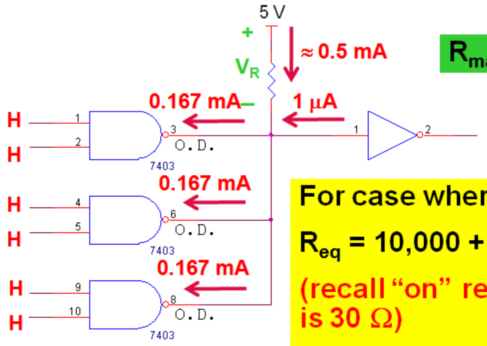
Also, power dissipation increases <u>slightly</u> as more O.D. gates are turned on.

Finally, turn on <u>all three</u> O.D. gates

The equivalent load impedance of circuit is 470+10 = 480 Ω (because have three 30 Ω "on" resistances in parallel)

I_R is now 5 / 480 = 0.0104 A = 10.4 mA, which is <u>split</u> among the three gates that are "on"

- **compare power dissipation of circuit using R_{min} vs. R_{max} as the pull-up resistor**



R_{max} (10,000 Ω)

For case where all gates are <u>on</u>:

R_{eq} = 10,000 + 10 = 10,010 Ω

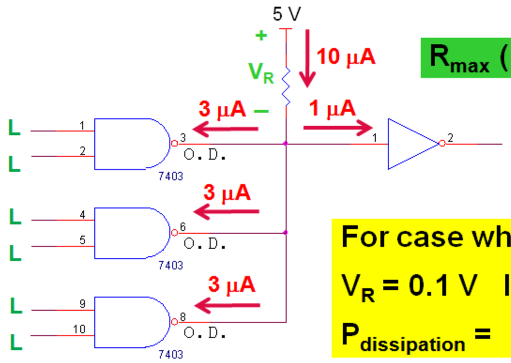
(recall "on" resistance of each gate is 30 Ω)

I_R ≈ 5 / 10,010 ≈ 0.5 mA (note - split among three gate outputs)

$P_{dissipation}$ = I_R^2 x R_{eq} ≈ 2.5 mW

<u>Note</u>: V_{IL} of inverter is nearly 0 V

- **open-drain outputs, continued…**
  - **pull-up resistor calculation example, continued…**
    - **power dissipation comparison, continued…**



R_{max} (10,000 Ω)

For case where all gates are <u>off</u>:

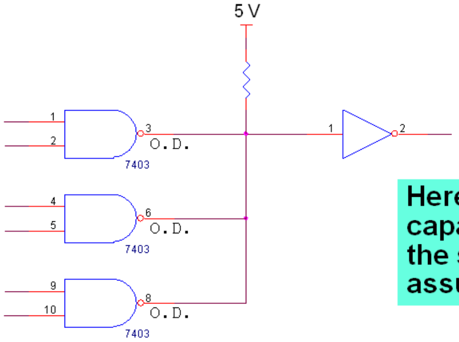
V_R = 0.1 V I_R = 10 µA

$P_{dissipation}$ = I_R^2 x R = 1 µW

<u>Note</u>: V_{IH} of inverter is 4.9 V

<u>Conclusion</u>: Power dissipation when R_{max} is used does not exceed 2.5 mW (vs. 52 mW for R_{min}); therefore, use of R_{max} minimizes the power dissipation

- **compare rise time estimates of circuit using R_{min} vs. R_{max} as the pull-up resistor**

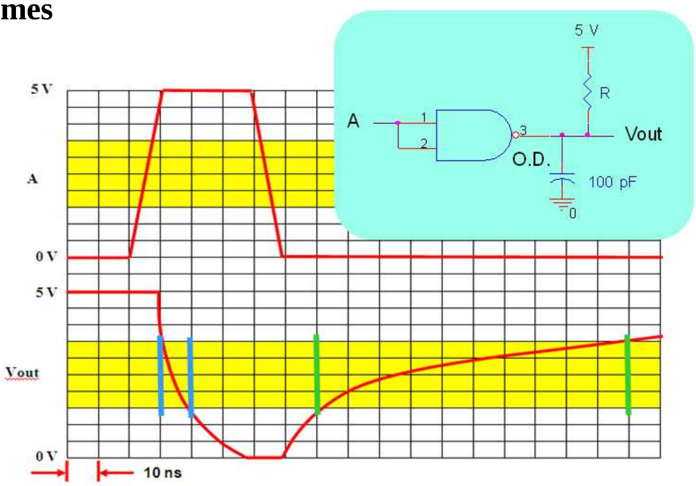


Here, need to know the capacitive load (C_L); for the sake of analysis, assume it is 100 pF

Comparison:

- For $R_{min,}$ rise time estimate is 470 x 100 x 10^{-12} = 47 ns
- For $R_{max,}$ rise time estimate is 10,000 x 100 x 10^{-12} = 1000 ns
- Conclusion: rise time for R_{max} case is <u>considerably longer</u>

  - **<u>example</u>: estimate the "on" resistance of an O.D. gate and pull-up resistor value based on rise/fall times**



rise time = 100 ns = $R_{pull\text{-}up}$ x 100 pF → $R_{pull\text{-}up}$ = 1000 Ω

fall time = 10 ns = R_{on} x 100 pF → R_{on} = 100Ω