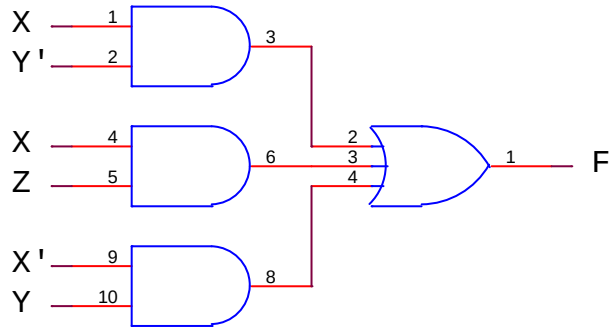
Practice Homework Solution for Module 2

1. Practice finding dual and complement functions/circuit realizations. Draw an AND-OR circuit realization of each, and write sum-of-products expressions for the dual and complement functions.

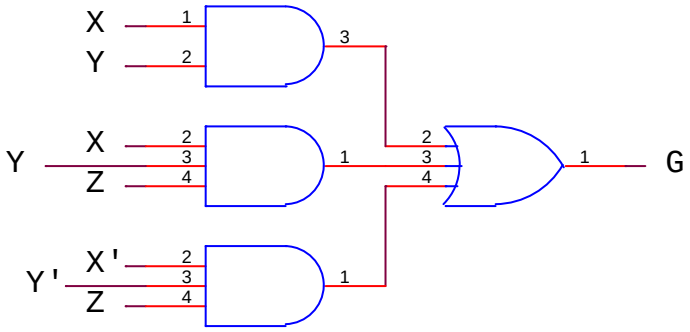
(a) F(X,Y,Z) = X•(Y′+Z) + X′•Y *(AND-OR circuit only)*

= X•Y′ + X•Z + X′•Y



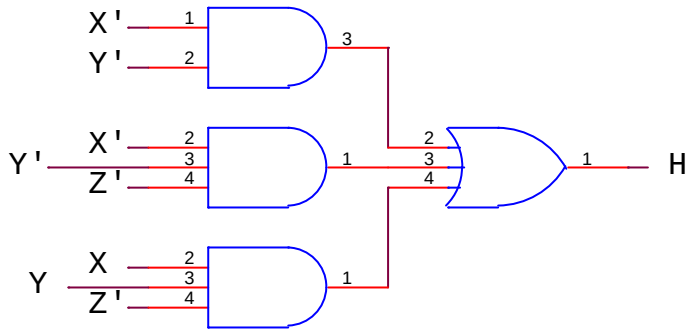
(b) G(X,Y,Z) = F^D(X,Y,Z) *the DUAL of function F, above, plus AND-OR circuit*

= (X+Y′) • (X+Z) • (X′+Y)
= X•Y + X•Y•Z +X′•Y′•Z

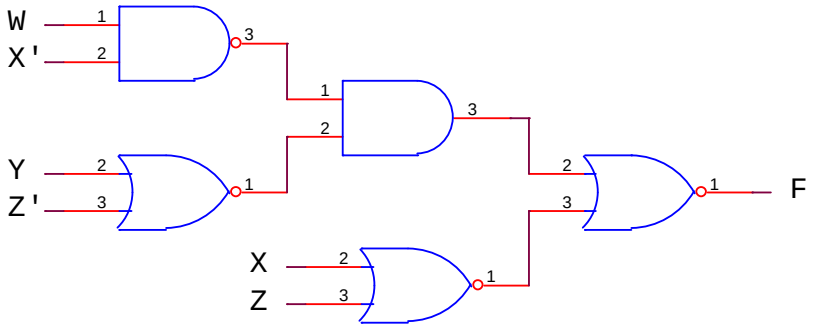


(c) H(X,Y,Z) = F′(X,Y,Z) *the COMPLEMENT of function F plus AND-OR circuit*

= (X′+Y) • (X′+Z′) • (X+Y′)
= X′•Y′ + X′•Y′•Z′ +X•Y•Z′

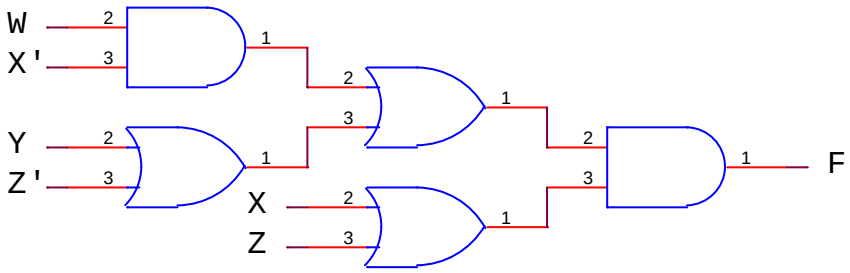


2. For the circuit shown below, derive the following formal descriptions:
   (a) equivalent circuit consisting of only AND and OR gates (obtained through *graphical transformation* of the original circuit)
   (b) minimum SoP expression
   (c) K-map
   (d) truth table
   (e) ON set
   (f) OFF set



W	X	Y	Z	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

equivalent AND-OR circuit



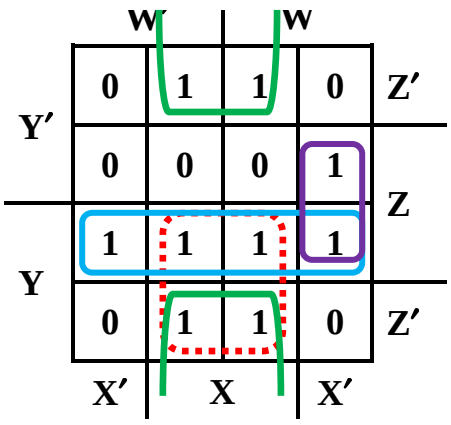
F(W,X,Y,Z) = (W•X′ + Y + Z′) • (X + Z)
= X•Y + Y•Z′ + W•X′•Z + Y•Z

ON set: **Σ w,x,y,z (3,4,6,7,9,11,12,14,15)**

OFF set: **Π w,x,y,z (0,1,2,5,8,10.13)**

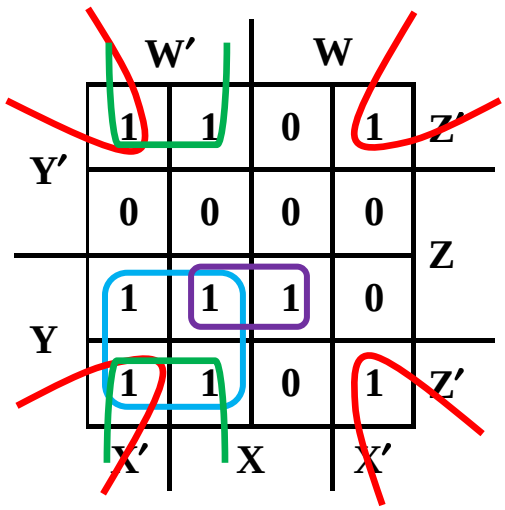
minimum SoP expression: **F(W,X,Y,Z) = X•Z′ + Y•Z + W•X′•Z**

K-map:



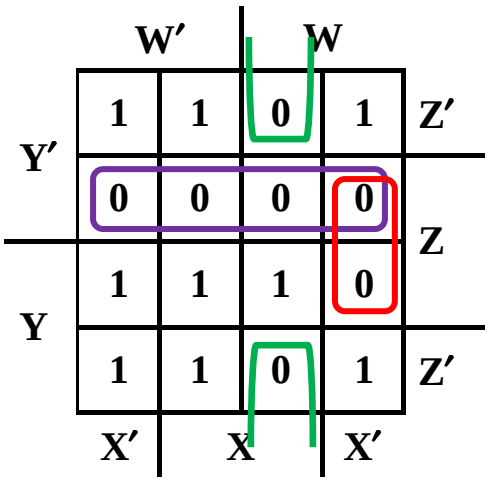
3. For the function mapped below:

(a) Write a minimal sum-of-products expression and calculate its cost:



F(W,X,Y,Z) = X′•Z′ + W′•Y + W′•Z′ + X•Y•Z
Cost = 13 inputs + 5 gates (outputs) = 18

(b) Write a minimal product-of-sums expression and calculate its cost:



F(W,X,Y,Z) = (Y+Z′)•(W′+X+Z′)•(W′+X′+Z)
Cost = 11 inputs + 4 gates (outputs) = 15

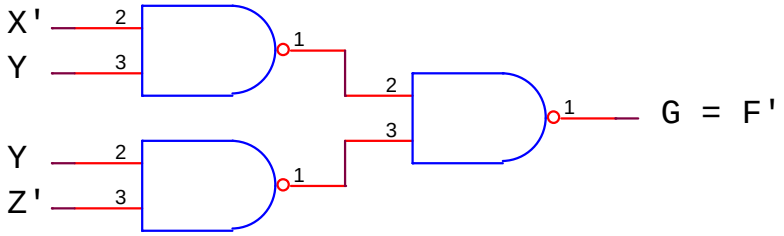
4. Express the *complement* of the following function as an ON SET and draw a NAND-NAND circuit realization:

$$F(X,Y,Z) = Y' + X \cdot Z$$

$$G = F' = Y \cdot (X'+Z') = X' \cdot Y + Y \cdot Z'$$

	X′		X	
Z′	0	1	1	0
Z	0	1	0	0
	Y′	Y		Y′

$$\text{ON set} = \Sigma_{X,Y,Z}\,(2,3,6)$$



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5. Express the *dual* of the following function as an OFF SET and draw a NOR-NOR circuit realization:

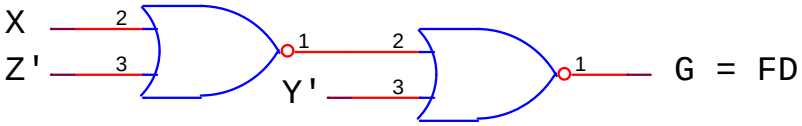
$$F(X,Y,Z) = Y + X \cdot Z'$$

$$G = F^D = Y \cdot (X+Z') = X \cdot Y + Y \cdot Z'$$

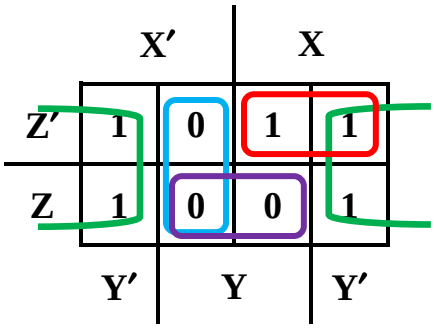
	X′		X	
Z′	0	1	1	0
Z	0	0	1	0
	Y′	Y		Y′

$$\text{OFF set} = \Pi_{X,Y,Z}\,(0,1,3,4,5)$$

$$G' = Y' + X' \cdot Z \;\rightarrow\; G = Y \cdot (X+Z')$$



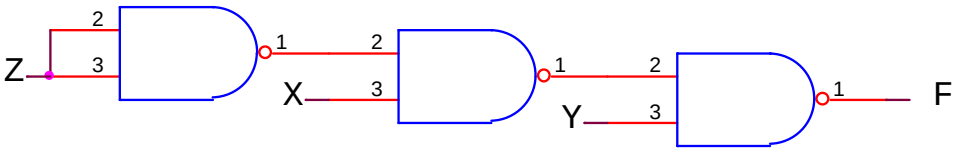
6. Assuming that *only true* variables are available, realize the function F(X,Y,Z) mapped below three different ways:
   (a) Using only 7400 (quad 2-input NAND) chips
   (b) Using only 7402 (quad 2-input NOR) chips
   (c) Using only 7403 (quad 2-input open-drain NAND) chips



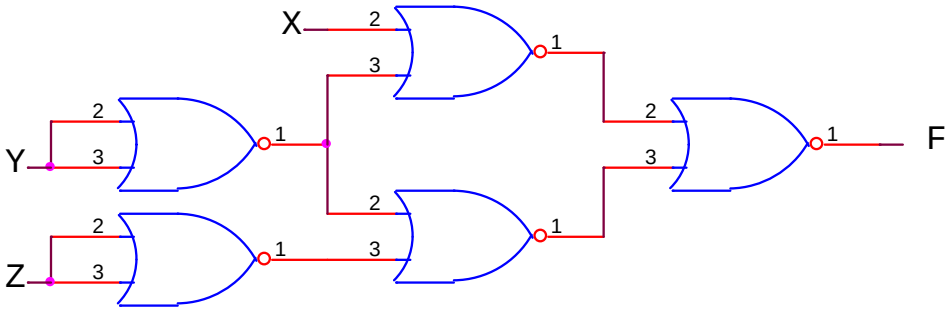
Show complete schematics for each realization, along with your derivations.

F(X,Y,Z) = Y′ + X•Z′ **F′ = X′•Y + Y•Z**

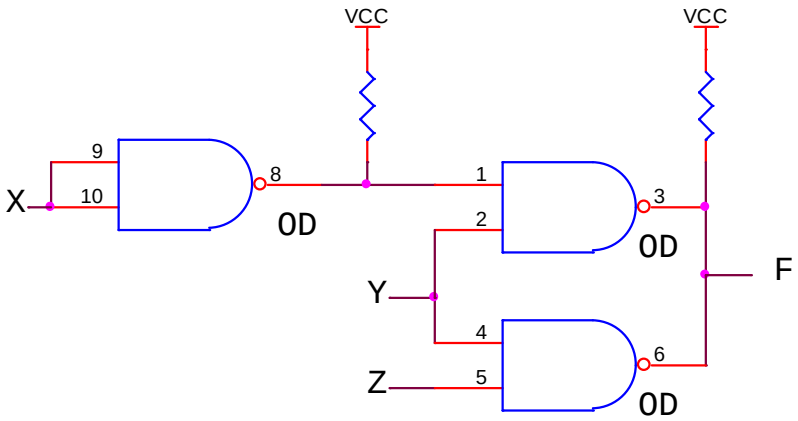
(a)



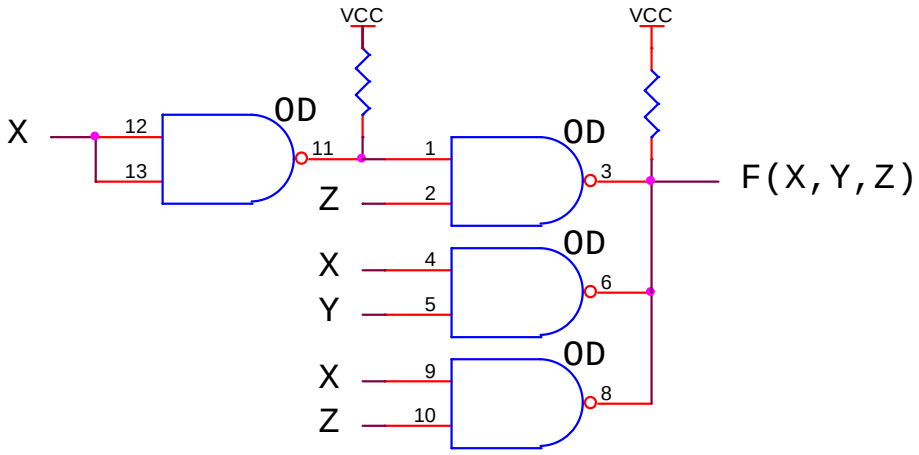
(b)



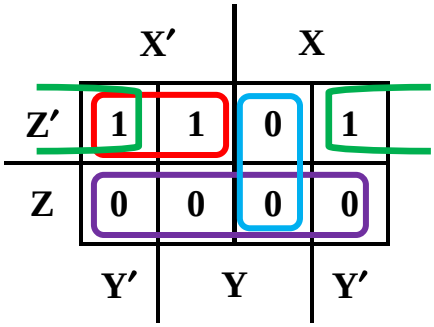
(c)



7. Given the following circuit, determine the ON set and write both a minimal SoP and minimal PoS expression for the function it realizes.



write by inspection, then map: F′ = X′•Z + X•Y + X•Z

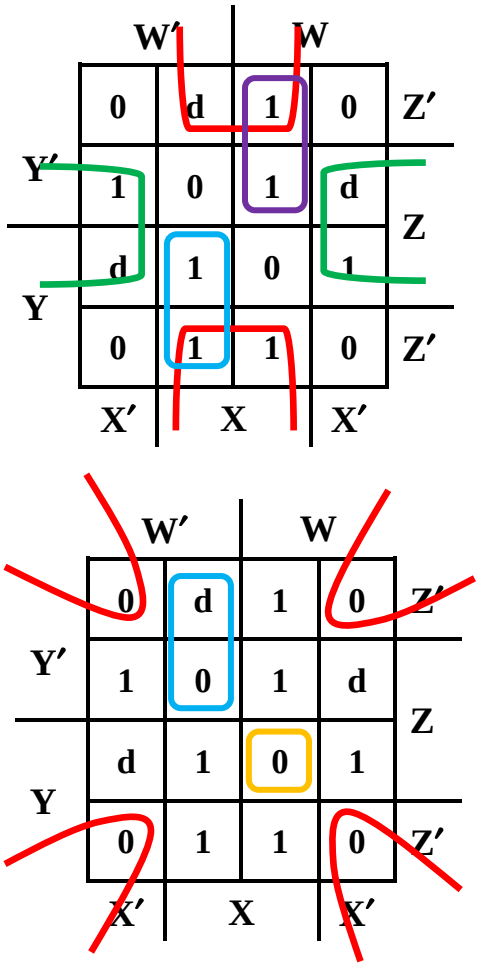


minimum SoP: F = X′•Z′ + Y′•Z′

minimum PoS: F′ = X•Y + Z → F = (X′ + Y′)•Z′

ON set = $\Sigma_{X,Y,Z}$ (0,2,4)

8. Simplify the function mapped below in terms of XOR or XNOR operators, draw a circuit realization, and compare the cost of this "simplified" version with minimal SoP (NAND-NAND) and PoS (NOR-NOR) realizations.

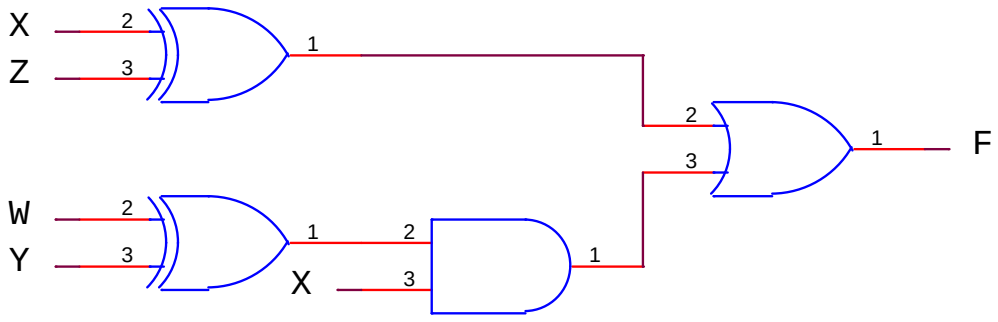


min SoP: F = X′•Z + X•Z′ + W′•X•Y + W•X•Y′ **cost = 14 inputs + 5 gates = 19**

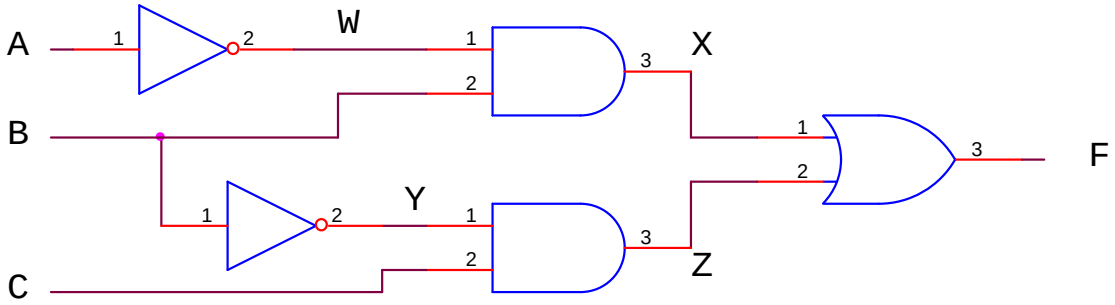
min PoS: F′ = X′•Z′ + W′•X•Y′ + W•X•Y•Z

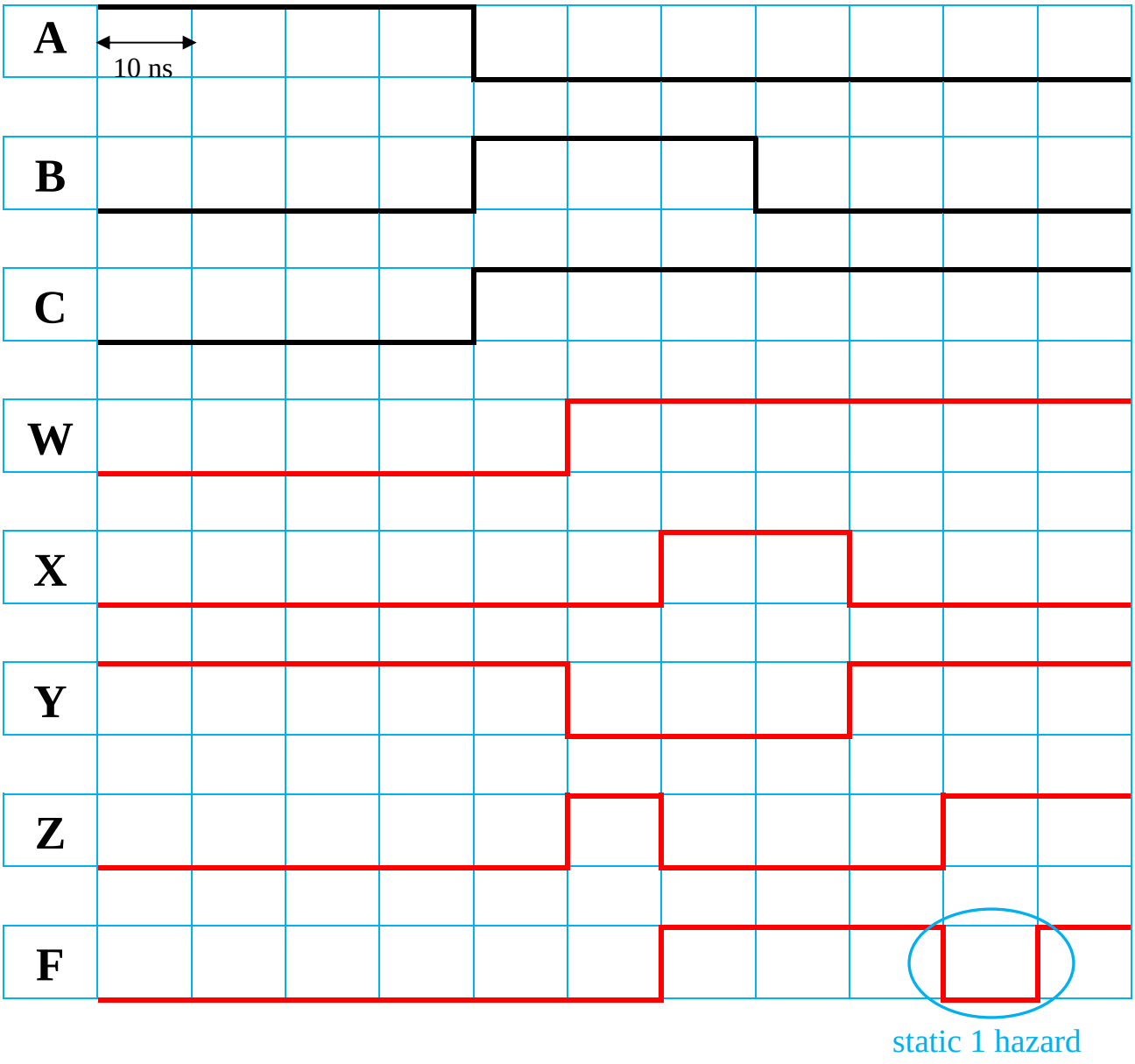
→ F = (X+Z)•(W+X′+Y)•(W′+X′+Y′+Z′) **cost = 12 inputs + 4 gates = 16**

XOR : F = (X ⊕ Z) + X•(W ⊕ Y) **cost = 8 inputs + 4 gates = 12**

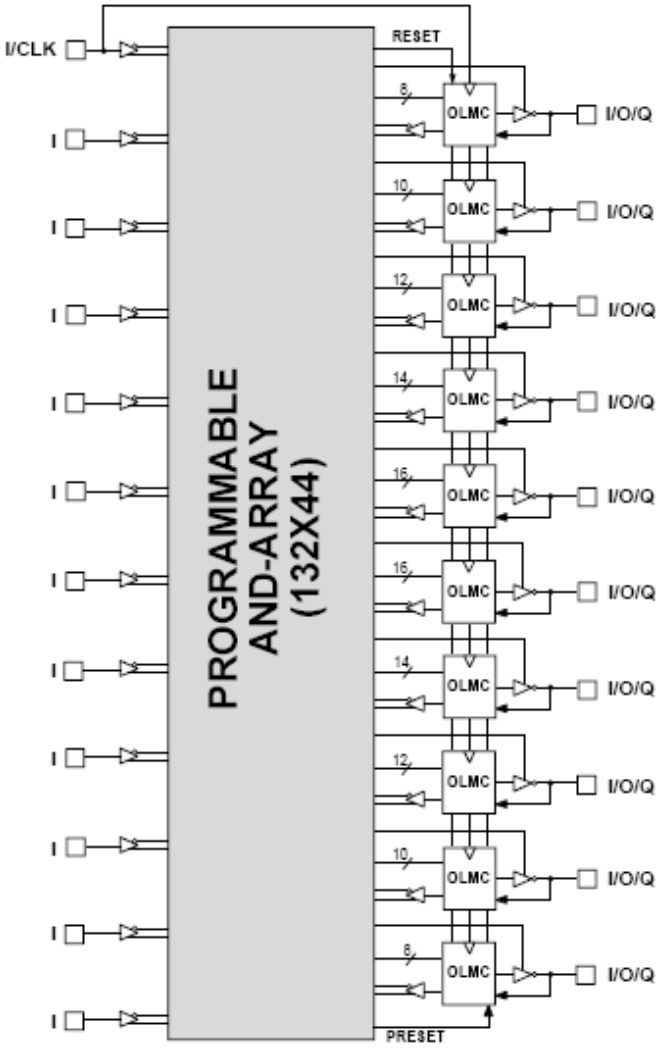


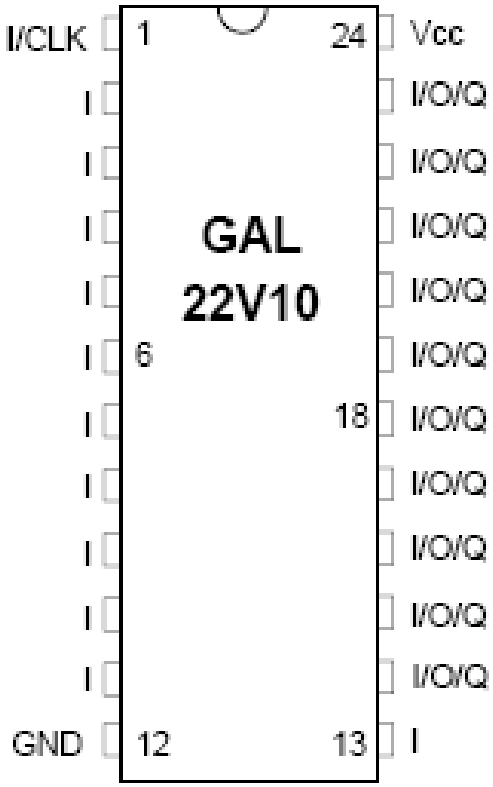
9. Sketch the response of the circuit, below, to the input signals provided. Assume the input signals (A, B, C) have been in the initial states shown prior to the beginning of the chart, and that each gate has a t_{PLH} and t_{PHL} of 10 ns. *Identify the hazard* (by name) if one occurs in the output (F).





10. Write a complete ABEL program that realizes the "largest" XOR function (number of inputs) possible using a GAL22V10 PLD. Assuming a 10 ns PLD is used, determine the worst case propagation delay. Attach a printout of your source file (handwritten code will not be graded) along with a printout of the chip report generated by ispLever. *Include explicit pin assignments.*



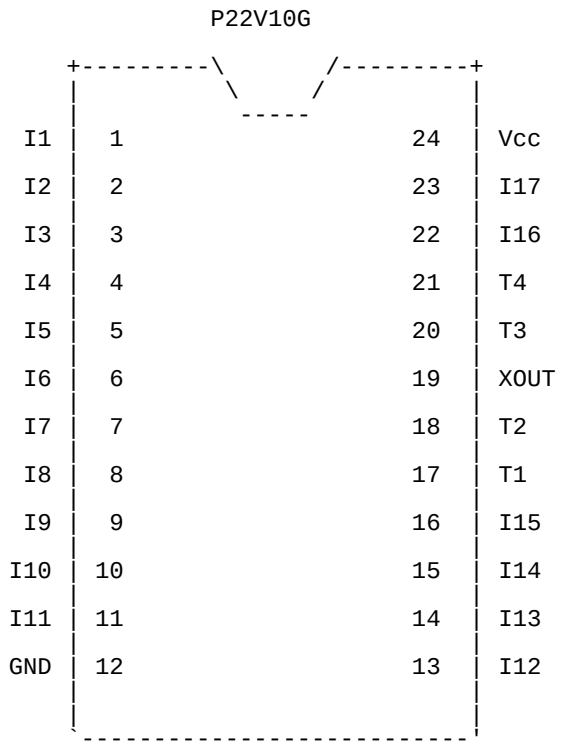


NOTE: Macrocells have a varying number of P-terms

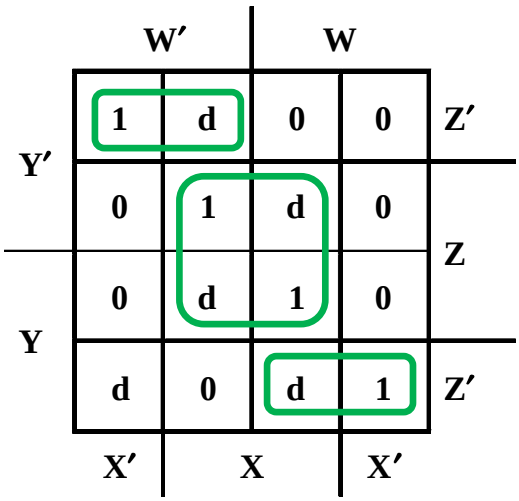
```
MODULE bigxor

TITLE 'Largest Possible XOR in 22V10'

DECLARATIONS

I1..I17 pin 1..11, 13..16, 22..23;   " XOR inputs
XOUT pin 19 istype 'com';   " XOR output

T1..T4 pin 17..18, 20..21 istype 'com';  " intermediate outputs

EQUATIONS

T1 = I1 $ I2 $ I3 $ I4;
T2 = I5 $ I6 $ I7 $ I8;
T3 = I9 $ I10 $ I11 $ I12;
T4 = I13 $ I14 $ I15 $ I16;
XOUT = T1 $ T2 $ T3 $ T4 $ I17;

END
```

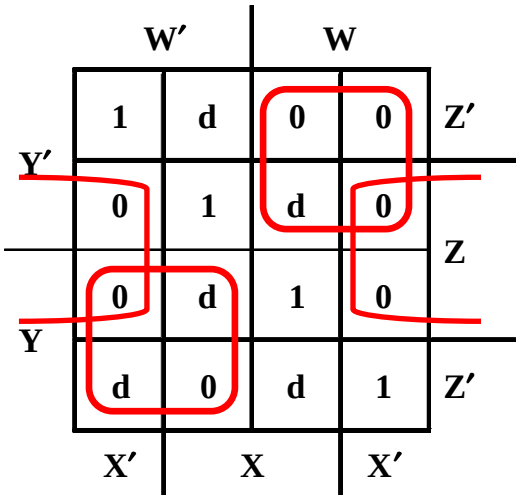
Maximum number of inputs possible is **17** (pin-limited)

Worst case delay is **20 ns** for 10 ns PLD

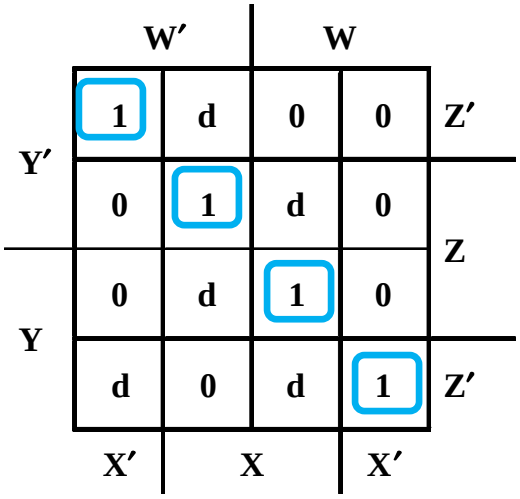


11. Assuming the availability of *both* true and complemented variables, find the *simplest* (lowest cost) realization of the function mapped below. Solution can be two-level NAND, two-level NOR, single-level open-drain NAND/wired-AND, or a "mixed" simplification that utilizes XOR/XNOR gates. Justify your choice based on a cost comparison among *all* potential options. Show the circuit for your "final answer".



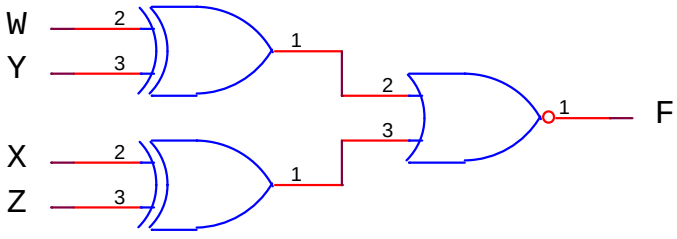


F = X•Z + W′•Y′•Z′ + W•Y•Z′ F′=X′•Z + W′•Y + W•Y′ → F = (X+Z′)•(W+Y′)•(W′+Y)
min SoP cost = 15 OD NAND cost = 9 min PoS cost = 13

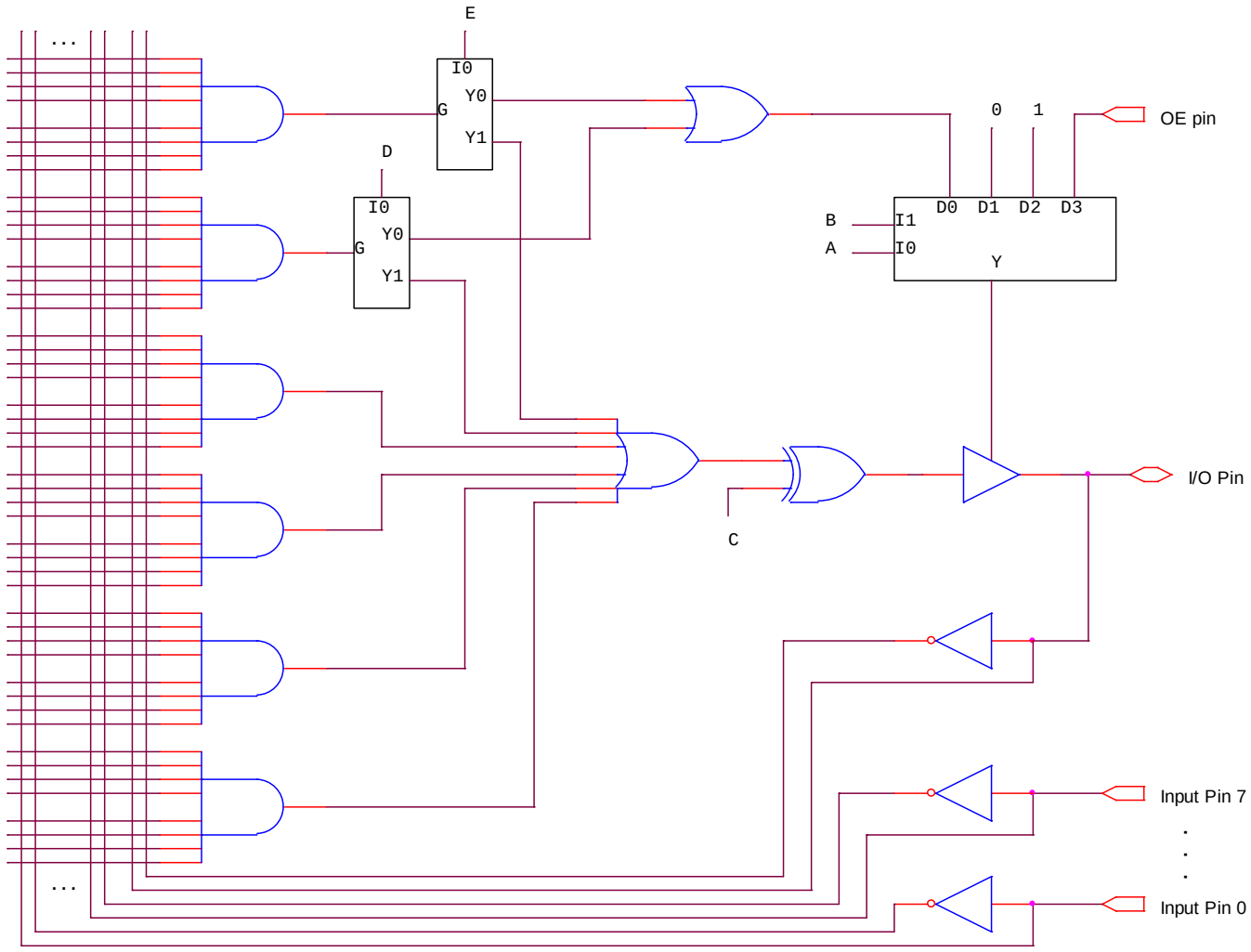


F = (W⊕Y)′•(X⊕Z)′
mixed XOR cost = 9

End up with a "tie" between the OD NAND/wired-AND configuration and the "mixed" simplification based on XOR/XNOR (cost of each = 9)



12. Assume a hypothetical PLD has macrocells of the following configuration:



Determine the following:

(a) The maximum number of *P-terms* available for a function realized by the macrocell if D=0 and E=0 4

(b) The maximum number of *P-terms* available for the *tri-state enable* function if D=0, E=1, A=0, and B=0 1

(c) All the possibilities for controlling the tri-state buffer enable one or two product term expression, off, on, controlled by OE pin

(d) The maximum number of *literals* that each P-term can have 8

(e) The settings for A, B, C needed to realize a *reverse polarity* equation with an *active low* output A=0, B=1, C=0

13. Demonstrate that you can implement *any* arbitrary 3-variable Boolean function using *just* a 3:8 decoder with active low outputs and a *single* 4-input NAND gate (plus some resistors and an LED).

HINT: The LED may be connected in either a sourcing or a sinking configuration.

(a) Implement the function **F(X,Y,Z) = X′·Z′ + X·Y·Z**

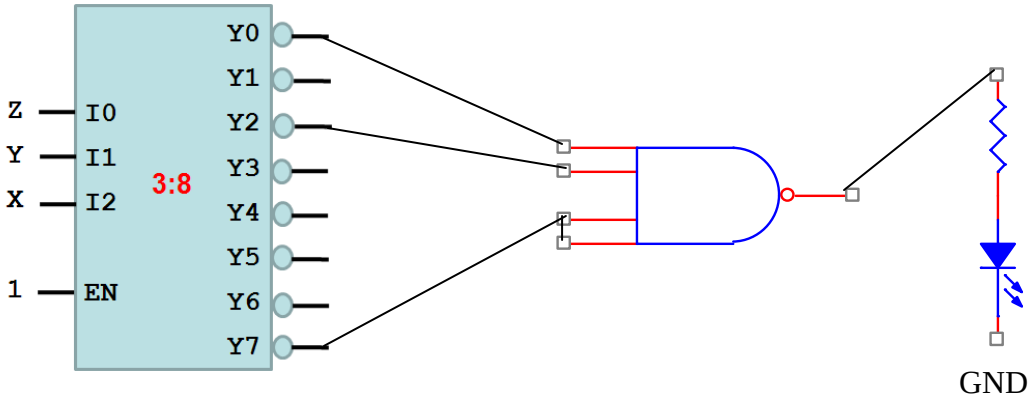
Derivation:

	X′		X	
Z′	1	1	0	0
Z	0	0	1	0
	Y′	Y		Y′

Use 1's (since fewer of them)

$\Sigma_{X,Y,Z}$ (0,2,7)

Yields F → source current to LED



(b) Implement the function **F(X,Y,Z) = X′·Y·Z′ + Y·Z + X·Z′**

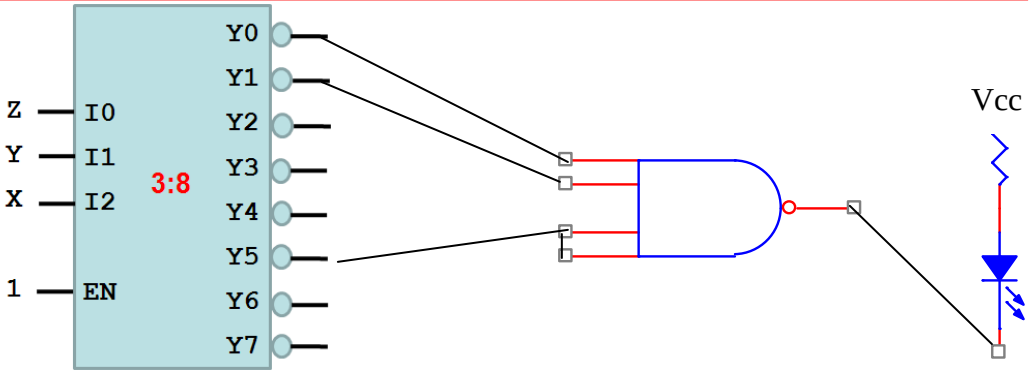
Derivation:

	X′		X	
Z′	0	1	1	1
Z	0	1	1	0
	Y′	Y		Y′

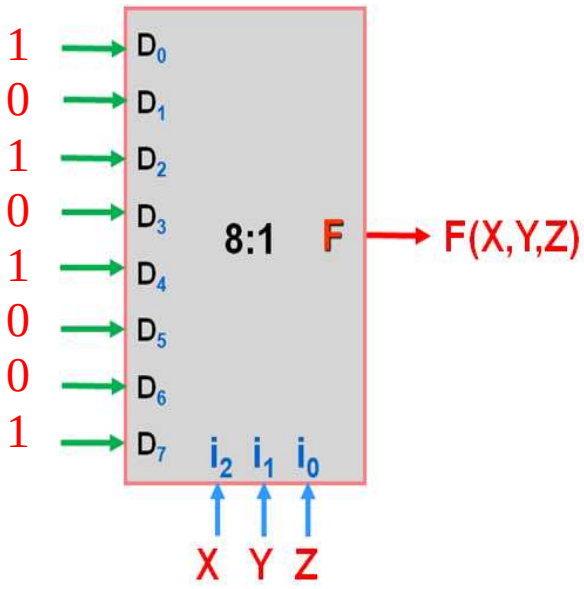
Use 0's (since fewer of them)

$\Pi_{X,Y,Z}$ (0,1,5)

Yields F′ → sink current through LED



14. Demonstrate you can implement *any* arbitrary 3-variable Boolean function using only an 8:1 multiplexer.



How many *different functions* of <u>three</u> variables are there? **256**

Determine the data input settings (D0-D7) required to implement the function **F(X,Y,Z) = X′·Z′ + X·(Y⊕Z)′** using the 8:1 multplexer depicted above.

Derivation:

F(X,Y,Z) = X′·Z′ + X·(Y⊕Z)′
= X′·Z′ + X·(Y′·Z′ + Y·Z)
= X′·Z′ + X·Y′·Z′ + X·Y·Z

$\Sigma_{X,Y,Z}$ (0,2,4,7)

$\Pi_{X,Y,Z}$ (1,3,5,6)

	X′		X	
Z′	1	1	0	1
Z	0	0	1	0
	Y′	Y		Y′

15. Given the following ABEL program:

```
MODULE  basic_pri

TITLE  'Basic 3-input Priority Encoder'

DECLARATIONS
X,Y,Z  pin;
E0..E1   pin istype 'com';
GS pin istype 'com';
TRIEN pin;
d = .X.;

TRUTH_TABLE ([ X, Y, Z]->[E1,E0,GS])
             [ 0, 0, 0]->[ 0, 0, 0];
             [ 0, 0, 1]->[ 0, 0, 1];
             [ 0, 1, d]->[ 0, 1, 1];
             [ 1, d, d]->[ 1, 0, 1];

EQUATIONS

[E0..E1].OE = TRIEN;

END
```

Determine the following:

(a) The outputs (E1,E0,GS) produced when all inputs are negated E1=HiZ, E0=HiZ, GS=0

(b) The outputs (E1,E0,GS) produced when input Z is asserted and input TRIEN is negated
E1=HiZ, E0=HiZ, GS=1

(c) The outputs (E1,E0,GS) produced when input Z is asserted and input TRIEN is asserted
E1=0, E0=0, GS=1

(d) The outputs (E1,E0,GS) produced when inputs Y and Z are asserted and input TRIEN is asserted E1=0, E0=1, GS=1

(e) The outputs (E1,E0,GS) produced when inputs X, Y, and Z are asserted and input TRIEN is asserted E1=1, E0=0, GS=1

16. Given the ispLever Reduced Equation and Chip Reports on the page which follows, determine the following:

(a) Which set of equations (circle one: ***positive polarity*** -or- *reverse polarity*) the fitter chose to burn into the PLD

(b) The pin numbers the fitter assigned to the X and Y outputs 14 and 23

(c) The number of P-terms needed to realize the X (positive polarity) equation 8

(d) The number of P-terms needed to realize the !X (reverse polarity) equation 8

(e) The number of P-terms needed to realize the Y (positive polarity) equation 4

(f) The number of P-terms needed to realize the !Y (reverse polarity) equation 4

(g) A possible ABEL source form of the equation for X based on XOR/XNOR operators

```
X = !A $ B $ C $ D;
```

(h) A possible ABEL source form of the equation for Y based on XOR/XNOR operators

```
Y = (A !$ C) & (B !$ D);
```

(i) The ON set for the function realized by the equation for X

$\Sigma_{A,B,C,D}(0,3,5,6,9,10,12,15)$

(j) The ON set for the function realized by the equation for Y

$\Sigma_{A,B,C,D}(0,5,10,15)$

REDUCED EQUATION REPORT:

```
 P-Terms   Fan-in  Fan-out  Type  Name (attributes)
---------  ------  -------  ----  -----------------
   8/8        4        1    Pin   X
   4/4        4        1    Pin   Y
=========
  12/12          Best P-Term Total: 12
                       Total Pins: 6
                      Total Nodes: 0
              Average P-Term/Output: 6


Positive-Polarity Equations:

X = (!A & !B & !C & !D # A & B & !C & !D # A & !B & C & !D # !A & B & C & !D
     # A & !B & !C & D # !A & B & !C & D # !A & !B & C & D # A & B & C & D);

Y = (!A & !B & !C & !D # A & !B & C & !D # !A & B & !C & D # A & B & C & D);

Reverse-Polarity Equations:

!X = (A & !B & !C & !D # !A & B & !C & !D # !A & !B & C & !D # A & B & C & !D
     # !A & !B & !C & D # A & B & !C & D  # A & !B & C & D  # !A & B & C & D);

!Y = (A & !C  # !A & C  # B & !D # !B & D);
```

CHIP REPORT:

```
X  = (  A & B & C & D  # !A & !B & C & D # !A & B & !C & D # A & !B & !C & D
     # !A & B & C & !D # A & !B & C & !D # A & B & !C & !D # !A & !B & !C & !D);

Y  = (  A & B & C & D  # !A & B & !C & D # A & !B & C & !D # !A & !B & !C & !D );
```