Chapter 15
Differential Amplifiers and Operational Amplifier Design

Microelectronic Circuit Design

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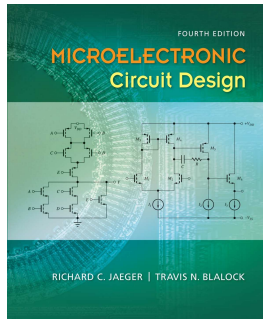
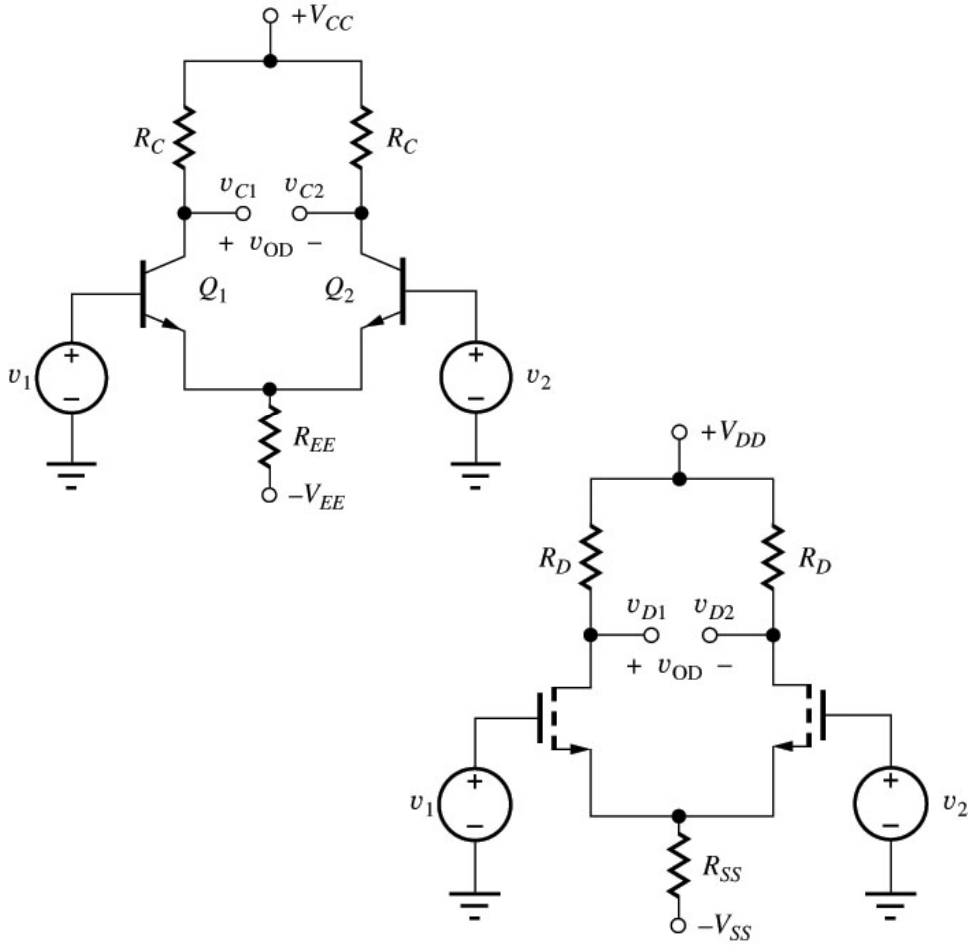


Chapter Goals

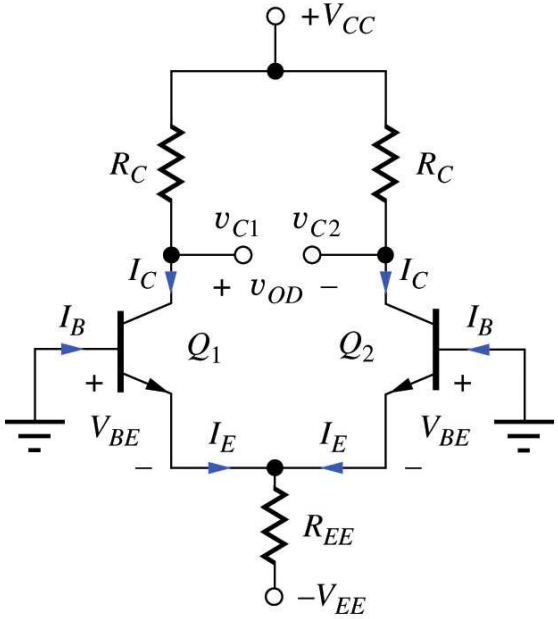
- Explore dc and ac properties of differential amplifiers.
- Understand basic three-stage op amp.
- Explore design of class-A, class-B, class-AB output stages.
- Discuss characteristics and design of electronic current sources.
- Explore high output resistance current sources.
- Design current sources for both discrete and integrated applications.
- Increase understanding of SPICE simulation techniques.

Differential Amplifiers



- Each circuit has two inputs.
- Difference of the two inputs is the *differential* input.
- Differential-mode output voltage is the voltage difference between collectors, drains of the two transistors.
- Ground referenced outputs can also be taken from collector/drain.
- Ideal differential amplifier uses perfectly matched transistors.

Bipolar Differential Amplifiers: DC Analysis



Terminal currents are also equal.

$$I_{C1} = I_{C2} = I_C$$

$$I_{E1} = I_{E2} = I_E$$

$$I_{B1} = I_{B2} = I_B$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_{EE}} \qquad I_C = \alpha_F I_E \qquad I_B = \frac{I_C}{\beta_F}$$

Both inputs are set to zero, emitters are connected together.

$$V_{C1} = V_{C2} = V_{CC} - I_C R_C \qquad V_{CE1} = V_{CE2}$$

$$\therefore V_{BE1} = V_{BE2} = V_{BE}$$

$$V_{OD} = V_{C1} - V_{C2} = 0\text{V}$$

If transistors are matched, $V_{C1} = V_{C2} = V_C$

Small-Signal Transfer Characteristic

The current switch is a digital application of the differential amplifier. Large-signal transfer characteristic of differential amplifier is given by:

$$I_{C1} - I_{C2} = 2I_C \tanh\left(\frac{v_{BE1} - v_{BE2}}{2V_T}\right) = 2I_C \tanh\left(\frac{v_{id}}{2V_T}\right)$$

$$= 2I_C\left(\left(\frac{v_{id}}{2V_T}\right) - \frac{1}{3}\left(\frac{v_{id}}{2V_T}\right)^3 + \frac{2}{15}\left(\frac{v_{id}}{2V_T}\right)^5 - \frac{17}{315}\left(\frac{v_{id}}{2V_T}\right)^7 + \ldots\right)$$

Even-order distortion terms are eliminated.This increases signal-handling capability of differential pair. For small-signal operation, linear term must be dominant. Hence, we set the third-order term to be one-tenth the linear term.

$$v_{id} \le 2V_T\sqrt{0.3} \rightarrow v_{id} \le 27\text{mV}$$

Bipolar Differential Amplifiers: DC Analysis (Example)

- **Problem:** Find Q-points of transistors in the differential amplifier.
- **Given data:** $V_{CC}=V_{EE}=15$ V, $R_{EE}=R_C=75\text{k}\Omega$, $\beta_F=100$
- **Analysis:**

$$I_E=\frac{V_{EE}-V_{BE}}{2R_{EE}}=\frac{(15-0.7)\text{V}}{2(75\times10^3)\Omega}=95.3\mu\text{A}$$

$$I_C=\alpha_F I_E=\frac{100}{101}I_E=94.4\mu\text{A}$$

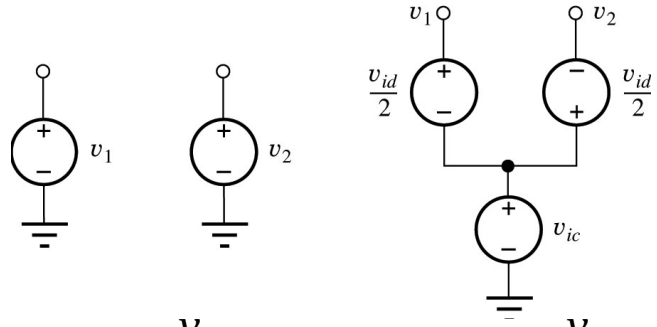
$$I_B=\frac{I_C}{\beta_F}=\frac{94.4\mu\text{A}}{100}=0.944\mu\text{A}$$

$$V_C=15-I_C R_C=7.92\text{V}$$

$$V_{CE}=V_C-V_E=7.92\text{V}\text{-}(\text{-}0.7\text{V})=8.62\text{V}$$

Due to symmetry, both transistors are biased at Q-point (94.4 μA, 8.62V)

Bipolar Differential Amplifiers: AC Analysis



$$v_1 = v_{ic} + \frac{v_{id}}{2} \qquad v_2 = v_{ic} - \frac{v_{id}}{2}$$

Circuit analysis is done by superposition of differential-mode and common-mode signal portions.

$$v_{od} = v_{c1} - v_{c2} \qquad v_{oc} = \frac{v_{c1} + v_{c2}}{2}$$

$$\begin{bmatrix} v_{od} \\ v_{oc} \end{bmatrix} = \begin{bmatrix} A_{dd} & A_{cd} \\ A_{dc} & A_{cc} \end{bmatrix} \begin{bmatrix} v_{id} \\ v_{ic} \end{bmatrix}$$

A_{dd} = differential-mode gain

A_{cd} = common-mode to differential-mode conversion gain

A_{cc} = common-mode gain

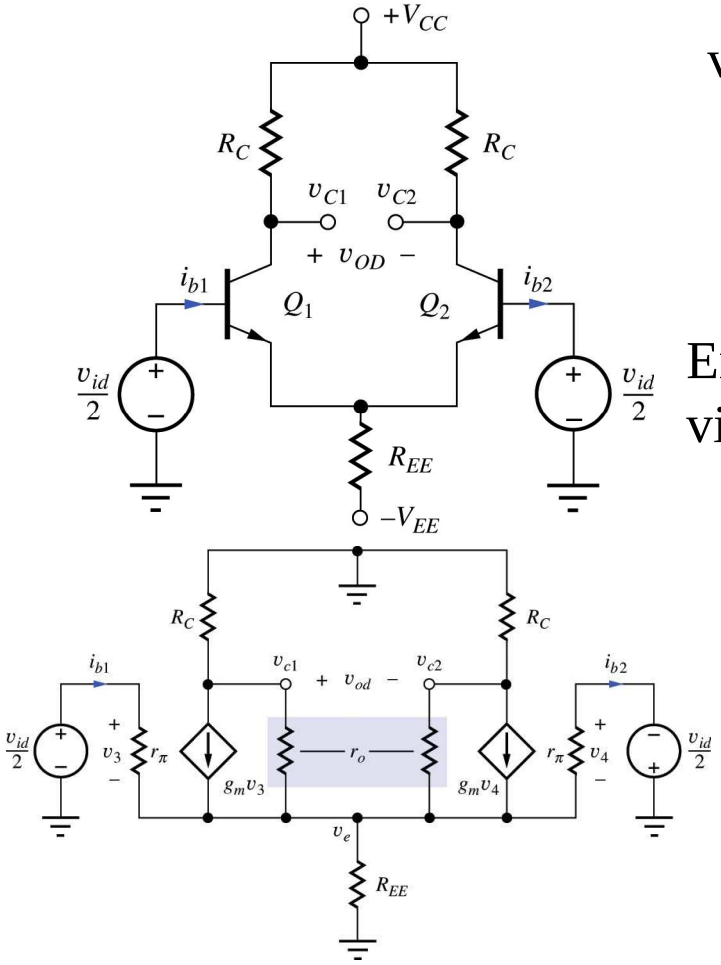
A_{dc} = differential mode to common-mode conversion gain

For ideal symmetrical amplifier, $A_{cd} = A_{dc} = 0$.

$$\therefore \begin{bmatrix} v_{od} \\ v_{oc} \end{bmatrix} = \begin{bmatrix} A_{dd} & 0 \\ 0 & A_{cc} \end{bmatrix} \begin{bmatrix} v_{id} \\ v_{ic} \end{bmatrix}$$

Purely differential-mode input gives purely differential-mode output and vice versa.

Bipolar Differential Amplifiers: Differential-mode Gain and Input Resistance



$$v_3 = \frac{v_{id}}{2} - v_e \qquad v_4 = -\frac{v_{id}}{2} - v_e$$

$$(g_m + g_\pi)(v_3 + v_4) = G_{EE} v_e$$

$$\therefore v_e (G_{EE} + 2g_\pi + 2g_m) = 0 \rightarrow v_e = 0$$

Emitter node in differential amplifier represents virtual ground for differential-mode input signals.

$$\therefore v_3 = \frac{v_{id}}{2} \qquad v_4 = -\frac{v_{id}}{2}$$

Output signal voltages are:

$$v_{c1} = -g_m R_C \frac{v_{id}}{2} \qquad v_{c2} = +g_m R_C \frac{v_{id}}{2}$$

$$\therefore v_{od} = -g_m R_C v_{id}$$

Bipolar Differential Amplifiers: Differential-mode Gain and Input Resistance (cont.)

Differential-mode gain for balanced output, $v_{od} = v_{c1} - v_{c2}$ is:

$$A_{dd} = \left.\frac{v_{od}}{v_{id}}\right|_{v_{ic}=0} = -g_m R_C$$

If either v_{c1} or v_{c2} is used alone as output, output is said to be single-ended.

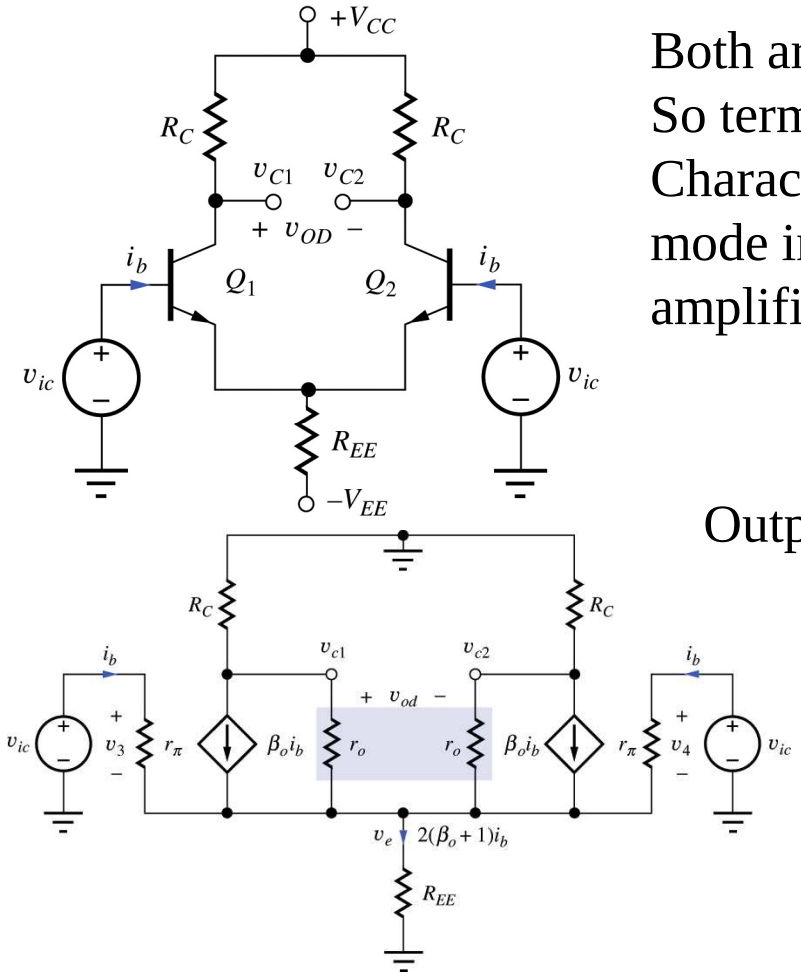
$$A_{dd1} = \left.\frac{v_{c1}}{v_{id}}\right|_{v_{ic}=0} = -\frac{g_m R_C}{2} = \frac{A_{dd}}{2} \qquad A_{dd2} = \left.\frac{v_{c2}}{v_{id}}\right|_{v_{ic}=0} = \frac{g_m R_C}{2} = -\frac{A_{dd}}{2}$$

Differential-mode input resistance is small-signal resistance presented to differential-mode input voltage between the two transistor bases.

$$i_{b1} = \frac{(v_{id}/2)}{r_\pi} \qquad \therefore R_{id} = v_{id}/i_{b1} = 2r_\pi$$

If $v_{id} = 0$, $R_{od} = 2(R_C \| r_o) \cong 2R_C$. For single-ended outputs, $R_{out} \cong R_C$

Bipolar Differential Amplifiers: Common-mode Gain and Input Resistance



Both arms of differential amplifier are symmetrical. So terminal currents and collector voltages are equal. Characteristics of differential pair with common-mode input are similar to those of a C-E (or C-S) amplifier with large emitter (or source) resistor.

$$i_b = \frac{v_{ic}}{r_\pi + 2(\beta_o + 1)R_{EE}}$$

Output voltages are:

$$v_{c1} = v_{c2} = -\beta_o i_b R_C = \frac{-\beta_o R_C}{r_\pi + 2(\beta_o + 1)R_{EE}} v_{ic}$$

$$v_e = 2(\beta_o + 1) i_b R_{EE}$$

$$= \frac{2(\beta_o + 1)R_{EE}}{r_\pi + 2(\beta_o + 1)R_{EE}} v_{ic} \cong v_{ic}$$

Bipolar Differential Amplifiers: Common-mode Gain and Input Resistance (cont.)

Common-mode gain is given by:

$$A_{cc} = \left.\frac{v_{oc}}{v_{ic}}\right|_{v_{id}=0} = -\frac{\beta_o R_C}{r_\pi + 2(\beta_o + 1)R_{EE}} \cong -\frac{R_C}{2R_{EE}} \cong \frac{V_C}{2V_{EE}}$$

For symmetrical power supplies, common-mode gain =0.5. Thus, common-mode output voltage and A_{cc} is 0 if R_{EE} is infinite. This result is obtained since output resistances of transistors are neglected. A more accurate expression is:

$$A_{cc} \cong R_C\left(\frac{1}{\beta_o r_o} - \frac{1}{2R_{EE}}\right)$$

$v_{od} = v_{c1} - v_{c2} = 0$ Therefore, common-mode conversion gain is found to be 0.

$$R_{ic} = \frac{v_{ic}}{2i_b} = \frac{r_\pi + 2(\beta_o + 1)R_{EE}}{2} = \frac{r_\pi}{2} + (\beta_o + 1)R_{EE}$$

Common-Mode Rejection ratio (CMRR)

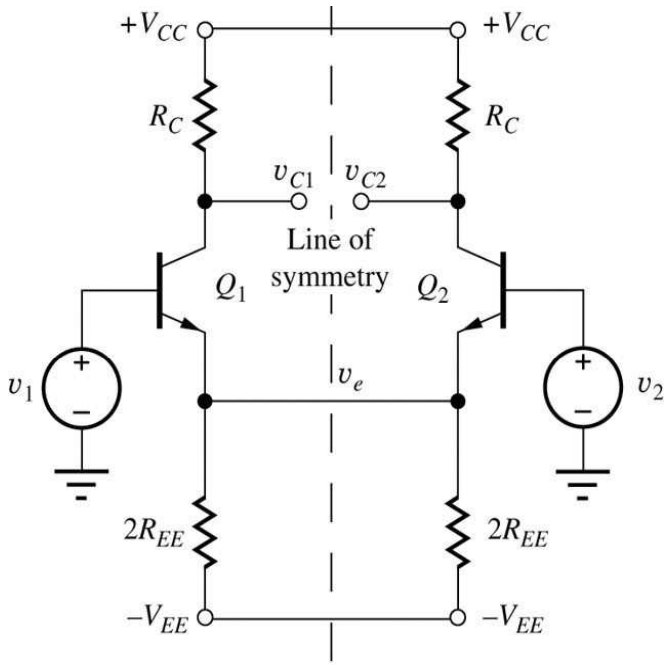
- Represents ability of amplifier to amplify desired differential-mode input signal and reject undesired common-mode input signal.
- For differential output, common-mode gain of balanced amplifier is zero, CMRR is infinite. For single-ended output,

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{A_{dd}/2}{A_{cc}}\right| = \frac{1}{2\left(\frac{1}{\beta_o \mu_f} - \frac{1}{2 g_m R_{EE}}\right)}$$

- For infinite R_{EE}, CMRR is limited by $\beta_o \mu_f$. If term containing R_{EE} is dominant $\text{CMRR} \cong g_m R_{EE} = 40 I_C R_{EE} \cong 20 V_{EE}$

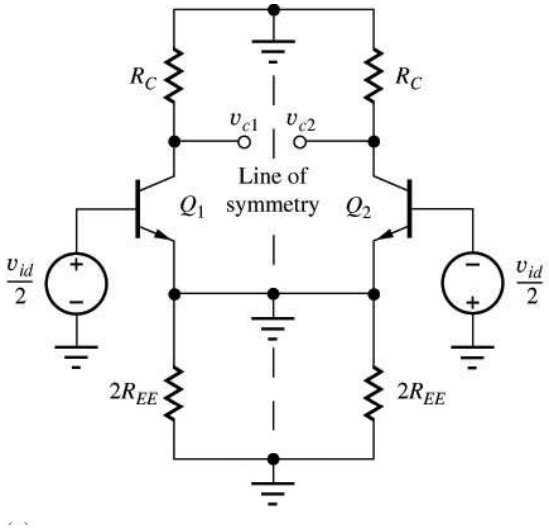
  Thus for differential pair biased by resistor R_{EE}, CMRR is limited by available negative power supply.
- Due to mismatches, $\text{CMRR} \propto g_m R_{EE}\left(\frac{\Delta g}{g}\right)$, $\frac{\Delta g}{g} = \frac{2(g_1 - g_2)}{g_1 + g_2}$ gives fractional mismatch between small-signal device parameters in the two arms of differential pair. Hence $g_m R_{EE}$ product is maximized.

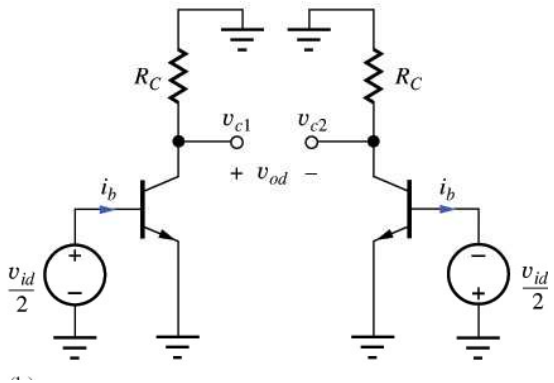
Analysis of Differential Amplifiers Using Half-Circuits



- Half-circuits are constructed by first drawing the differential amplifier in a fully symmetrical form- power supplies are split into two equal halves in parallel, emitter resistor is separated into two equal resistors in parallel.
- None of the currents or voltages in the circuit are changed.
- For differential mode signals, points on the line of symmetry are virtual grounds connected to ground for ac analysis
- For common-mode signals, points on line of symmetry are replaced by open circuits.

Bipolar Differential-mode Half-circuits





Direct analysis of the half-circuits yield:

$$v_{c1} = -g_m R_C \frac{v_{id}}{2}$$

$$v_{c2} = +g_m R_C \frac{v_{id}}{2}$$

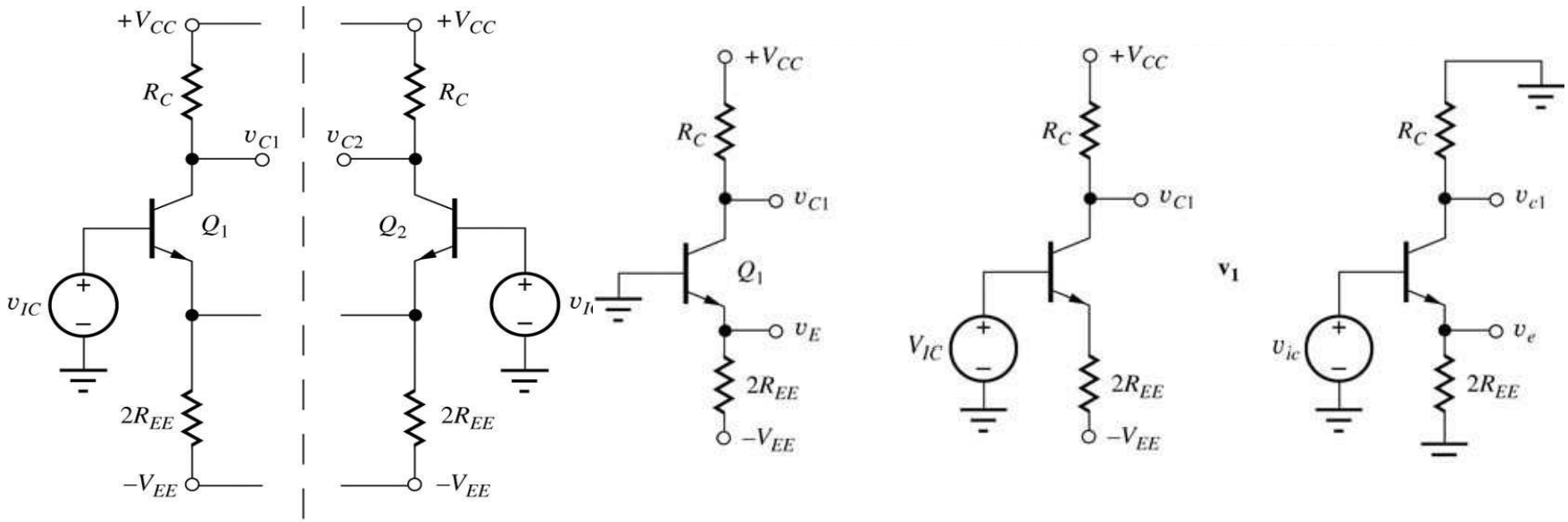
$$v_o = v_{c1} - v_{c2} = -g_m R_C v_{id}$$

$$R_{id} = v_{id}/i_{b1} = 2r_\pi$$

$$R_{od} = 2(R_C \| r_o)$$

Applying rules for drawing half-circuits, the two power supply lines and emitter become ac grounds. The half-circuit represents a C-E amplifier stage.

Bipolar Common-mode Half-circuits



- All points on line of symmetry become open circuits.
- DC circuit with V_{IC} set to zero is used to find amplifier's Q-point.
- Last circuit is used for for common-mode signal analysis and represents the C-E amplifier with emitter resistor $2R_{EE}$.

Bipolar Common-mode Input Voltage Range

$$V_{CB} = V_{CC} - I_C R_C - V_{IC} \geq 0$$

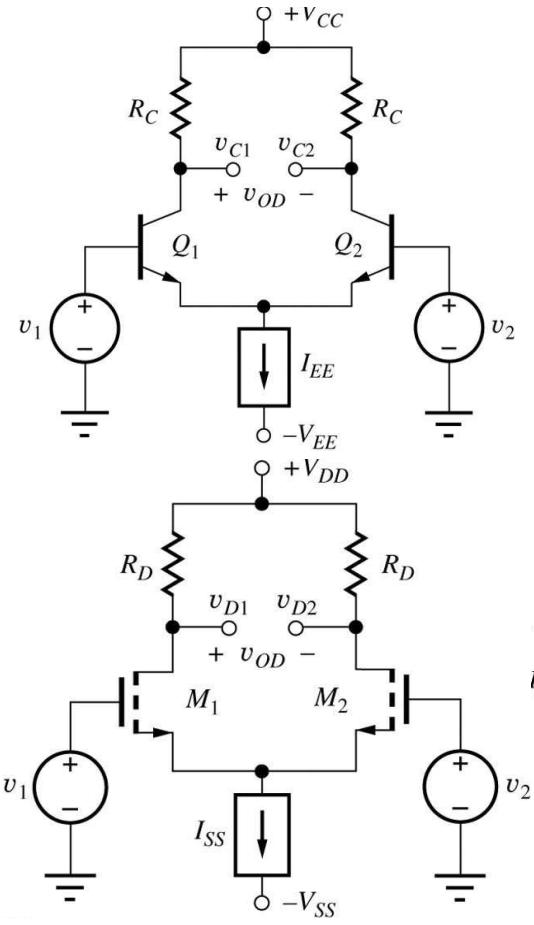
$$I_C \leq \alpha_F \frac{V_{IC} - V_{BE} + V_{EE}}{2R_{EE}}$$

$$\therefore V_{IC} \leq V_{CC} \frac{1 - \alpha_F \dfrac{R_C}{2R_{EE}} \dfrac{\left(V_{EE} - V_{BE}\right)}{V_{CC}}}{1 + \alpha_F \dfrac{R_C}{2R_{EE}}}$$

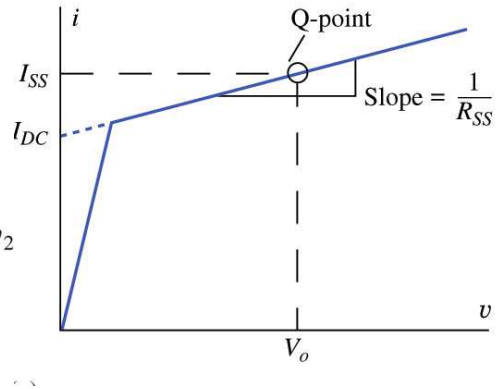
For symmetrical power supplies, $V_{EE} >> V_{BE}$, and $R_C = R_{EE}$,

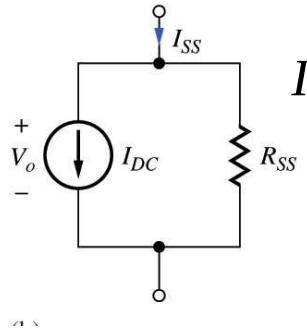
$$V_{IC} \leq \frac{V_{CC}}{3}$$

Biasing with Electronic Current Sources



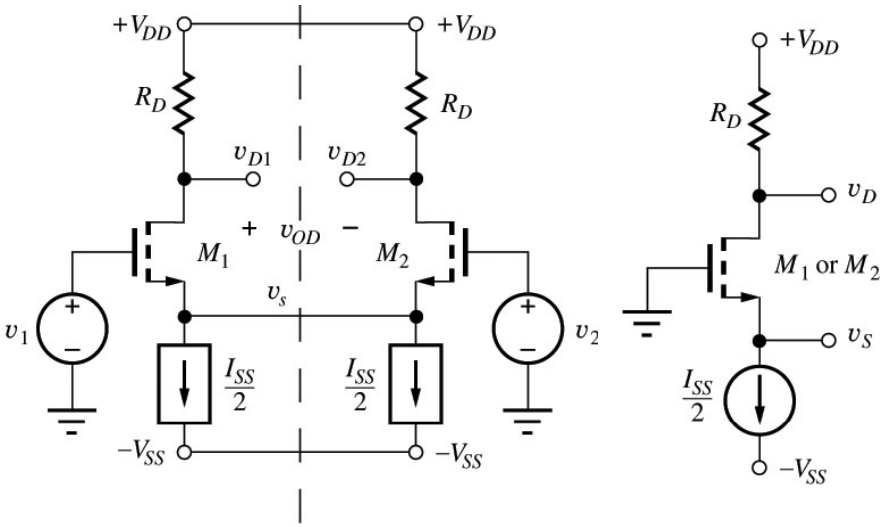
- Differential amplifiers are biased using electronic current sources to stabilize the operating point and increase effective value of R_{EE} to improve CMRR
- Electronic current source has a Q-point current of I_{SS} and an output resistance of R_{SS} as shown.
- DC model of the electronic current source is a dc current source, I_{SS} while ac model is a resistance R_{SS}. SPICE model includes both ac and dc models.





$$I_{DC} = I_{SS} - \frac{V_0}{R_{SS}}$$

MOSFET Differential Amplifiers: DC Analysis



$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2$$

$$V_{GS} = V_{TN} + \sqrt{\frac{2I_D}{K_n}} = V_{TN} + \sqrt{\frac{I_{SS}}{K_n}}$$

Op amps with MOSFET inputs have a high input resistance and much higher slew rate that those with bipolar input stages.

Using half-circuit analysis method, we see that $I_S = I_{SS}/2$.

$$V_{D1} = V_{D2} = V_{DD} - I_D R_D \quad \text{and} \quad V_o = 0$$

$$V_{DS} = V_D - V_S = V_{DD} - I_D R_D + V_{GS}$$

Small-Signal Transfer Characteristic

MOS differential amplifier gives improved linear input signal range and distortion characteristics over that of a single transistor.

$$I_{D1}-I_{D2}=\frac{K_n}{2}\left[\left(v_{GS1}-V_{TN}\right)^2-\left(v_{GS2}-V_{TN}\right)^2\right]$$

For symmetrical differential amplifier with purely differential-mode input

$$v_{GS1}=V_{GS}+\frac{v_{id}}{2} \qquad v_{GS2}=V_{GS}-\frac{v_{id}}{2}$$

$$\therefore I_{D1}-I_{D2}=K_n\left(V_{GS}-V_{TN}\right)v_{id}=g_m v_{id}$$

Second-order distortion product is eliminated and distortion is greatly reduced. However some distortion prevails as MOSFETs are nor perfect square law devices and some distortion arises through voltage dependence of output impedances of the transistors.

MOSFET Differential Amplifiers: DC Analysis (Example)

- **Problem:** Find Q-points of transistors in the differential amplifier.
- **Given data:** $V_{DD}=V_{SS}=12$ V, $I_{SS}=200$ μA, $R_{SS}=500$ kΩ, $R_D=62$ kΩ, $\lambda=0.0133\ \text{V}^{-1}$, $K_n=5\ \text{mA/V}^2$, $V_{TN}=1$V
- **Analysis:**

$$I_D=\frac{I_{SS}}{2}=100\mu\text{A}$$

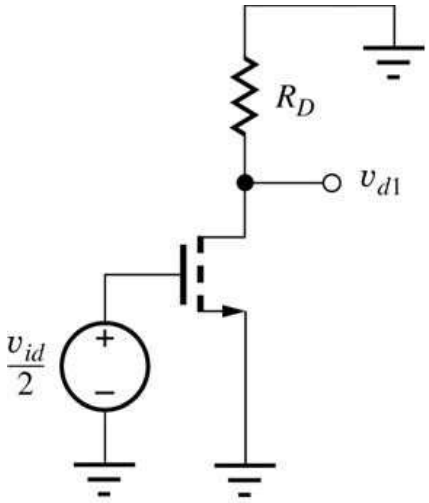
$$V_{GS}=1+\sqrt{\frac{200\mu\text{A}}{5\text{mA/V}^2}}=1.20\text{V}$$

$$V_{DS}=12\text{V}-(100\mu\text{A})(62\text{k}\Omega)+1.2\text{V}=7\text{V}$$

To maintain pinch-off operation of M_1 for nonzero V_{IC} ,

$$V_{GD}=V_{IC}-\left(V_{DD}-I_DR_D\right)\le V_{TN}$$
$$\therefore V_{IC}\le V_{DD}-I_DR_D+V_{TN}=6.8\text{V}$$

MOSFET Differential Amplifiers: Differential-mode Input Signals



Source node in differential amplifier represents virtual ground

Differential-mode gain for balanced output is

$$A_{dd} = \left.\frac{v_{od}}{v_{id}}\right|_{v_{ic}=0} = -g_m R_D$$

Gain for single-ended output is

$$A_{dd1} = \left.\frac{v_{d1}}{v_{id}}\right|_{v_{ic}=0} = -\frac{g_m R_D}{2} = \frac{A_{dd}}{2}$$

$$v_{d1} = -g_m R_D \frac{v_{id}}{2}$$

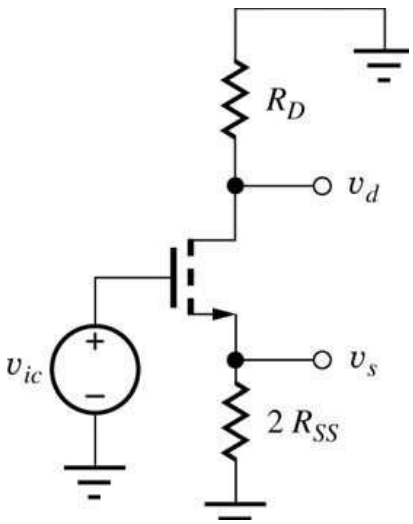
$$A_{dd2} = \left.\frac{v_{d2}}{v_{id}}\right|_{v_{ic}=0} = +\frac{g_m R_D}{2} = -\frac{A_{dd}}{2}$$

$$v_{d2} = +g_m R_D \frac{v_{id}}{2}$$

$$\therefore v_{od} = -g_m R_D v_{id}$$

$$R_{id} = \infty \qquad R_{od} = 2R_D$$

MOSFET Differential Amplifiers: Common-mode Input Signals



Electronic current source is modeled by twice its small-signal output resistance representing output resistance of the current source.

Common-mode half-circuit is similar to inverting amplifier with $2R_{SS}$ as source resistor.

$$v_{d1} = v_{d2} = \frac{-g_m R_D}{1+2g_m R_{SS}} v_{ic} \qquad v_s = \frac{2g_m R_{SS}}{1+2g_m R_{SS}} v_{ic} \cong v_{ic}$$

$v_{od} = v_{d1} - v_{d2} = 0$ Thus, common-mode conversion gain= 0

$$A_{CC} = \left.\frac{v_{oc}}{v_{ic}}\right|_{v_{id}=0} = -\frac{g_m R_D}{1+2g_m R_{SS}} \cong -\frac{R_D}{2R_{SS}}$$

Due to infinite current gain of FET, r_o can be neglected.

$$R_{ic} = \infty$$

Common-Mode Rejection ratio (CMRR)

- For purely common-mode input signal, output of balanced MOS amplifier is zero, CMRR is infinite. For single-ended output,

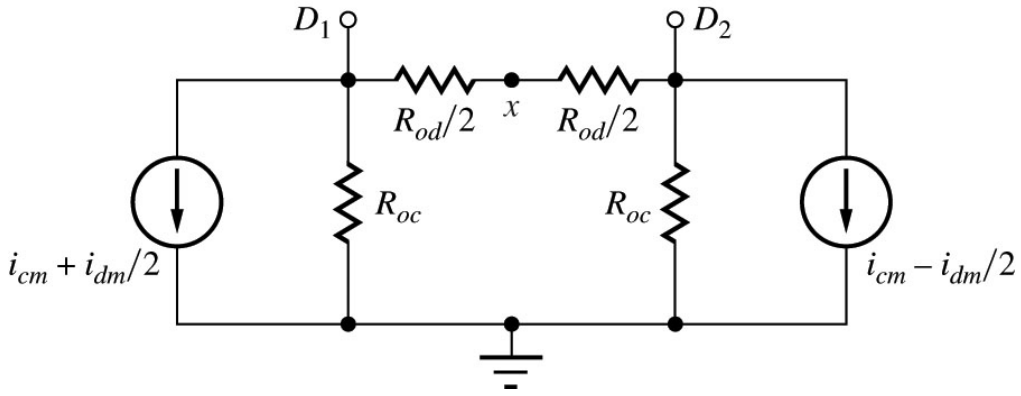
$$\text{CMRR}=\left|\frac{A_{dm}}{A_{cm}}\right|=\left|\frac{A_{dd}/2}{A_{cc}}\right|=\left|\frac{-(g_m R_D)/2}{-R_D/(2R_{SS})}\right|=g_m R_{SS}$$

- R_{SS} (which is much > R_{EE} and thus provides more Q-point stability) should be maximized.
- To compare MOS amplifier directly to BJT amplifier, assume that MOS amplifier is biased by

$$R_{SS}=\frac{V_{SS}-V_{GS}}{I_{SS}} \quad \therefore \text{CMRR}=\frac{2I_D R_{SS}}{V_{GS}-V_{TN}}=\frac{I_{SS}R_{SS}}{V_{GS}-V_{TN}}=\frac{(V_{SS}-V_{GS})}{V_{GS}-V_{TN}}$$

- From given data in example, MOS amplifier's CMRR=54 or 35 dB (almost 10 dB worse than BJT amplifier).To increase CMRR in BJT and FET amplifiers, current sources with higher R_{SS} or R_{EE} are used.

Two-port model for Differential Amplifiers



$$i_{dm} = g_m v_{dm}$$

$$i_{cm} = \frac{g_m}{1+2g_m R_{EE}} v_{cm} \cong \frac{v_{cm}}{2R_{EE}}$$

$$R_{od} = 2r_o$$

$$R_{oc} \cong 2\mu_f R_{EE}$$

Two-port model simplifies circuit analysis of differential amplifiers.

Expressions for FET are obtained by substituting R_{SS} for R_{EE}.

Differential Amplifier Design (Example)

- **Problem:** Find Q-points of transistors in the differential amplifier.
- **Given data:** A_{dm}=40 dB, R_{id} >250 kΩ, single-ended CMRR> 80 dB, V_{IC} at least ±5V, MOSFETs with: λ = 0.0133 V^{-1}, $K_{n'}$ = 50 μA/ V^2, V_{TN} =1V,

BJTs with : β_F =100, V_A =75V, I_S =0.5 fA

- **Assumptions:** Active-region operation, symmetrical power supplies, β_o = β_F, v_{id} maximum of ±30 mV.
- **Analysis:**

A_{dm}=40 dB =100. To achieve this gain with resistively loaded amplifier, we use BJT. For $A_{dm} = g_m R_C$ =40 $I_C R_C$, required gain can be obtained with voltage drop of 2.5 V across R_C.

For bipolar differential amplifier, R_{id} =2r_π, so, r_π =125 kΩ.

$$\therefore I_C \le \frac{\beta_o V_T}{r_\pi} = 20\mu\text{A}$$

Differential Amplifier Design (Example cont.)

Choose I_C = 15 μA to provide safety margin. So R_C =2.5 V/15 μA =167 kΩ.

Choose R_C = 180 kΩ as the nearest value with 5% tolerance and also to compensate for neglecting r_o in the analysis.

V_{IC} of 5V requires collector voltage to be at least 5 V at all times. We also know that v_{id} can be a maximum of ±30 mV for linearity. So ac component of differential output will not be greater than 100(0.03 V)=3V, half of which appears at each collector. Thus dc signal across R_C won't exceed 4 V(2.5 V dc + 1.5 V ac) and positive power supply must fulfill

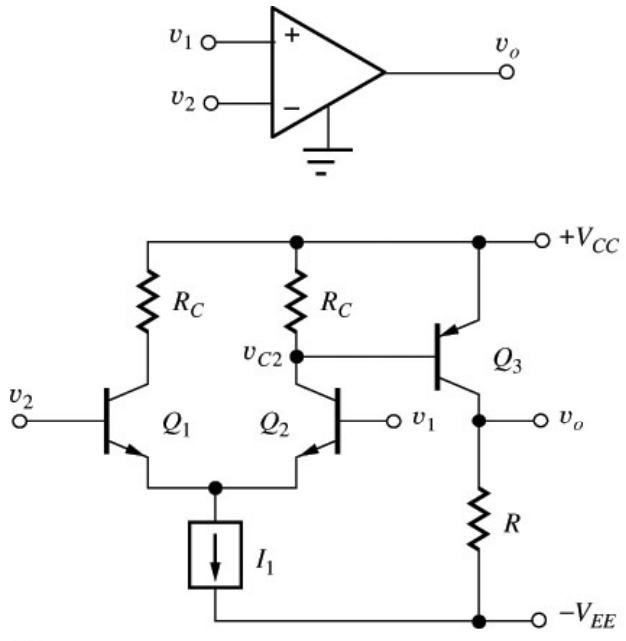
$$V_{CC} \geq V_{IC} + 4\text{V} = (5+4)\text{V} = 9\text{V}$$

Choose V_{CC} =10 V to dive desired margin of 1 V, For symmetrical supplies, V_{EE} = -10 V. Single-ended CMRR of 80 dB needs

$$R_{EE} \geq \frac{\text{CMRR}}{g_m} = \frac{10^4}{(40/\text{V})(15?\text{A})} = 16.7\text{M}\Omega$$

Choose current source with I_{EE} =30 μA and R_{EE} > 20 MΩ

Two-stage Prototype of an Op Amp

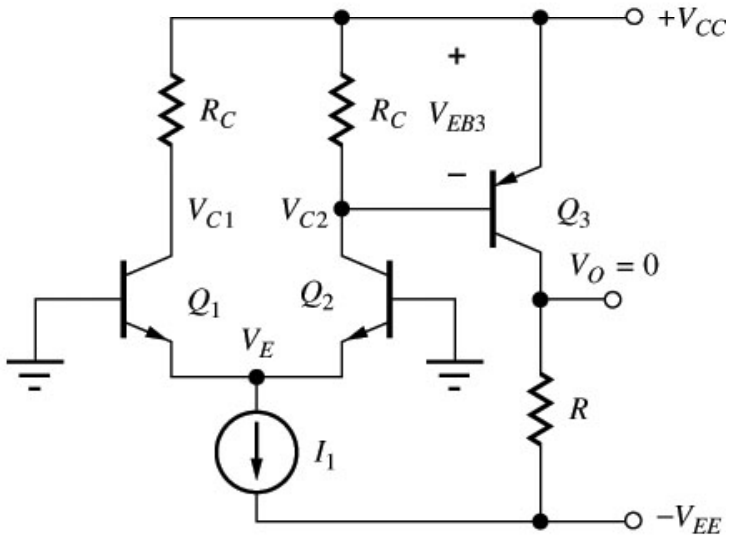


Differential amplifier provides desired differential input,CMRR and ground referenced output as the input stage of op amp.

- For higher gain, *pnp* C-E amplifier is connected at output of the input stage differential amplifier.
- Virtual ground at emitter node allows input stage to achieve full inverting amplifier gain without needing emitter bypass capacitor.
- *PNP* transistor permits direct coupling between stages, allows emitter of *pnp* to be connected to ac ground and provides required voltage level shift to bring output back to zero.
- Bypass and coupling capacitors are thus eliminated.

Two-stage Op Amp: DC Analysis

This circuit requires a resistance in series with emitter of Q_3 to stabilize Q-point (as collector current of Q_3 is exponentially dependent on base-emitter voltage), at the expense of voltage gain loss.



From dc equivalent circuit, $I_{E1} = I_{E2} = I_1/2$. If base current of Q_3 is neglected and C-B current gains are one,

$$V_{CE1} \cong V_{CE2} \cong V_{CC} - \frac{I_1 R_C}{2} + V_{BE}$$

As both inputs are zero, output also=0

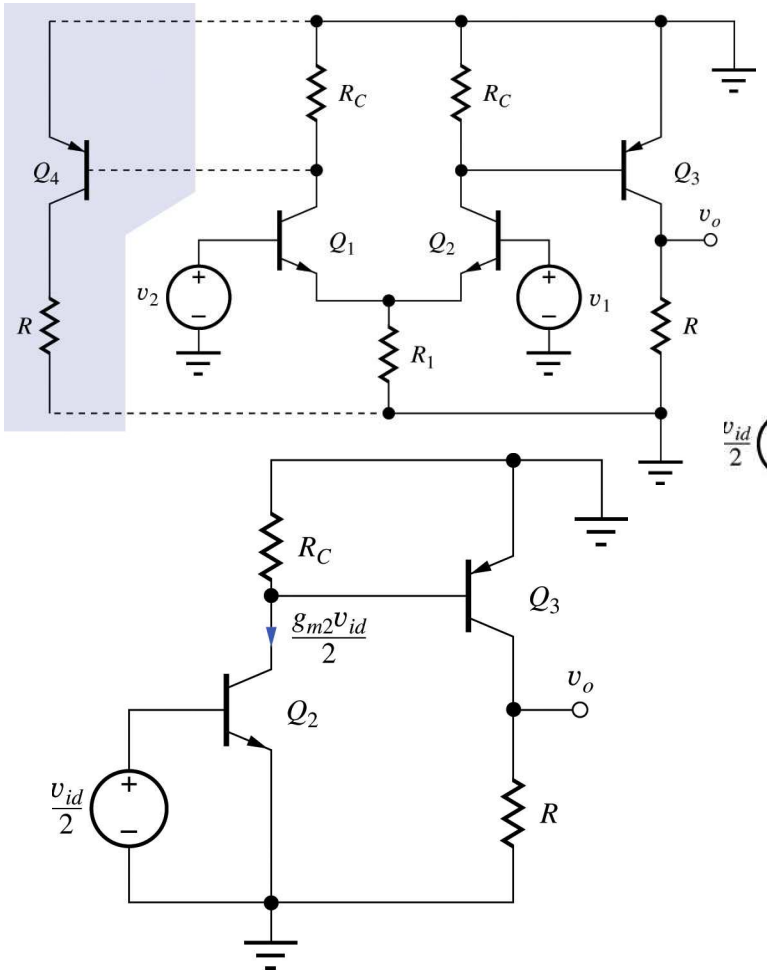
$$I_{C3} = V_{EE}/R \qquad V_{EC3} = V_{CC}$$

$$V_{EB3} = V_T \ln\left(1 + \frac{I_{C3}}{I_{S3}}\right)$$

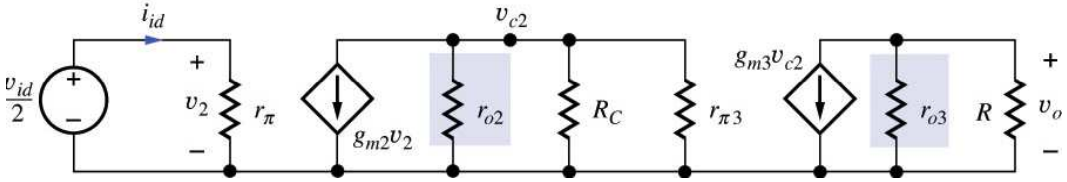
I_{S3} is saturation current. For zero offset voltage

$$R_C = \frac{V_T}{\left(\alpha_{F2}\frac{I_1}{2} - \frac{I_{C3}}{\beta_{F3}}\right)} \ln\left(1 + \frac{I_{C3}}{I_{S3}}\right)$$

Two-stage Op Amp: AC Analysis (Differential Mode)



Half-circuit can be constructed from ac equivalent circuit in spite of asymmetry, as voltage variations at collector of Q_2 don't substantially alter transistor current in forward-active operation region.



From small-signal circuit model,

$$A_{vt1} = \frac{v_{c2}}{v_{id}} = -\frac{g_{m2}}{2} R_{L1} = -\frac{g_{m2}}{2}(R_C \| r_{\pi 3})$$

$$A_{vt2} = \frac{v_o}{v_{c2}} = -g_{m3} R$$

Two-stage Op Amp: AC Analysis (Differential Mode cont.)

$$A_{dm}=\frac{v_o}{v_{id}}=\frac{v_{c2}}{v_{id}}\frac{v_o}{v_{c2}}=A_{vt1}A_{vt2}=-\frac{g_{m2}}{2}(R_C\|r_{\pi 3})(-g_{m3}R)=\frac{g_{m2}R_C}{2}\frac{\beta_{o3}R}{R_C+r_{\pi 3}}$$

This can be rewritten as

$$A_{dm}=\frac{1}{2}\frac{\left(g_{m2}R_C\right)\beta_{o3}R\left(g_{m3}R\right)}{g_{m3}R_C+\beta_{o3}}=\frac{1}{2}\frac{\left(40I_{C2}R_C\right)\beta_{o3}\left(40I_{C3}R\right)}{40\frac{I_{C3}}{I_{C2}}I_{C2}R_C+\beta_{o3}}$$

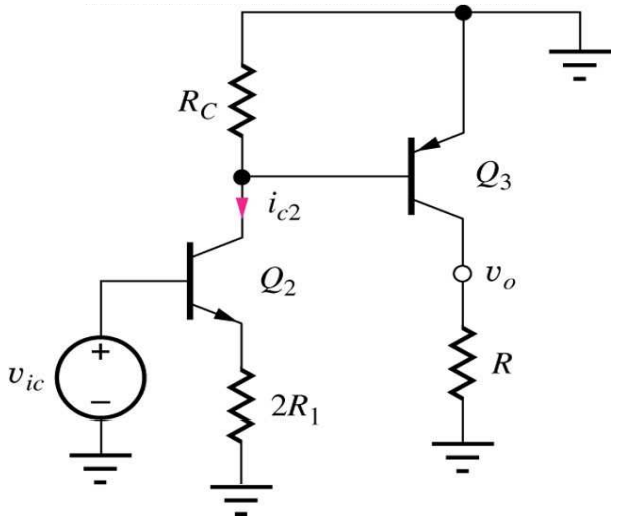
Base current of Q_3 is neglected so, $I_{C2}R_C=V_{BE3}=0.7$ V, $I_{C3}R=V_{EE}$,

$$\therefore A_{dm}=\frac{560V_{EE}}{1+\frac{28}{\beta_{o3}}\left(\frac{I_{C3}}{I_{C2}}\right)}$$

Upper limit on I_{C2} and I_1 is set by maximum dc bias current at input, lower limit on I_{C3} is set by minimum current to drive total load impedance at output.

$$R_{id}=v_{id}/i_{id}=2r_{\pi 2}=2r_{\pi 1}\qquad R_{out}=R\|r_{o3}\cong R$$

Two-stage Op Amp: AC Analysis (Common Mode)



From ac equivalent circuit, we observe that circuitry beyond collector of Q_2 is same as that in differential mode half-circuit. The difference in collector currents causes difference in output voltage.

From ac equivalent circuit for common-mode inputs,

$$i_{c2} = \frac{\beta_{o2} v_{ic}}{r_{\pi 2} + 2(\beta_{o2}+1)R_1} = \frac{g_{m2} v_{ic}}{1 + 2\frac{g_{m2}}{\alpha_{o2}} R_1} \cong \frac{g_{m2} v_{ic}}{1 + 2 g_{m2} R_1}$$

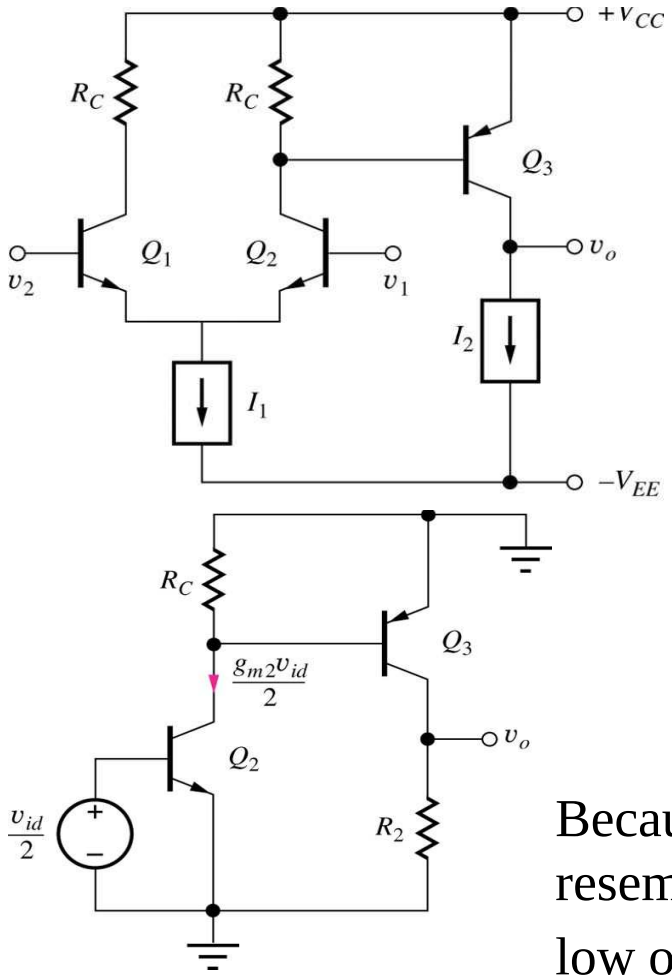
For differential-mode inputs, collector current was $i_{c2} = \frac{g_{m2}}{2} v_{id}$

Thus,

$$\frac{g_{m2} R_C}{1 + 2 g_{m2} R_1} \frac{\beta_{o3} R}{R_C + r_{\pi 3}} = \frac{2 A_{dm}}{1 + 2 g_{m2} R_1}$$

$$\text{CMRR} = \left| \frac{A_{dm}}{A_{cm}} \right| = \frac{1 + 2 g_{m2} R_1}{2} \cong g_{m2} R_1$$

Improving Op Amp Voltage Gain



Overall amplifier gain decreases rapidly as the quiescent current of second stage decreases. Voltage gain can improve if resistor in second stage is replaced by current source with $R_2 >> r_{o3}$, if R_2 is neglected,

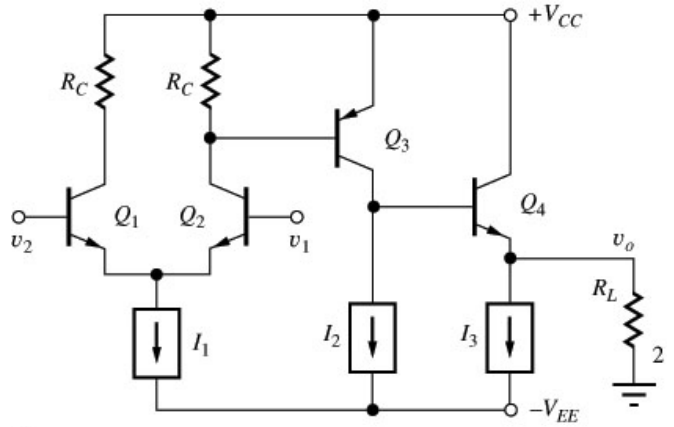
$$A_{dm} = A_{vt1}A_{vt2} = -\frac{g_{m2}}{2}(R_C \| r_{\pi 3})(-g_{m3}r_{o3})$$

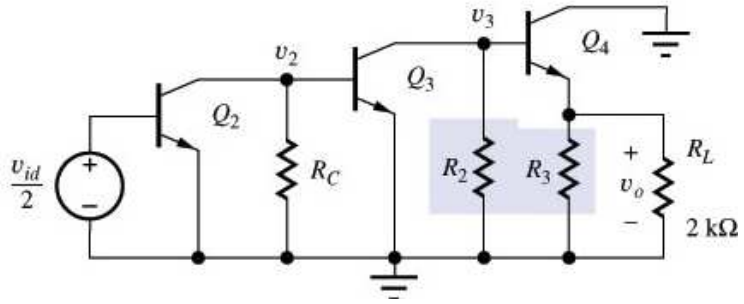
This expression can be reduced to

$$\therefore A_{dm} \cong \frac{560V}{1+\frac{28}{\beta_{o3}}\left(\frac{I_{C3}}{I_{C2}}\right)} \qquad R_{out} = R_2 \| r_{o3} \cong r_{o3}$$

Because of the high output resistance the amplifier resembles a transconductance amplifier more than a true low output resistance voltage amplifier.

Reducing Output Resistance





A C-C stage is added to the prototype to maintain voltage gain but reduce output resistance.

From ac equivalent circuit,

$$A_{v1} = -\frac{g_{m2}}{2}(R_C \| r_{\pi 3})$$

$$A_{v2} = -g_{m3}(r_{o3} \| R_{in}^{CC}) \qquad R_{in}^{CC} = r_{\pi 4} + (\beta_{o4}+1)R_L$$

$$A_{v3} = \frac{(\beta_{o4}+1)R_L}{r_{\pi 4} + (\beta_{o4}+1)R_L} \cong 1$$

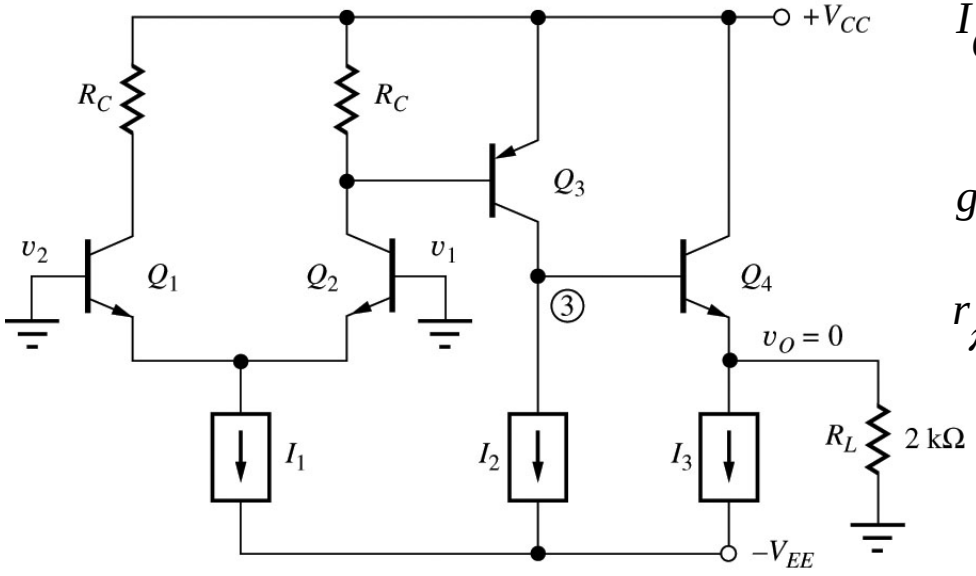
$$A_{dm} = \frac{v_2}{v_{id}}\frac{v_3}{v_2}\frac{v_o}{v_3} = A_{vt1}A_{vt2}A_{vt3} \qquad R_{id} = 2r_{\pi 2}$$

$$R_{out} = \frac{1}{g_{m4}} + \frac{R_{th4}}{\beta_{o4}+1} = \frac{1}{g_{m4}} + \frac{r_{o3}}{\beta_{o4}+1}$$

$$= \frac{1}{g_{m4}}\left(1 + \frac{\mu_{f3}}{\beta_{o4}+1}\frac{I_{C4}}{I_{C3}}\right)$$

Three-Stage Bipolar Op Amp Analysis

- **Problem:** Find differential-mode gain, CMRR, input and output resistances.
- **Given data:** V_{CC}=V_{EE}=15 V, $\beta_{o1} = \beta_{o2} = \beta_{o3} = \beta_{o4}$ =100, V_{A3} =75V, I_1 = 100 μA, I_2 = 500 μA, I_3 = 5 mA, R_1 = 750 kΩ , R_L = 2 kΩ, R_2 and R_3 are infinite.
- **Analysis:**



$$g_{m2} = 40 I_{C2} = 40(\alpha_{F2} I_{E2}) = 1.98\,\text{mS}$$

$$I_{C3} = I_2 + I_{B4} = I_2 + \frac{I_{E4}}{\beta_{F4}+1} = I_2 + \frac{I_3}{\beta_{F4}+1}$$

$$= 550\,\mu\text{A}$$

$$g_{m3} = 40 I_{C3} = 2.2\times10^{-2}\,\text{S}$$

$$r_{\pi 3} = \frac{\beta_{o3}}{g_{m3}} = 4.55\,\text{k}\Omega$$

Voltage at node 3 is one base-emitter voltage drop above zero. V_{EC3}=15-0.7=14.3 V.

Three-Stage Bipolar Op Amp Analysis (cont.)

$$r_{o3}=\frac{V_{A3}+V_{EC3}}{I_{C3}}=162\text{k}\Omega$$

$$I_{C4}=\alpha_{F4}I_{E4}=4.95\text{mA}$$

$$r_{\pi 4}=\frac{\beta_{o4}V_T}{I_{C4}}=505\Omega$$

$$R_C=\frac{V_{EB3}}{I_{C2}-\frac{I_{C3}}{\beta_{F3}}}=15.9\text{k}\Omega$$

$$A_{v1}=-\frac{g_{m2}}{2}(R_C\|r_{\pi 3})=-3.50$$

$$A_{v2}=-g_{m3}\left(r_{o3}\|(r_{\pi 4}+(\beta_{o4}+1)R_L)\right)=-1980$$

$$A_{v3}=\frac{(\beta_{o4}+1)R_L}{r_{\pi 4}+(\beta_{o4}+1)R_L}=0.998\cong 1$$

$$A_{dm}=A_{vt1}A_{vt2}A_{vt3}=6920$$

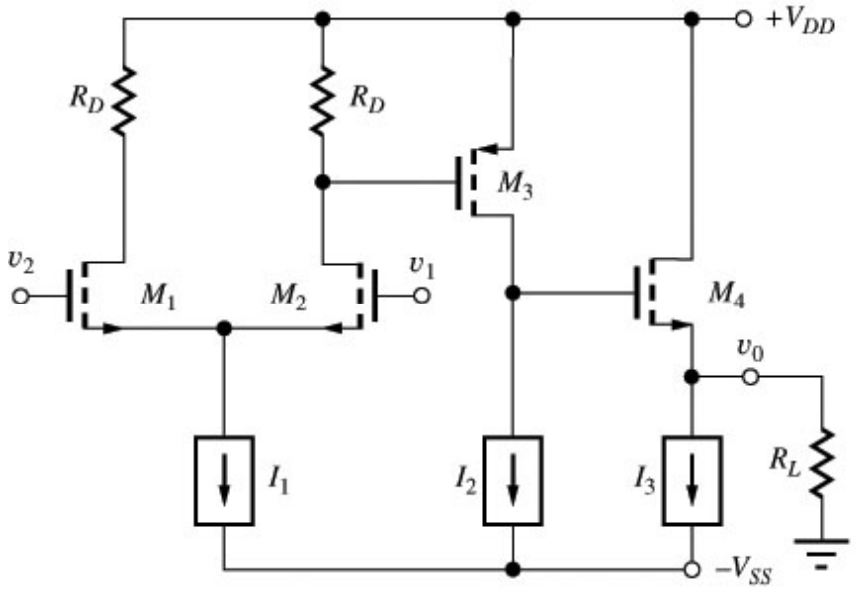
$$R_{id}=2r_{\pi 2}=101\text{k}\Omega$$

$$R_{out}=\frac{1}{g_{m4}}+\frac{r_{o3}}{\beta_{o4}}=1.62\text{k}\Omega$$

$$\text{CMRR}=g_{m2}R_1=1490=63.5\text{dB}$$

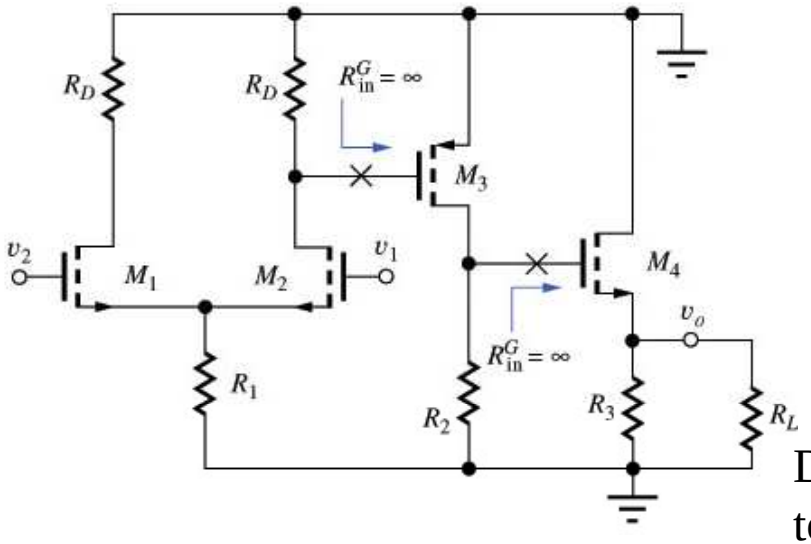
Overall gain is lower because of lower gain of first stage (since $r_{\pi 3} << R_C$) and lower gain than expected for second stage (as reflected loading of R_L is of same order as r_{o3}).

CMOS Op Amp Prototype: Circuit



- Differential amplifier (M_1 and M_2) followed by C-S stage M_3 and source follower M_4.
- Current sources are used to bias differential input and source follower stages and as load for M_3.

CMOS Op Amp Prototype: AC Analysis



$$A_{dm} = A_{vt1}A_{vt2}(1) = \mu_{f3}\left(\frac{V_{GS3}}{V_{GS2} - V_{TN2}}\right)$$

$$= \frac{1}{\lambda_3}\sqrt{\frac{K_{n2}}{I_{D2}}\frac{K_{p3}}{I_{D3}}}\left(\sqrt{\frac{2I_{D3}}{K_{p3}}} - V_{TP3}\right)$$

Design freedom is higher than in bipolar case due to Q-point dependence of μ_f. Operating currents should be reduced and M_3 should have small λ to achieve higher gain. Input bias current doesn't restrict I_{D1} as I_G =0.

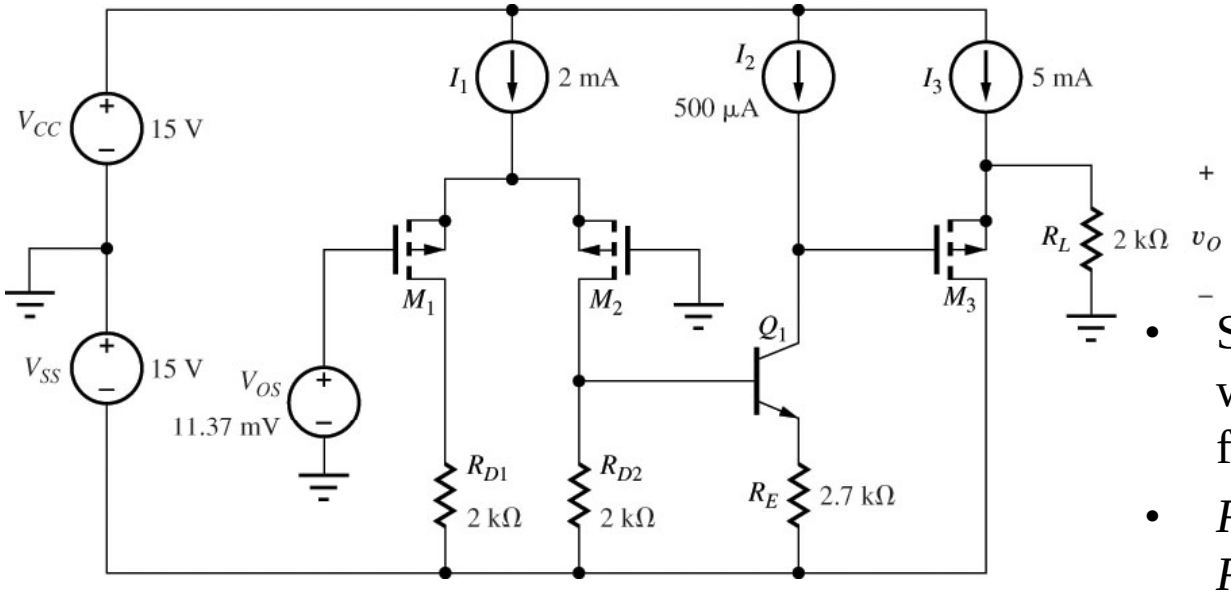
$$A_{dm} = A_{vt1}A_{vt2}A_{vt3} =$$

$$= \mu_{f3}\left(\frac{g_{m2}}{2}R_D\right)\left(\frac{g_{m4}R_L}{1 + g_{m4}R_L}\right)$$

$$R_{id} = \infty \qquad R_{out} = \frac{1}{g_{m4}} \| R_3$$

Since source follower has unity gain, $\quad \text{CMRR} = g_{m2}R_1$

BiCMOS Amplifiers



- Integrated circuit processes with both BJT and MOS transistors or bipolar transistors and JFETs are called BiCMOS and BiFET technologies respectively.
- Input PMOS transistors give high input resistance, can be biased at relatively high input currents, which can improve slew rate.

- Second gain stage uses BJT with superior amplification factor than FET.
- R_E increases voltage across R_{D2} and hence the voltage gain of first stage without reducing amplification factor of Q_1.
- Follower stage uses another FET to maximize second-stage gain while maintaining reasonable output resistance.

Op Amp Output Stages

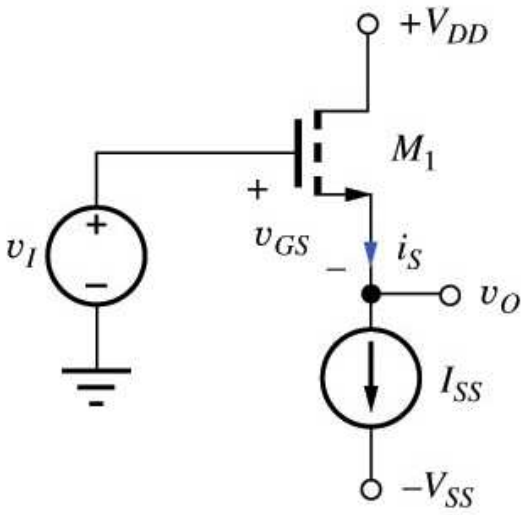
- Output stage is designed to provide low output resistance and relatively high current drive capability.
- Followers: Class-A amplifiers- transistors conduct during full 360^0 of signal waveform, conduction angle $=360^0$.
- Push-pull: Class-B- each of the two transistors conducts during $180^0$of signal wavefrom, conduction angle $=180^0$.
- Class-AB: Characteristics of Class-A and Class-B are combined, most commonly used as output stage in op amps.

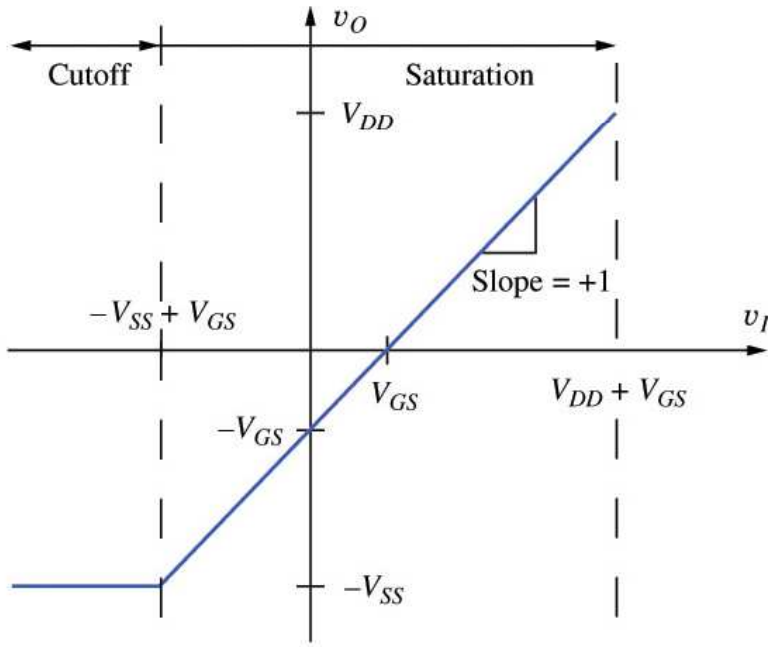
Source-Follower: Class-A Output Stage

For a source-follower,difference between input and output voltages is fixed and voltage transfer characteristic is as shown. If load resistor is connected to output, total source current:

$$i_S = I_{SS} + \frac{v_o}{R_L} > 0$$

$v_{MIN} = -I_{SS} R_L$ and i_S=0, M_1cuts off when $v_I = -I_{SS} R_L + V_{TN}$.





Source-Follower: Class-A Output Stage

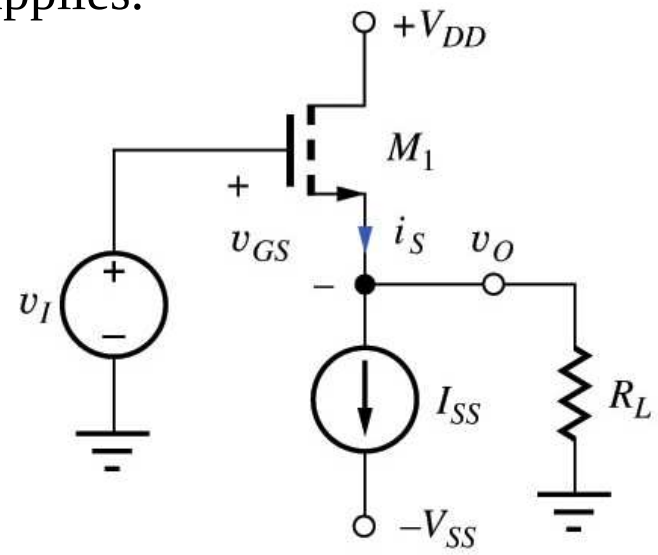
If output signal is given by:

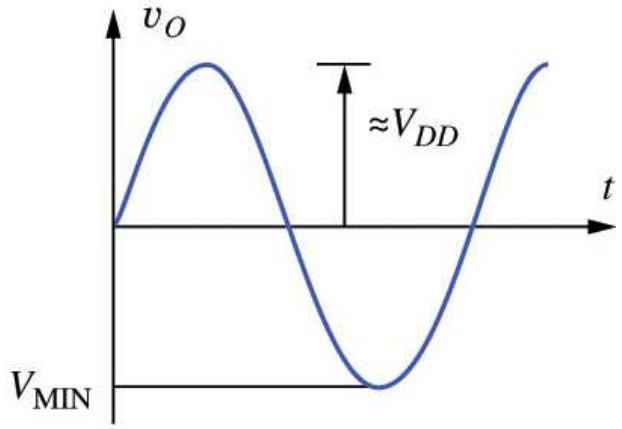
$$v_o \cong V_{DD} \sin \omega t$$

Efficiency of amplifier is given by:

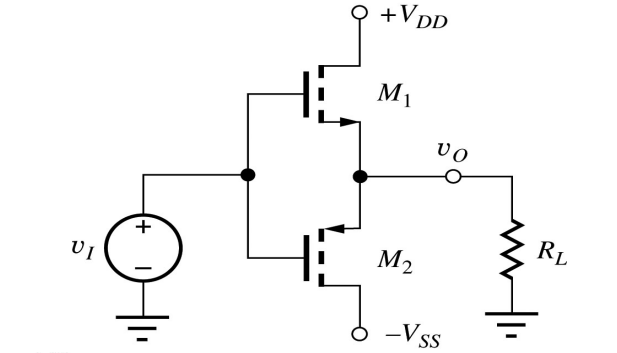
$$\zeta = \frac{P_{ac}}{P_{av}} = \frac{\frac{V_{DD}^2}{2R_L}}{2I_{SS}V_{DD}} = 25\%$$

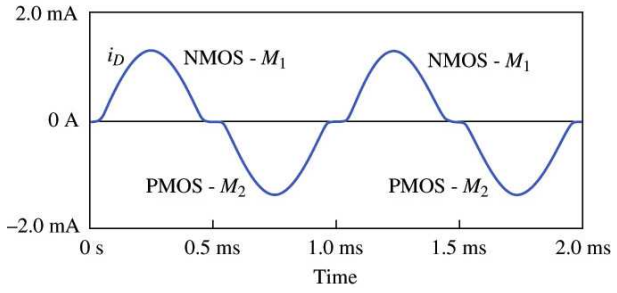
Low efficiency is due to current I_{SS} that constantly flows between the two supplies.





Class-B Push-Pull Output Stage





Improve efficiency by operating transistors at zero Q-point current eliminating quiescent power dissipation. NMOS transistor is a source-follower for positive input signals and NMOS transistor is a source-follower for negative input signals.

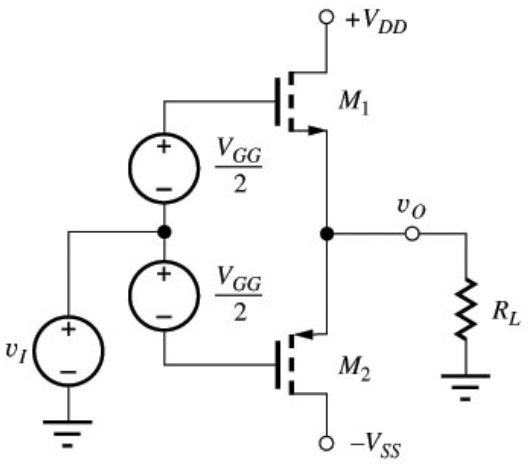
$$\zeta = \frac{P_{ac}}{P_{av}} = \frac{\frac{V_{DD}^2}{2R_L}}{2\frac{V_{DD}^2}{\pi R_L}} = 78.5\%$$

Since neither transistor conducts when,

$$V_{TP} \le v_{GS} \le V_{TN}$$

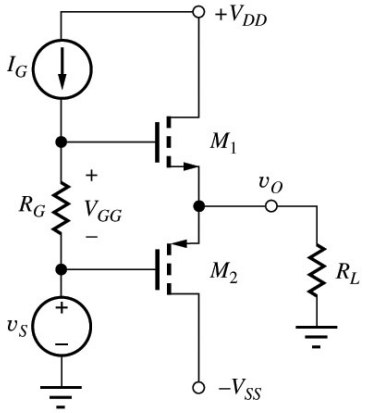
output waveform suffers from a dead-zone or crossover distortion.

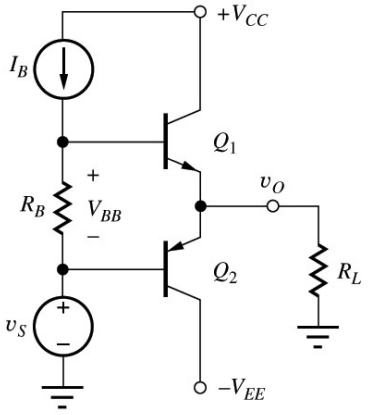
Class-AB Amplifiers



Benefits of Class-B amplifier can be maintained without dead zone by biasing transistors into conduction but at a low quiescent current level (<< peak ac current delivered to load). For each transistor, 180^0< conduction angle <360^0.

The required bias voltage can be developed as shown.We assume that bias voltage splits equally between gate-source(or base-drain) terminals.

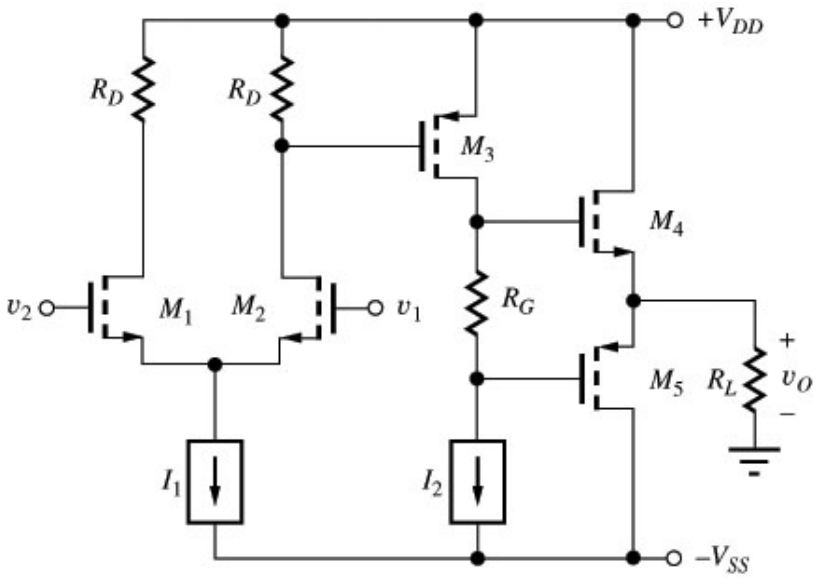


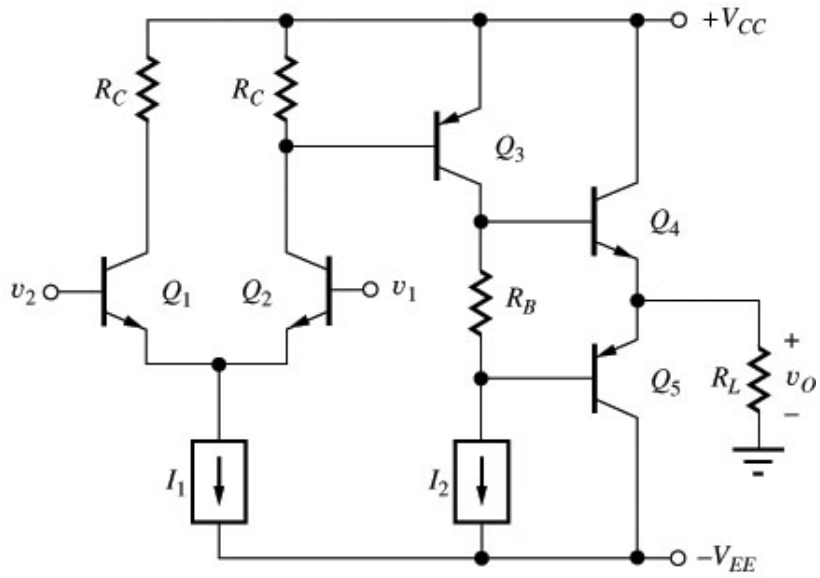


Currents are given by

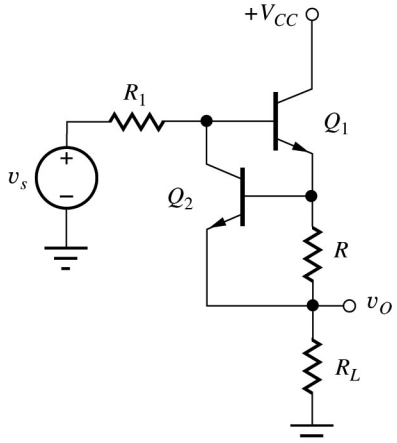
$$I_D = \frac{K_n}{2}\left(\frac{V_{GG}}{2} - V_{TN}\right)^2 \qquad I_C = I_S \exp\left(\frac{I_B R_B}{2V_T}\right)$$

Class-AB Output Stages for Op Amps



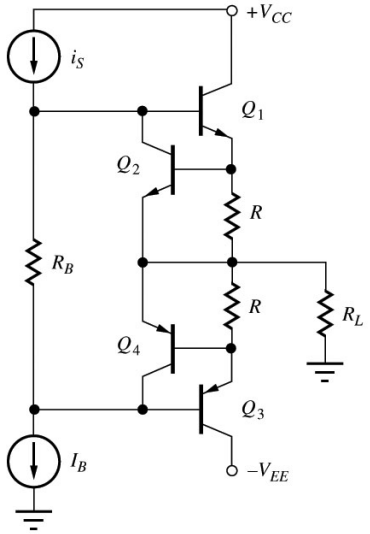


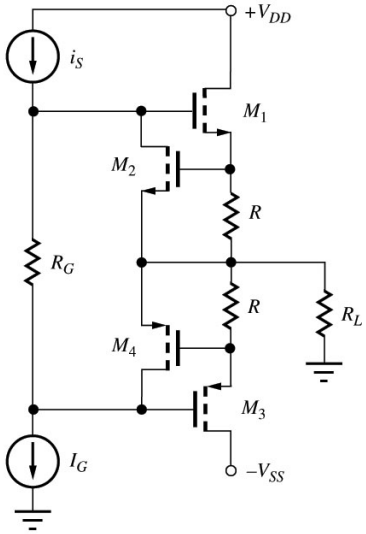
Short-Circuit Protection



High current, high power dissipation or direct destruction of base-emitter junction can destroy the BJT if output of a follower circuit is accidentally shorted to ground. Q_2 is added to protect the emitter follower.

Normally, voltage across R is <0.7 V, Q_2 is cutoff. Q_2 turns on to shunt extra current away from base of Q_1. I_{E1} is limited to $I_{E1} = V_{BE2}/R = 0.7/R$

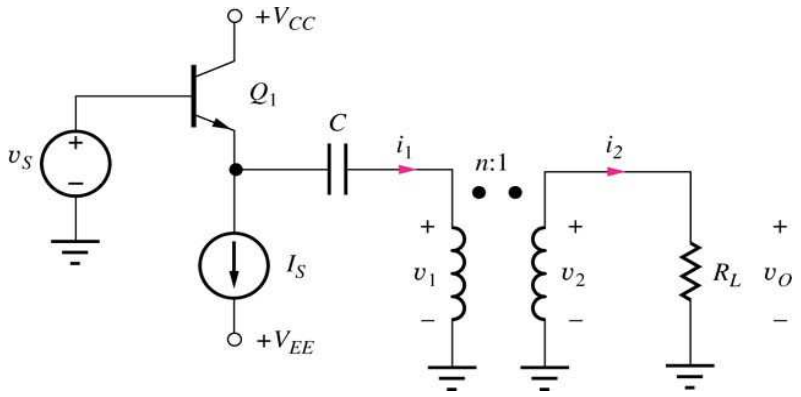




For complementary output stage, similar current-limiting circuitry is used. In MOSFET complementary output stages, output current is limited to

$$I_{S1} = \frac{V_{GS2}}{R} = \frac{V_{TN2} + \sqrt{2I_G/K_{n2}}}{R}$$

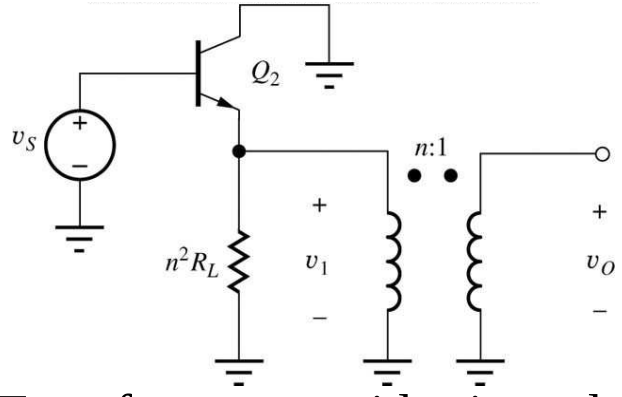
Transformer Coupling: Follower



Transformer coupling is used in amplifiers to achieve high voltage gain and efficiency while delivering power to low impedance loads.

Coupling capacitor blocks dc path through primary of transformer.

$$v_1 = n v_2 \qquad i_2 = n i_1 \qquad \therefore Z_1 = n^2 Z_L$$

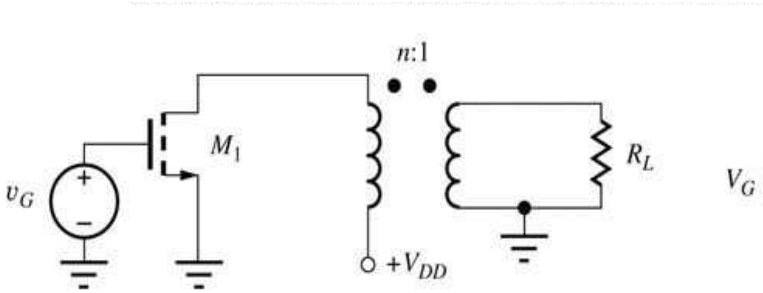


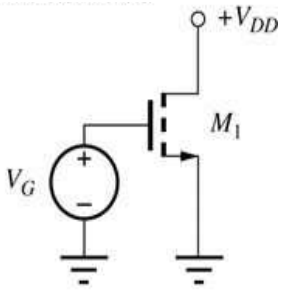
Transformer provides impedance transformation by n^2 . From ac equivalent circuit,transistor must drive $R_{EQ} = n^2 R_L$

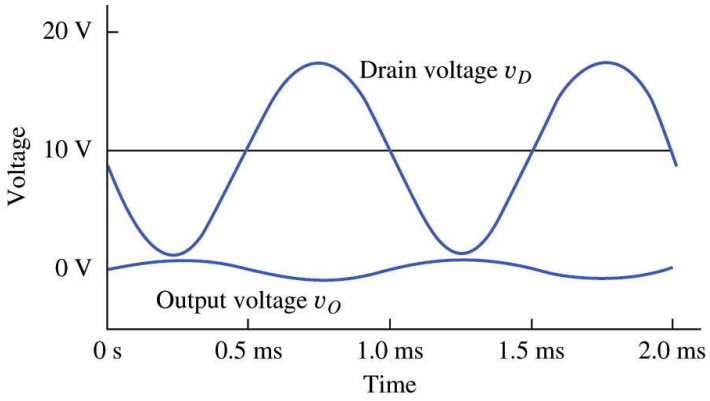
$$v_o = \frac{v_1}{n}$$

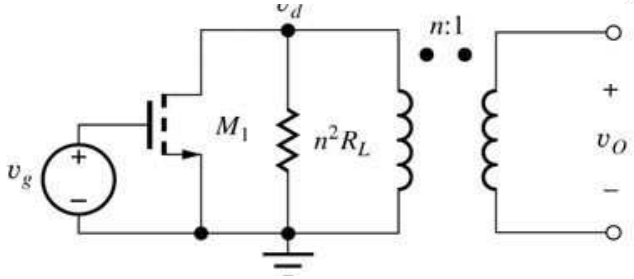
Transformer restricts operation to frequencies >dc.

Transformer Coupling: Inverting Amplifier and Class-B Output Stage



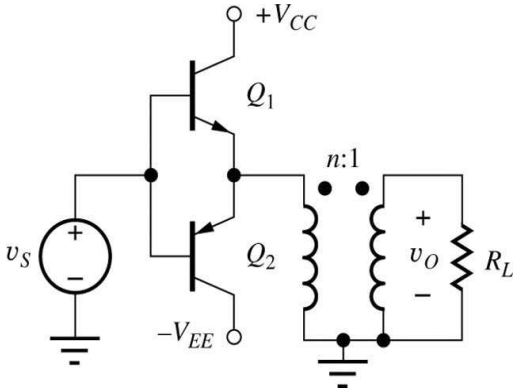






Inductance permits signal voltage to swing symmetrically above and below V_{DD}.

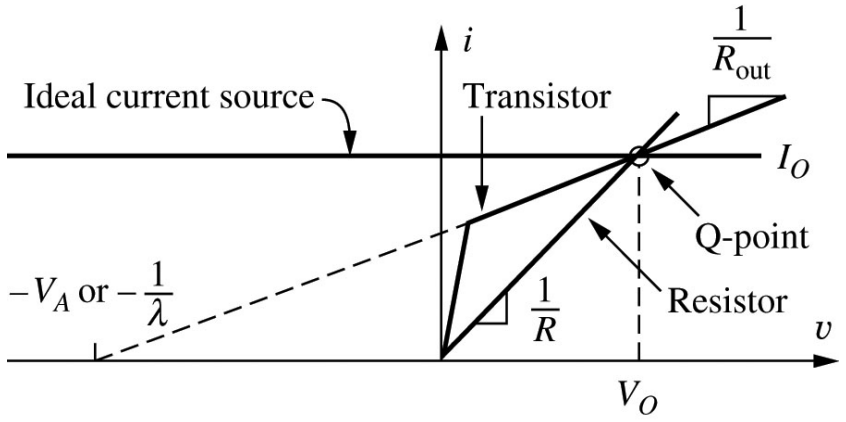
At dc, transformer is a short circuit, quiescent operating current is supplied through transformer primary. At signal frequency load n^2R_L is presented to transistor.

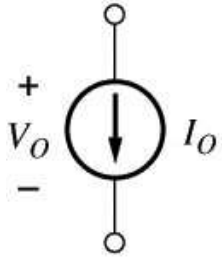


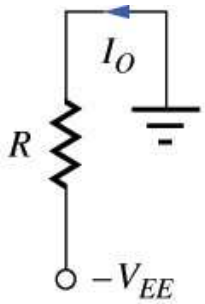
As both quiescent operating currents = 0, emitters can be directly connected to transformer primary.

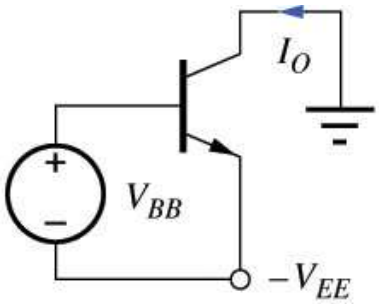
Electronic Current Sources: Introduction

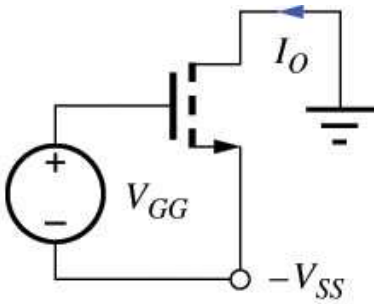
- Current through ideal current source is independent of voltage across its terminals and the output resistance is infinite.
- In electronic current sources, current depends on voltage across the terminals and they have a finite output resistance.
- Single-transistor current sources operate in only one quadrant of *i-v* space but realize very high output resistances.











Current Sources: Figure of Merit

$$V_{CS} = I_o R_{out}$$

is used as a figure of merit for comparing different current sources.

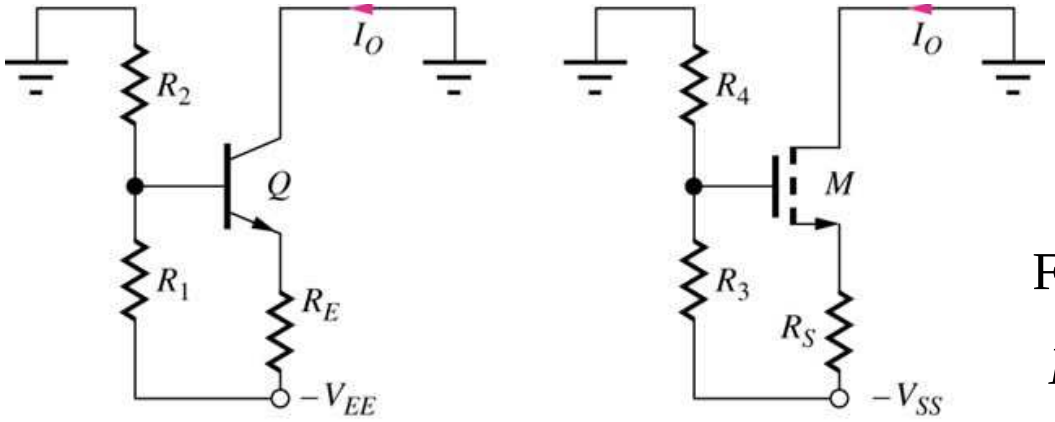
For a given Q-point current, V_{CS} represents the equivalent voltage that will be needed across a resistor to achieve same output resistance as given current source.

For resistor: $$V_{CS} = I_o R_{out} = \frac{V_{EE}}{R} R = V_{EE}$$

For BJT: $$V_{CS} = I_o R_{out} = I_C r_o = I_C \frac{V_A + V_{CE}}{I_C} = V_A + V_{CE} \cong V_A$$

For MOSFET: $$V_{CS} = I_o R_{out} = I_D r_o = I_D \frac{\frac{1}{\lambda} + V_{DS}}{I_D} = \frac{1}{\lambda} + V_{DS} \cong \frac{1}{\lambda}$$

Higher Output Resistance Sources



Output resistance of the current source can be increased by placing a resistor in series with the emitter or source of the transistor.

For MOSFET:

$$R_{out} = r_o(1+g_m R_S) \cong \mu_f R_S$$

$$V_{CS} \cong \mu_f \frac{V_{SS}}{3}$$

For BJT:

$$R_{out} = r_o\left(1+\frac{\beta_o R_E}{R_1 \| R_2 + r_\pi + R_E}\right) \le r_o(\beta_o+1)$$

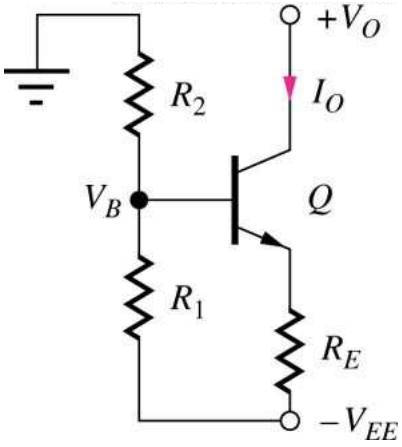
$$V_{CS} = \beta_o(V_A+V_{CE}) \cong \beta_o V_A V_{CS} = \beta_o(V_A+V_{CE}) \cong \beta_o V_A$$

Current Source Comparison

TYPE OF SOURCE	R_{out}	V_{CS}	TYPICAL VALUES
Resistor	R	V_{EE}	15 V
Single transistor	r_o	V_A or $\frac{1}{\lambda}$	50–100 V
BJT with emitter resistor R_E	$\beta_o r_o$	$\cong \beta_o V_A$	5000 V
FET with source resistor R_S ($V_{SS} = 15$ V)	$\mu_f R_S$	$\cong \mu_f \frac{V_{SS}}{3}$	500 V or more

Bipolar Transistor Current Source Design Example

- **Problem:** Design a current source with the largest possible output voltage range that meets the given output resistance specification.
- **Given data**: V_{EE} = 15 V, I_o = 200 μA, I_{EE} < 250 μA, R_{out} > 2 MΩ, BJTs available with (β_o, V_A) = (80, 100 V) and (150, 75 V), V_B must be as low as possible.
- **Assumptions:** Active region and small-signal operating conditions. V_{BE} = 0.7 V, V_T = 0.025 V, choose V_o = 0 V as representative output value.



Analysis:

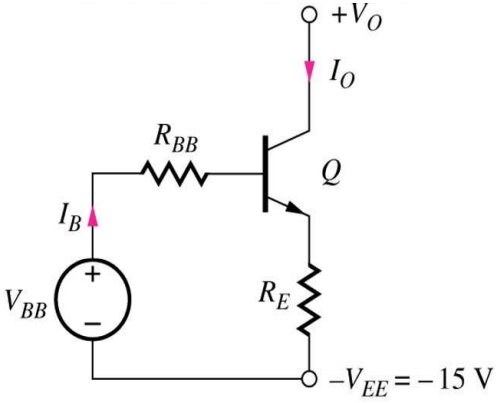
$$R_{out} = r_o\left(1+\frac{\beta_o R_E}{R_1 \| R_2 + r_\pi + R_E}\right) \le \beta_o r_o$$

$$V_{CS} = I_o R_{out} \le \beta_o V_A$$

$$\beta_o V_A = I_o R_{out} \ge (200\mu\text{A})(10\text{M}\Omega) = 2000\text{V}$$

Bipolar Transistor Current Source Design Example (contd.)

Both BJTs can satisfy these conditions. But, we choose BJT (150, 75V) with higher $\beta_o V_A$ product.



Total current < 250 μA. As output current is 200 μA, maximum of 50 μA can be used by base bias network. Current used by base bias network must be 5 to 10 times base current of BJT (1.33 μA for BJT with a current gain of 150). So bias network current =20 μA.

Large R_{BB} reduces output resistance and output compliance range (increase V_{BB}).Trading increased operating current for wider compliance range, choose bias network current of 40 μA.

$$\therefore R_1 + R_2 \cong \frac{15\text{V}}{40\mu\text{A}} = 375\text{k}\Omega$$

Bipolar Transistor Current Source Design Example (contd.)

- Following set of equations can be used in a spreadsheet analysis to determine design variables. Primary design variable is V_{BB} which can be used to determine other variables.

$$I_B = \frac{I_o}{\beta_F}$$

$$R_1 = (R_1 + R_2)\frac{V_{BB}}{15} = 375\text{k}\Omega\left(\frac{V_{BB}}{15}\right)$$

$$R_2 = (R_1 + R_2) - R_1 = 375\text{k}\Omega - R_1$$

$$R_{BB} = R_1 \| R_2$$

$$R_E = \alpha_F\left(\frac{V_{BB} - V_{BE} - I_B R_{BB}}{I_o}\right)$$

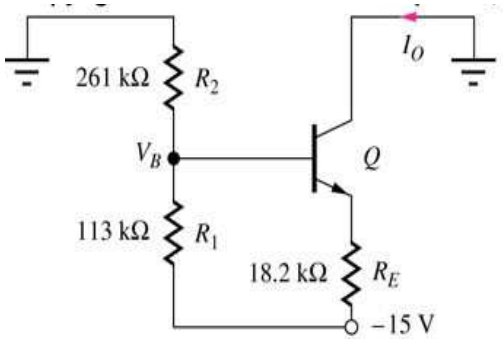
$$V_{CE} = V_{EE} - (V_{BB} - V_{BE} - I_B R_{BB})$$

$$r_o = \frac{V_A + V_{CE}}{I_o} \qquad r_\pi = \frac{\beta_o V_T}{I_o}$$

$$R_{out} = r_o\left(1 + \frac{\beta_o R_E}{R_1 \| R_2 + r_\pi + R_E}\right)$$

Bipolar Transistor Current Source Design Example (contd.)

- From spreadsheet, smallest V_{BB} for which output resistance > 10MΩ with some safety margin is 4.5 V, resulting output resistance is 10.7MΩ.
- Analysis of circuit with 1% resistor values gives I_o = 200 μA and supply current = 244 μA.
- Final current source design is as shown.



- MOSFET current source design can also be analyzed in similar manner.

End of Chapter 15