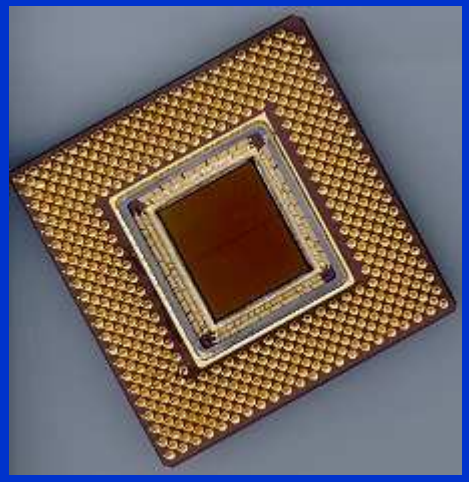


Introduction to Digital System Design

Module 1

Switching Algebra and CMOS Logic Gates

Glossary of Common Terms

- **INTEGRATED CIRCUIT (IC or "CHIP")** – a collection of logic gates and/or other electronic circuits fabricated on a single silicon die
- **CMOS** – a silicon chip fabrication technology based on use of complementary pairs of NMOS and PMOS field effect transistors (MOSFETs)
- **DISCRETE LOGIC** – a circuit constructed using small-scale integrated (SSI) and medium-scale integrated (MSI) logic devices (NAND gates, decoders, multiplexers, etc.)

Glossary of Common Terms

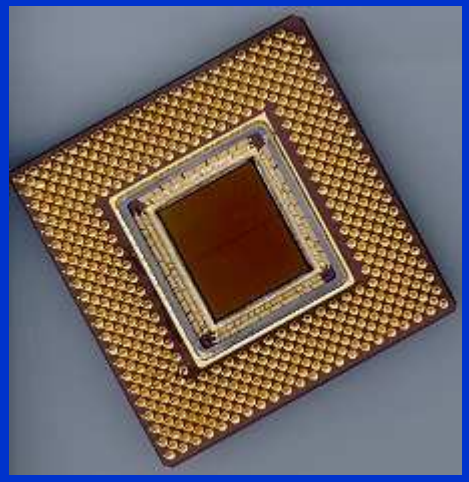
- **PROGRAMMABLE LOGIC DEVICE (PLD)** – an integrated circuit onto which a generic logic circuit can be programmed (and subsequently erased and re-programmed)
- **COMPUTER** – a digital device that sequentially executes a stored program
- **MICROPROCESSOR** – single-chip embodiment of the major functional blocks of a computer
- **MICROCONTROLLER** – a complete computer on a chip, including memory and various integrated peripherals (analog-to-digital conversion, serial communications, pulse-width modulation, timers, network interface)

Glossary of Common Terms

- **PRINTED CIRCUIT BOARD (PCB)** – fiberglass reinforced epoxy substrate with etched copper circuitry (typically in multiple layers) used to create virtually all electronic devices
- **SOCIALLY REDEEMING** – something that has inherent value (like studying digital systems design)
- **DIGIJOCK(ETTE)** – a person who enjoys learning about digital systems

Module 1

- **Learning Outcome: "An ability to design and analyze CMOS logic circuits"**
  - **A. Number Systems**
  - **B. Switching Algebra**
  - **C. Basic Electronic Components and Concepts**
  - **D. Logic Signals and CMOS Logic Circuits**
  - **E. Logic Levels and Noise Margins**
  - **F. Current Sourcing and Sinking**
  - **G. Transition Time and Propagation Delay**
  - **H. Power Consumption and Decoupling**
  - **I. Schmitt Triggers and Transmission Gates**
  - **J. Three-State and Open-Drain Outputs**



Introduction to Digital System Design

Module 1-A
Number Systems

Reading Assignment:

DDPP 4th Ed., pp. 25-31

Learning Objective:

- **Convert numbers from one base (radix) to another**

Outline:

- **Unsigned Integer Base Conversion**
  - **Base R to Base 10**
  - **Base 10 to Base R**
- **Shortcut for Conversion Among Powers of 2**

Unsigned Integer Base Conversion

- **The first item of interest when discussing arithmetic is how to convert from one number base (or radix) to another**
- **A *table of correspondence* is a useful tool for comparing numbers in different bases**
- **The following notation will be used:**

$(d_3d_2d_1d_0)_R = (N)_R$ = number in base R

$(c_3c_2c_1c_0)_R = (N)_{10}$ = number in base 10

Note that the c's represent the *converted corresponding digits*, base 10

Table of Correspondence - Unsigned Integers

N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{16}
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1
10	2	2	2	2	2	2	2	2	2
11	10	3	3	3	3	3	3	3	3
100	11	10	4	4	4	4	4	4	4
101	12	11	10	5	5	5	5	5	5
110	20	12	11	10	6	6	6	6	6
111	21	13	12	11	10	7	7	7	7
1000	22	20	13	12	11	10	8	8	8
1001	100	21	14	13	12	11	10	9	9
1010	101	22	20	14	13	12	11	10	A
1011	102	23	21	15	14	13	12	11	B
1100	110	30	22	20	15	14	13	12	C
1101	111	31	23	21	16	15	14	13	D
1110	112	32	24	22	20	16	15	14	E
1111	120	33	30	23	21	17	16	15	F
10000	121	100	31	24	22	20	17	16	10

Table of Correspondence - Unsigned Integers

N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{16}
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1
10	2	2	2	2	2	2	2	2	2
11	10	3	3	3	3	3	3	3	3
100	11	10	4	4	4	4	4	4	4
101	12	11	10	5	5	5	5	5	5
110	20	12	11	10	6	6	6	6	6
111	21	13	12	11	10	7	7	7	7
1000	22	20	13	12	11	10	8	8	8
1001	100	21	14	13	12	11	10	9	9
1010	101	22	20	14	13	12	11	10	A
1011	102	23	21	15	14	13	12	11	B
1100	110	30	22	20	15	14	13	12	C
1101	111	31	23	21	16	15	14	13	D
1110	112	32	24	22	20	16	15	14	E
1111	120	33	30	23	21	17	16	15	F
10000	121	100	31	24	22	20	17	16	10

Table of Correspondence - Unsigned Integers

N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{16}
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1
10	2	2	2	2	2	2	2	2	2
11	10	3	3	3	3	3	3	3	3
100	11	10	4	4	4	4	4	4	4
101	12	11	10	5	5	5	5	5	5
110	20	12	11	10	6	6	6	6	6
111	21	13	12	11	10	7	7	7	7
1000	22	20	13	12	11	10	8	8	8
1001	100	21	14	13	12	11	10	9	9
1010	101	22	20	14	13	12	11	10	A
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1100	110	30	22	20	15	14	13	12	C
1101	111	31	23	21	16	15	14	13	D
1110	112	32	24	22	20	16	15	14	E
1111	120	33	30	23	21	17	16	15	F
10000	121	100	31	24	22	20	17	16	10

Unsigned Integer Base Conversion

- **<u>IMPORTANT</u>: The conversion methods described here are only applicable to *unsigned* (or, "positive") numbers**
- **<u>ALSO NOTE</u>: Since the numbers we are dealing with are unsigned, *leading zeroes* have "no social significance" (i.e., they can be *added or removed* without changing the value of the number)**

Conversion of Integers: Base R→10

- **Method: Iterative Multiply and Add**
  - **based on the fact that a number can be expressed in nested form, as follows:**

$$(d_3 d_2 d_1 d_0)_R = (N)_{10}$$

$$= c_3 x R^3 + c_2 x R^2 + c_1 x R^1 + c_0 x R^0$$

$$= (((c_3 \times R + c_2) \times R + c_1) \times R + c_0)$$

  - **the expression evaluation proceeds from the inner-most level of parenthesis to the outer-most level**

Conversion of Integers: Base R→10

- **Example: Convert $(4352)_8$ to base 10**

  4 x 8 + 3 = 35

  35 x 8 + 5 = 285

  285 x 8 + 2 = 2282

  Therefore, $(4352)_8 = (2282)_{10}$

Conversion of Integers: Base R→10

- **Example: Convert $(01101011)_2$ to base 10**

0	x	2	+	1	=	1
1	x	2	+	1	=	3
3	x	2	+	0	=	6
6	x	2	+	1	=	13
13	x	2	+	0	=	26
26	x	2	+	1	=	53
53	x	2	+	1	=	107

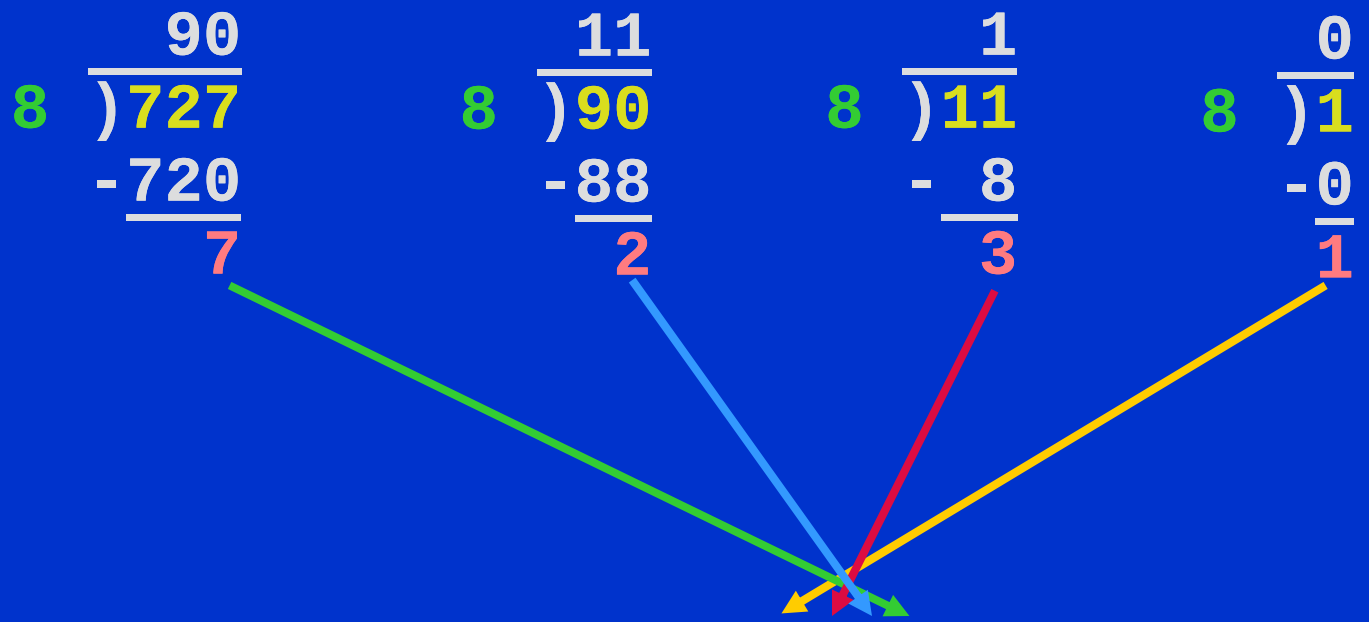
Therefore, $(01101011)_2$ = (107)$_{10}$

Conversion of Integers: Base 10→R

- **Method: Iterative Division**
  - **based on an iterative division of the number by the radix (base) to which it is being converted**
  - **the *remainders* of each division become the digits of the converted number**
  - **a *quotient of zero* indicates the conversion is complete**

Conversion of Integers: Base 10→R

- **Example: Convert $(727)_{10}$ to base 8**



Therefore, $(727)_{10} = (1327)_8$

Conversion of Integers: Base 10→R

- **Example: Convert $(2623)_{10}$ to base 16**

Therefore, $(2623)_{10}$ = (_A3F_)$_{16}$

Short Cut for Conversion Among Powers of 2

- **<u>Method</u>: Size Log_2R Groupings**
  - **when converting a number from base "A" to base "B", where A and B are *powers of 2* (e.g., 2, 4, 8, and 16), a "short cut" can be used**
  - **an *n-digit binary number* can be written for each *base A* digit in the original number, where $n = log_2A$**
  - **starting at the *least significant position,* the converted binary digits can be *regrouped* into *m-digit* binary numbers, where $m = log_2B$**

Short Cut for Conversion Among Powers of 2

- **Example: Convert $(136)_8$ to base 2 and base 16**

1	3	6
001	011	110
0101	1110	
5	E	

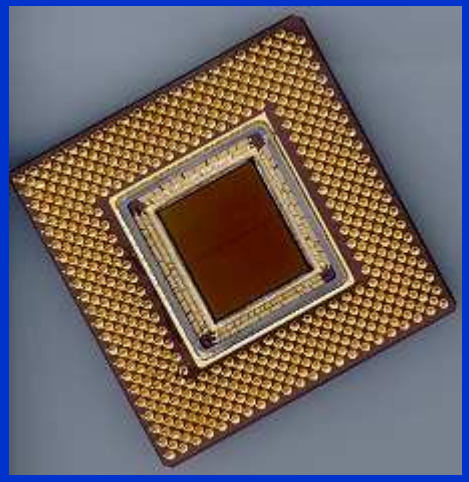
Therefore, $(136)_8 = (1011110)_2 = (5E)_{16}$

Short Cut for Conversion Among Powers of 2

- **Example: Convert $(110101)_2$ to bases 8 and 16**

```
   6     5
  110   101
  110101
  0011  0101
   3     5
```

Therefore, $(110101)_2$ = (65)$_8$ = (35)$_{16}$



Introduction to Digital System Design

Module 1-B
Switching Algebra

Reading Assignment:

DDPP 4th Ed., pp. 183-199

Learning Objectives:

- **Define a binary variable**
- **Identify the theorems and postulates of switching algebra**
- **Describe the principle of duality**
- **Describe how to form a complement function**
- **Prove the equivalence of two Boolean expressions using perfect induction**

Outline

- Overview
- Basic logic gates
- Axioms
- Duality
- Theorems
  - Single-Variable
  - Two- and Three-Variable
  - n-Variable

Overview

- **Formal analysis techniques for digital circuits are based on a two-valued algebraic system called *Boolean algebra* (named after George Boole, who invented it in 1854)**
- **Claude Shannon (1938) showed how to adapt Boolean algebra to analyze and describe the behavior of circuits built from relays**
- **In Shannon's *switching algebra*, the condition of a relay contact (open/closed) is represented by a variable X (equal to 0/1)**
- **In today's logic technologies, these values correspond to *voltage* LOW or HIGH**

Definitions

- **Definition: The *axioms* (or *postulates*) of a mathematical system are a minimal set of basic definitions that we assume to be true, from which all other information about the system can be derived**
- **Notation: A *prime* (′) will be used to denote an inverter's function (i.e., the *complement* of a logic signal) – note that *prime* is an *algebraic operator*, that X′ is an *expression*, and that Y=X′ is an *equation***

X′ can be read as X prime, NOT X, or X bar

Example

Given the truth table for F(X,Y,Z), determine the truth table for the COMPLEMENT function, F'(X,Y,Z)

X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Example

Given the truth table for F(X,Y,Z), determine the truth table for the COMPLEMENT function, F′(X,Y,Z)

X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

X	Y	Z	F′(X,Y,Z)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

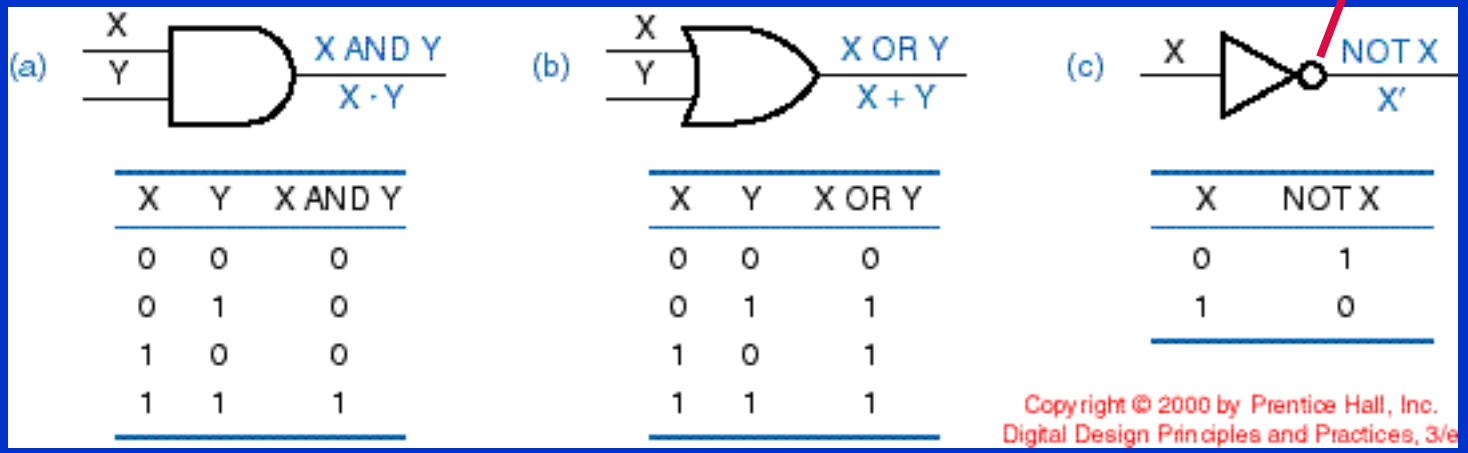
Definitions

- **Definition: A *binary variable*, X, is a two-valued quantity such that:**
  - **if $X \neq 1$, then $X = 0$**
  - **if $X \neq 0$, then $X = 1$**
- **Definition: The function of a 2-input AND gate is called *logical multiplication* and is symbolized by a *multiplication dot* (•)**
- **Definition: The function of a 2-input OR gate is called *logical addition* and is symbolized algebraically by a *plus sign* (+)**
- **Convention: Multiplication (AND) has *implied precedence* over addition (OR)**

Example: $W \bullet X + Y \bullet Z = (W \bullet X) + (Y \bullet Z)$

Basic Logic Gates

- An **AND gate** produces a 1 output if and only if all of its inputs are 1
- An **OR gate** produces a 1 output if one or more of its inputs are 1
- A **NOT gate** (usually called an **inverter**) produces an output value that is the opposite of its input value



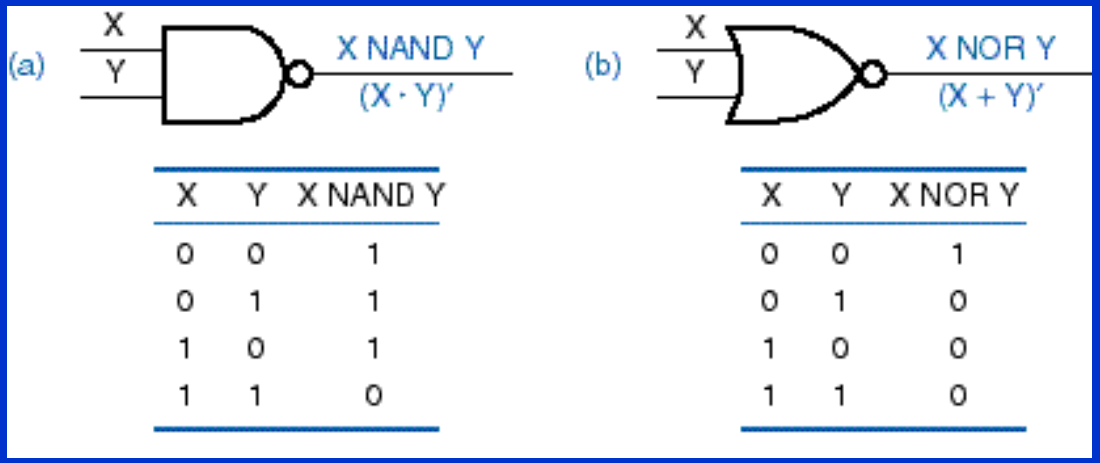
X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

X	NOT X
0	1
1	0

Other Basic Gates (More Commonly Used)

- **Other "basic gates" are possible:**
  - **a NAND ("Not AND") gate produces the *opposite* of an AND gate's output**
  - **a NOR ("Not OR") gate produces the *opposite* of an OR gate's output**



X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0

X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0

NAND / NOR gates are easier to make (require fewer transistors) than AND / OR gates

- **Logical completeness: "anything digital" can be built solely using AND, OR, and NOT gates or solely using NAND or NOR gates**

Axioms

(A1) $X = 0$ if $X \neq 1$

(A2) If $X = 0$, then $X' = 1$

(A3) $0 \bullet 0 = 0$

(A4) $1 \bullet 1 = 1$

(A5) $0 \bullet 1 = 1 \bullet 0 = 0$

(A1^D) $X = 1$ if $X \neq 0$

(A2^D) If $X = 1$, then $X' = 0$

(A3^D) $1 + 1 = 1$

(A4^D) $0 + 0 = 0$

(A5^D) $1 + 0 = 0 + 1 = 1$

Note: The second axiom in each pair is referred to as the *dual* of the first one (and vice versa)

Also Note: *These 5 pairs of axioms completely define switching algebra*

Duality

- **Definition: The *dual* of an expression is formed through the simultaneous interchange of the operators "•" and "+" and the elements "0" and "1"**
- **Important Principle: If two Boolean expressions can be proven to be equivalent using a given sequence of axioms or theorems, then the *dual expressions* may be proven to be equivalent by simply applying the sequence of *dual* axioms or theorems**

Example

Given the truth table for F(X,Y,Z), determine the truth table for the DUAL function, $F^D(X,Y,Z)$

X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Example

Given the truth table for F(X,Y,Z), determine the truth table for the DUAL function, $F^D(X,Y,Z)$

X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

X	Y	Z	$F^D(X,Y,Z)$
1	1	1	0
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	1
0	0	1	0
0	0	0	0

Example

Given the truth table for F(X,Y,Z), determine the truth table for the DUAL function, $F^D(X,Y,Z)$

X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

X	Y	Z	$F^D(X,Y,Z)$
1	1	1	0
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	1
0	0	1	0
0	0	0	0

X	Y	Z	$F^D(X,Y,Z)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Theorems

- **Definition: Switching algebra *theorems* are statements, known always to be true, that allow manipulation of algebraic expressions**
- **Definition: A technique called *perfect induction* can be used to prove switching algebra theorems ("perfect" implies the use of *all possible combinations* of the values of the variables – thus, it is an *exhaustive* type of proof)**

Single-Variable Theorems

(T1) $X + 0 = X$	**(T1^D)** $X \bullet 1 = X$	***Identities***
(T2) $X + 1 = 1$	**(T2^D)** $X \bullet 0 = 0$	***Null elements***
(T3) $X + X = X$	**(T3^D)** $X \bullet X = X$	***Idempotency***
(T4) $(X')' = X$		***Involution***
(T5) $X + X' = 1$	**(T5^D)** $X \bullet X' = 0$	***Complements***

Two- and Three-Variable Theorems

(T6) $X + Y = Y + X$ ***Commutivity***

($T6^D$) $X \bullet Y = Y \bullet X$

(T7) $(X + Y) + Z = X + (Y + Z)$ ***Associativity***

($T7^D$) $(X \bullet Y) \bullet Z = X \bullet (Y \bullet Z)$

(T8) $X \bullet Y + X \bullet Z = X \bullet (Y + Z)$ ***Distributivity***

($T8^D$) $(X + Y) \bullet (X + Z) = X + Y \bullet Z$

(T9) $X + X \bullet Y = X$ ***Covering***

($T9^D$) $X \bullet (X + Y) = X$

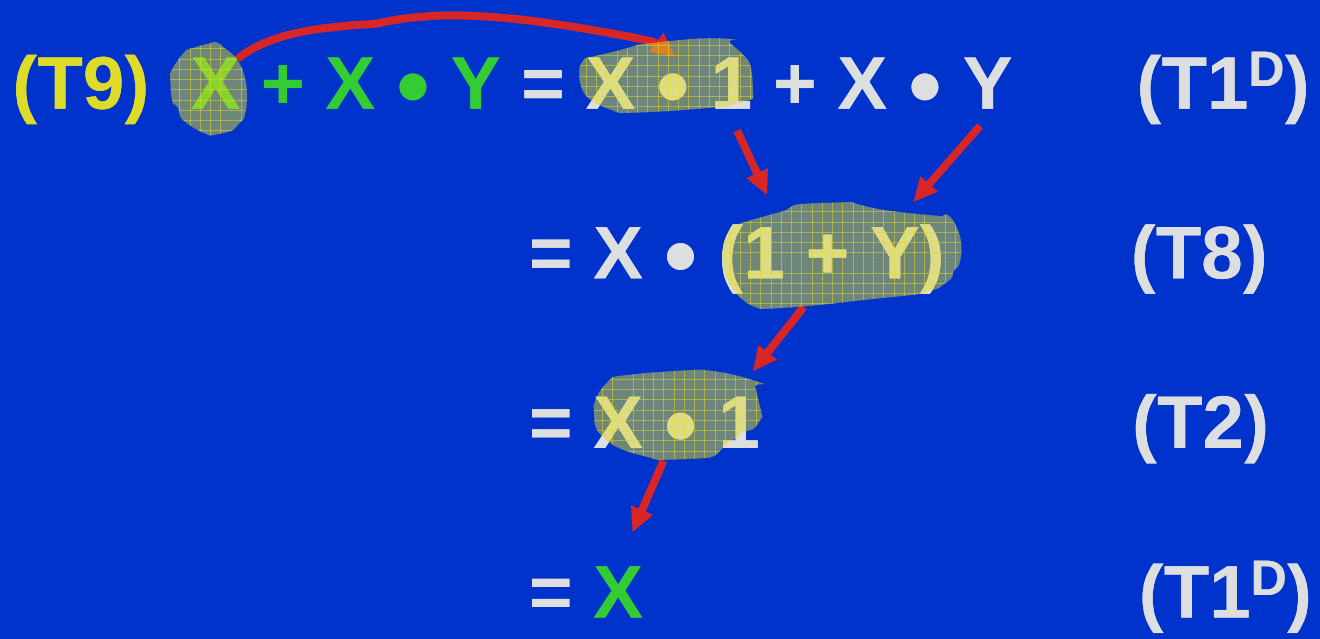
Two- and Three-Variable Theorems

Example: Proof of T8^D using perfect induction

X Y Z	Y•Z	X + Y•Z	X + Y	X + Z	(X+Y)•(X+Z)
0 0 0	0	0	0	0	0
0 0 1	0	0	0	1	0
0 1 0	0	0	1	0	0
0 1 1	1	1	1	1	1
1 0 0	0	1	1	1	1
1 0 1	0	1	1	1	1
1 1 0	0	1	1	1	1
1 1 1	1	1	1	1	1
		r.h.s.			l.h.s.

Two- and Three-Variable Theorems

Example: Proof of T9 using other theorems



Two- and Three-Variable Theorems

(T10) $X \bullet Y + X \bullet Y' = X$ ***Combining***

(T10^D) $(X + Y) \bullet (X + Y') = X$

Consensus

(T11) $X \bullet Y + X' \bullet Z + Y \bullet Z = X \bullet Y + X' \bullet Z$

(T11^D) $(X + Y) \bullet (X' + Z) \bullet (Y + Z) = (X + Y) \bullet (X' + Z)$

Note: In all theorems, it is possible to replace each variable with an arbitrary logic expression

Two- and Three-Variable Theorems

Example: Using only the axioms and theorems described thus far, verify the following equivalence expression:

$$X \bullet Y + Y \bullet Z + X' \bullet Z = X \bullet Y + X' \bullet Z$$

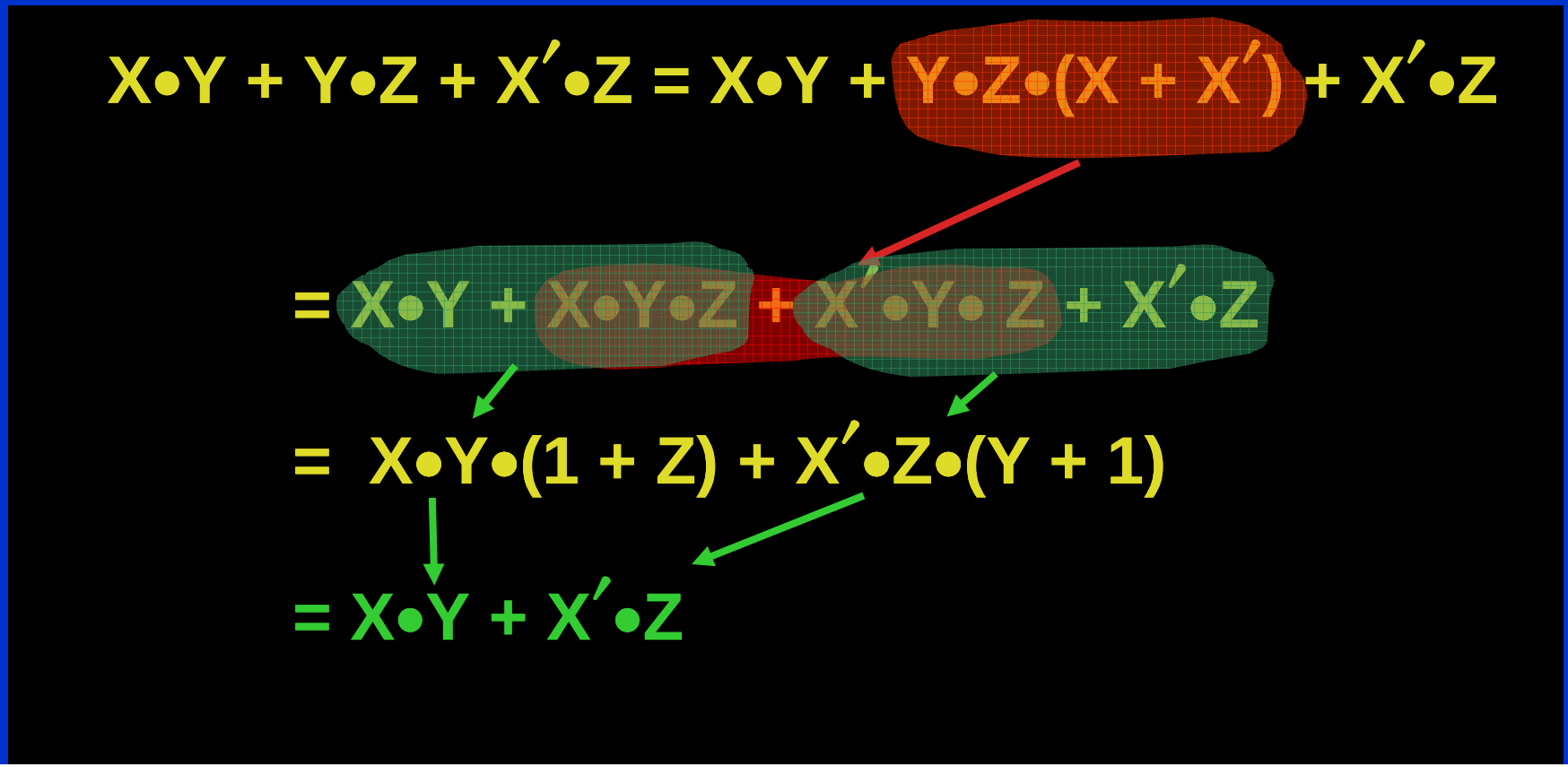
Main "Tricks":

- Multiply by (X + X′)

- Factor out common terms

Two- and Three-Variable Theorems

Example: Using only the axioms and theorems described thus far, verify the following equivalence expression:



n-Variable Theorems

Generalized Idempotency

(T12) $X + X + \ldots + X = X$

(T12^D) $X \bullet X \bullet \ldots \bullet X = X$

DeMorgan's Law

(T13) $(X1 \bullet X2 \bullet \ldots \bullet Xn)' = X1' + X2' + \ldots + Xn'$

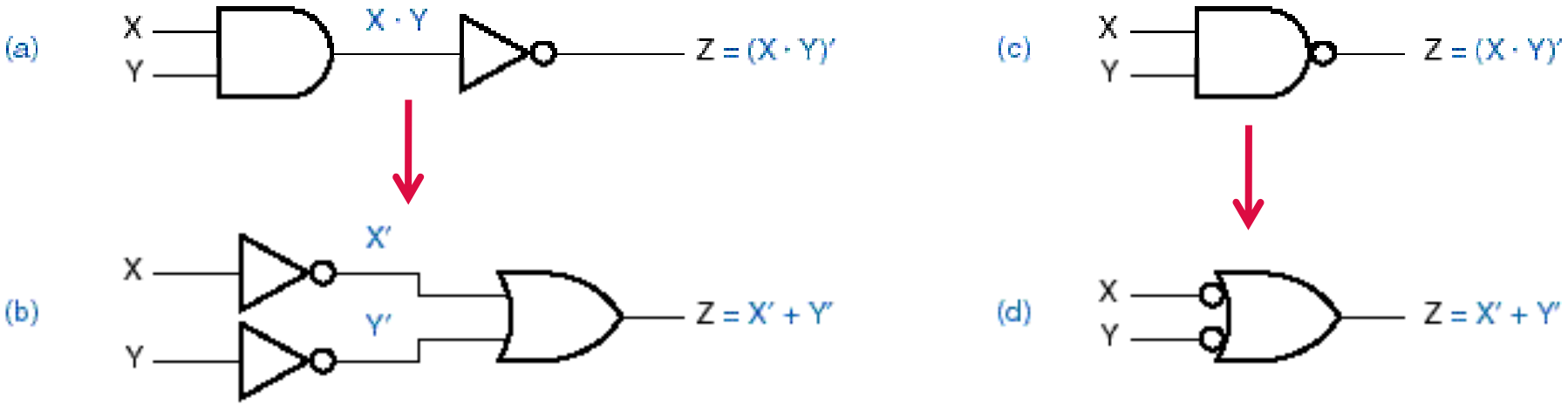
(T13^D) $(X1 + X2 + \ldots + Xn)' = X1' \bullet X2' \bullet \ldots \bullet Xn'$

Generalized DeMorgan's Law

(T14) $[F(X1, X2, \ldots, Xn)]' = F^D(X1', X2', \ldots, Xn')$

Equivalent Circuits According to DeMorgan's Theorem

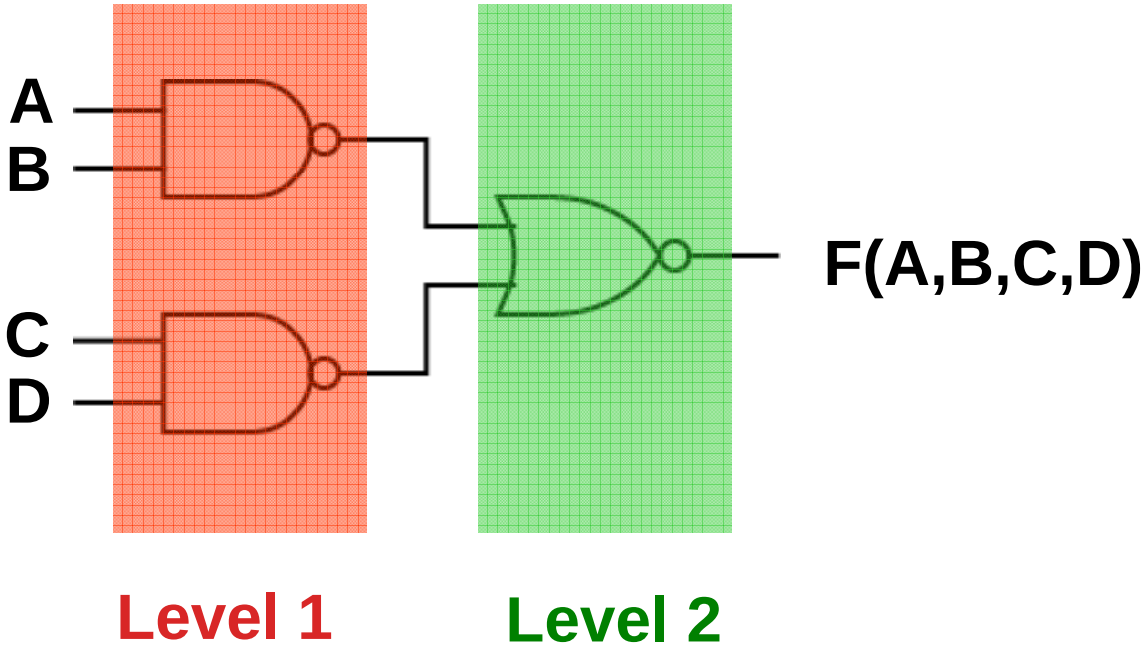
$(X \bullet Y)' = X' + Y'$ (T13)



<u>Observation</u>: A *logically equivalent circuit* can be formed by taking the *dual* of the operator(s) and *complementing* all the inputs and outputs

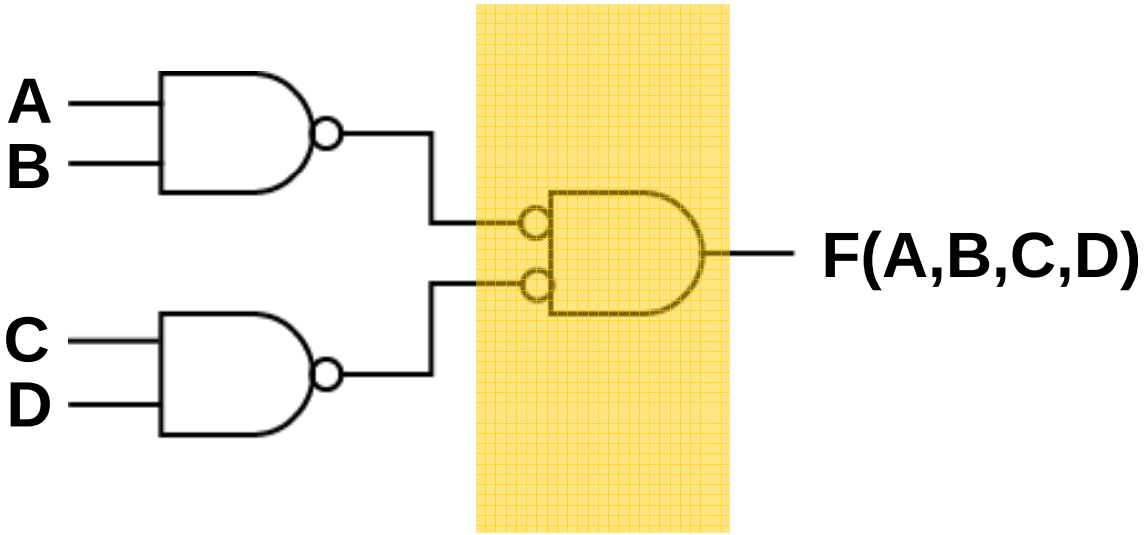
Example - Graphical Application of DeMorgan's Law

- **Determine the function implemented by a two-level NAND-NOR circuit**



Example - Graphical Application of DeMorgan's Law

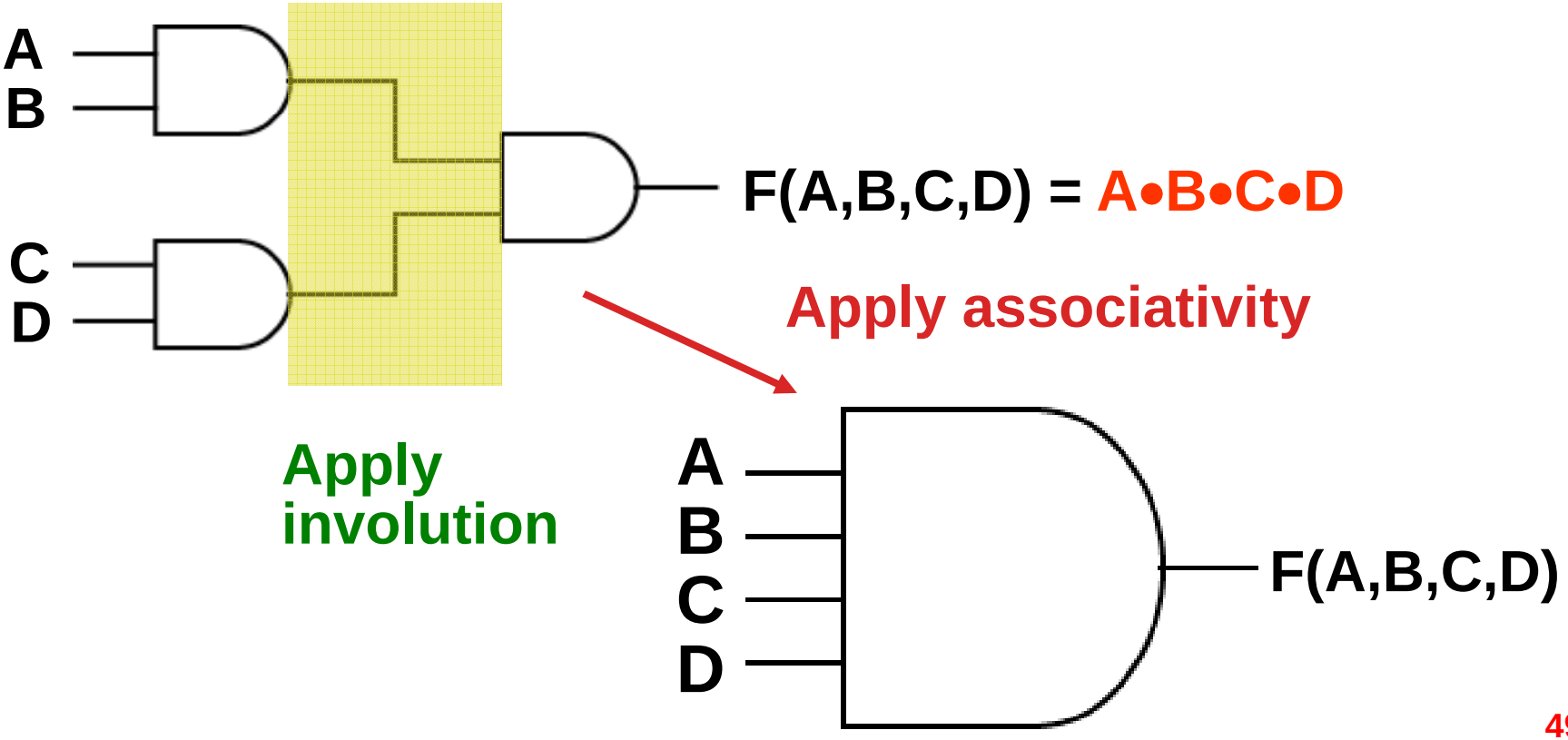
- **Determine the function implemented by a two-level NAND-NOR circuit**



Equivalent symbol for NOR gate

Example - Graphical Application of DeMorgan's Law

- **Determine the function implemented by a two-level NAND-NOR circuit**



Examples – Name the Switching Algebra Axiom or Theorem

Null Elements ($T2^D$)	**$X \cdot 0 = 0$**
Complements (T5)	**$X' + X = 1$**
Complements ($T5^D$)	**$X' \cdot X = 0$**
(Generalized) Idempotency (T3 or T12)	**$X + X + X = X$**
Involution (T4)	**$(X')' = X$**

Examples – Name the Switching Algebra Axiom or Theorem

Covering ($T9^D$)	**$X \bullet (X+Y) = X$**
Distributivity (T8)	**$(X+Y) \bullet (X+Z) = X + Y \bullet Z$**
Associativity (T7)	**$(X+Y)+Z = X+(Y+Z)$**
Commutivity ($T6^D$)	**$X \bullet Y \bullet Z = Z \bullet X \bullet Y$**

Example – Proof Using Perfect Induction

T9^D $X \bullet (X + Y) = X$

X	Y	(X + Y)	X•(X+Y)	X
0	0	0	0	0
0	1	1	0	0
1	0	1	1	1
1	1	1	1	1

Example – Proof Using Other Theorems

$T9^D$ $X \bullet (X + Y) = X$

$X \bullet (X + Y)$	$= X \bullet X + X \bullet Y$	(T8)
	$= X + X \bullet Y$	($T3^D$)
	$= X \bullet (1 + Y)$	(T8)
	$= X \bullet (1)$	(T2)
	$= X$	($T1^D$)

Clicker Quiz

1. The expression **(X•Y)•Z = X•(Y•Z)** is an example of:

A. commutitivity

B. associativity

C. distributivity

D. consensus

E. none of the above

2. The expression **X + Y + Z = Y + Z + X** is an example of:

A. commutitivity

B. associativity

C. distributivity

D. consensus

E. none of the above

3. The expression **(X+Y)•(X′+Z)•(Y+Z) =**

(X+Y)•(X′+Z) is an example of:

A. commutitivity

B. associativity

C. distributivity

D. consensus

E. none of the above

4. The expression **(X+Y)·(X+Z) = X + Y·Z** is an example of:

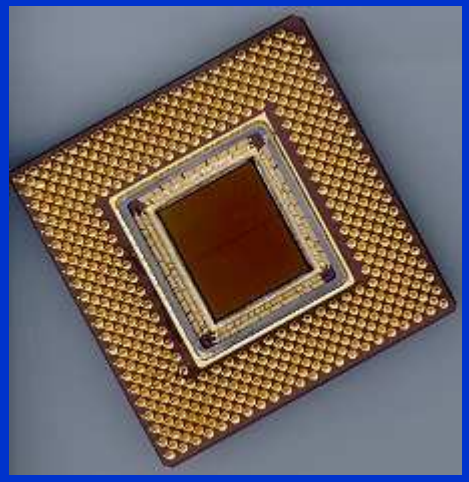
A. commutitivity

B. associativity

C. distributivity

D. consensus

E. none of the above



Introduction to Digital System Design

Module 1-C

Basic Electronic Components and Concepts

Reading Assignment:

on-line supplement

Learning Objective:

- **Describe the function and utility of basic electronic components: resistors, capacitors, diodes, transistors**

Outline:

- **Voltage and current**
- **Resistors**
- **Power dissipation**
- **Capacitors**
- **Diodes**
- **Transistors**

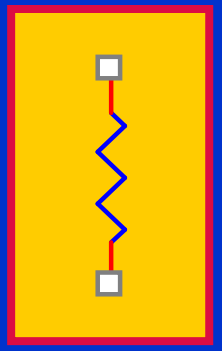
Voltage and Current

- **VOLTAGE – difference in electrical potential, expressed in *volts***
- **CURRENT – the flow of charge in a conductor between two points having a difference in potential, expressed in *amperes* (amps)**
- **Waterfall analogy – voltage is proportional to *height* of waterfall, current is proportional to *flow* of waterfall**

Resistors

- **RESISTOR – a device that limits the amount of current flowing through a circuit, measured in *ohms* (Ω)**
- **Resistance is also referred to as *impedance***
- **The inverse of impedance is *admittance***
- **Fundamental relationship**
  - **the voltage drop (V_R) across a resistor is equal to the product of the current flowing through it (I_R) and the value of the resistance (R) ⇒ called *Ohm's Law***

$$V_R = I_R \times R$$

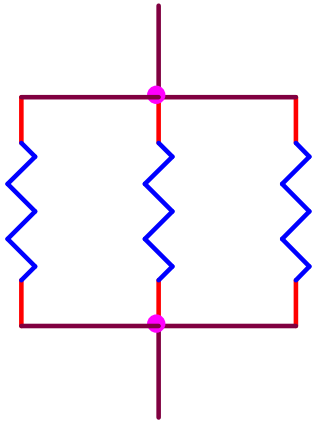


Resistors

- **Fundamental relationships**
  - **Resistors in series**

$$R_T = R_1 + R_2 + R_3$$

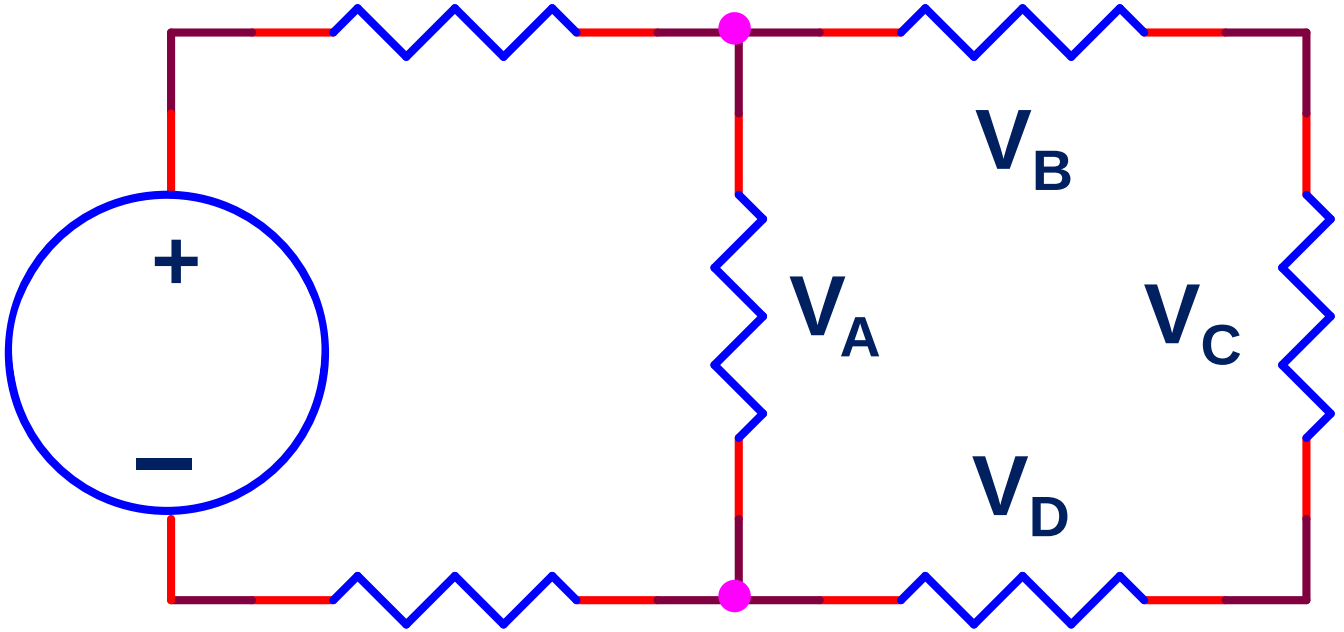
  - **Resistors in parallel**



$$1/R_T = 1/R_1 + 1/R_2 + 1/R_3$$

Voltage and Current

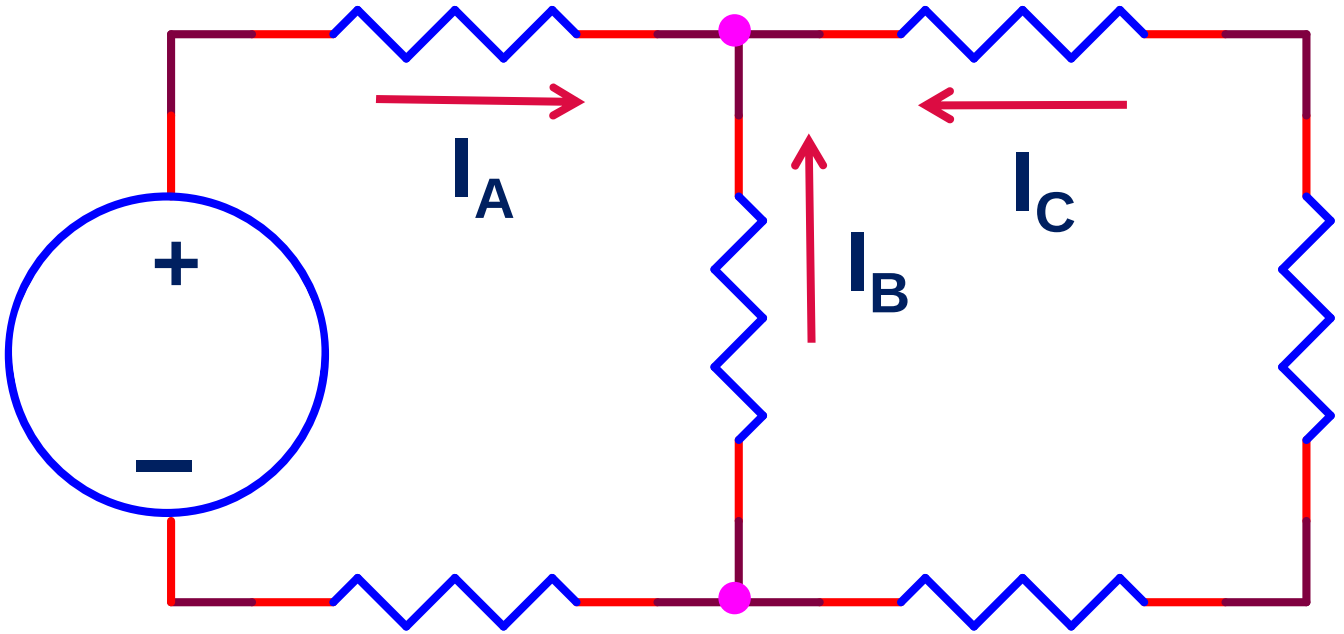
- **Kirchhoff's Voltage Law (KVL) – voltage around a loop sums to zero (based on conservation of energy)**



$$V_A + V_B + V_C + V_D = 0$$

Voltage and Current

- **Kirchhoff's Current Law (KCL) – sum of currents at any node is zero (based on conservation of electric charge)**



$$I_A + I_B + I_C = 0$$

Power Dissipation

- **POWER – amount of energy, expressed in *watts*, typically calculated as the product of the *voltage* drop across a device and the *current* flowing through it**
- **Multiple ways to calculate:**
  - **$P = V \times I$**
  - **$P = V^2 / R$**
  - **$P = I^2 \times R$**

Based on Ohm's law substitutions:

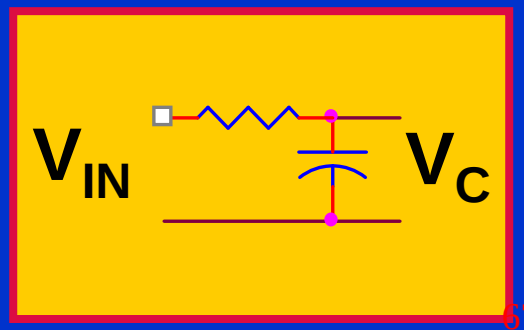
$$I = V / R$$

$$V = I \times R$$

Capacitors

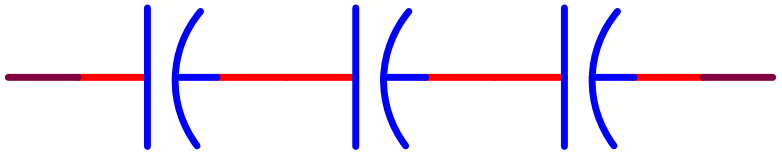
- **CAPACITOR – a device that stores an electric charge, measured in *farads* (F)**
- **Fundamental relationships**
  - **a resistor-capacitor (RC) network charges and discharges exponentially**
  - **the voltage across a capacitor cannot change instantaneously**
  - **the product of R and C is called the *RC time constant***

$$V_C = V_{IN} \times (1 - e^{-t/RC})$$



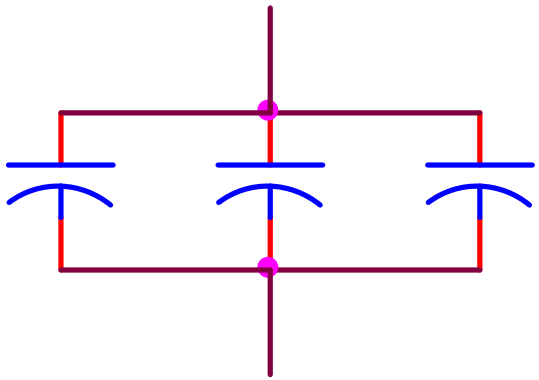
Capacitors

- **Fundamental relationships**
  - **Capacitors in series**



$$1/C_T = 1/C_1 + 1/C_2 + 1/C_3$$

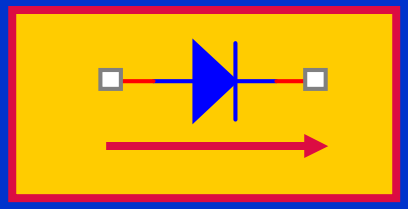
  - **Capacitors in parallel**



$$C_T = C_1 + C_2 + C_3$$

Diodes

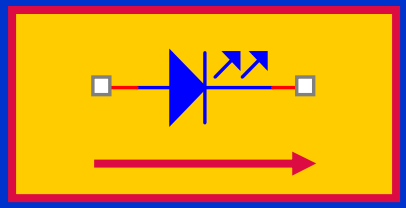
- **DIODE – a device that restricts the flow of current to a single direction (from its *anode* to its *cathode*)**



- **Fundamental relationships**
  - **a diode through which current is flowing (because the voltage at the anode is greater than at the cathode) is *forward biased***
  - **if current is not flowing through a diode (because the voltage at the cathode is greater than at the anode), the diode is *reverse biased***

Light Emitting Diodes

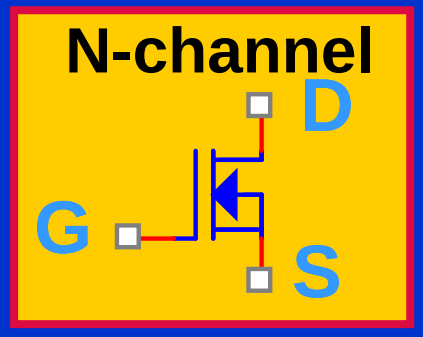
- **LIGHT EMITTING DIODE (LED) – a diode that emits visible (red/yellow/green/blue/white) or invisible (infrared) light when forwarded biased**

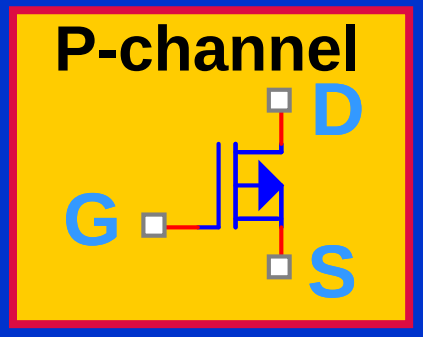


- **Fundamental relationships**
  - **the brightness of an LED is proportional to the amount of current flowing through it (called the *forward current*)**
  - **a *resistor* is placed in series with an LED to limit the amount of current flowing through it**
  - **the voltage drop across an LED when it is forward biased is called the *forward voltage***

Transistors

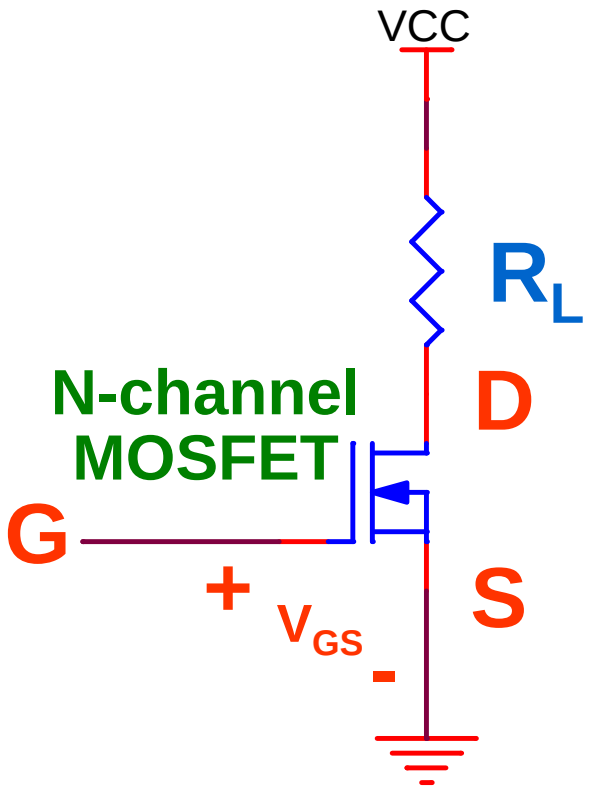
- **FIELD EFFECT TRANSISTOR (MOSFET)**
  - **a 3-terminal device (G-gate, S-source, D-drain) that provides a voltage-controlled *impedance***
- **Two basic types**
  - **N-channel: *high* potential on G (gate) relative to S (source) causes transistor to turn on (low impedance between S and D terminals)**
  - **P-channel: *low* potential on G (gate) relative to S (source) causes transistor to turn on**





Transistors

- A **MOSFET** can be used as a **voltage-controlled switch** for a **DC load**

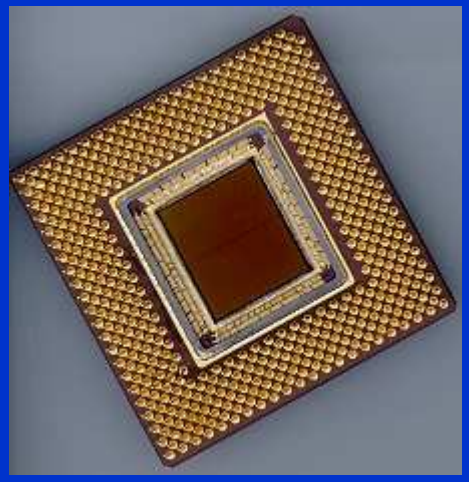


Voltage-controlled resistance:

increase V_{GS} → decrease R_{DS}

Note: normally, $V_{GS} \geq 0$

As R_{DS} decreases, power delivered to load (R_L) increases



Introduction to Digital System Design

Module 1-D

Logic Signals and CMOS Logic Circuits

Reading Assignment:

DDPP 4th Ed., pp. 79-96, 141-148

Learning Objectives:

- **Define the switching threshold of a logic gate and identify the voltage ranges typically associated with a "logic high" and a "logic low"**
- **Define assertion level and describe the difference between a positive logic convention and a negative logic convention**
- **Describe the operation of basic logic gates (NOT, NAND, NOR) constructed using N- and P-channel MOSFETs and draw their circuit diagrams**
- **Define "fighting" among gate outputs wired together and describe its consequence**
- **Define logic gate fan-in and describe the basis for its practical limit**

Outline

- Logic signals and assertion levels
- CMOS logic circuits
  - Inverter (NOT)
  - NAND
  - NOR
- Fighting
- Fan-in

Logic Signals

- **A logic value, 0 or 1, is often referred to as a *binary digit* or *bit***
- **The words "LOW" and "HIGH" are often used in place of "0" and "1" to refer to *logic signals***
  - **LOW - a signal in the range of "lower" voltages (e.g., 0 - 1.5 volts for 5V CMOS logic), which is interpreted as a logic 0**
  - **HIGH - a signal in the range of "higher" voltages (e.g., 3.5 - 5.0 volts for 5V CMOS logic), which is interpreted as a logic 1**

Positive Logic Convention

- **The *assignment* of 0 and 1 to LOW and HIGH, respectively, is referred to as a *positive logic convention* (or simply "positive logic")**
  - **a positive logic signal that is *asserted* is in the HIGH state, and is therefore referred to as an "active high" signal**
  - **a positive logic signal that is *negated* is in the LOW state**

Negative Logic Convention

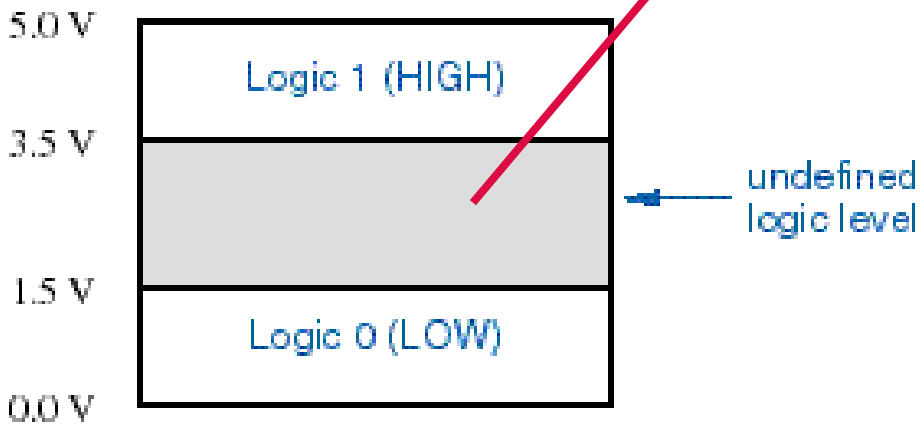
- **The *opposite assignment* (1 to LOW and 0 to HIGH) is referred to as a *negative logic convention* (or "negative logic")**
  - **a negative logic signal that is *asserted* is in the LOW state, and is therefore referred to as an "active low" signal**
  - **a negative logic signal that is *negated* is in the HIGH state**

Logic Families

- There are ***many*** ways to design a digital logic gate, from mechanical relays and vacuum tubes to microscopic transistors
- **C**omplementary **M**etal-**O**xide **S**emiconductor (**CMOS**) circuits now account for the vast majority of the worldwide **I**ntegrated **C**ircuit (**IC**) market
- **CMOS** logic is both the most capable and the easiest to understand commercial digital logic technology

CMOS Logic

- **5 V CMOS logic levels**



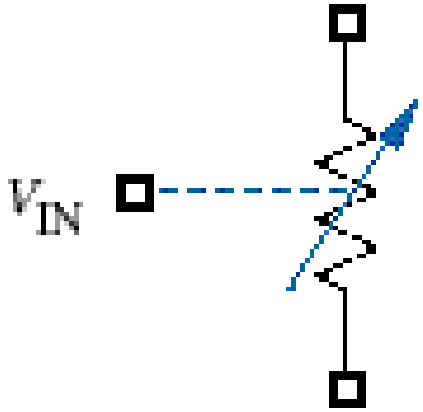
indeterminate region

undefined input yields undefined output

<u>Note</u>: CMOS circuits using other power supply voltages (e.g., 3.3 or 2.7 volts) partition the voltage range similarly

CMOS Logic

- **MOS Field Effect Transistor (MOSFET)**
  - **modeled as a 3-terminal device that acts like a voltage-controlled resistance**

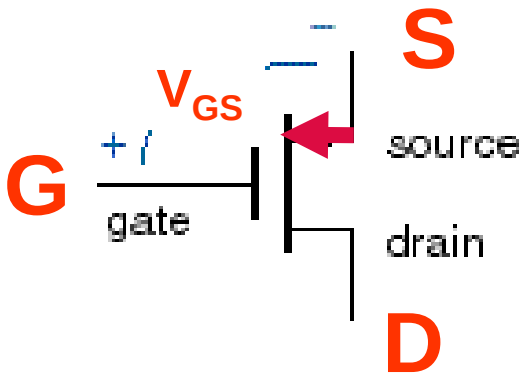


NOTE: Current only flows through the resistance one way

  - **in digital logic applications, MOSFETs are operated so that their resistance is either *very high* (transistor is "off") or *very low* (transistor is "on")**

CMOS Logic

- **There are two types of MOSFETs**
  - **P-channel MOS (PMOS)**



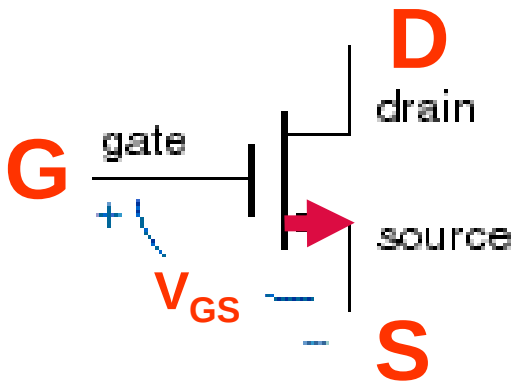
Voltage-controlled resistance:

decrease V_{GS} → decrease R_{DS}

(current flows from S terminal to D)

Note: normally, $V_{GS} \leq 0$

  - **N-channel MOS (NMOS)**



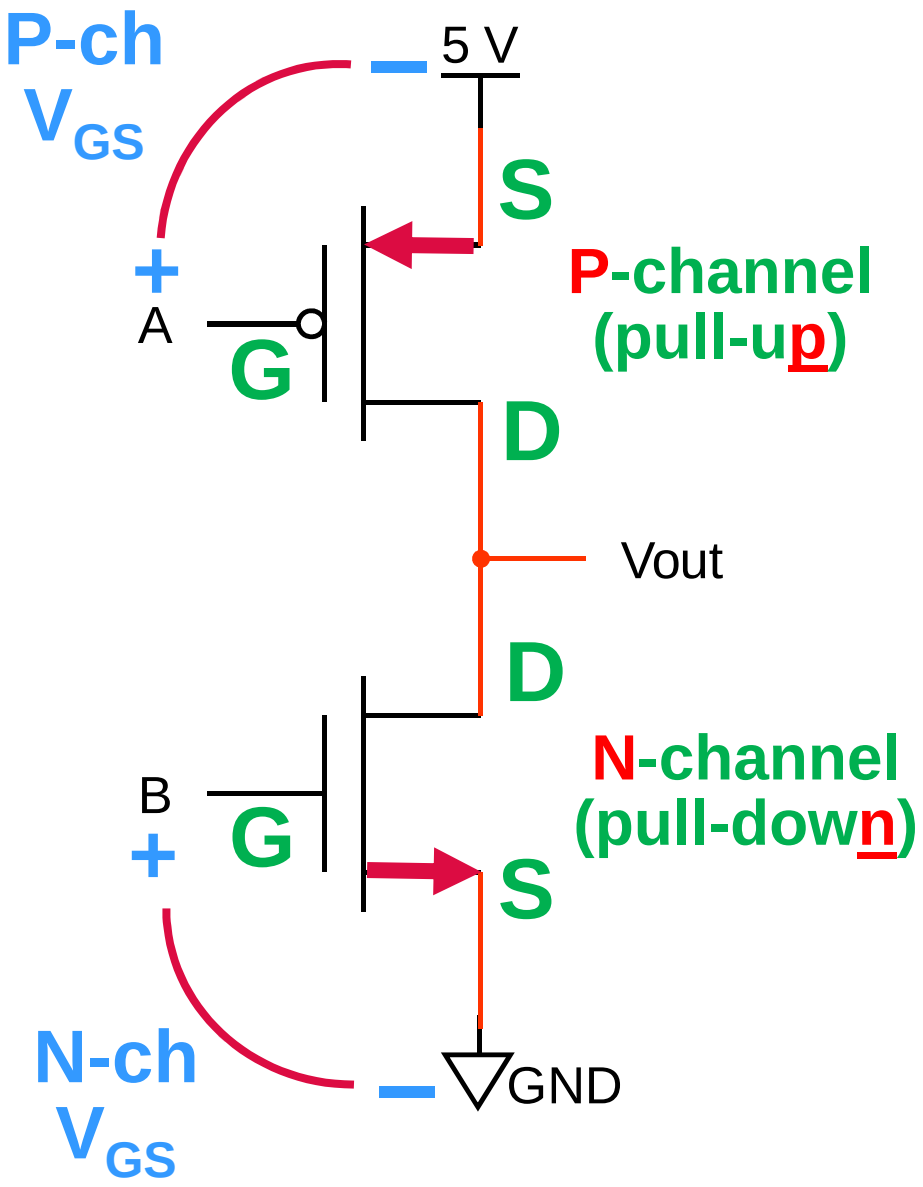
Voltage-controlled resistance:

increase V_{GS} → decrease R_{DS}

(current flows from D terminal to S)

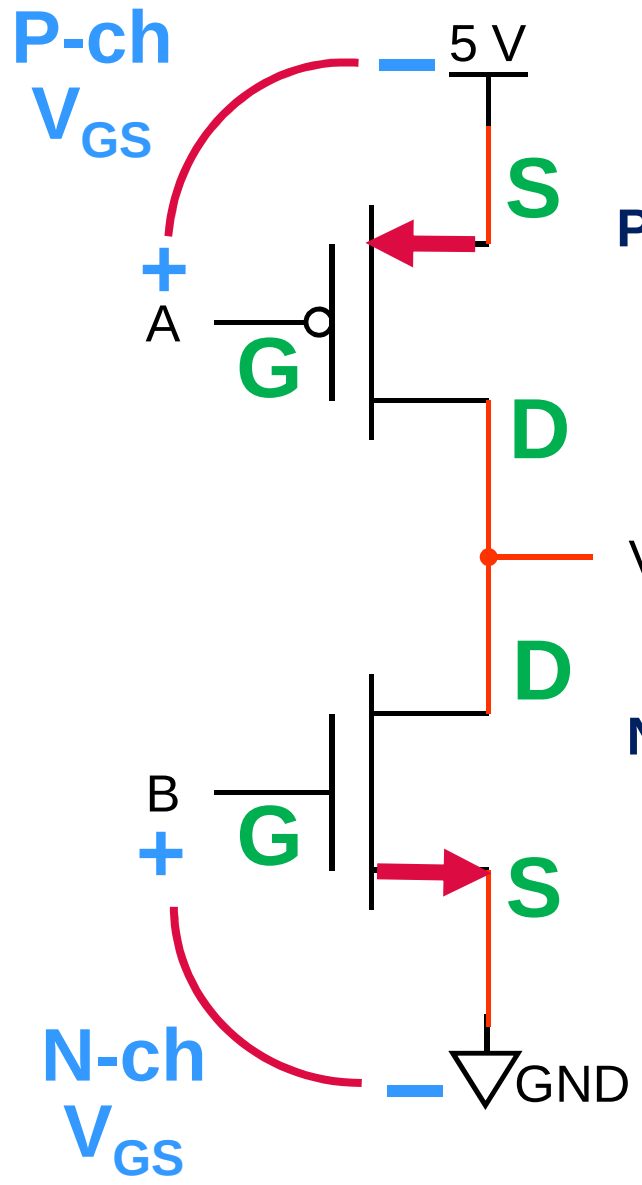
Note: normally, $V_{GS} \geq 0$

Basic CMOS Logic Circuit



- The S terminal of the P-ch MOSFET is connected to 5 V
- The S terminal of the N-ch MOSFET is connected to GND
- The D terminals of both MOSFETs are connected to the output (Vout)
- The direction of current flow in the P-ch device is from the S terminal to the D terminal ("sources" current)
- The direction of current flow in the N-ch device is from the D terminal to the S terminal ("sinks" current)
- A high voltage on the G terminal of the N-ch MOSFET (relative to GND) turns it on
- A low voltage on the G terminal of the P-ch MOSFET (relative to 5 V) turns it on

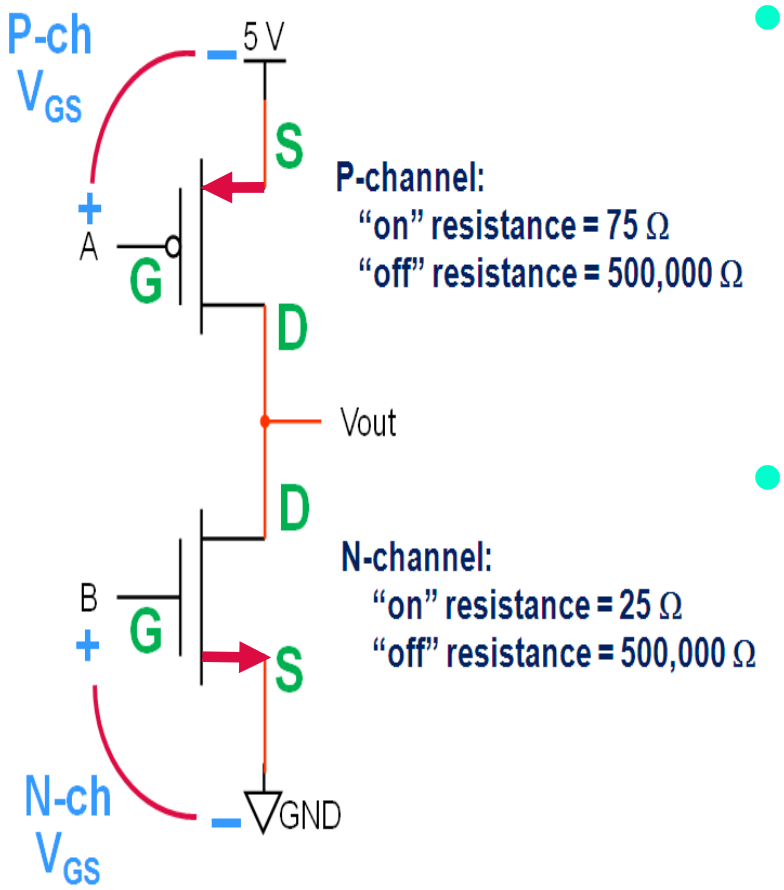
Example (Hypothetical Impedances)



P-channel:
"on" resistance = 75 Ω
"off" resistance = 500,000 Ω

N-channel:
"on" resistance = 25 Ω
"off" resistance = 500,000 Ω

Example: Inverter Operation



- **Calculate V_{out} for the case A=B=0V**

  P-ch device is "on" (R_{DS} = 75 Ω)

  N-ch device is "off" (R_{DS} = 500,000 Ω)

  V_{out} = 5 x (500,000 / 500,075) ≈ 4.999 V

  $P_{dissipation}$ = 5^2 / 500,075 ≈ 0.05 mW

- **Calculate V_{out} for the case A=B=5V**

  P-ch device is "off" (R_{DS} = 500,000 Ω)

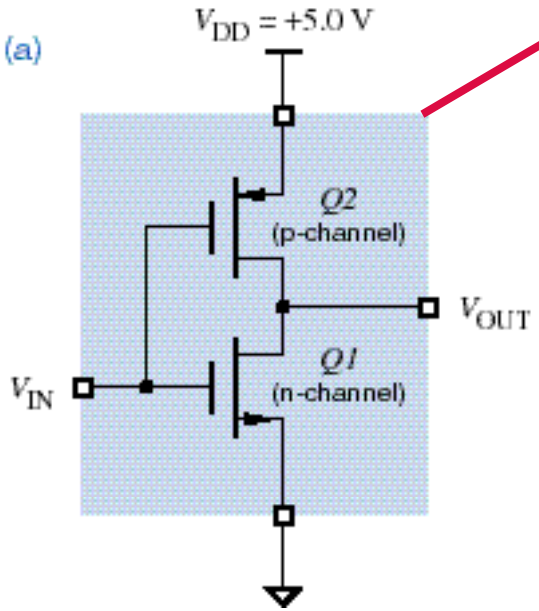
  N-ch device is "on" (R_{DS} = 25 Ω)

  V_{out} = 5 x (25 / 500,025) ≈ 0.00025 V

  $P_{dissipation}$ = 5^2 / 500,025 ≈ 0.05 mW

Note: Very low power dissipation for either high or low output, and very small voltage drop across "on" device (for "no load" condition)

Basic CMOS Inverter Circuit



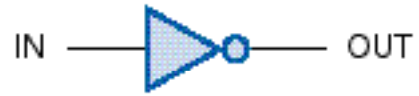
circuit diagram

(b)

V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

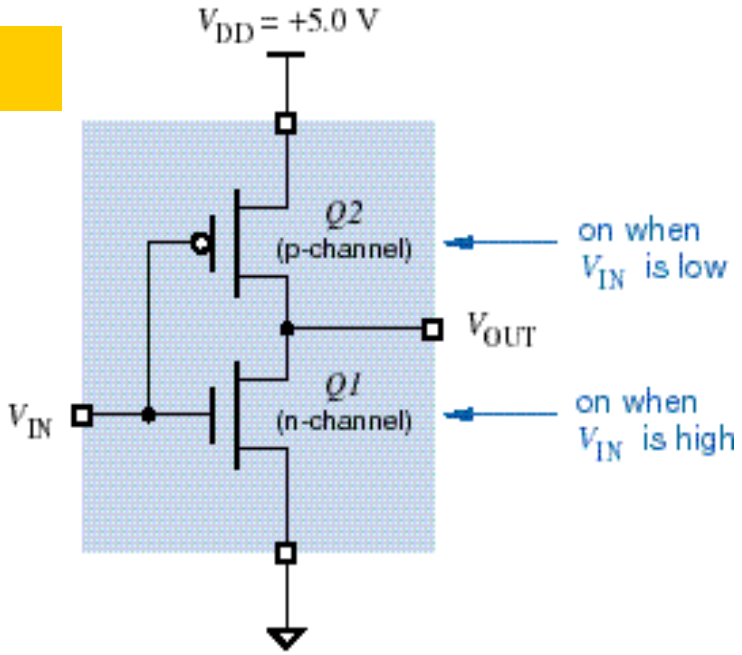
function ("truth") table

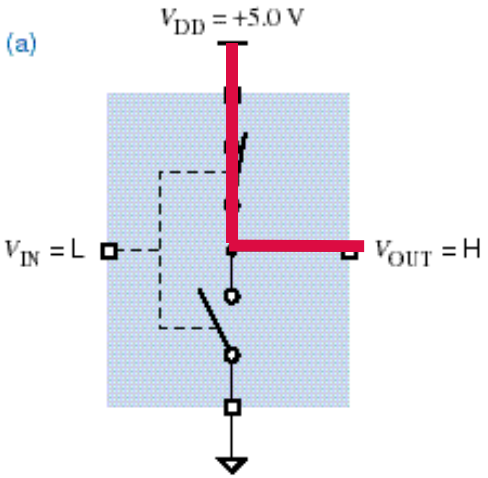
(c)

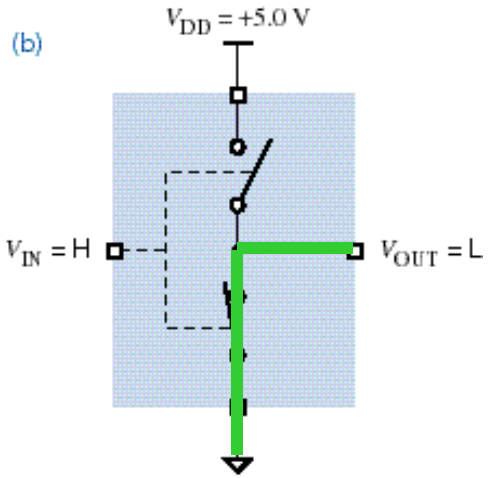


logic symbol

logical behavior

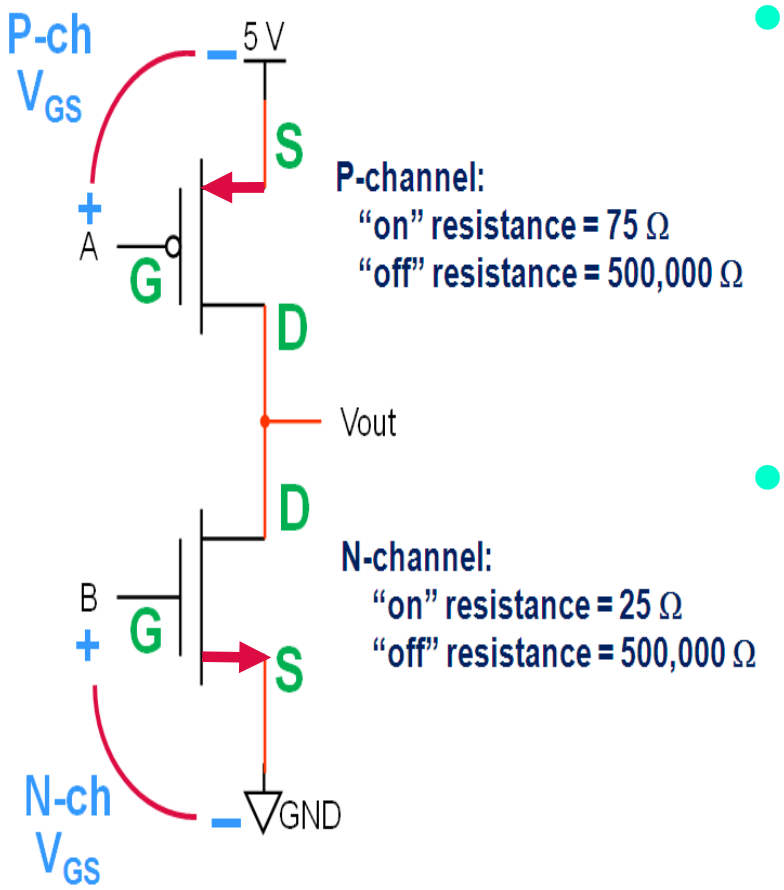






switch analogy

Example: "Non-Inverter" Operation



- **Calculate V_{out} for the case A=0, B=5 V**

  P-ch device is "on" (R_{DS} = 75 Ω)

  N-ch device is "on" (R_{DS} = 25 Ω)

  V_{out} = 5 x (25 / 100) = 1.25 V

  $P_{dissipation}$ = 5^2 / 100 = 250 mW

- **Calculate V_{out} for the case A=5V, B=0**

  P-ch device is "off" (R_{DS} = 500,000 Ω)

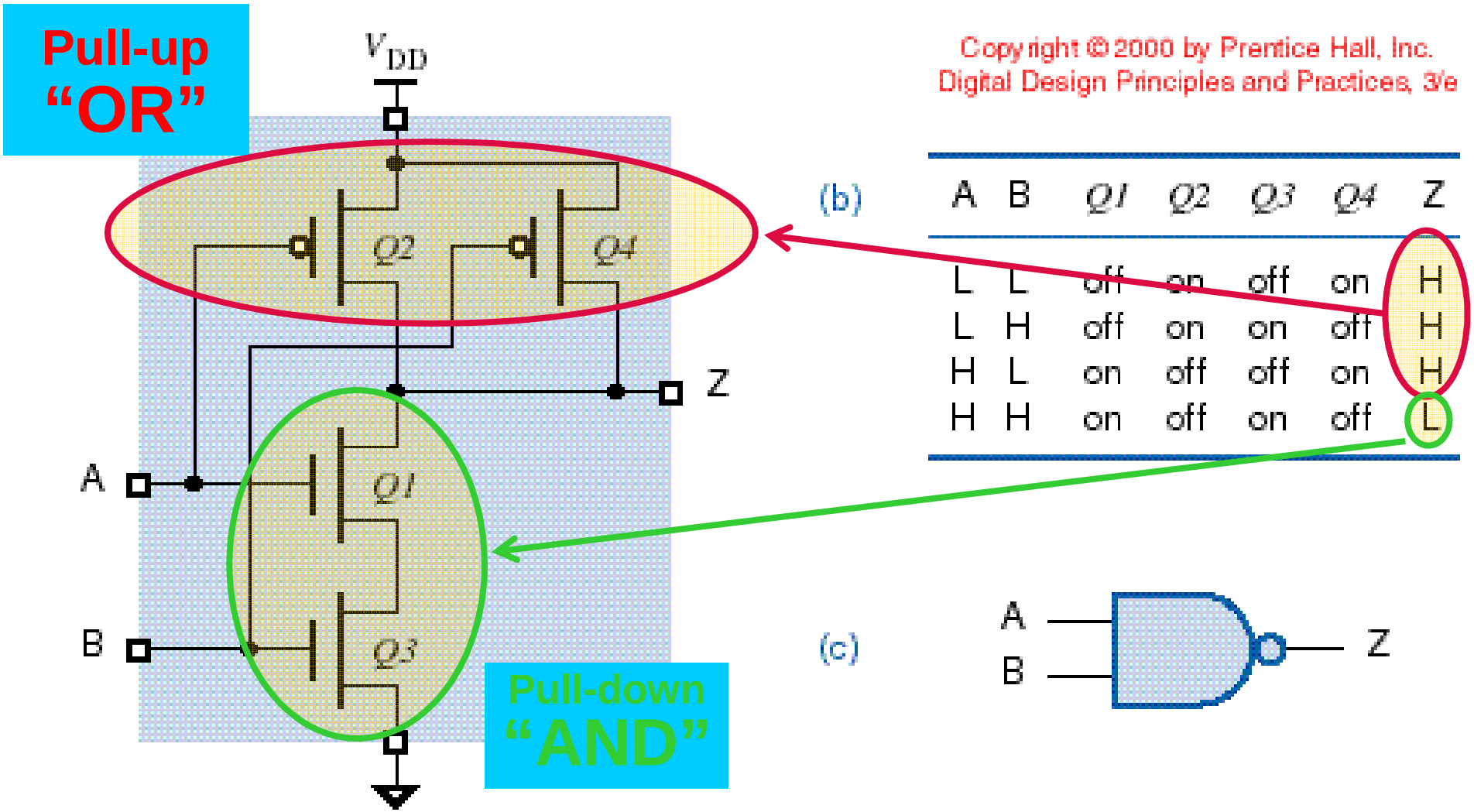
  N-ch device is "off" (R_{DS} = 500,000 Ω)

  V_{out} = 5 x (500,000 / 1,000,000) = 2.5 V

  $P_{dissipation}$ = 5^2 / 1,000,000 = 0.025 mW

Question: What would you call each of these cases?

Basic CMOS NAND Gate



A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

Illustration of “Fighting”

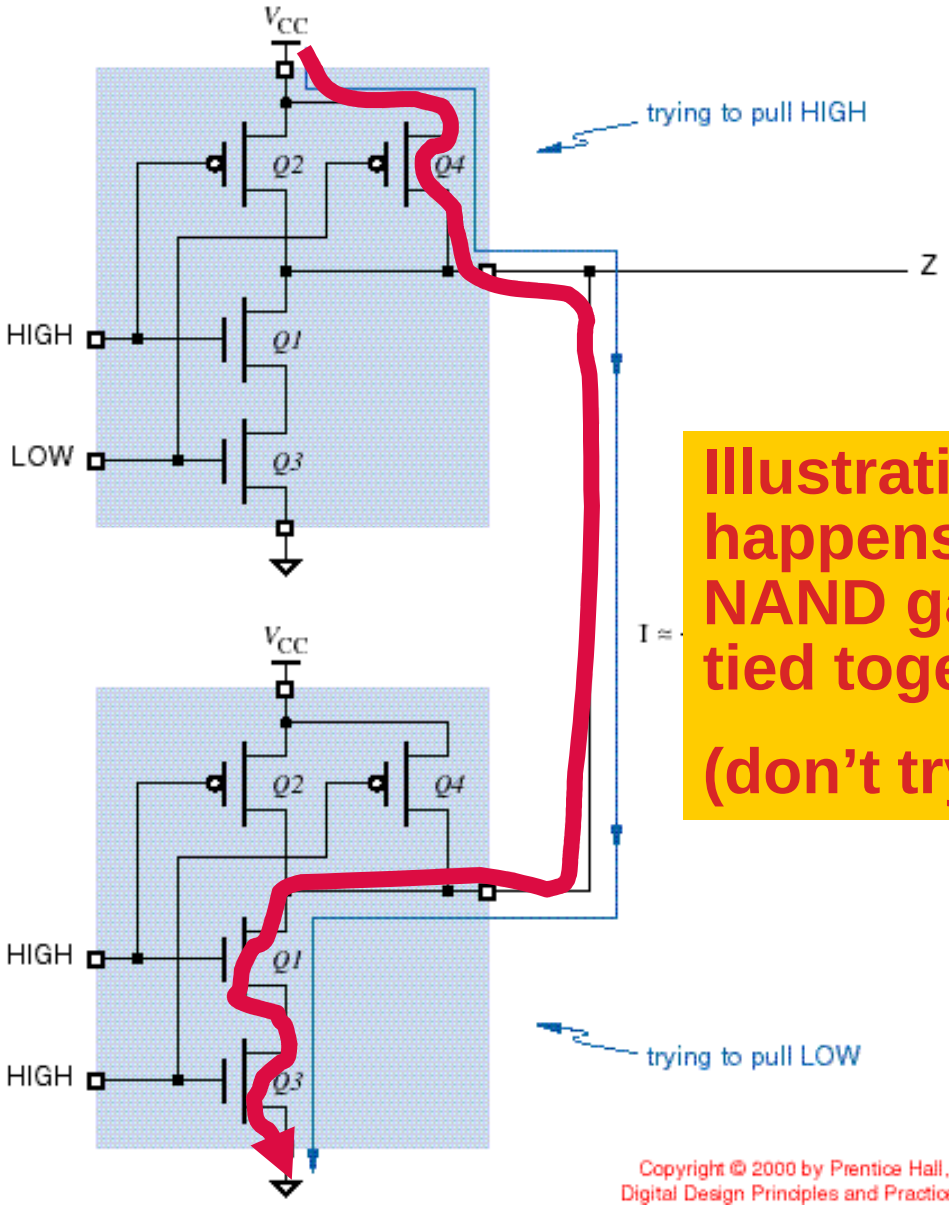
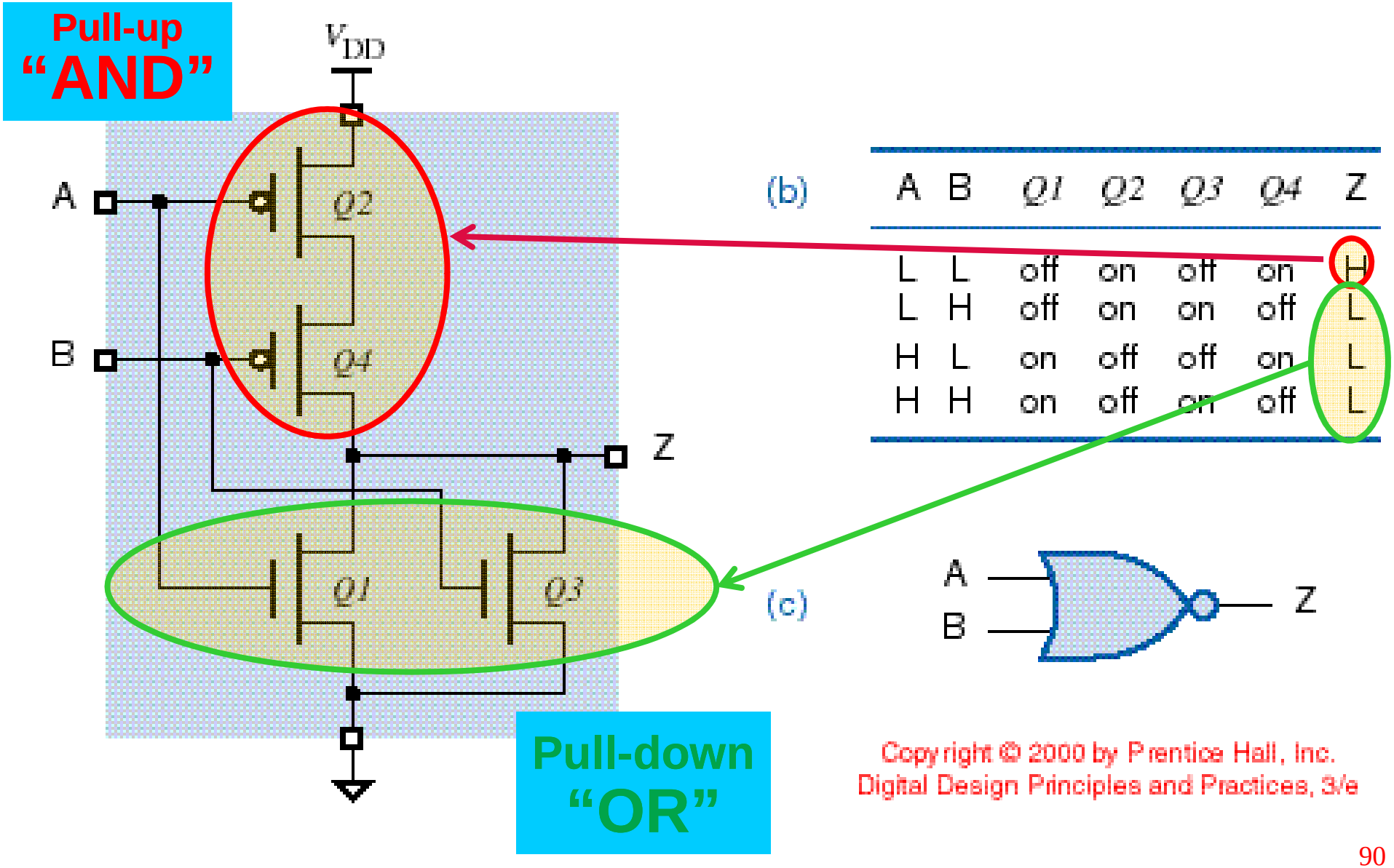


Illustration of what happens if two CMOS NAND gate outputs are tied together…

(don’t try this at home!)

Basic CMOS NOR Gate

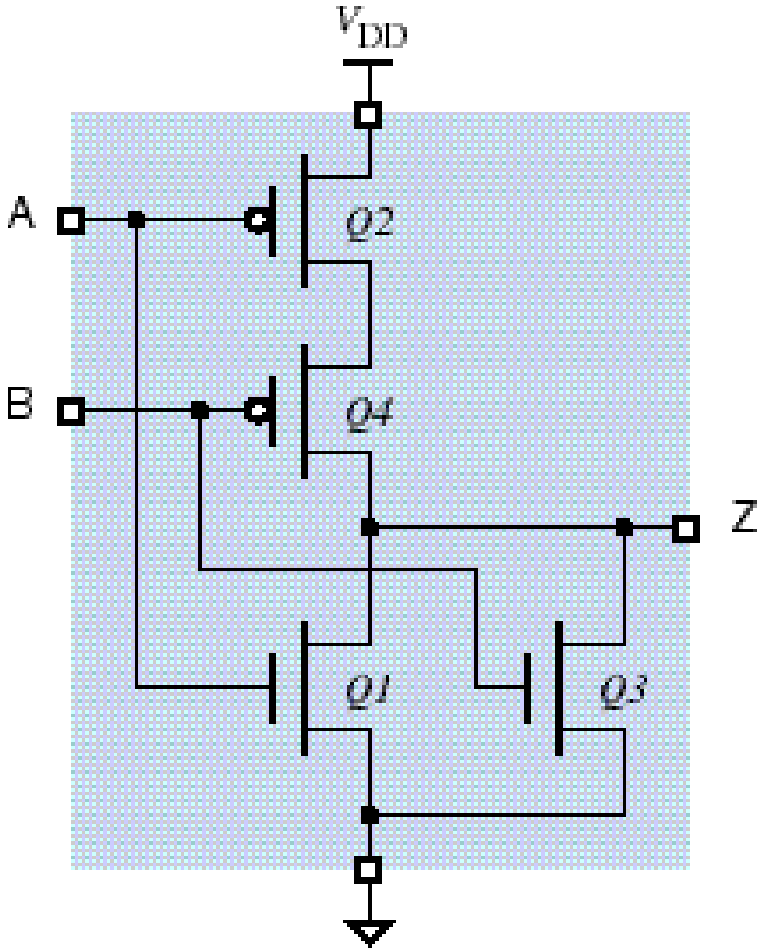


A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

Fan-in

- **Definition: The number of inputs a gate can have in a particular logic family is called the logic family's *fan-in***
- **CMOS gates with more than two inputs can be obtained by extending the "series-parallel" circuit designs (e.g., for NAND and NOR gates) illustrated previously**
- **In practice, the additive "on" resistance of series transistors limits the fan-in of CMOS gates to a relatively small number**
- **Gates with a large number of inputs can be made faster and smaller by cascading gates with fewer inputs**

Example - Expand the fan-in of a 2-input NOR gate to 3 inputs



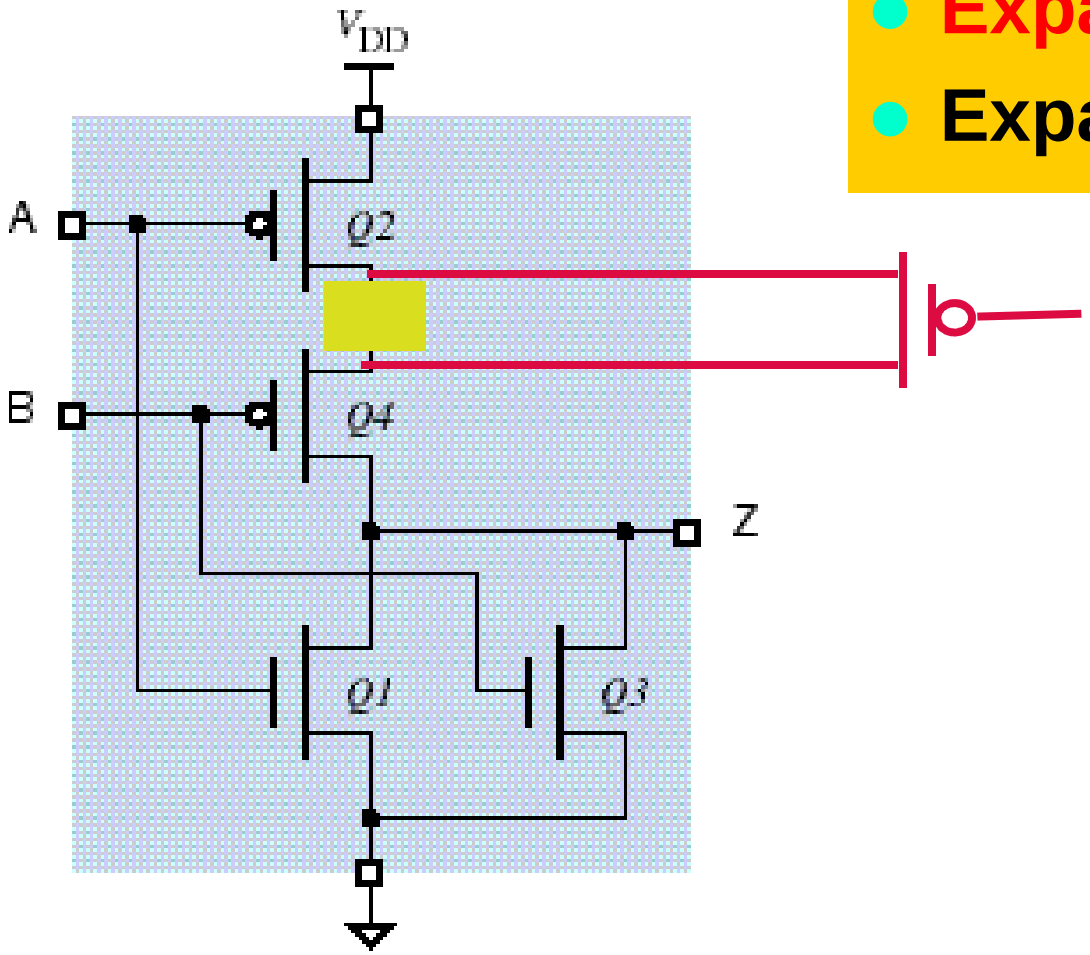
Method:

- **Expand serial chain**
- **Expand parallel train**

Example - Expand the fan-in of a 2-input NOR gate to 3 inputs

Method:

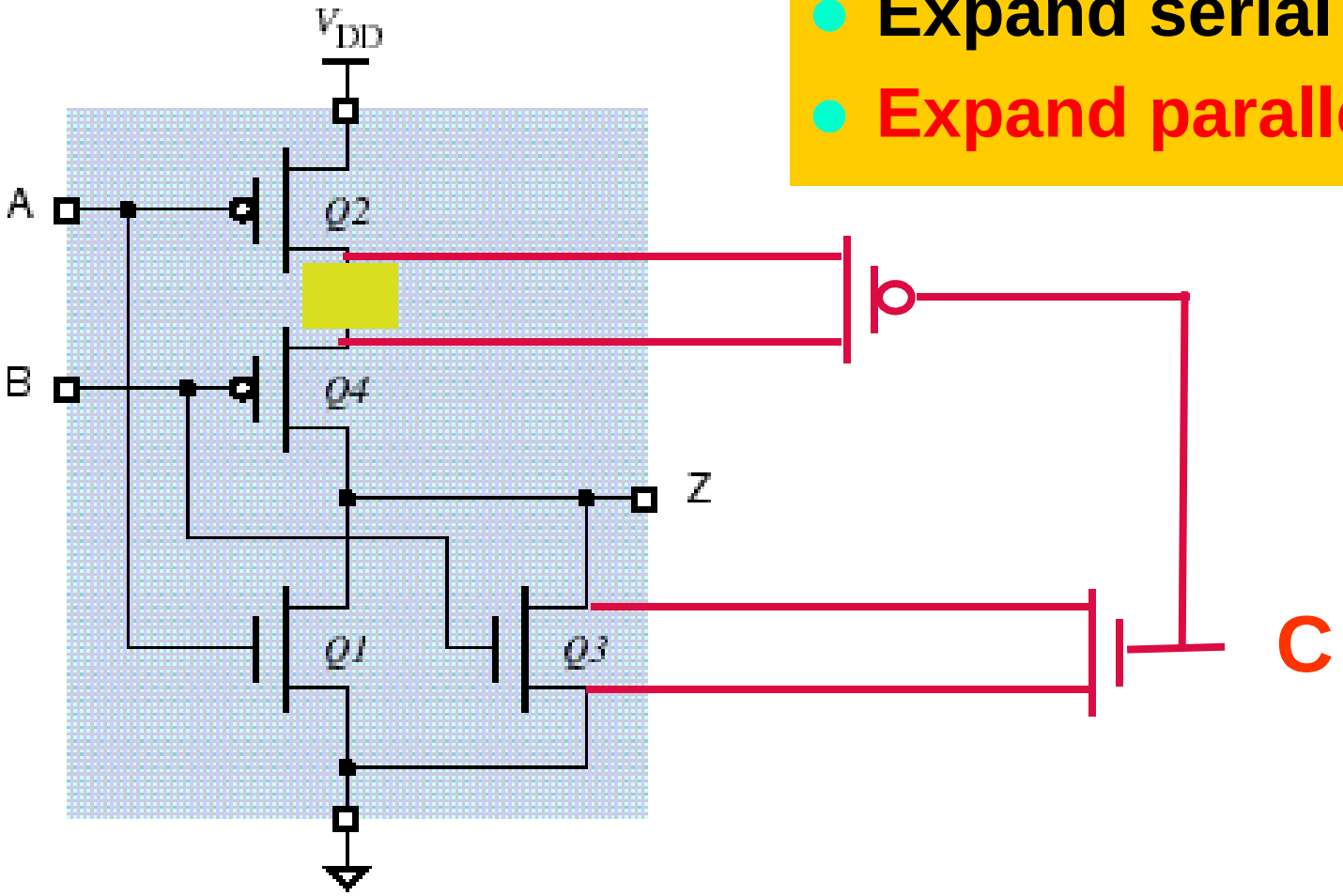
- **Expand serial chain**
- **Expand parallel train**



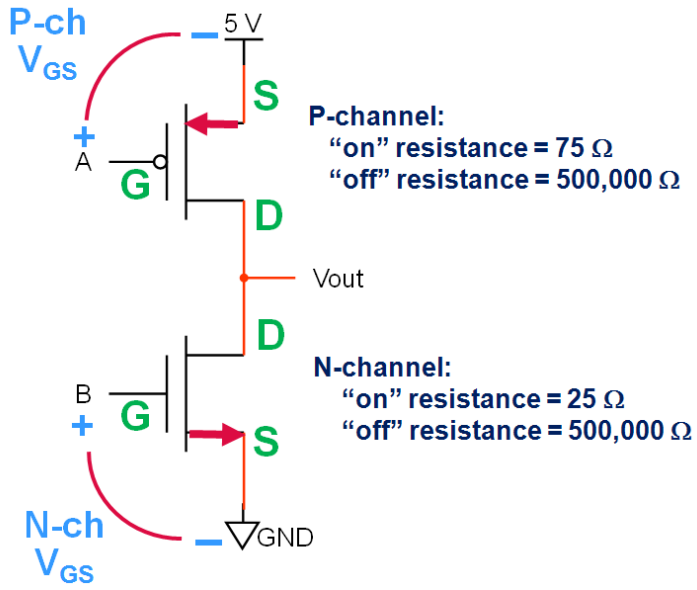
Example - Expand the fan-in of a 2-input NOR gate to 3 inputs

Method:

- **Expand serial chain**
- **Expand parallel train**



Clicker Quiz



1. Which of the following input combinations will cause a maximum amount of power dissipation?

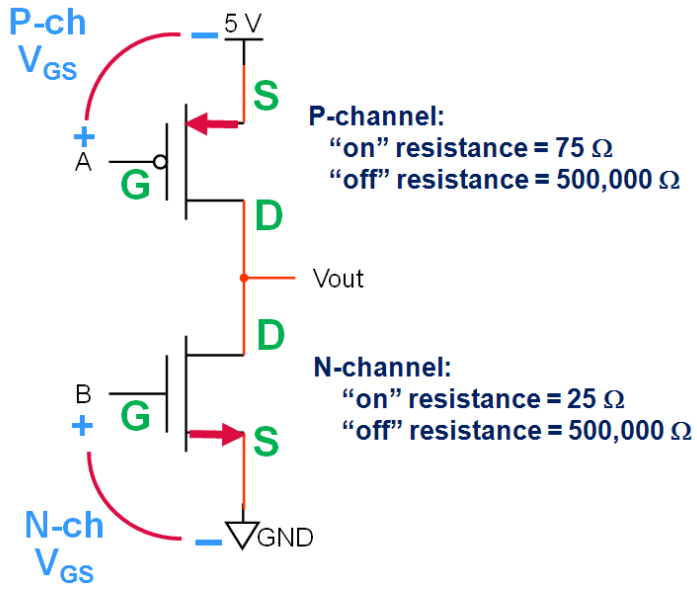
A. A=0V, B=0V

B. A=0V, B=5V

C. A=5V, B=0V

D. A=5V, B=5V

E. none of the above



2. Which of the following input combinations will cause a minimum amount of power dissipation?

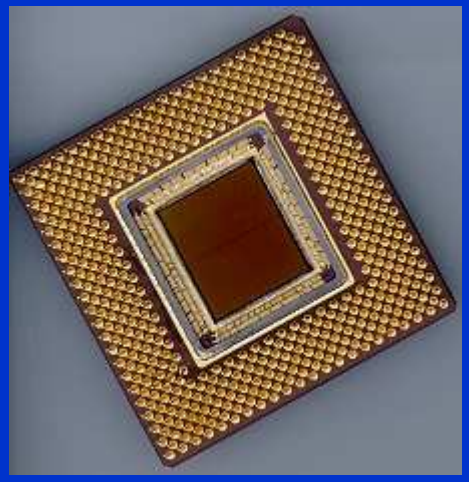
A. A=0V, B=0V

B. A=0V, B=5V

C. A=5V, B=0V

D. A=5V, B=5V

E. none of the above



Introduction to Digital System Design

Module 1-E

Logic Levels and Noise Margins

Reading Assignment:

DDPP 4th Ed., pp. 96-103

Learning Objectives:

- **Identify key information contained in a logic device data sheet**
- **Calculate the DC noise immunity margin of a logic circuit and describe the consequences of an insufficient margin**
- **Describe the consequences of a "non-ideal" voltage applied to a logic gate input**
- **Describe how unused ("spare") CMOS inputs should be terminated**

Outline

- Overview
- Data sheets
- Noise
- Logic levels and noise margins
- Non-ideal inputs
- Unused (“spare”) inputs
- Electrostatic discharge

Overview

- **Objective:** To be able to design ***real*** circuits using CMOS or other logic families
  - need to ensure that the "***digital abstraction***" is valid for a given circuit
  - need to provide adequate engineering ***design margins*** to ensure that a circuit will work properly under a variety of conditions
  - need to be able to read and understand data sheets and specifications, in order to create reliable and robust real-world circuits and systems

Data Sheet for a Typical CMOS Device

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE
The following conditions apply unless otherwise specified:
Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0$ V		—	—	−1	μA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	−0.7	−1.2	V
I_{OS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	−35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20$ μA	4.4	4.499	—	V
			$I_{OH} = -4$ mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	$I_{OL} = 20$ μA	—	.001	0.1	V
			$I_{OL} = 4$ mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	μA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

NOTES:

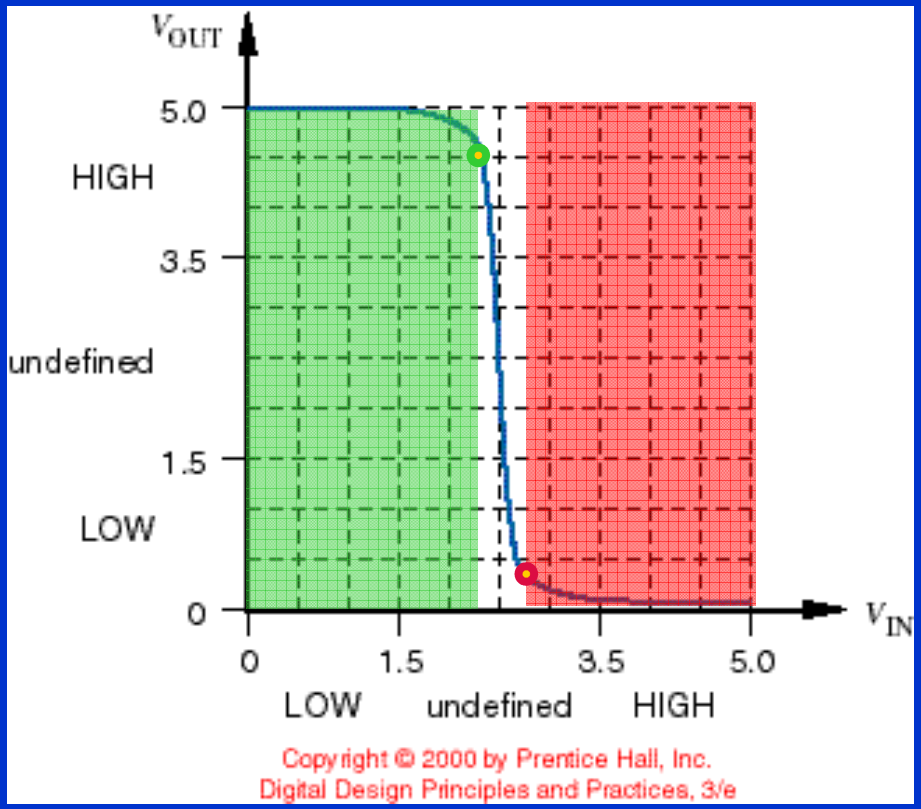
1. *For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.*
2. *Typical values are at $V_{CC} = 5.0$ V, +25°C ambient.*
3. *Not more than one output should be shorted at a time. Duration of short-circuit test should not exceed one second.*
4. *This parameter is guaranteed but not tested.*

Noise

- **The main reason for providing engineering design margins is to ensure proper operation in the presence of *noise***
- **Examples of noise sources:**
  - **cosmic rays**
  - **magnetic fields generated by machinery**
  - **power supply disturbances**
  - **the "*switching action*" of the logic circuits themselves**

Logic Levels and Noise Margins

- **Typical input-output transfer characteristic of a CMOS inverter**



<u>Problem</u>:
Typical*, NOT *guaranteed!

Logic Levels and Noise Margins

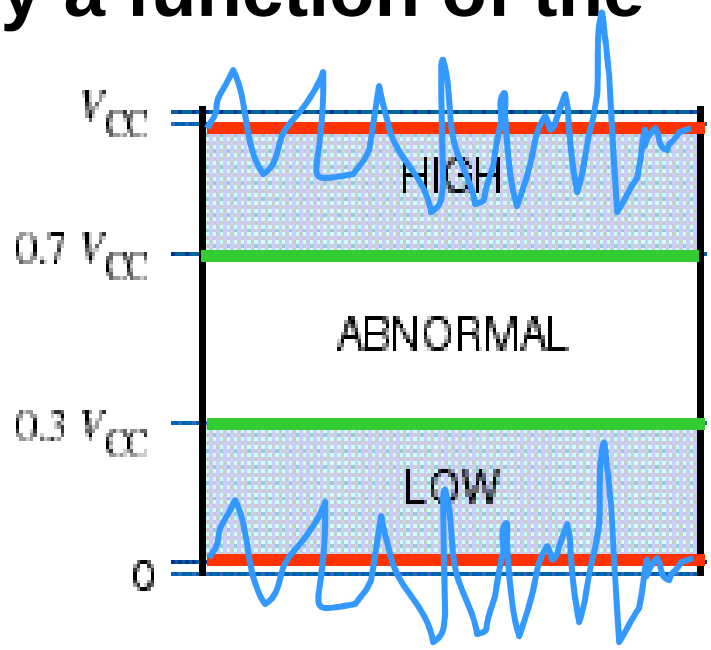
- **Factors that cause the transfer characteristic to vary**
  - **power supply voltage**
  - **temperature**
  - **output loading**
  - **conditions under which a device was fabricated**
- **Sound engineering practice dictates that we use more "*conservative*" specifications for LOW and HIGH**

Logic Levels and Noise Margins

- **Definitions:**
  - $V_{OH_{min}}$ - the minimum output voltage in the HIGH state
  - $V_{IH_{min}}$ - the minimum input voltage guaranteed to be recognized as a HIGH
  - $V_{IL_{max}}$ - the maximum input voltage guaranteed to be recognized as a LOW
  - $V_{OL_{max}}$ - the maximum output voltage in the LOW state

Logic Levels and Noise Margins

- **CMOS levels are typically a function of the power supply "rails"**
  - **$V_{OH_{min}}$ Vcc – 0.1v**
  - **$V_{IH_{min}}$ 70% of Vcc**
  - **$V_{IL_{max}}$ 30% of Vcc**
  - **$V_{OL_{max}}$ GND + 0.1v**



DC noise margin is a measure of how much noise it takes to *corrupt* a worst-case output voltage into a value that may not be recognized properly by an input

Data Sheet for a Typical CMOS Device

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:

Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

Logic Levels and Noise Margins

- **Calculation of DC noise margin (or the "noise immunity margin")**

$$DCNM = \min (V_{OH_{min}} - V_{IH_{min}}, V_{IL_{max}} - V_{OL_{max}})$$

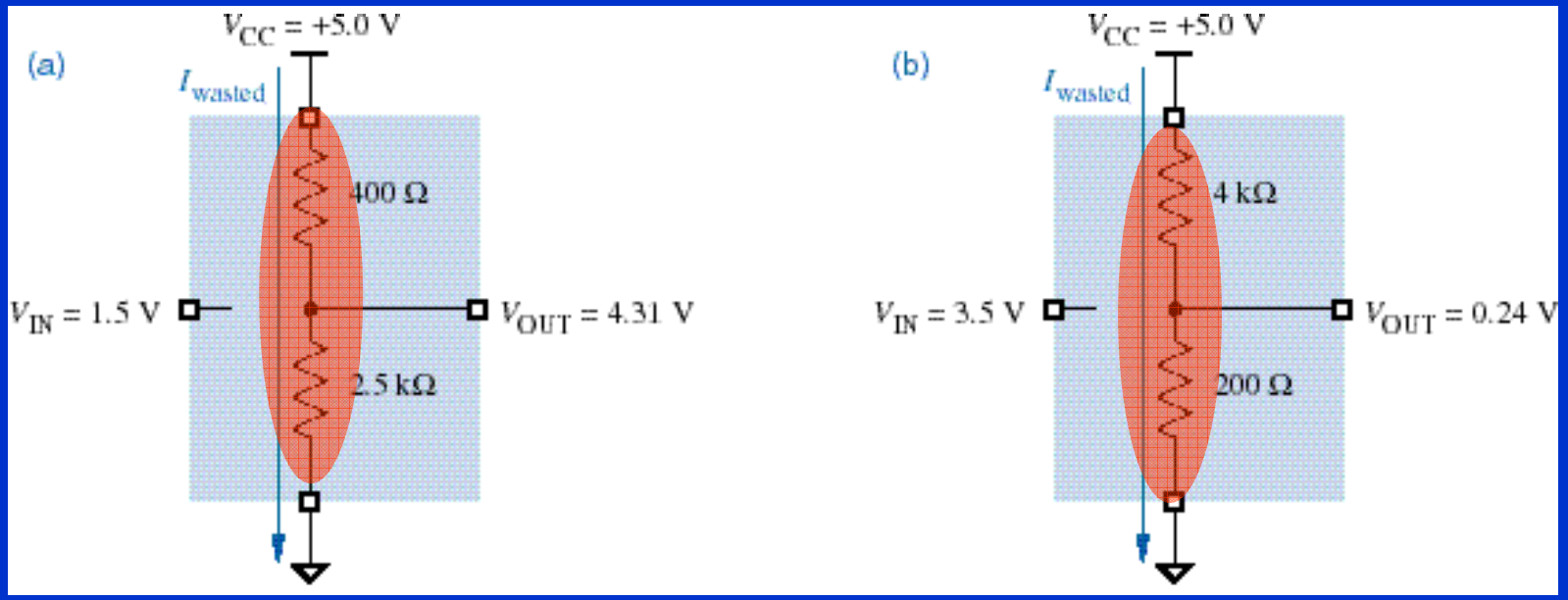
- **Example: HC-series CMOS**

$$DCNM = \min (4.4 - 3.15, 1.35 - 0.1)$$

$$= 1.25 \text{ v}$$

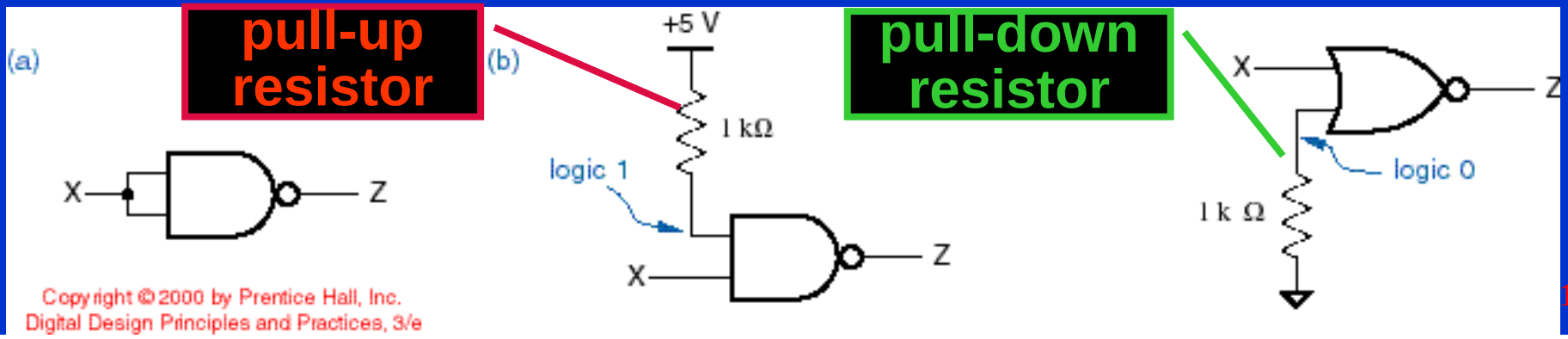
Non-ideal Inputs

- **If the inputs to a CMOS circuit are not close to the Vcc / GND rails, the "on" transistor may not be *fully on* and the "off" transistor may not be *fully off* – causing power dissipation of the device to *increase***



Unused ("Spare") Inputs

- **Unused ("spare") CMOS inputs should *never* be left unconnected ("floating")**
- **A small amount of circuit noise can temporarily make a floating input look HIGH**
- **Instead, unused inputs should be:**
  - **tied to another input of the same gate**
  - **tied HIGH (for AND and NAND gates)**
  - **tied LOW (for OR and NOR gates)**



Electrostatic Discharge

- **CMOS device inputs are subject to damage from electrostatic discharge (ESD)**
- **Apply these precautions in lab:**
  - **before handling a CMOS device, touch a source of *earth ground***
  - **transport CMOS devices in *conductive* bags, foam, or tubes**
  - **handle circuit boards containing CMOS devices by the *edges*; touch a ground terminal on the board to earth ground before "poking around with it"**

Clicker Quiz

1. For CMOS gates, V_{IHmin} is typically:

A. 10% of the supply voltage (Vcc)

B. 30% of the supply voltage (Vcc)

C. 50% of the supply voltage (Vcc)

D. 70% of the supply voltage (Vcc)

E. 90% of the supply voltage (Vcc)

2. For CMOS gates, the *switching threshold* is typically:

A. **10% of the supply voltage (Vcc)**
B. **30% of the supply voltage (Vcc)**
C. **50% of the supply voltage (Vcc)**
D. **70% of the supply voltage (Vcc)**
E. **90% of the supply voltage (Vcc)**

3. If a CMOS gate input voltage is 50% of its V_{cc} (power supply) voltage, then:

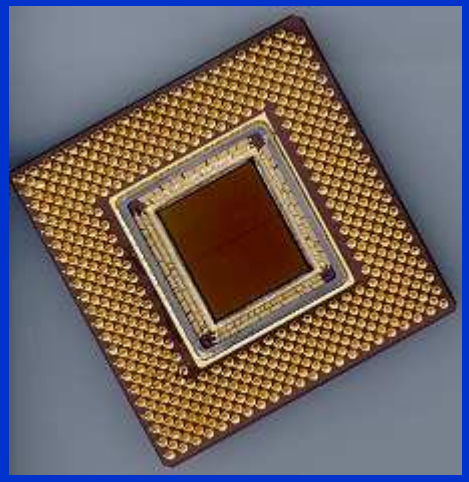
A. the logic gate will dissipate ***less* power** than it would if the input was 1% of its power supply voltage

B. the logic gate will dissipate ***less* power** than it would if the input was 99% of its power supply voltage

C. the logic gate will dissipate ***more* power** than it would if the input was *either* 1% *or* 99% of its power supply voltage

D. the logic gate will dissipate ***no* power**

E. none of the above



Introduction to Digital System Design

Module 1-F
Current Sourcing and Sinking

Reading Assignment:

DDPP 4th Ed., pp. 103-114

Learning Objectives:

- **Identify key information contained in a logic device data sheet**
- **Describe the relationship between logic gate output voltage swing and current sourcing/sinking capability**
- **Describe the difference between "DC loads" and "CMOS loads"**
- **Calculate V_{OL} and V_{OH} of a logic gate based on the "on" resistance of the active device and the amount of current sourced (I_{OH}) or sunk (I_{OL}) by the gate output**
- **Calculate logic gate fan-out and identify a practical lower limit**
- **Calculate the value of current limiting resistor needed for driving an LED**
- **Describe the deleterious effects associates with loading a gate output beyond its rated specifications**

Outline

- Sourcing and sinking current
- CMOS and DC loads
- Fan-out
- Driving LEDs
- Effects of excessive loading

Sourcing and Sinking Current

- **CMOS gate inputs have a very high impedance and consume very little current from the circuits that drive them**
  - **I_{IL} the maximum current that flows into the input in the LOW state**
  - **I_{IH} the maximum current that flows into the input in the HIGH state**

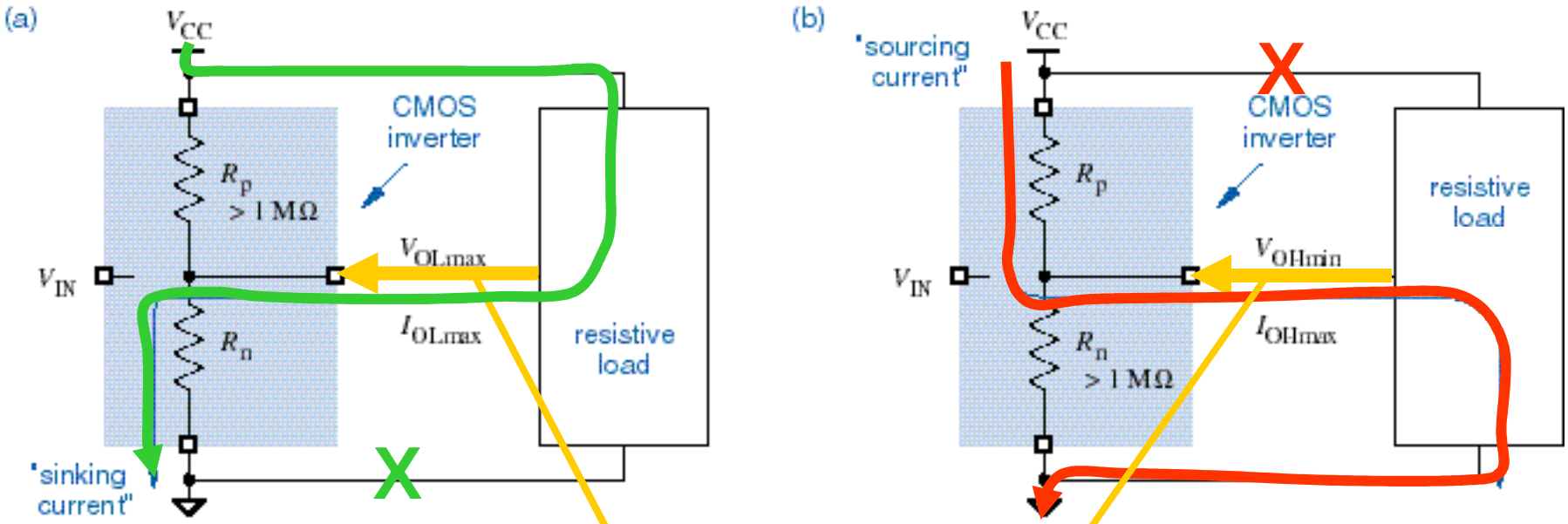
For CMOS logic, the input current is *very small* (about one microamp) – it takes very little power to maintain a CMOS input in either the HIGH or LOW state

Sourcing and Sinking Current

- **IC manufacturers specify a maximum load for the output in each state (HIGH or LOW) and guarantee a worst-case output voltage for that load**
  - **$I_{OL_{max}}$ - the maximum current that the output can "sink" in the LOW state while still maintaining an output voltage *no greater than* $V_{OL_{max}}$**
  - **$I_{OH_{max}}$ - the maximum current that the output can "source" in the HIGH state while still maintaining an output voltage *no less than* $V_{OH_{min}}$**

Sourcing and Sinking Current

- **Circuit definitions of $I_{OL_{max}}$ and $I_{OH_{max}}$**



sinking current (positive)

current arrow

NOTE:
Convention is for the input/output current arrows to point "in"

sourcing current (negative)

Sourcing and Sinking Current

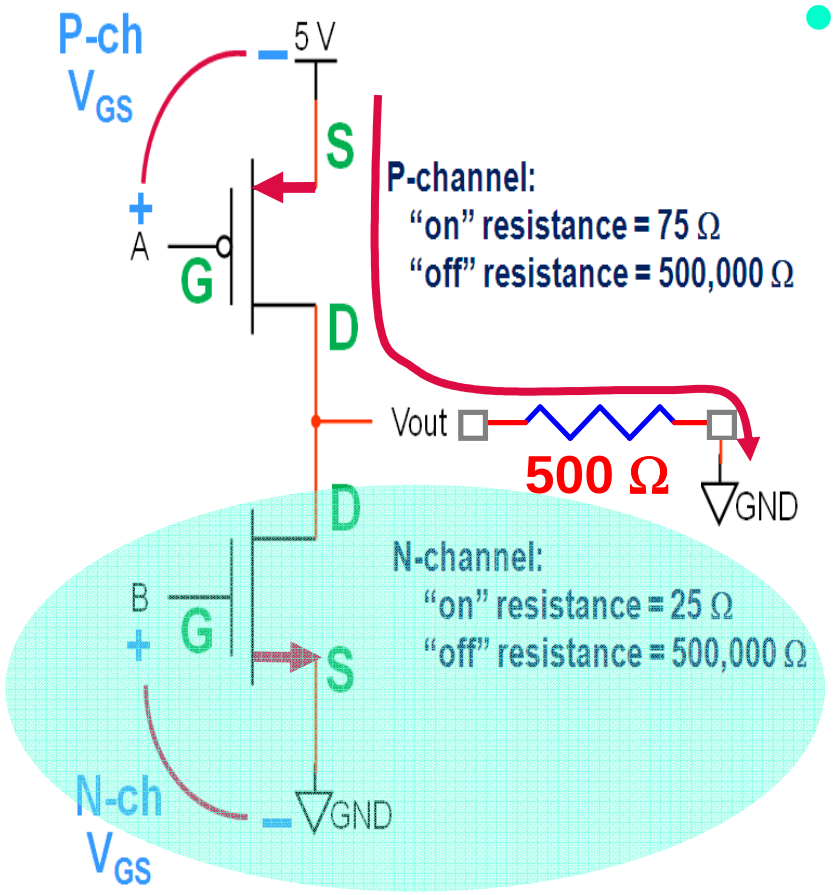
- **Often times gate outputs need to drive devices that require a non-trivial amount of current to operate – called a *resistive* load or *DC* load**
- **When driving a resistive load, the output of a CMOS circuit is not nearly as *ideal* as described previously**
- **In either output state, the CMOS output transistor that is "on" has a non-zero resistance, and a load connected to its output terminal will cause a voltage drop across this resistance**

CMOS and DC Loads

- **Consequently, most CMOS devices have two sets of loading specifications:**
  - **"CMOS loads" – device output connected to other CMOS inputs, which require *very little current* to recognize a "high" input or "low" input**
  - **"DC loads" – device output connected to resistive loads (devices that consume significant current, typically several milliamps)**

Note: With "DC loads" the output voltage swing of a CMOS circuit may significantly *degrade*

Example: Inverter - Current Sourcing



- **Calculate V_{OH} and I_{OH} for A=B=0V**

Current SOURCING configuration

DC Load is 500 Ω resistor between V_{out} and GND

P-ch device is "on" (R_{DS} = 75 Ω)

N-ch device is "off" (R_{DS} = 500,000 Ω)

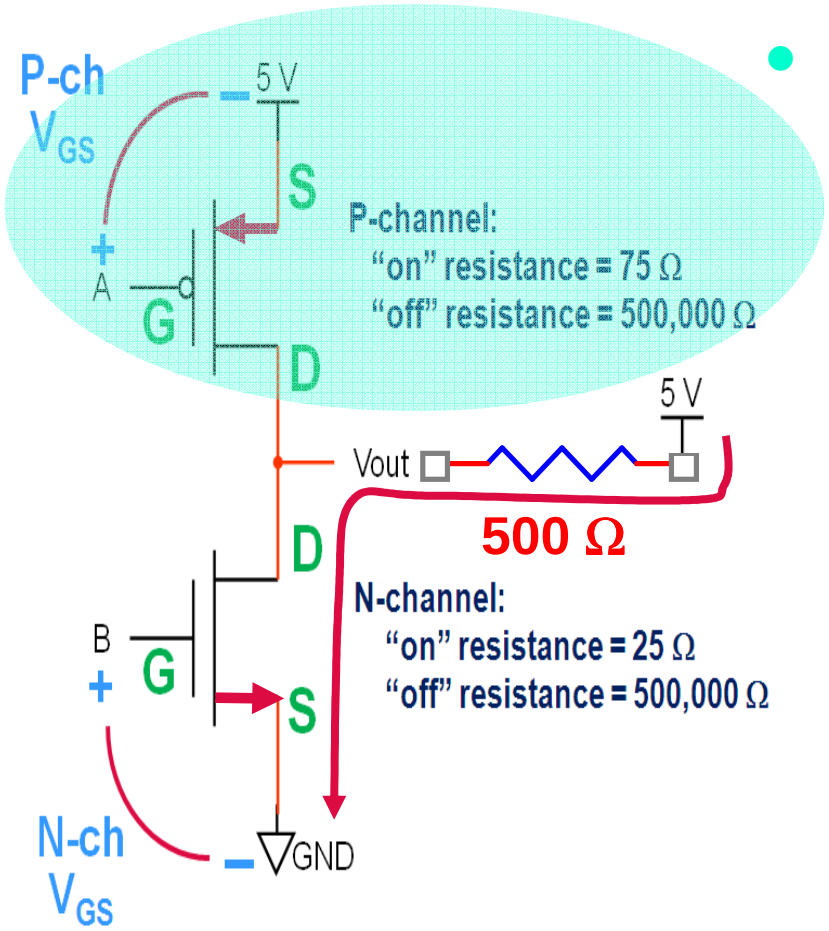
Load impedance is 500,000 Ω in parallel with 500 Ω ≈ 500 Ω

V_{OH} ≈ 5 x (500 / 575) ≈ 4.35 V

I_{OH} ≈ 5 / (75 + 500) ≈ 0.0087 A (8.7 mA)

Note: In the current SOURCING configuration, the inverter output is active high ("asserted high"); the N-channel pull-down virtually "disappears"

Example: Inverter - Current Sinking



- **Calculate V_{OL} and I_{OL} for A=B=5V**

Current SINKING configuration

DC Load is 500 Ω resistor between 5 V supply and V_{out}

P-ch device is "off" (R_{DS} = 500,000 Ω)

N-ch device is "on" (R_{DS} = 25 Ω)

Load impedance is 500,000 Ω in parallel with 500 Ω ≈ 500 Ω

V_{OL} ≈ 5 x (25 / 525) ≈ 0.24 V

I_{OL} ≈ 5 / (25 + 500) ≈ 0.0095 A (9.5 mA)

Note: In the current SINKING configuration, the inverter output is active low ("asserted low"); the P-channel pull-up virtually "disappears"

Fan-out

- **Definition: The number of gate inputs that a gate output can drive *without exceeding* its worst-case loading specifications**
  - **depends on characteristics of both the output device and the inputs being driven**
  - **must be examined for both the "sourcing" and "sinking" cases**
  - **limitations due to capacitive loading (impact on rise/fall times may be more of a limiting factor than fan-out or DCNM)**

$$\text{Fan-out} = \min\left(I_{OH_{max}} / I_{IH}, I_{OL_{max}} / I_{IL} \right)$$

Data Sheet for a Typical CMOS Device

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE
The following conditions apply unless otherwise specified:
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I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0$ V		—	—	−1	μA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	−0.7	−1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	−35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20$ μA	4.4	4.499	—	V
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			$I_{OL} = 4$ mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	μA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

Fan-out Calculation

- **Example: HC-series CMOS**

$$\text{Fan-out} = \min\left(I_{OH_{max}} / I_{IH}, I_{OL_{max}} / I_{IL} \right)$$

$$= \min(0.02\ \text{mA} / 0.001\ \text{mA}, -0.02\ \text{mA} / -0.001\ \text{mA})$$

$$= 20$$

Note: DC fan-out is considerably greater in this case if the output voltage swing is degraded … *but* DCNM is lower and signal transitions times are longer, causing speed degradation

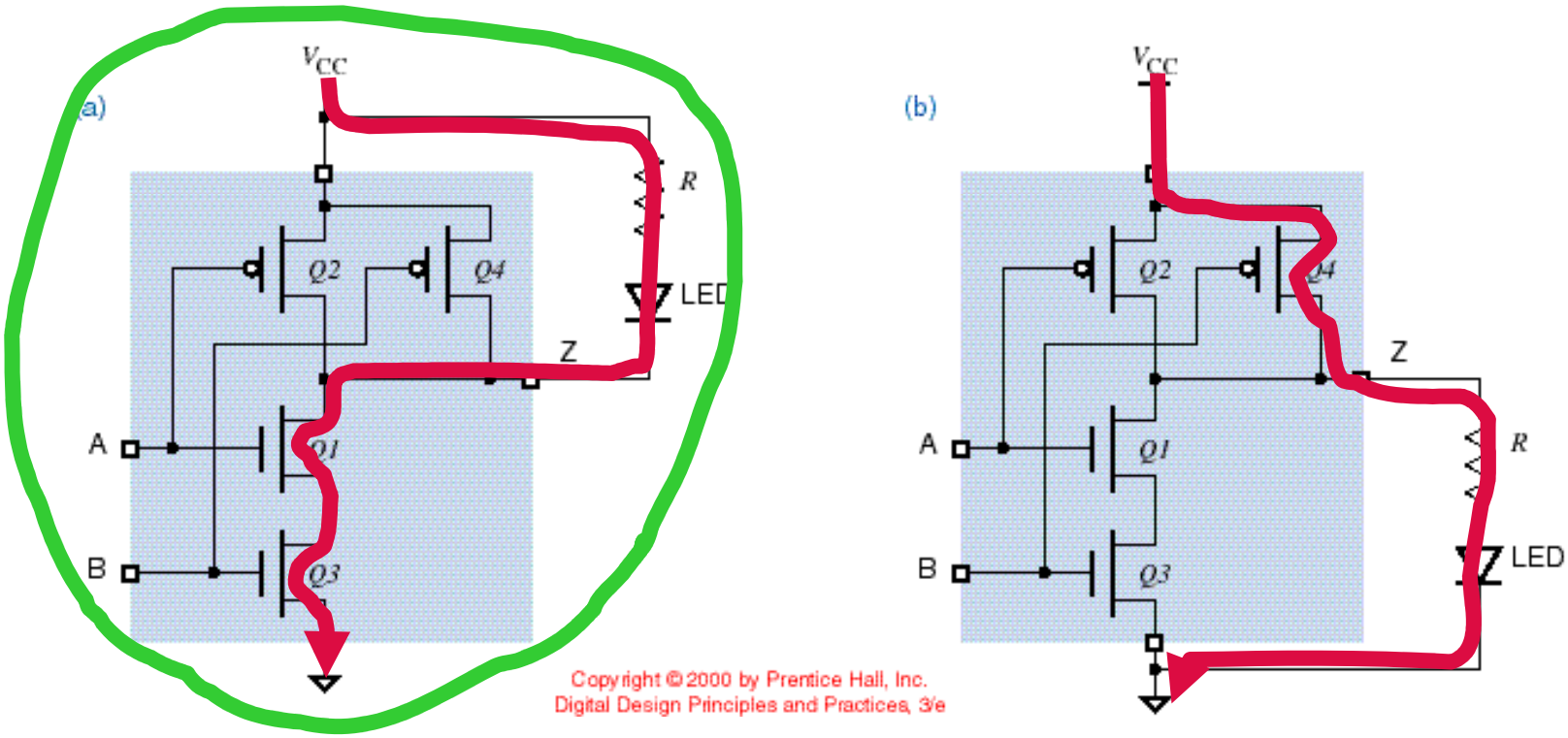
Practical Fan-out

- In a practical application, a gate output may drive a "mixture" of loads
- **HIGH-state fan-out** – The sum of the I_{IHmax} values of all the driven inputs must be *less than or equal* to the I_{OHmax} of the driving output
- **LOW-state fan-out** – The sum of the I_{ILmax} values of all the driven inputs must be *less than or equal* to the I_{OLmax} of the driving output

The "practical" fan-out is the *minimum* of the HIGH- and LOW-state fan-outs

Driving LEDs

- **LEDS represent "DC loads" and can be interfaced to a CMOS gate output either by sinking current (LOW output) or sourcing current (HIGH output)**



<u>Question</u>: Which method is generally preferred?

Example: **Based on the data provided in Table 3-3 of the course text, calculate the value of the LED current limiting resistor for the worst case *current sinking* configuration. Also calculate the amount of power dissipated by the current limiting resistor. Assume V_{LED} is 1.9 volts.**

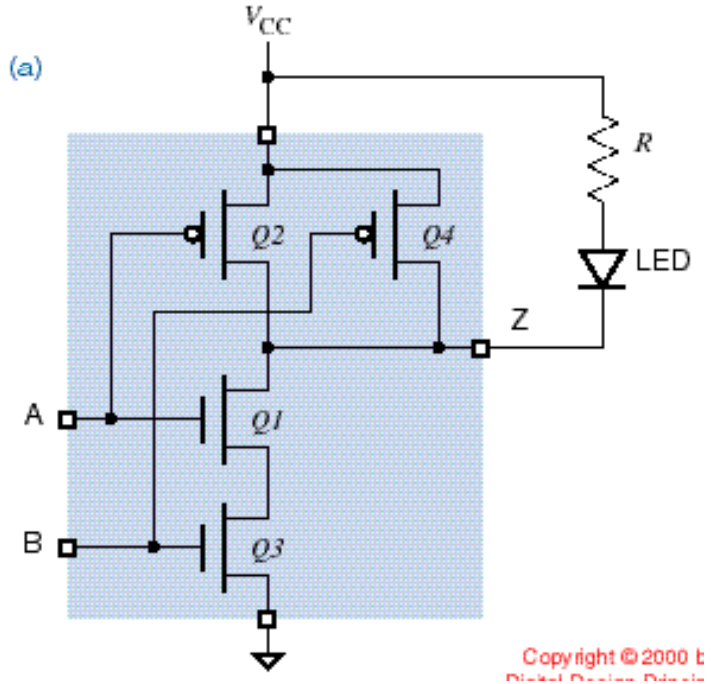


Table 3.3 from *DDPP*

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE
The following conditions apply unless otherwise specified:
Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$

Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	µA
I_{IL}	Input LOW current	V_{CC} = Max., V_I = 0 V		—	—	−1	µA
V_{IK}	Clamp diode voltage	V_{CC} = Min., I_N = −18 mA		—	−0.7	−1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	−35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	I_{OH} = −20 µA	4.4	4.499	—	V
			I_{OH} = −4 mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	I_{OL} = 20 µA	—	.001	0.1	V
			I_{OL} = 4 mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, I_O = 0		—	2	10	µA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, C_L = 50 pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	V_{IN} = 0 V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

NOTES:

1. *For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.*
2. *Typical values are at V_{CC} = 5.0 V, +25°C ambient.*
3. *Not more than one output should be shorted at a time. Duration of short-circuit test should not exceed one second.*
4. *This parameter is guaranteed but not tested.*

SOLUTION:

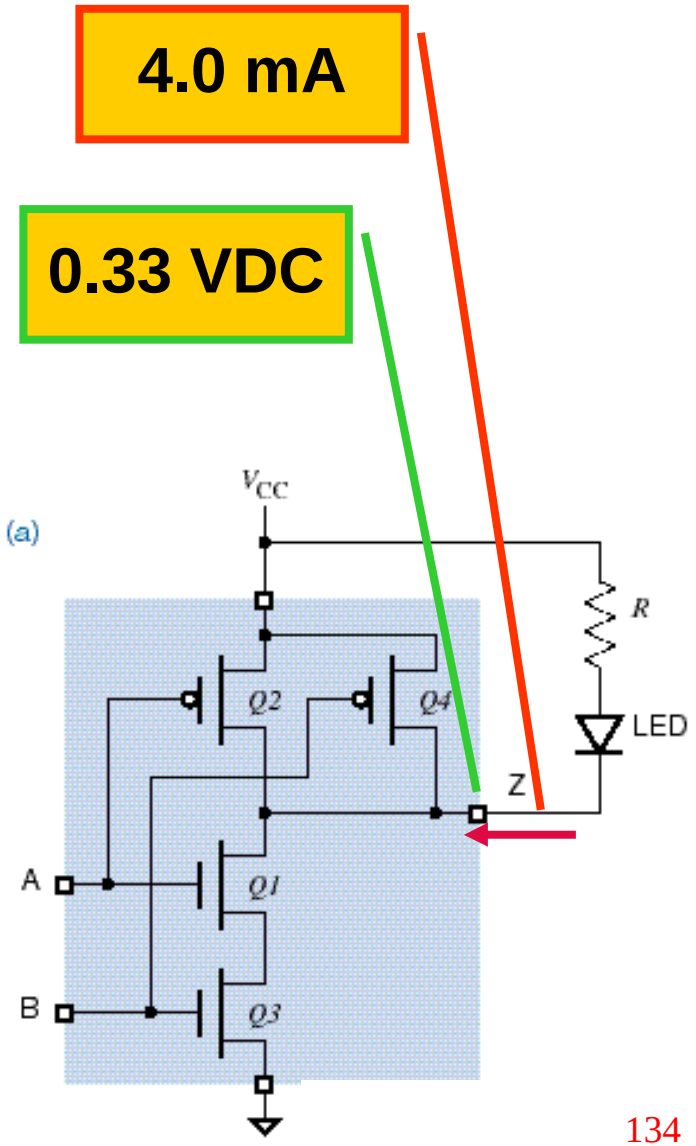
$V_R = 5.0 - V_{LED} - V_{OL} = 5.0 - 1.9 - 0.33 = 2.77$ V

NOTE: Here, use "Max" value indicated for V_{OL} of 0.33 V

$R = V_R / I_{OL} = 2.77/0.004 = 693\ \Omega$

$P_R = R \times I_{OL}^2 = 693 \times (0.004)^2 = 11.1$ milliwatts

NOTE: Can also calculate power dissipation of resistor using $V_R \times I_{OL}$ or $(V_R^2)/R$



Example: **Based on the data provided in Table 3-3 of the course text, calculate the value of the LED current limiting resistor for the worst case *current sourcing* configuration. Also calculate the amount of power dissipated by the current limiting resistor.**

Assume V_{LED} is 1.9 volts.

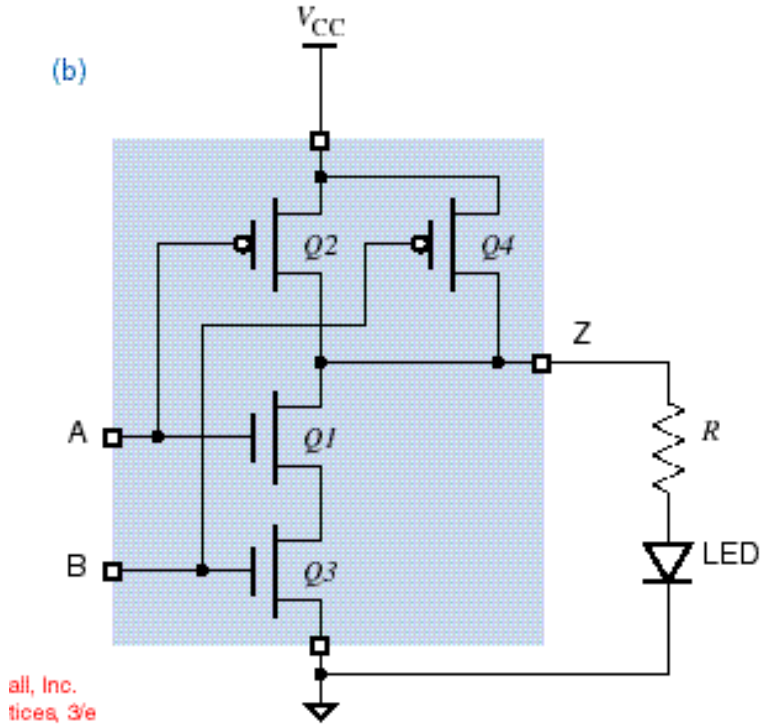


Table 3.3 from *DDPP*

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE
The following conditions apply unless otherwise specified:
Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0$ V		—	—	−1	μA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	−0.7	−1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	−35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20$ μA	4.4	4.499	—	V
			$I_{OH} = -4$ mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	$I_{OL} = 20$ μA	—	.001	0.1	V
			$I_{OL} = 4$ mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	μA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

NOTES:

1. *For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.*
2. *Typical values are at $V_{CC} = 5.0$ V, +25°C ambient.*
3. *Not more than one output should be shorted at a time. Duration of short-circuit test should not exceed one second.*
4. *This parameter is guaranteed but not tested.*

SOLUTION:

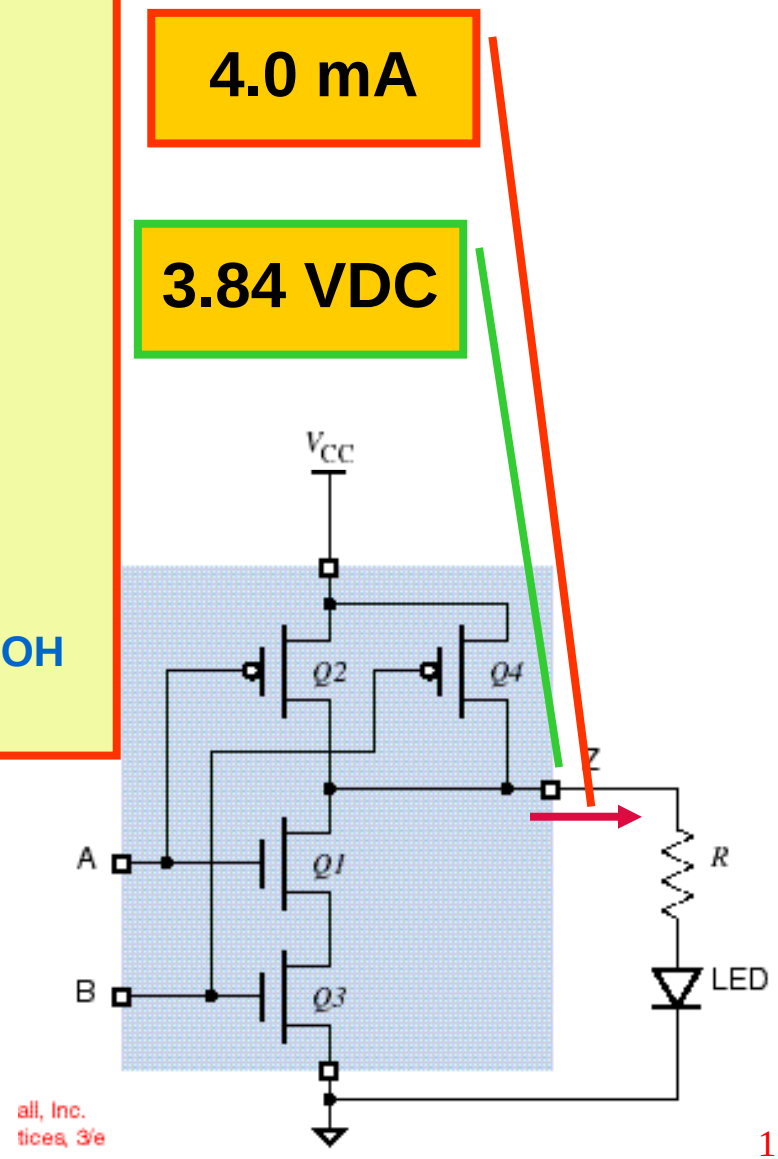
$V_R = V_{OH} - V_{LED} = 3.84 - 1.9 = 1.94$ V

NOTE: Here, use "Min" value indicated for V_{OH} of 3.84 V

$R = V_R / I_{OH} = 1.94/0.004 = 485\ \Omega$

$P_R = R \times I_{OH}^2 = 485 \times (0.004)^2 = 7.8$ milliwatts

NOTE: Can also calculate power dissipation of resistor using $V_R \times I_{OH}$ or $(V_R^2)/R$



Effects of Excessive Loading

- **Loading a gate output beyond its rated fan-out can have several deleterious effects:**
  - **in the LOW state, the output voltage (V_{OL}) may increase beyond $V_{OL_{max}}$**
  - **in the HIGH state, the output voltage (V_{OH}) may fall below $V_{OH_{min}}$**
  - **output rise and fall times may increase beyond their specifications**
  - **the operating temperature of the device may increase, thereby *reducing* the *reliability* of the device and eventually causing device *failure***

Example – DCNM, Family A → Family B

Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 μA	I_{IL} = -0.4 μA

Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 μA	I_{OL} = 8 mA	I_{IH} = 40 μA	I_{IL} = -0.4 mA

$$DCNM_{A \rightarrow B} = \min(4.4-2.6,\ 1.6-0.4) = 1.2V$$

Question: Is this a "good" DCNM (for 5 V CMOS logic)?

Example – DCNM, Family B → Family A

Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 μA	I_{IL} = -0.4 μA

Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 μA	I_{OL} = 8 mA	I_{IH} = 40 μA	I_{IL} = -0.4 mA

$$DCNM_{B \rightarrow A} = \min(3.3-3.6,\ 1.6-0.3) = -0.3V$$

Question: What is the consequence of a negative DCNM?

What is the minimum DCNM required? DCNM > 0

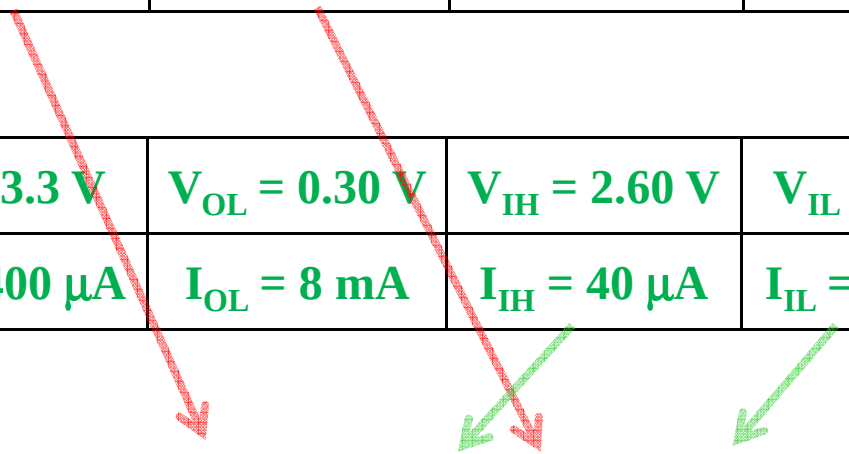
Example – Fan-out, Family A → Family B

Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 μA	I_{IL} = -0.4 μA

Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 μA	I_{OL} = 8 mA	I_{IH} = 40 μA	I_{IL} = -0.4 mA



$$\text{Fanout}_{A \to B} = \min(4 / 0.04, 4 / 0.4) = 10$$

Note: Current arrows for I_O and I_I point in *opposite directions*

Question: Is it possible for the fan-out to be negative? NO!

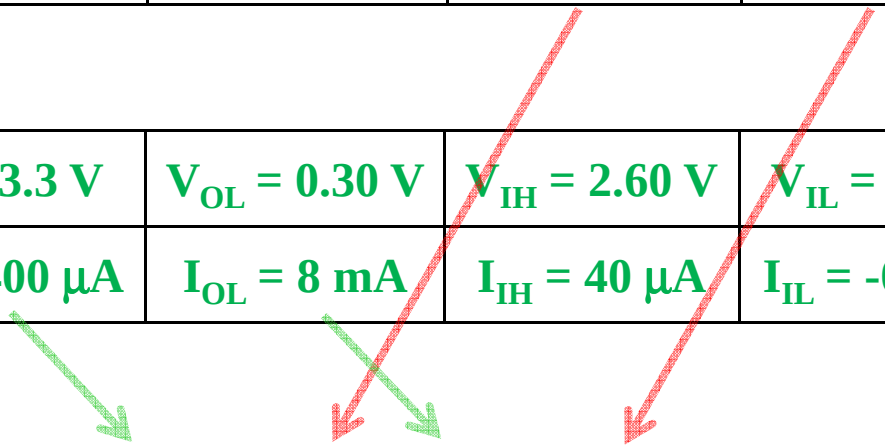
Example – Fan-out, Family B → Family A

Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 μA	I_{IL} = -0.4 μA

Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 μA	I_{OL} = 8 mA	I_{IH} = 40 μA	I_{IL} = -0.4 mA



$$\text{Fanout}_{B \to A} = \min(400/0.4,\ 8/0.0004) = 1000$$

Question: What is the minimum fan-out required?

Fan-out ≥ 1

Clicker Quiz

DC Characteristics of a Hypothetical Logic Family

$V_{CC} = 5$ V	$V_{OH} = 3.50$ V	$V_{OL} = 0.50$ V	$V_{IH} = 2.50$ V	$V_{IL} = 1.00$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -5.0$ mA	$I_{OL} = 10$ mA	$I_{IH} = 500$ μA	$I_{IL} = -2.0$ mA

1. The ***DC noise margin*** for this logic family is:

A. 0.50 V
B. 1.00 V
C. 1.50 V
D. 2.00 V
E. none of the above

DC Characteristics of a Hypothetical Logic Family

$V_{CC} = 5$ V	$V_{OH} = 3.50$ V	$V_{OL} = 0.50$ V	$V_{IH} = 2.50$ V	$V_{IL} = 1.00$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -5.0$ mA	$I_{OL} = 10$ mA	$I_{IH} = 500$ μA	$I_{IL} = -2.0$ mA

2. The ***practical fanout*** for this logic family is:

A. 1
B. 2
C. 5
D. 10
E. none of the above

3. The **nominal (minimum) case** for the **outputs of logic family "A"** to be able to successfully drive the **inputs of logic family "B"** is:

A. $\text{fanout}_{A\rightarrow B} \leq 1$ and $\text{DCNM}_{A\rightarrow B} < 0$

B. $\text{fanout}_{A\rightarrow B} \leq 0$ and $\text{DCNM}_{A\rightarrow B} < 1$

C. $\text{fanout}_{A\rightarrow B} \geq 1$ and $\text{DCNM}_{A\rightarrow B} > 0$

D. $\text{fanout}_{A\rightarrow B} \geq 0$ and $\text{DCNM}_{A\rightarrow B} > 1$

E. none of the above

DC Characteristics of a Hypothetical Logic Family

$V_{CC} = 5$ V	$V_{OH} = 3.50$ V	$V_{OL} = 0.50$ V	$V_{IH} = 2.50$ V	$V_{IL} = 1.00$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -5.0$ mA	$I_{OL} = 10$ mA	$I_{IH} = 500$ μA	$I_{IL} = -2.0$ mA

4. When interfacing an **LED** that has a **forward voltage of 1.5 V** to this logic family in a ***current sourcing*** configuration, **maximum brightness** will be achieved (within the rated specifications) using a current limiting resistor of the value:

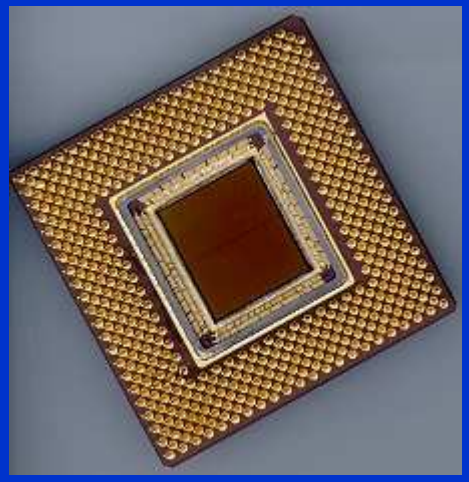
A. 200Ω **B. 300Ω** **C. 400Ω** **D. 500Ω** **E. none of these**

DC Characteristics of a Hypothetical Logic Family

$V_{CC} = 5$ V	$V_{OH} = 3.50$ V	$V_{OL} = 0.50$ V	$V_{IH} = 2.50$ V	$V_{IL} = 1.00$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -5.0$ mA	$I_{OL} = 10$ mA	$I_{IH} = 500$ μA	$I_{IL} = -2.0$ mA

5. When interfacing an **LED** that has a **forward voltage of 1.5 V** to this logic family in a ***current sinking*** configuration, **maximum brightness** will be achieved (within the rated specifications) using a current limiting resistor of the value:

A. 200Ω **B. 300Ω** **C. 400Ω** **D. 500Ω** **E. none of these**



Introduction to Digital System Design

Module 1-G

Propagation Delay and Transition Time

Reading Assignment:

DDPP 4th Ed., pp. 114-122

Learning Objectives:

- **Define propagation delay and list the factors that contribute to it**
- **Define transition time and list the factors that contribute to it**
- **Estimate the transition time of a CMOS gate output based on the "on" resistance of the active device and the capacitive load**
- **Describe ways in which load capacitance can be minimized**

Outline

- Overview
- Propagation delay
- Transition time
- Equivalent circuit transition time analysis
  - Calculation
  - Estimation
- Load capacitance

Overview

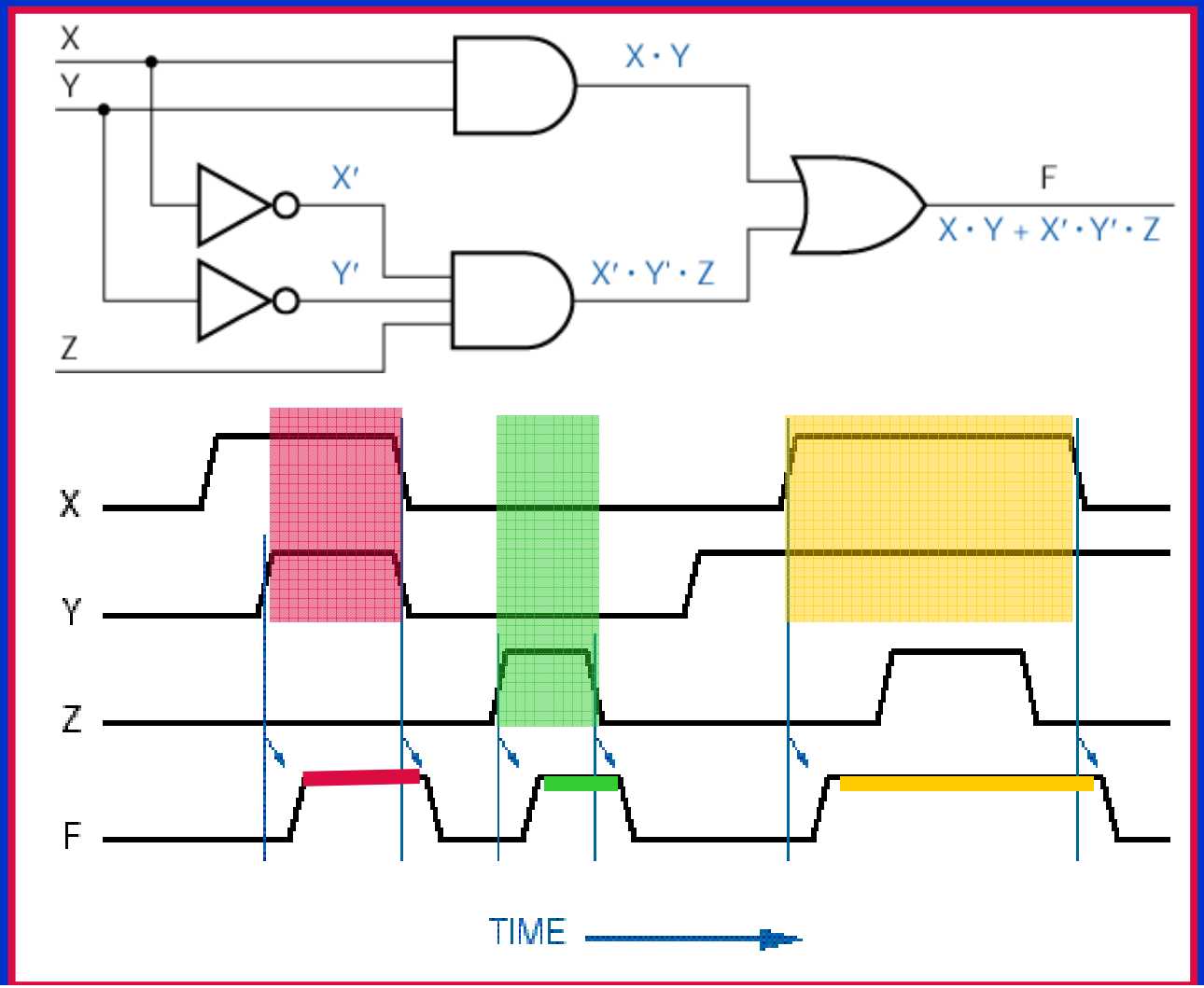
- **The *speed* and *power dissipation* of a CMOS device depend on the dynamic ("AC") characteristics of the device and its load**
- **Logic designers must carefully examine the effects of output loading and redesign where the loading is too high**
- **Speed (performance) depends on two characteristics:**
  - ***propagation delay***
  - ***transition time***

Time Matters

- **Logic gates require a certain amount of "think time" to produce a new output in response to changing inputs – referred to as the *propagation delay* of the gate**
- **Logic gate outputs can not change from a low voltage to a high voltage (or vice-versa) "instantaneously" – referred to as the *transition time* of the gate**
- **A *timing diagram* can be used to show how a logic circuit responds to time-varying input signals**

Time Matters

- **Time response of a combinational circuit**

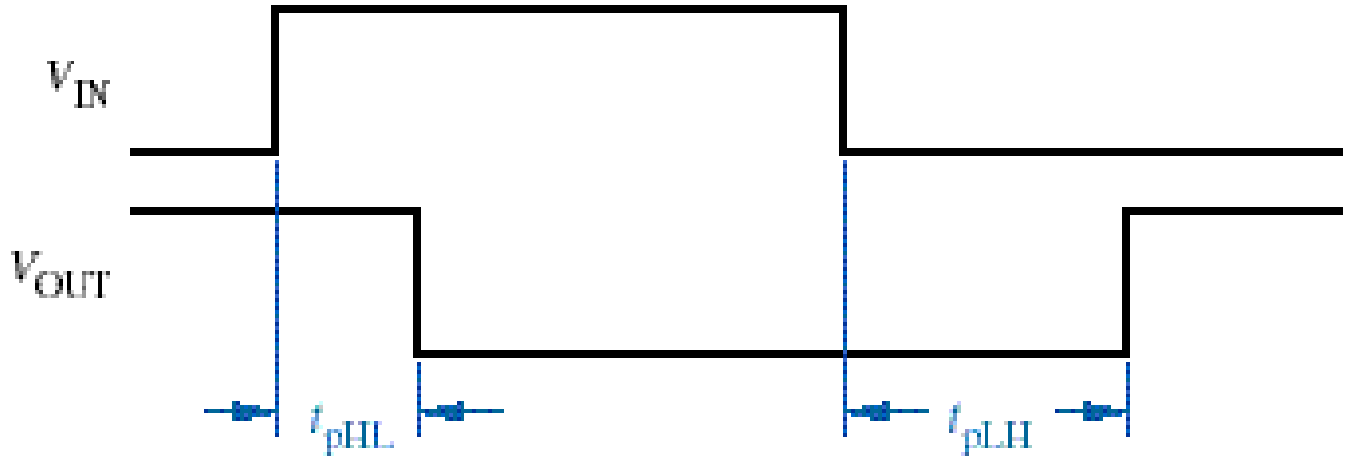


Propagation Delay – Definition

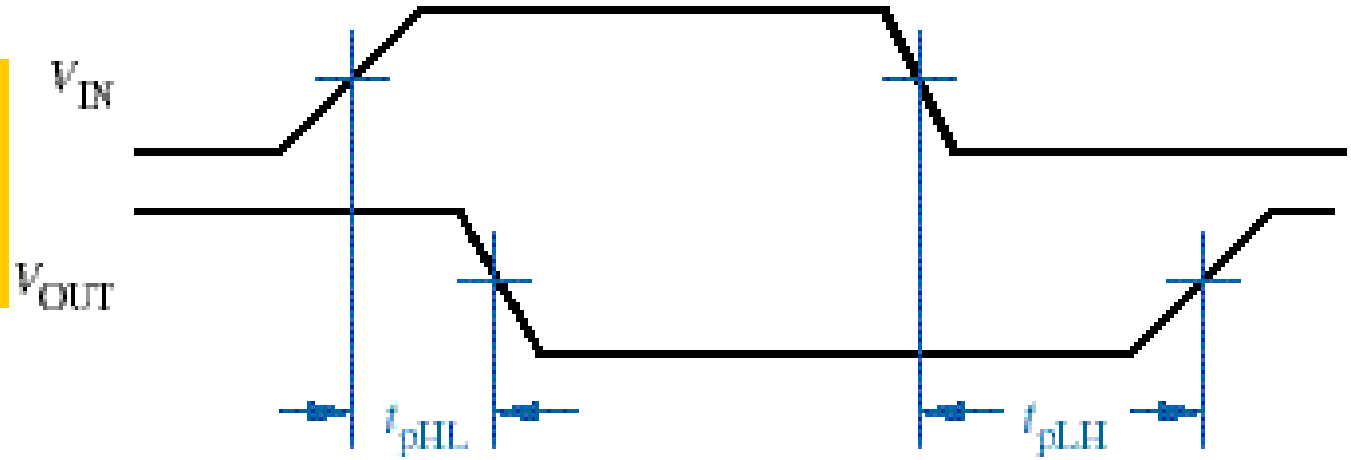
- **Definition: The electrical path from a particular input signal of a logic element to its output signal is called a *signal path***
- **Definition: The amount of time it takes for a change in an input signal to cause a corresponding change in a gate's output signal is called the *propagation delay* (t_p)**
- **The propagation delay for an output signal going from LOW-to-HIGH (t_{PLH}) may be different than the propagation delay of that signal going from HIGH-to-LOW (t_{PHL})**

Propagation Delay – Measurement

Ignoring rise and fall times



Measured at midpoints of transitions

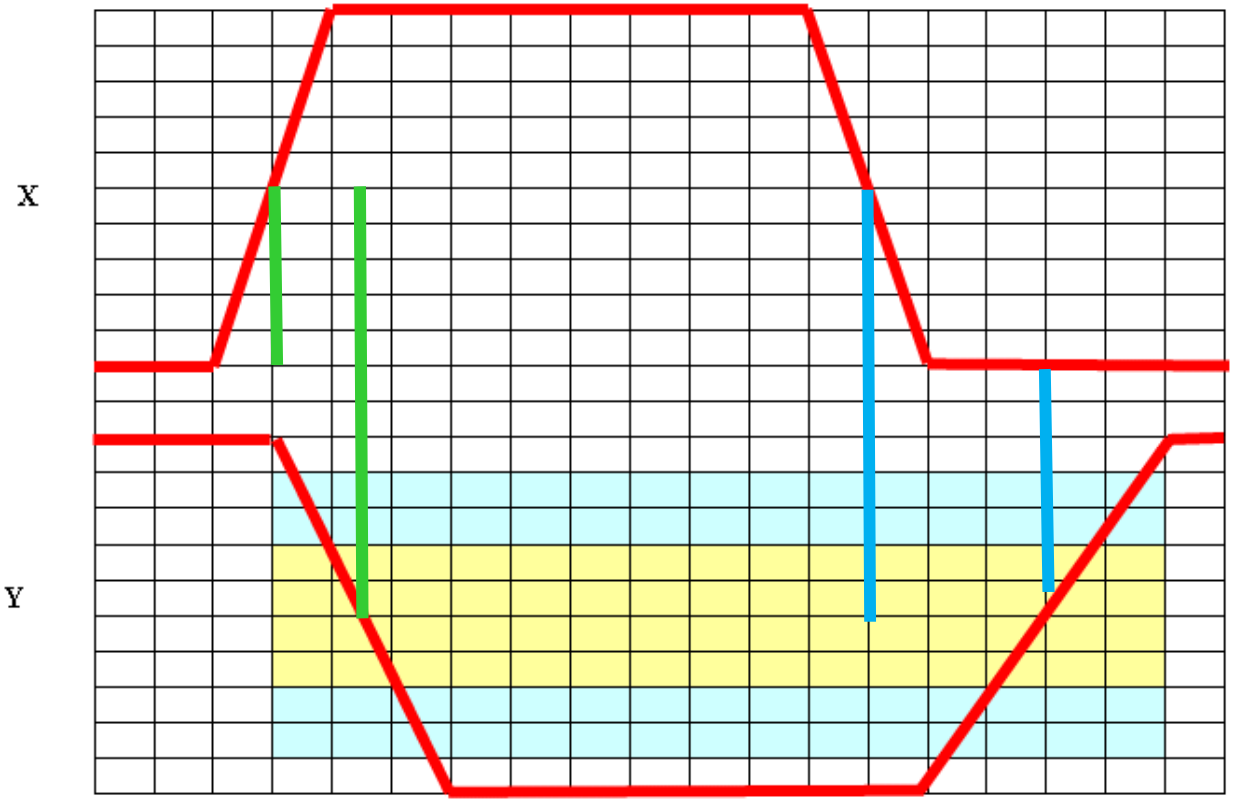


Propagation Delay – Why Non-zero

- **Several factors lead to *non-zero* propagation delays in CMOS circuits:**
  - **the rate at which transistors change state is influenced both by semiconductor physics and the circuit environment (input signal transition time, input capacitance, and output loading)**
  - **multistage devices (e.g., non-inverting gates) may require several internal transistors to change state before the output can change state**

Example – Propagation Delay Measurement

Find each of the following, rounded to the nearest ½ ns (assume each division is 1 ns)



Rise propagation delay (t_{PLH}) = 3 ns

Fall propagation delay (t_{PHL}) = 1.5 ns

Transition Time – Definition

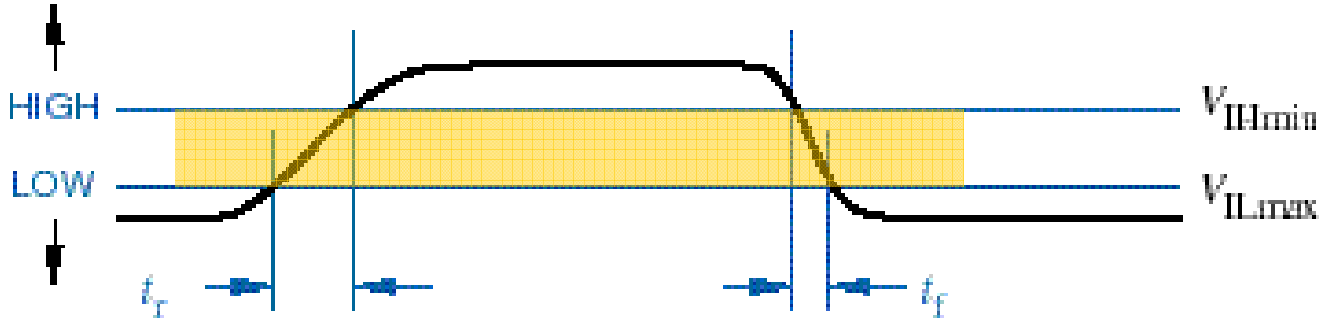
- **Definition: The amount of time that the output of a logic circuit takes to change from one state to another**
  - **rise time (tr or t_{TLH}): the time an output signal takes to transition from low-to-high**
  - **fall time (tf or t_{THL}): the time an output signal takes to transition from high-to-low**
- **Gate outputs can *not* change state *instantaneously* (i.e., with a transition time of zero) because they need to *charge the stray capacitance* of the wires and other components they drive**

Transition Time – Measurement

“ideal”

“less ideal”

“reality”



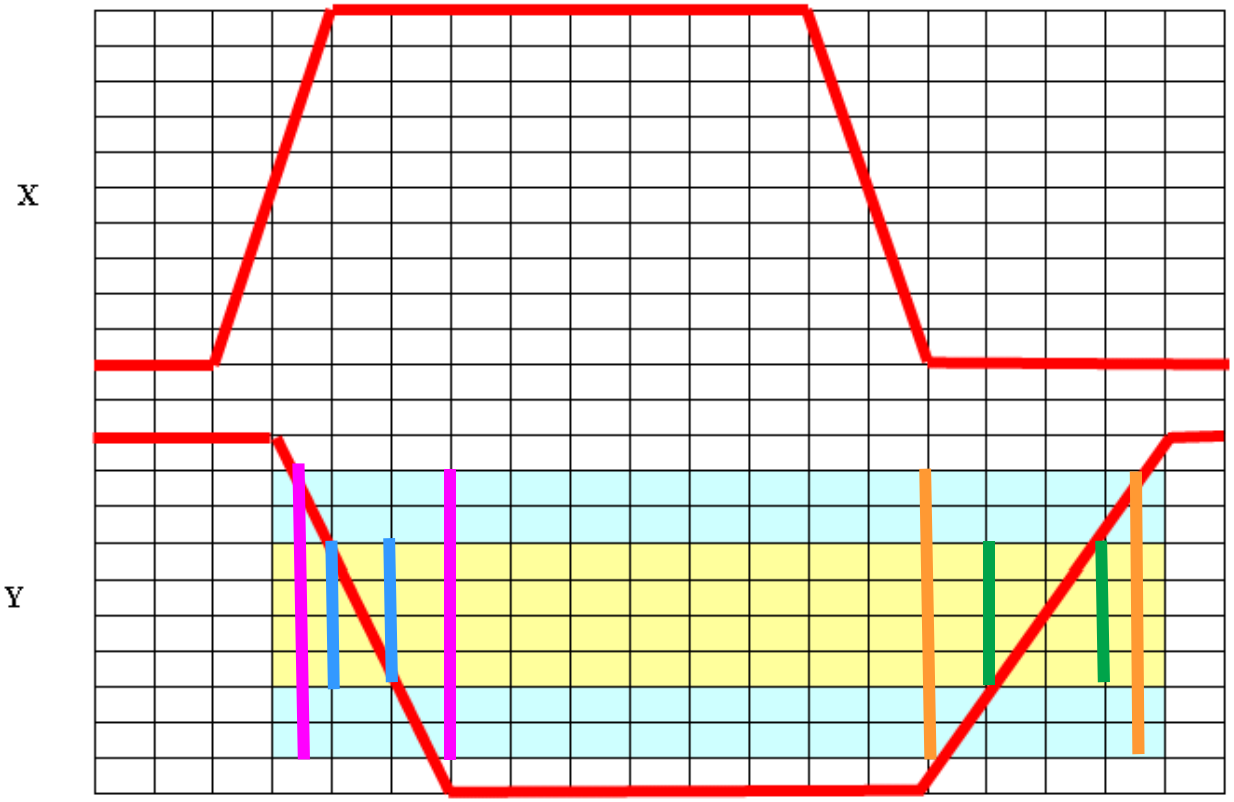
Note: tf is typically *not* equal to tr

Transition Time – Endpoints

- **To avoid difficulties in defining the endpoints, transition times are normally measured one of two different ways:**
  - **at the boundaries of the valid logic levels (i.e., $V_{IH_{min}}$ and $V_{IL_{max}}$)**
  - **at the 10% and 90% points of the output waveform**
- **Using the first convention (above), the rise and fall times indicate how long it takes for an output signal to pass through the (undefined) *indeterminate region* between LOW and HIGH**

Example – Transition Time Measurement

Find each of the following, rounded to the nearest ½ ns (assume each division is 1 ns)



Rise time (t_{TLH}) based on Wakerly's (30%-70%) definition = 2 ns

Rise time (t_{TLH}) based on standard 10%-90% definition = 3.5 ns

Fall time (t_{THL}) based on Wakerly's (70%-30%) definition = 1 ns

Fall time (t_{THL}) based on standard 90%-10% definition = 2.5 ns

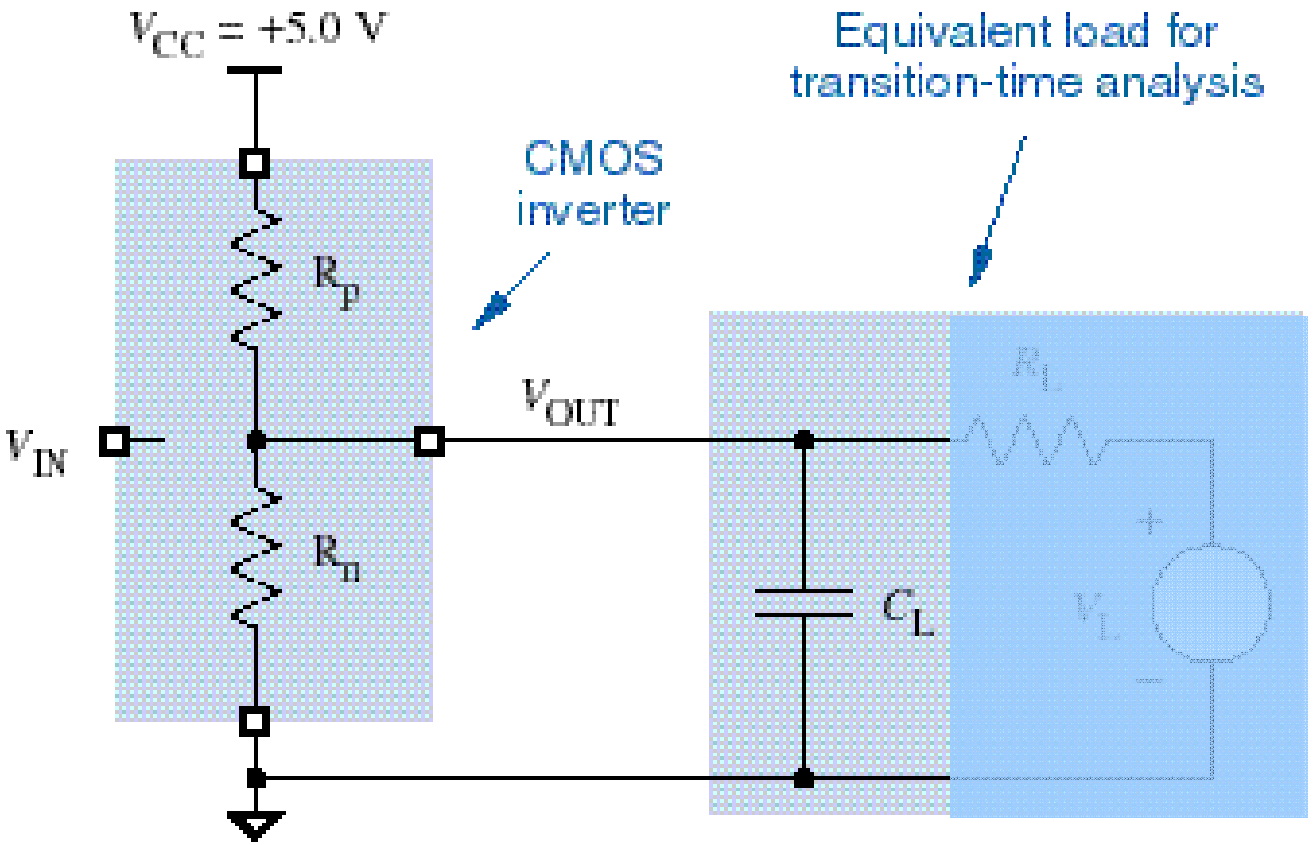
Transition Time – Factors

- **The transition times of a CMOS circuit depend mainly on two factors:**
  - ***the "on" transistor resistance***
  - ***the load capacitance***
- ***Stray capacitance*** **(called an "*AC load*") arises from at least three different sources:**
  - **output circuits – including transistors, internal wiring, and packaging**
  - **wiring that connects a gate output to other gate inputs**
  - **input circuits – including transistors, internal wiring, and packaging**

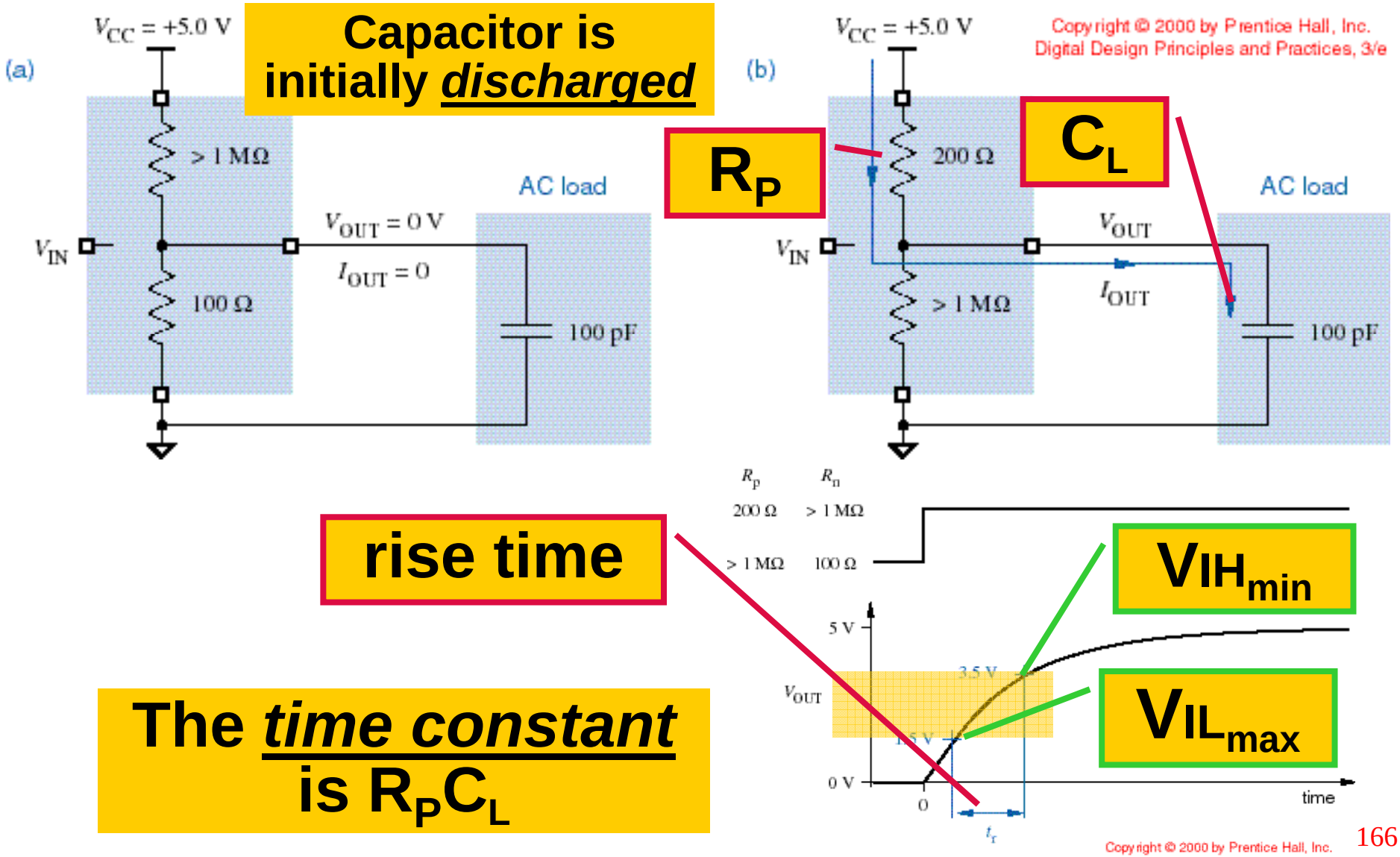
Transition Time – Equivalent Circuit

- A gate output's load can be modeled by an equivalent load circuit with 3 components:
  - R_L and V_L represent the DC load – they determine the steady state voltages and currents present and do not have much effect on transition times
  - C_L represents the AC (capacitive) load – it determines the voltages and currents present while the output is changing, as well as how long it takes to change from one state to another

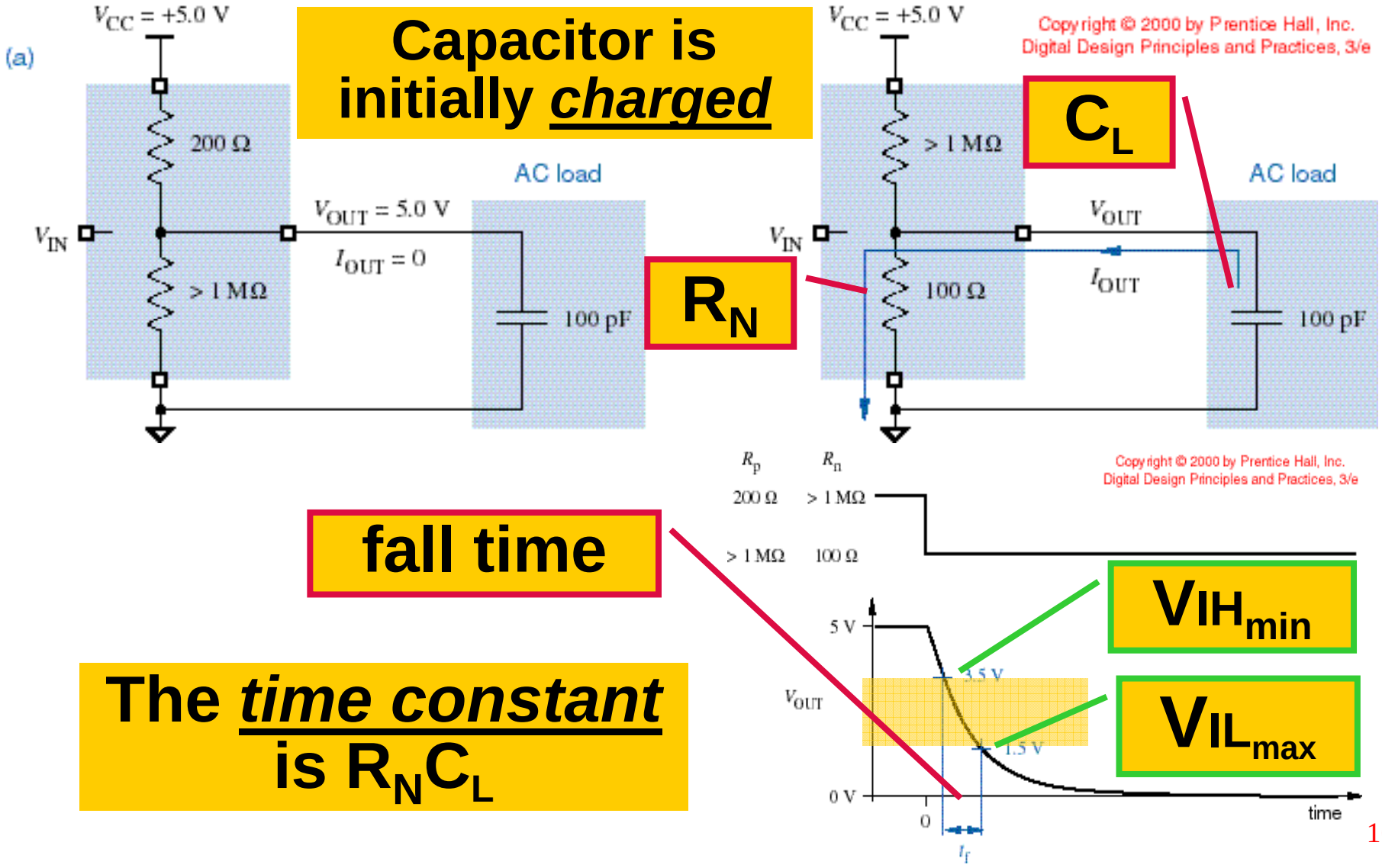
Equivalent Circuit for Transition Time Analysis of a CMOS Output



Model of a CMOS LOW-to-HIGH Transition (with Negligible DC Load)

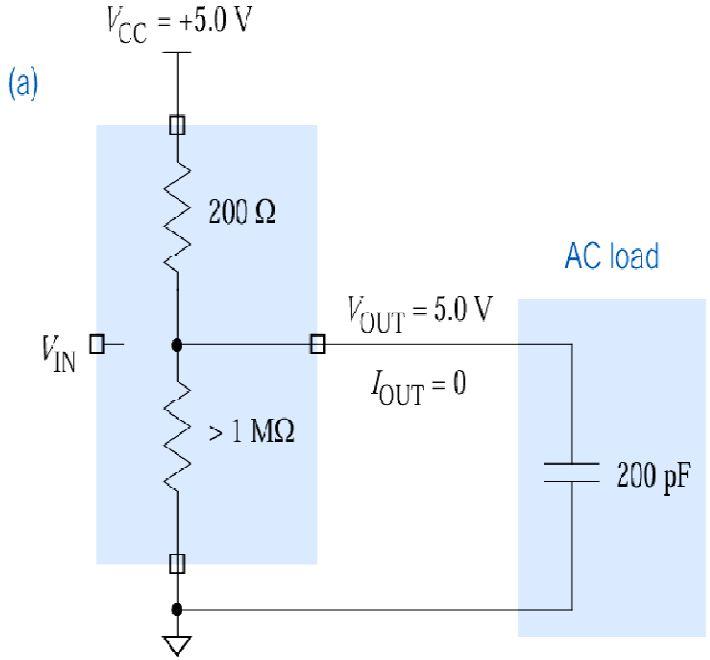


Model of a CMOS HIGH-to-LOW Transition (with Negligible DC Load)



Example

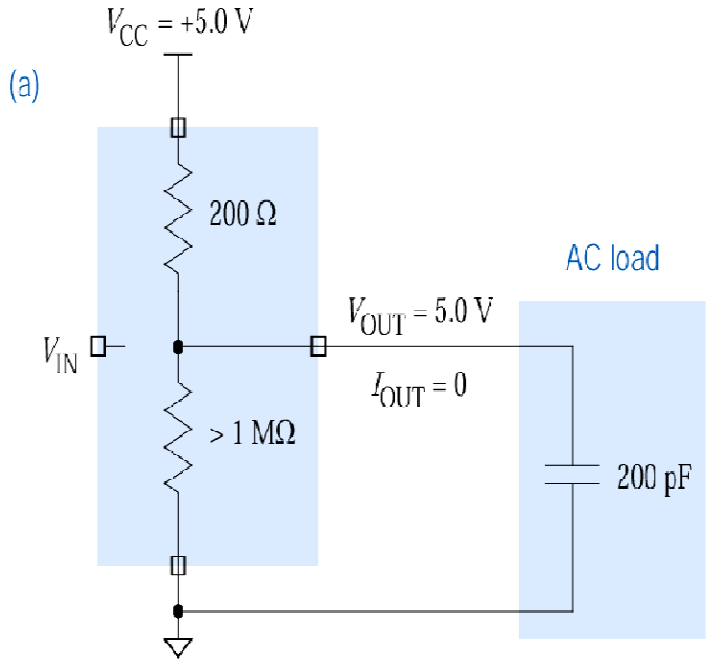
- **Given that a CMOS inverter's P-channel MOSFET has an ON resistance of 200Ω, that its N-channel MOSFET has an ON resistance of 100Ω, and that the capacitive (or AC) load C_L = 200 pF, calculate the fall time**



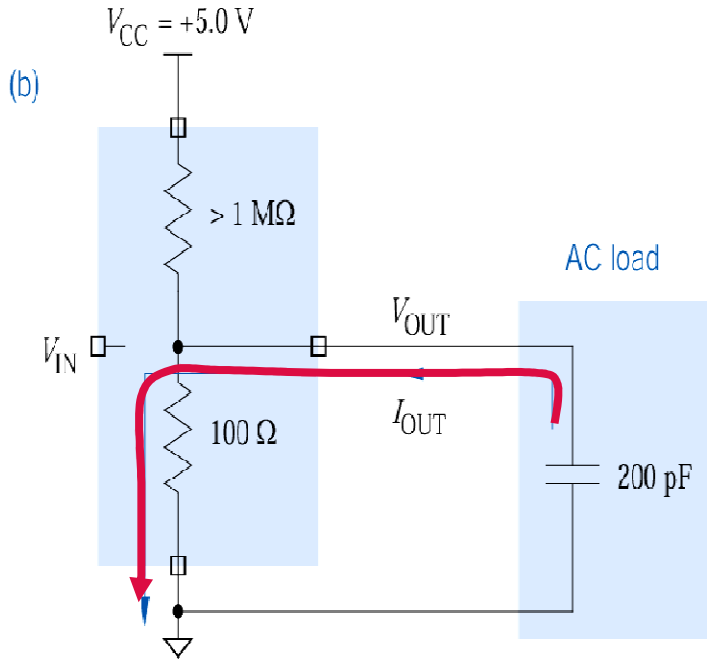
initial conditions

Example – Fall Time Calculation

- **Given that a CMOS inverter's P-channel MOSFET has an ON resistance of 200Ω, that its N-channel MOSFET has an ON resistance of 100Ω, and that the capacitive (or AC) load C_L = 200 pF, calculate the fall time**

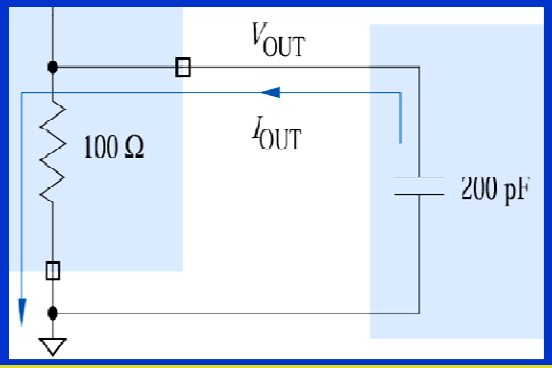


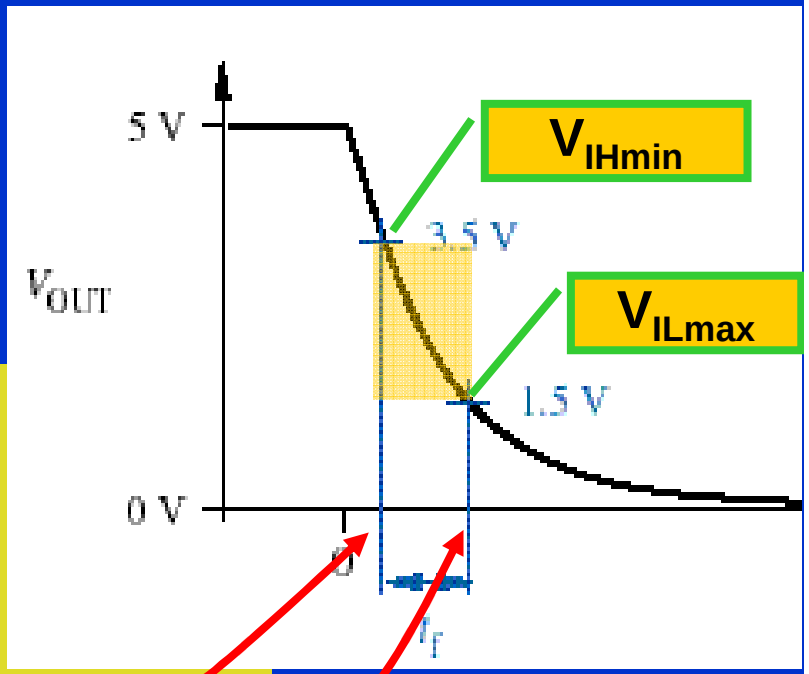
initial conditions



output goes low

Example – Fall Time Calculation





$t = -R_n * C_L * \ln (V_{out}/V_{DD})$

$= -100 * 200 * 10^{-12} * \ln (V_{out} / 5.0)$

$= -20 * 10^{-9} * \ln (V_{out} / 5.0)$

$t_{3.5} = -20 * 10^{-9} * \ln (3.5/5.0) = 7.13$ ns

$t_{1.5} = -20 * 10^{-9} * \ln (1.5/5.0) = 24.08$ ns

$t_{PHL} = t_f$ ***(fall time)*** $= 24.08 - 7.13 = 16.95$ ns

Note: ***Calculated transition times are sensitive to the choice of logic levels*** **(i.e., V_{IHmin} and V_{ILmax})**

Transition Time Estimation

- **Rule of Thumb: In practical circuits, the transition time can be *estimated* using the RC time constant of the charging or discharging circuit**

Example – Transition Time Estimates

- **Given that a CMOS inverter's P-channel MOSFET has an ON resistance of 200Ω, that its N-channel MOSFET has an ON resistance of 100Ω, and that the capacitive (or "A.C.") load C_L = 200 pF, *estimate* the fall time and rise time**

Fall time estimate:

$R_N \times C_L = 100 \times 200\ pF$

$= 1 \times 10^2 \times 2 \times 10^{-10}$

$= 2 \times 10^{-8} = 20 \times 10^{-9}$

= 20 ns

Rise time estimate:

$R_P \times C_L = 200 \times 200\ pF$

$= 2 \times 10^2 \times 2 \times 10^{-10}$

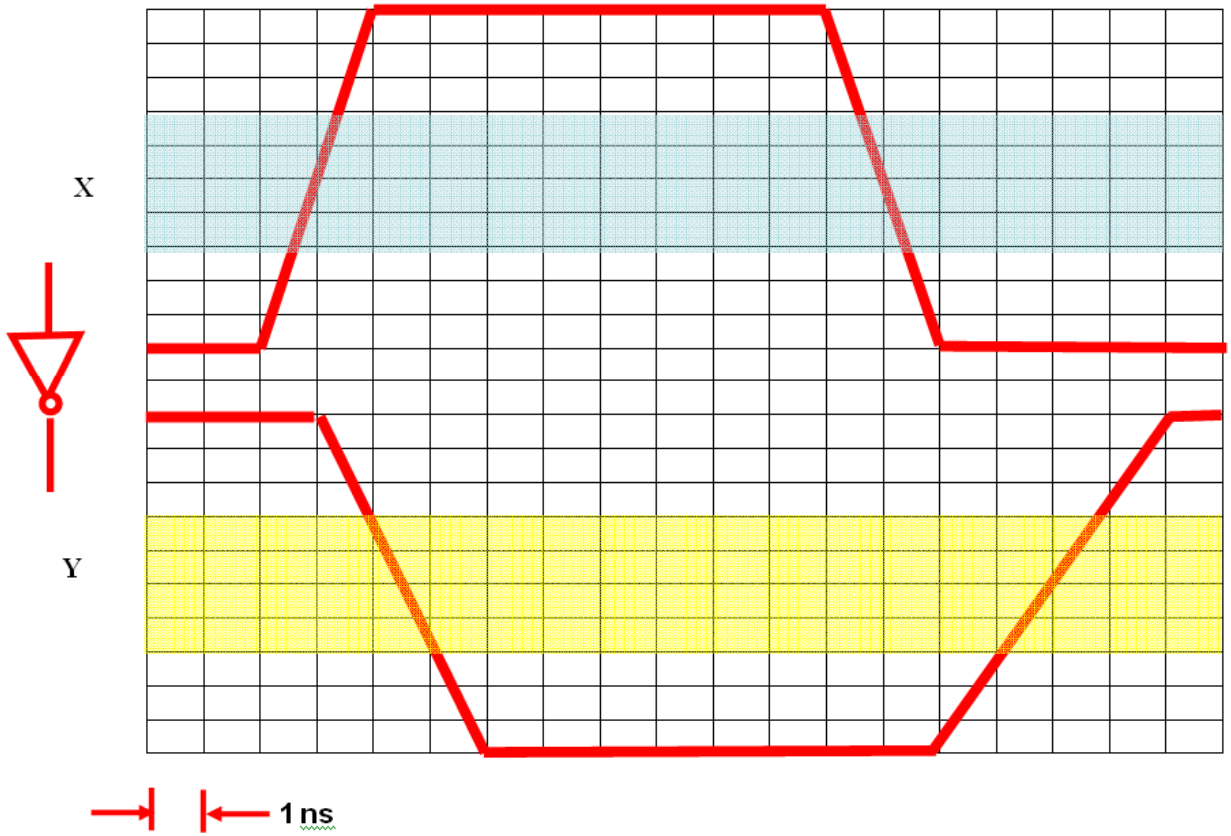
$= 4 \times 10^{-8} = 40 \times 10^{-9}$

= 40 ns

Load Capacitance

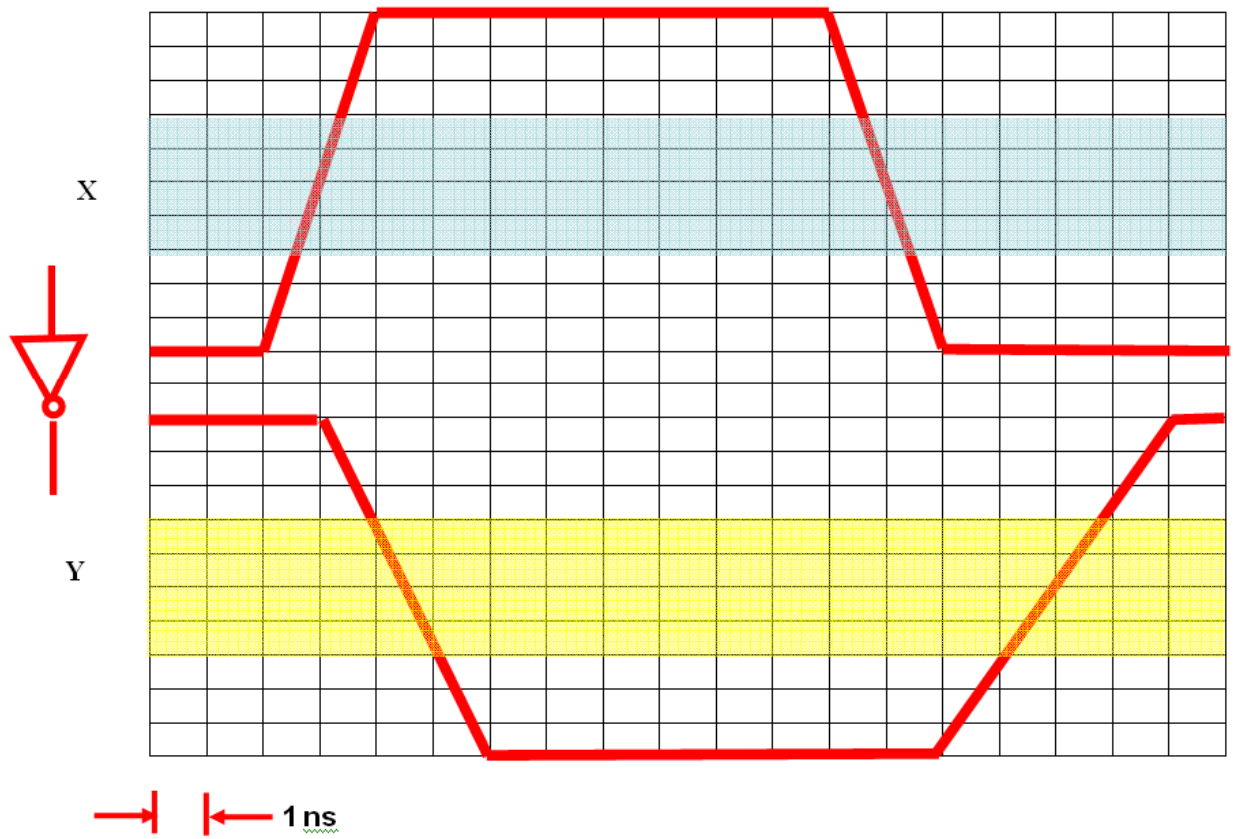
- **Conclusion: An increase in load capacitance causes an increase in the RC time constant and a corresponding increase in the output transition (rise/fall) times**
- **Load capacitance must be *minimized* to obtain high circuit performance – this can be achieved by:**
  - **minimizing the number of inputs driven by a given signal**
  - **creating multiple copies of the signal (using "buffers")**
  - **careful *physical layout* of the circuit**

Clicker Quiz



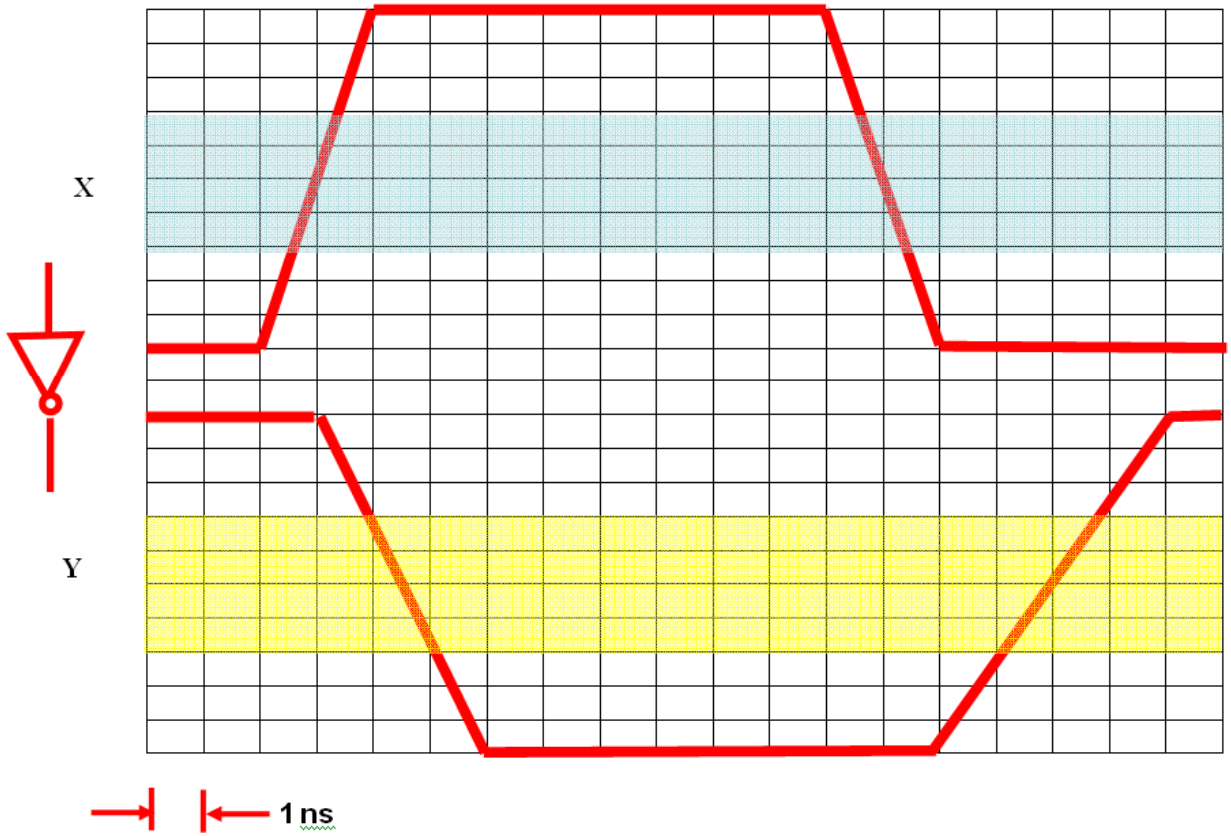
1. The **rise time** for the inverter is approximately:

A. 1.0 ns B. 1.5 ns C. 2.0 ns D. 3.0 ns E. none



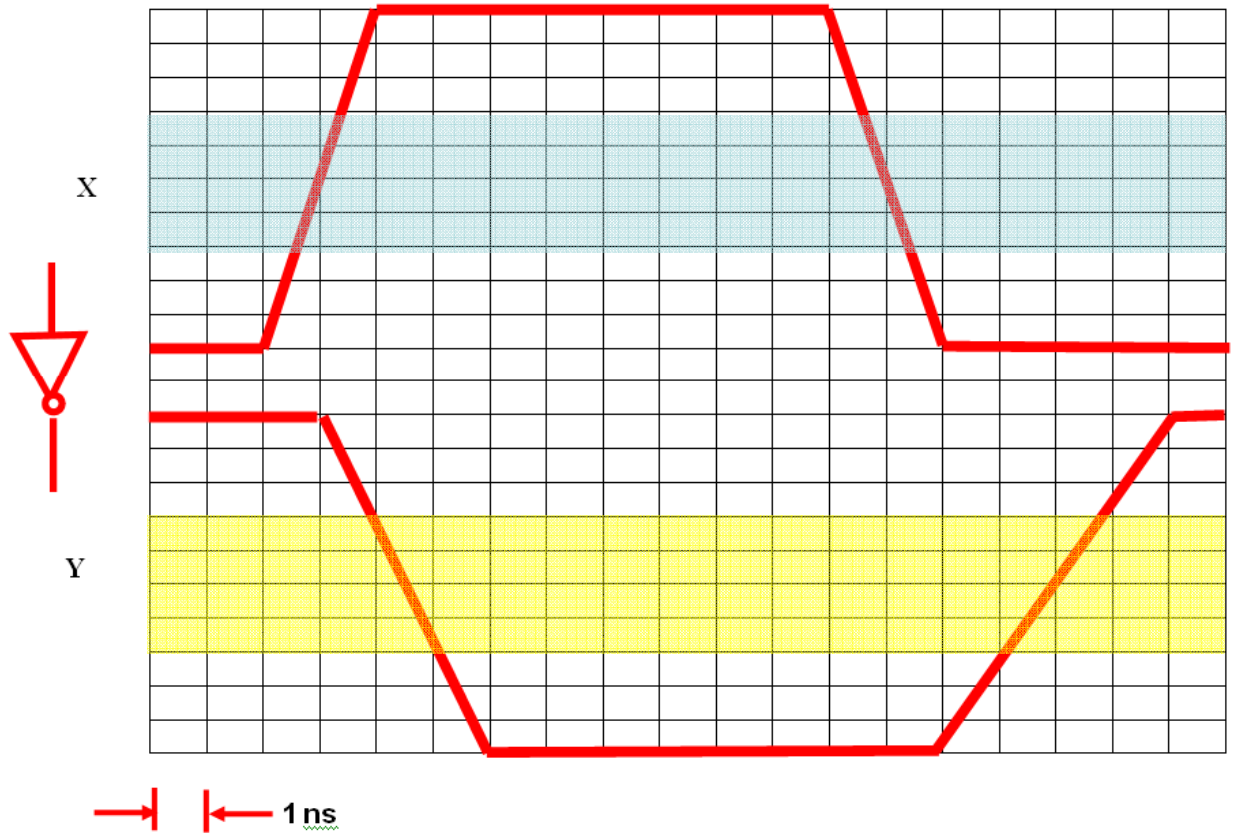
2. The **fall time** for the inverter is approximately:

A. 1.0 ns **B.** 1.5 ns **C.** 2.0 ns **D.** 3.0 ns **E.** none



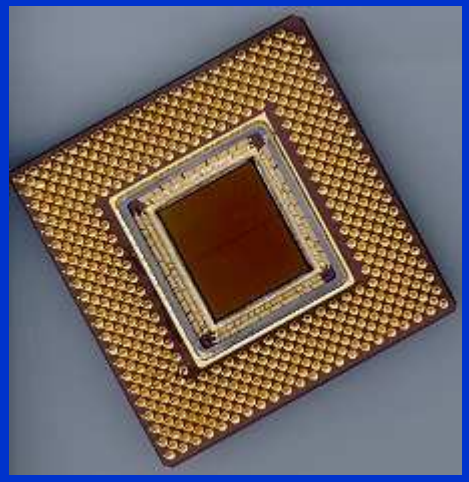
3. The **fall propagation delay** for the inverter is approx:

A. 1.0 ns **B.** 1.5 ns **C.** 2.0 ns **D.** 3.0 ns **E.** none



4. The **rise propagation delay** for the inverter is approx:

A. 1.0 ns **B.** 1.5 ns **C.** 2.0 ns **D.** 3.0 ns **E.** none



Introduction to Digital System Design

Module 1-H

Power Consumption and Decoupling

Reading Assignment:

DDPP 4th Ed., pp. 122-124

Learning Objectives:

- **Identify sources of dynamic power dissipation**
- **Plot power dissipation of CMOS logic circuits as a function of operating frequency**
- **Plot power dissipation of CMOS logic circuits as a function of power supply voltage**
- **Describe the function and utility of decoupling capacitors**

Outline

- Overview
- Dynamic power dissipation
- Power dissipation as a function of operating frequency
- Power dissipation as a function of supply voltage
- Current spikes and decoupling

Overview

- **Definition: The power dissipation (consumption) of a CMOS circuit whose output is *not changing* is called *static (quiescent) power dissipation***
- **Most CMOS circuits have *very low* static power dissipation**
- **CMOS circuits only dissipate a significant amount of power during *transitions* – this is called *dynamic power dissipation***

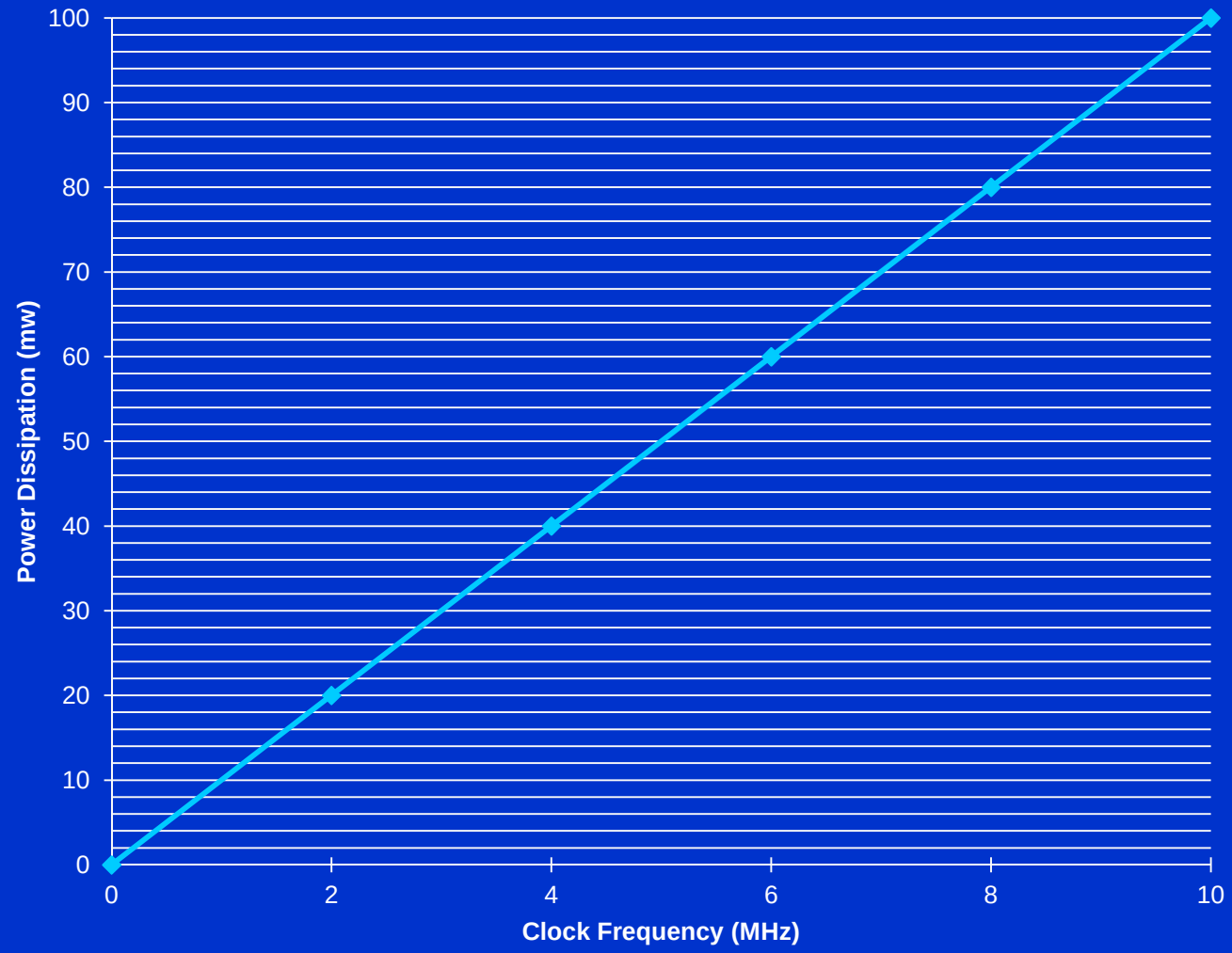
Dynamic Power Dissipation

- **Sources of dynamic power dissipation:**
  - **the partial "short-circuiting" of the CMOS output structure (e.g., when the input voltage is not close to one of the power supply rails) – called "P_T" (power due to output transitions)**
  - **the capacitive load on the output (power is dissipated in the "on" resistance of the active transistor to charge/discharge the capacitive load) – called "P_L" (power due to charging/discharging load)**

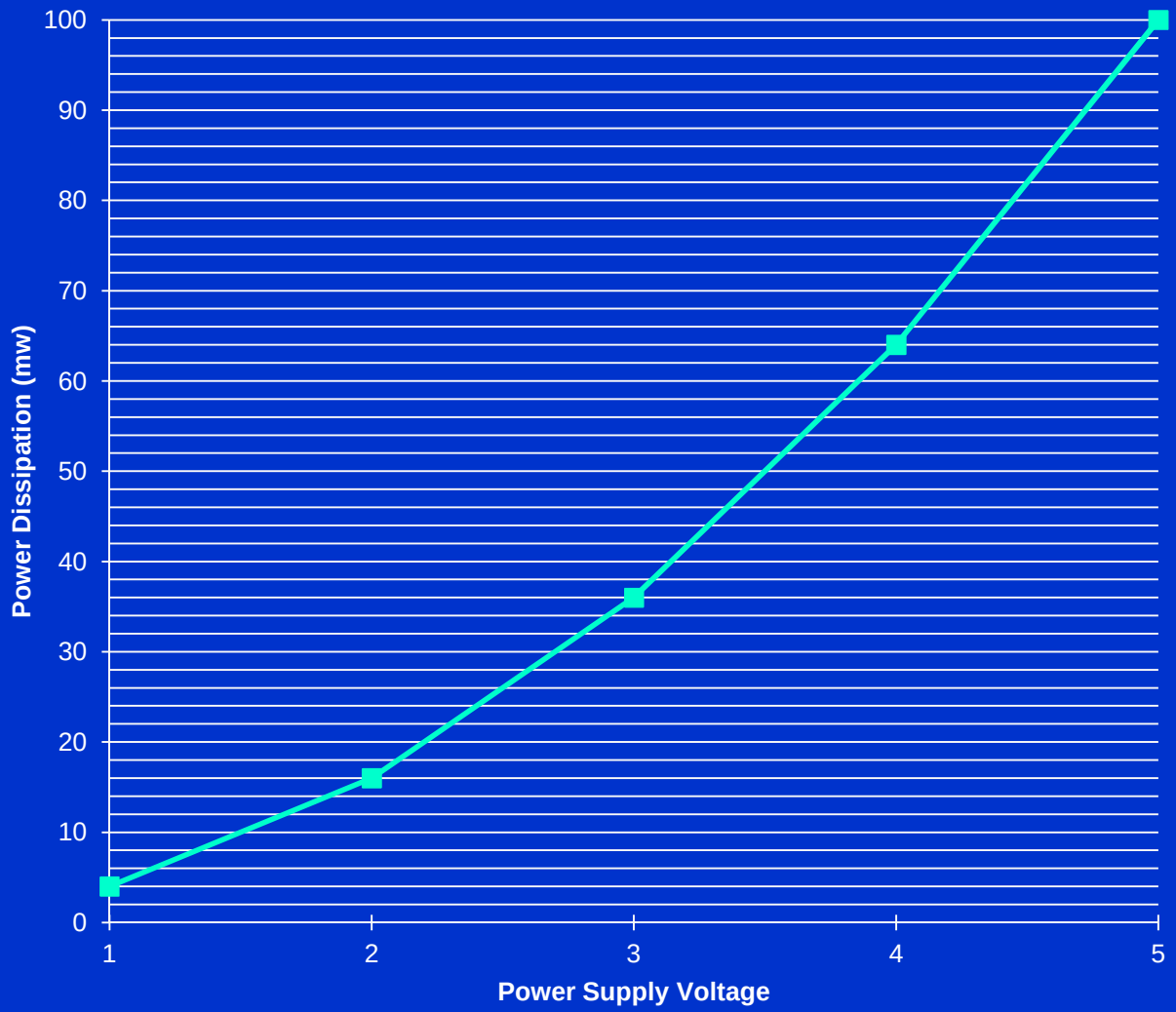
Power Consumption

- **Total dynamic power dissipation ($P_T + P_L$) is proportional to the *square* of the power supply voltage times the transition frequency**
- **Conclusions:**
  - **power dissipation increases *linearly* as the frequency of operation increases**
  - **reducing the power supply voltage results in a *quadratic* reduction of the power dissipation**

Example - A microcontroller can operate over a frequency range of **0 Hz to 10 MHz**, and dissipates **100 mW** when operated at **10 MHz**; plot its power dissipation over **the specified frequency range**



Example - A microcontroller can operate over a power supply range of 1 to 5 volts, and dissipates 100 mW when operated at 5 VDC; plot its power dissipation over the specified power supply range



$100 \times (4/5)^2 = 64$

$100 \times (3/5)^2 = 36$

$100 \times (2/5)^2 = 16$

$100 \times (1/5)^2 = 4$

Current Spikes and Decoupling

- **When a CMOS gate output changes state, the P- and N-channel transistors are both partially on simultaneously, causing a *current spike***
- **Current spikes often show up as *noise* on the power supply and ground connections**
- ***Decoupling capacitors* (between Vcc and GND) must be distributed throughout a printed circuit board (PCB) to serve as a source of instantaneous current during output transitions – *this helps mitigate noise and improve signal quality***

Decoupling Capacitors

- **Decoupling capacitors should be located as *physically close* as possible to each IC**
- **Use 0.1 μF decoupling capacitors for system frequencies up to 15 MHz**
- **Above 15 MHz, use 0.01 μF decoupling capacitors**

Clicker Quiz

1. Assume a CMOS microprocessor dissipates **100 milliwatts** of power when operated at a clock frequency of **100 MHz** with a supply voltage of **5 V**. If the frequency of operation is reduced from **100 MHz** to **40 MHz** (and the supply voltage remains 5 V), the power dissipation will be reduced to:

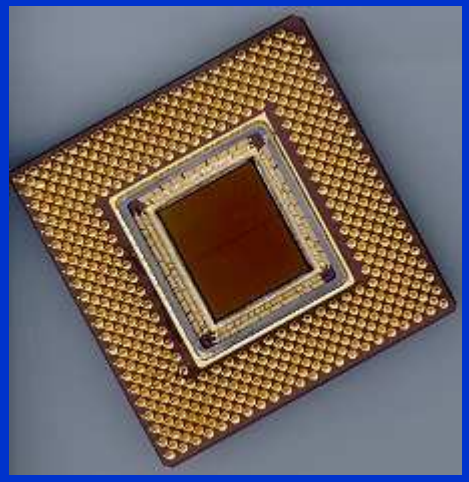
A. 16 mW **B. 25 mW** **C. 40 mW** **D. 64 mW** **E. none**

2. Assume a CMOS microprocessor dissipates **100 milliwatts** of power when operated at a clock frequency of **100 MHz** with a supply voltage of **5 V**. If the supply voltage is reduced from **5 V** to **4 V** (and the frequency of operation remains 100 MHz), the power dissipation will be reduced to:

A. 16 mW **B. 25 mW** **C. 40 mW** **D. 64 mW** **E. none**

3. Assume a CMOS microprocessor dissipates **100 milliwatts** of power when operated at a clock frequency of **100 MHz** with a supply voltage of **5 V**. If the frequency of operation is reduced to **1 Hz** (and the supply voltage remains 5 V) , the power dissipation will be reduced to (approximately):

A. 16 mW **B. 25 mW** **C. 40 mW** **D. 64 mW** **E. none**



Introduction to Digital System Design

Module 1-I

Schmitt Triggers and Transmission Gates

Reading Assignment:

DDPP 4th Ed., pp. 129-131

Learning Objectives:

- **Define hysteresis and describe the operation of Schmitt-trigger inputs**
- **Describe the operation and utility of a transmission gate**

Outline:

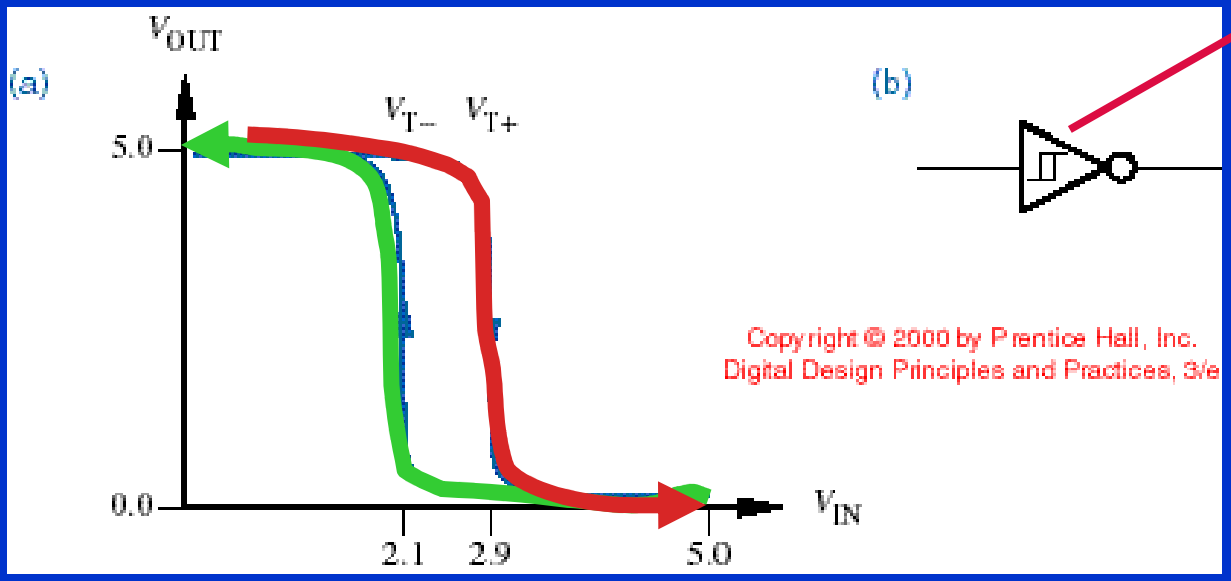
- **Overview**
- **Schmitt-trigger inputs**
- **Transmission gates**

Overview

- The basic CMOS circuit has been “tailored” in many ways to produce gates for specific applications
- This circuit tailoring has been motivated by the need for:
  - higher performance than can be achieved with “standard” NAND/NOR gates
  - “conditioning” noisy, slowly changing logic signals
  - allowing logic elements to communicate via buses

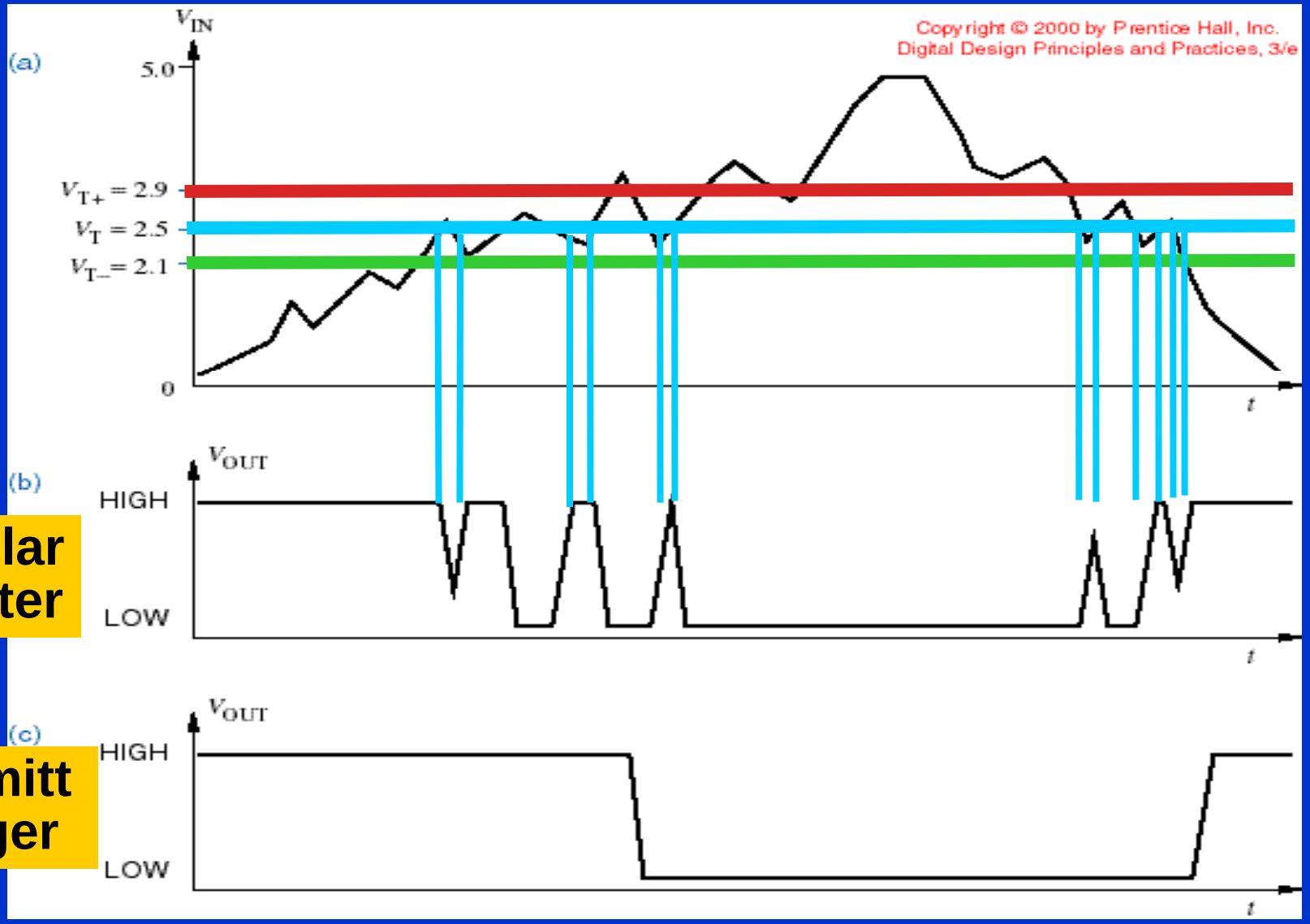
Schmitt-Trigger Inputs

- A ***Schmitt trigger*** **is a special circuit that shifts the switching threshold depending on whether the input is changing from LOW-to-HIGH (V_{T+}) or from HIGH-to-LOW (V_{T-})**
- **The difference between the two thresholds is called *hysteresis***



Symbol used to denote *hysteresis*

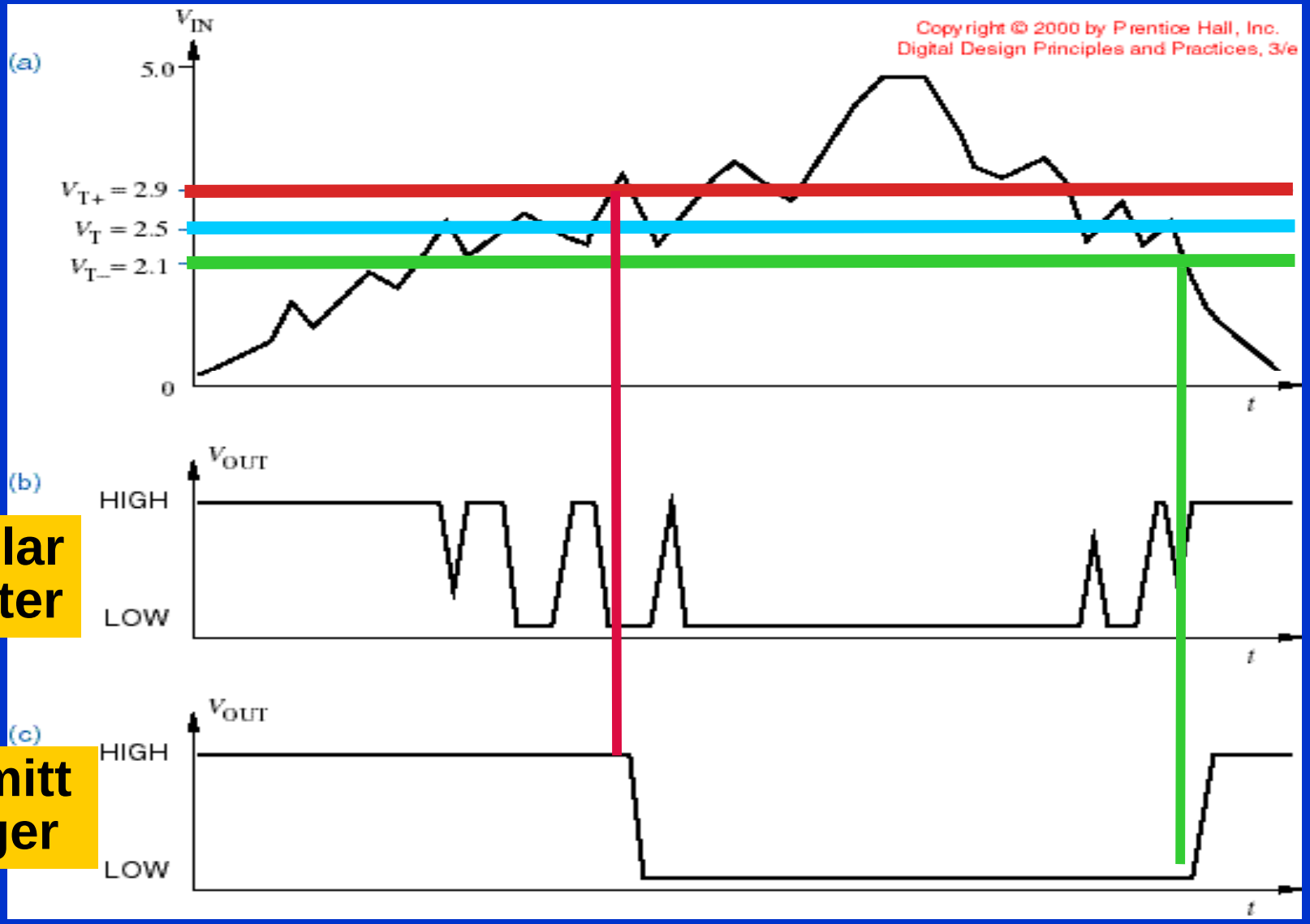
Comparison of an Ordinary Inverter to a Schmitt Trigger for a Noisy, Slowly Changing Input Signal



Regular Inverter

Schmitt trigger

Comparison of an Ordinary Inverter to a Schmitt Trigger for a Noisy, Slowly Changing Input Signal



Regular Inverter

Schmitt trigger

Schmitt-Trigger Inputs

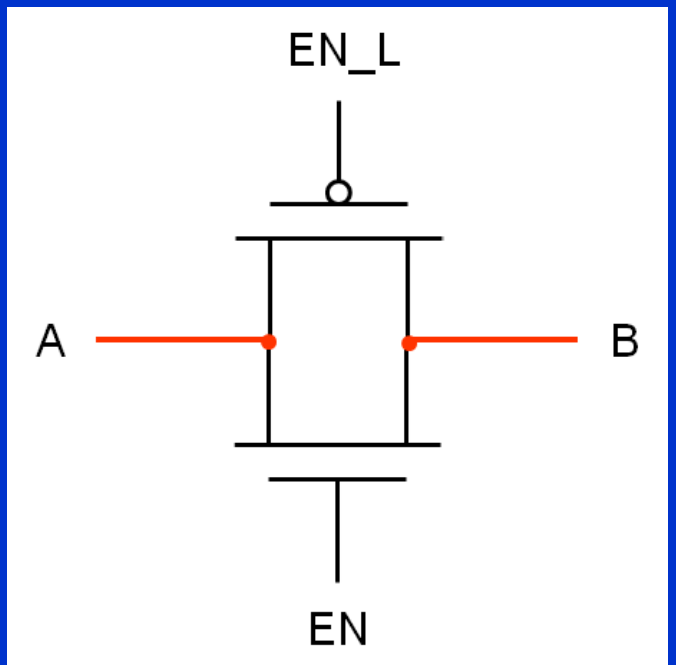
- **Observations:**
  - **Schmitt-trigger inputs have *better noise immunity* margin than ordinary gates for *noisy or slowly changing signals***
  - **"Distorted" logic signals of this type typically occur in *physically long connections*, such as I/O buses and computer interface cables**

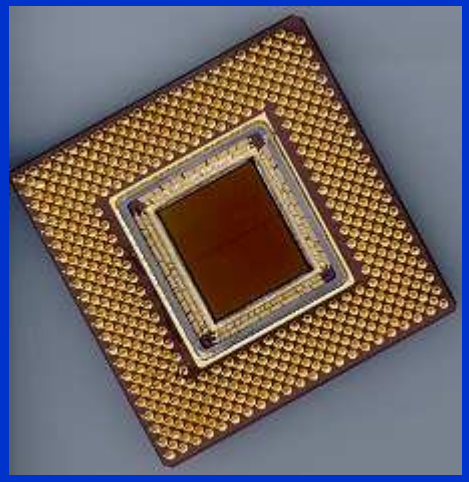
Rule of "foot" – Logic-level signals can be sent reliably over a cable for only a *few feet*

Transmission Gates

- The P- and N-channel transistor pair can be connected together to form a logic-controlled switch, called a ***transmission gate***
- Control signals EN_L and EN are at opposite levels
- When EN is asserted, there is a low-impedance connection between A and B; when EN is negated, A and B are disconnected

A high performance multiplexer (input selector switch) can be constructed using a pair of transmission gates and an inverter





Introduction to Digital System Design

Module 1-J

Three-State and Open-Drain Outputs

Reading Assignment:

DDPP 4th Ed., pp. 132-136, 138-141

Learning Objectives:

- **Define high-impedance state and describe the operation of a tri-state buffer**
- **Define open drain as it applies to a CMOS logic gate output and calculate the value of pull-up resistor needed**
- **Describe how to create “wired logic” functions using open drain logic gates**
- **Calculate the value of pull-up resistor needed for an open drain logic gate**

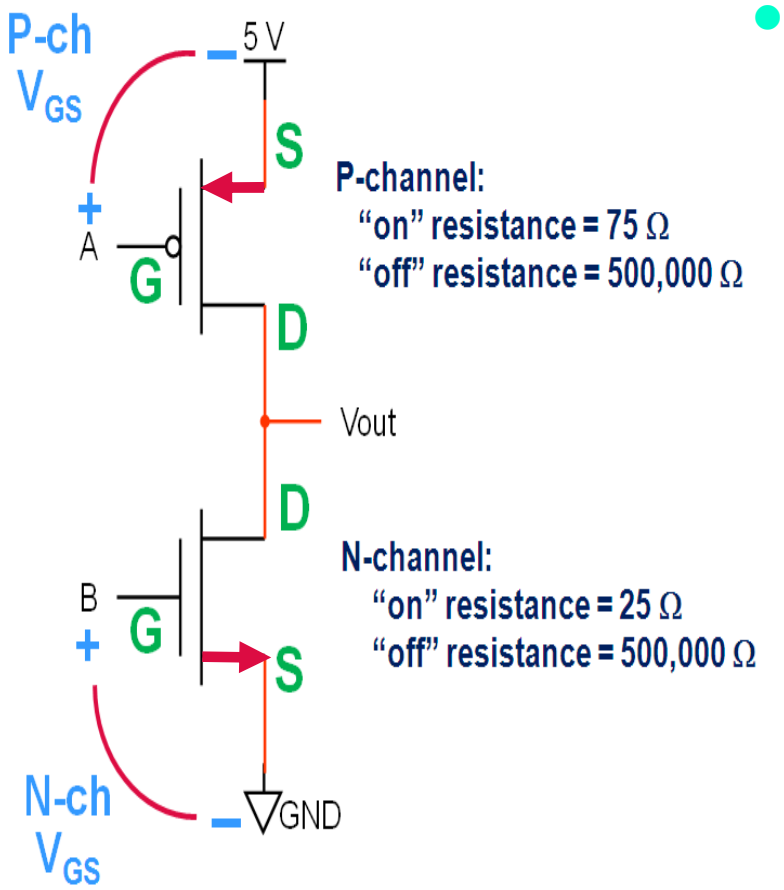
Outline

- Three-state (tri-state) outputs
- CMOS tri-state buffer circuit
- Tri-state buffer application – buses
- Tri-state buffer float delay
- Open drain outputs
- Driving LEDs
- Wired logic
- Pull-up resistor calculations

Three-State (Tri-State) Outputs

- **Definition: A gate output that has a third "electrical state" is called a *three-state output* (or *tri-state output*)**
- **This third electrical state is called the *high impedance*, *Hi-Z*, or *floating* state**
- **In the high impedance state, the gate output effectively appears to be *disconnected* from the rest of the circuit**
- **Three-state devices have an extra input, typically called the *Output Enable* (OE), for enabling data to "flow through" the device (when asserted) or placing the output in the high impedance state (when negated)**

Basic CMOS Logic Circuit Revisited



- **Calculate V_{out} for the case A=5V, B=0**

  P-ch device is "off" (R_{DS} = 500,000 Ω)

  N-ch device is "off" (R_{DS} = 500,000 Ω)

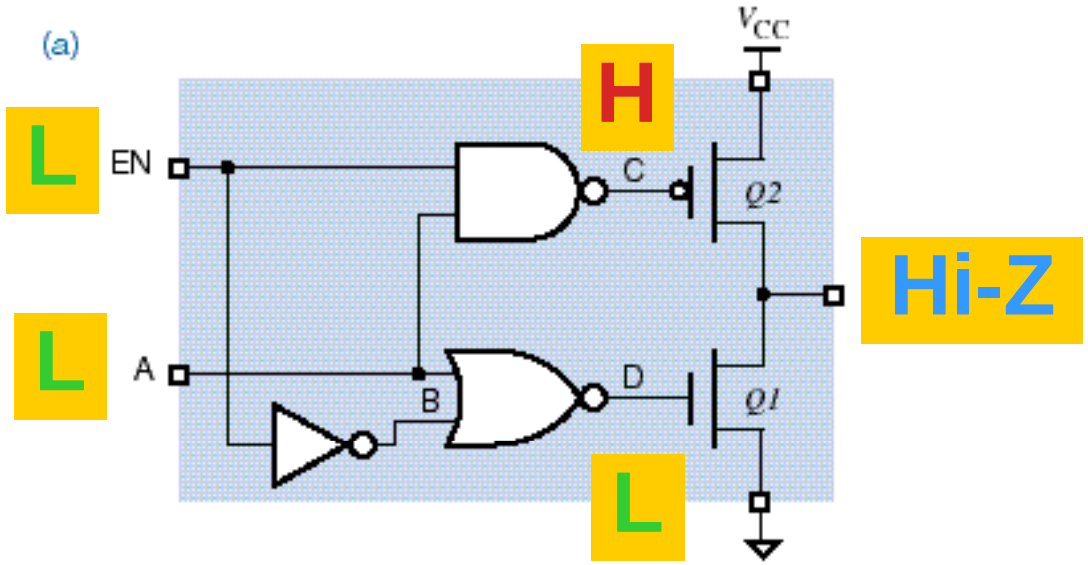
  V_{out} = 5 x (500,000 / 1,000,000) = 2.5 V

  $P_{dissipation}$ = 5^2 / 1,000,000 = 0.025 mW

Here, Vout is effectively disconnected (in the "Hi-Z state") when A is high and B is low

Use OE (output enable) signal to force A high and B low when OE is negated

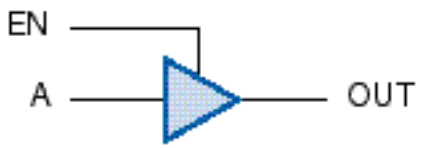
CMOS Tri-State Buffer Circuit

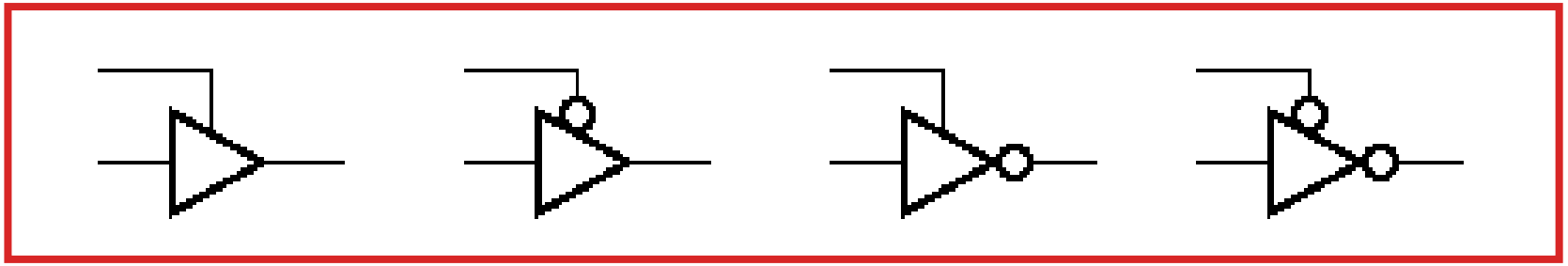


(b)

EN	A	B	C	D	Q1	Q2	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

(c)

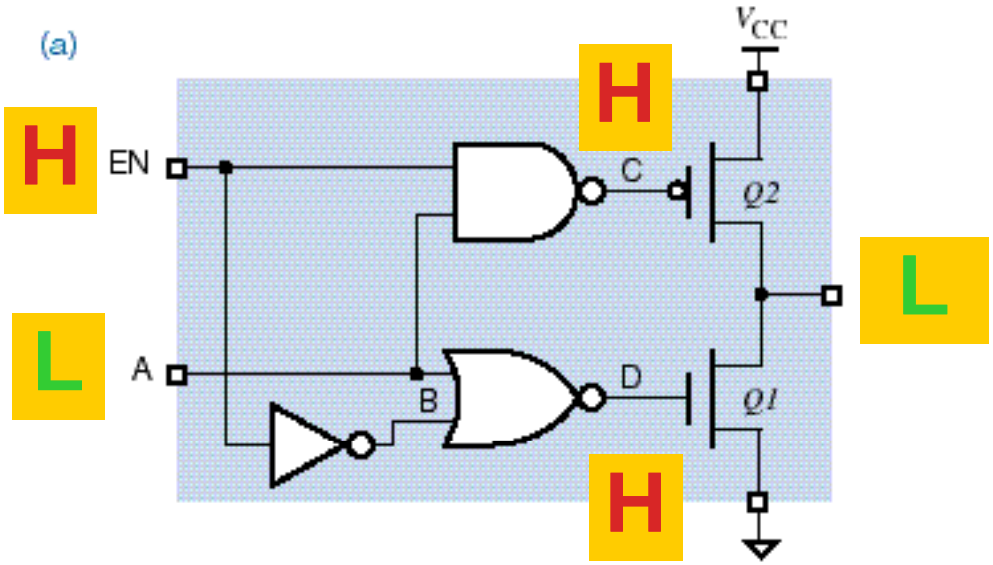




<u>Basic variations</u>: The buffer may be inverting or non-inverting, and the tri-state enable can either be active low or active high

CMOS Tri-State Buffer Circuit

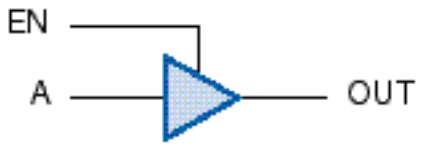
(a)

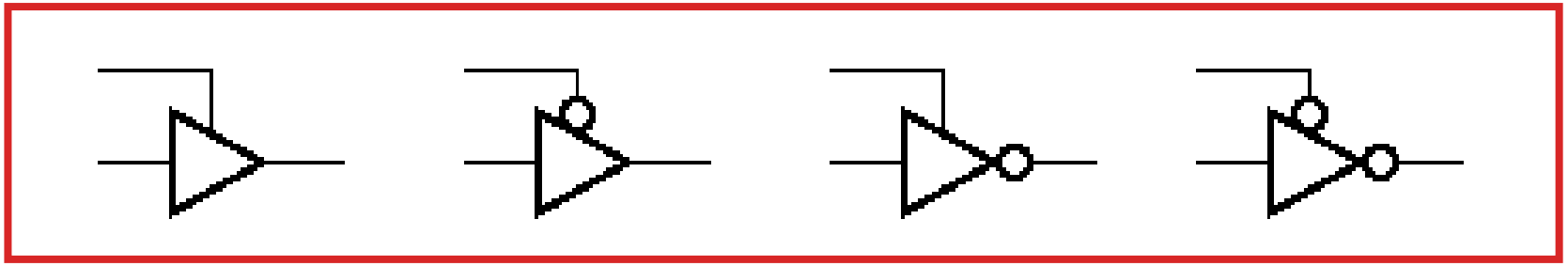


(b)

EN	A	B	C	D	Q1	Q2	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

(c)

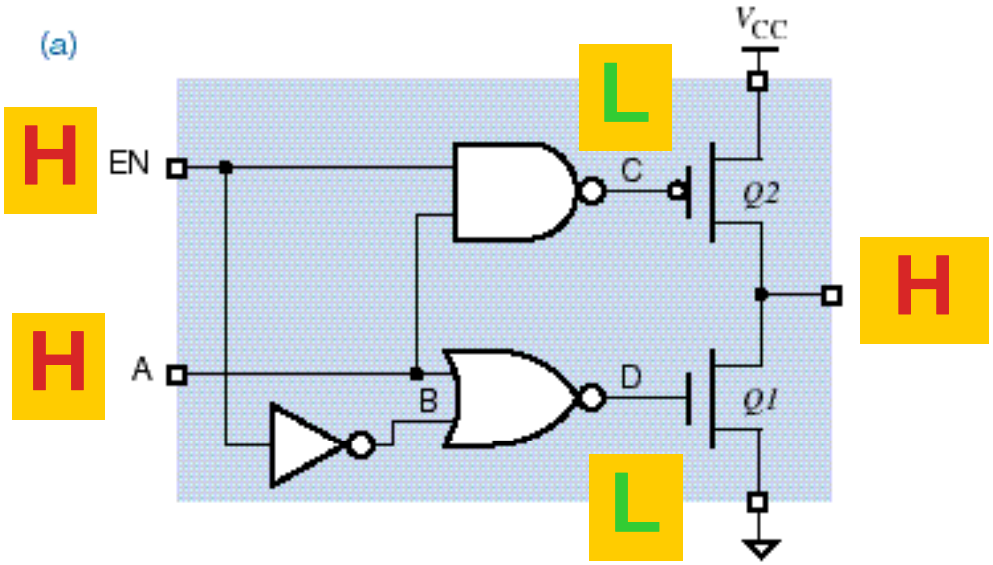




<u>Basic variations</u>: The buffer may be inverting or non-inverting, and the tri-state enable can either be active low or active high

CMOS Tri-State Buffer Circuit

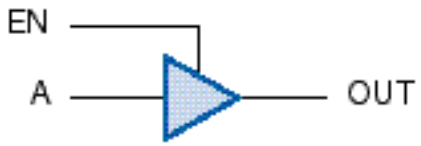
(a)

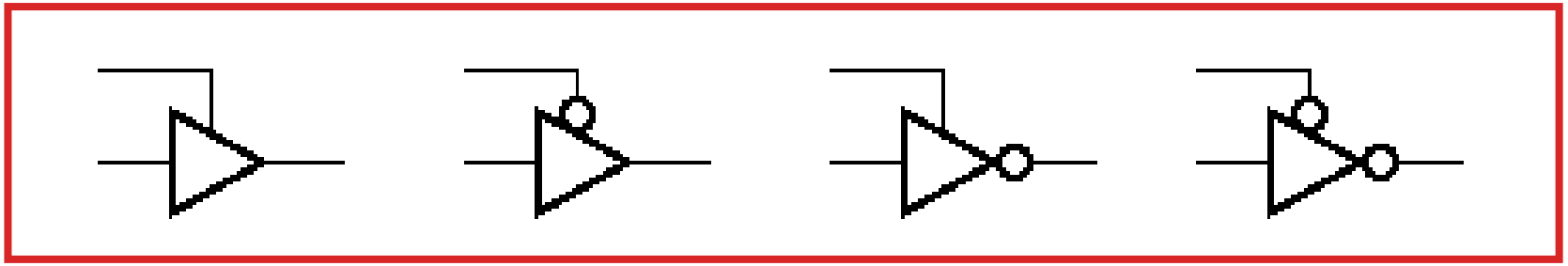


(b)

EN	A	B	C	D	Q1	Q2	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

(c)





<u>Basic variations</u>: The buffer may be inverting or non-inverting, and the tri-state enable can either be active low or active high

Tri-State Buffer Application – Buses

- **The most common use of tri-state buffers is to create *data buses* over which digital subsystems can (bi-directionally) send and receive data**
- **Definition: A *bus* is a collection of signals with a "common purpose" (e.g., sending the address of an item in memory, sending the data to be written to memory, etc.)**
- **A *bus transceiver* contains pairs of tri-state buffers connected in opposite directions between each pair of pins, so that data can be transferred in *either direction***

Tri-State Buffer Float Delay

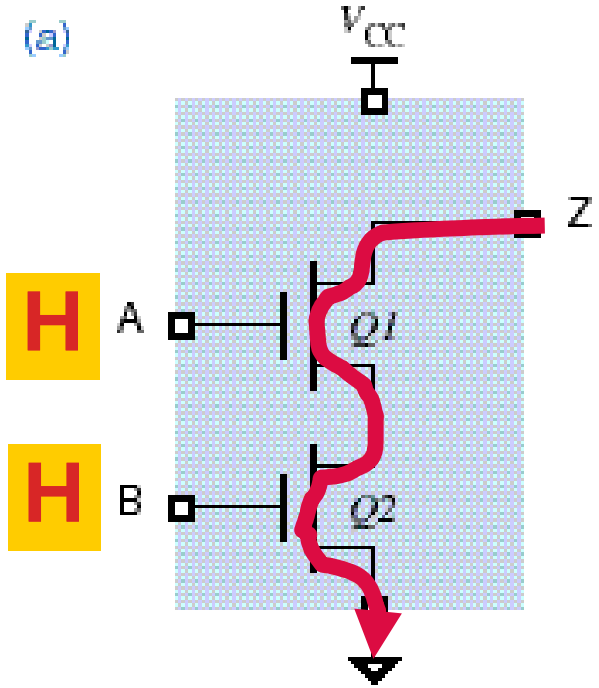
- **Tri-state outputs are typically designed so that they *go into* the Hi-Z (high impedance) state faster than they *come out of* the Hi-Z state (i.e., t_{pLZ} and t_{pHZ} are both less than t_{pZL} and t_{pZH})**
- **The time it takes to go from a "driven" state (valid logic level) to the Hi-Z "floating" state is called the *float delay***
- **Given this "rule", if one tri-state device is disabled and another tri-state device is enabled simultaneously, then the first device will get *off* the bus before the second one gets *on* – this helps prevent *fighting***

Open-Drain Outputs

- **Definition: A CMOS output structure that does not include a P-channel (pull-up) transistor is called an *open-drain output***
- **An open-drain output is in one of two states: LOW or "open" (i.e., disconnected)**
- **An *underscored diamond* (or "O.D.") is used to indicate that an output is open drain**
- **An open-drain output requires an external pull-up resistor to *passively* pull it high in the "open" state (since the output structure does NOT include a P-channel active pull-up)**

Open-Drain CMOS NAND Gate

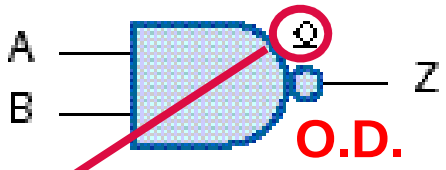
(a)



(b)

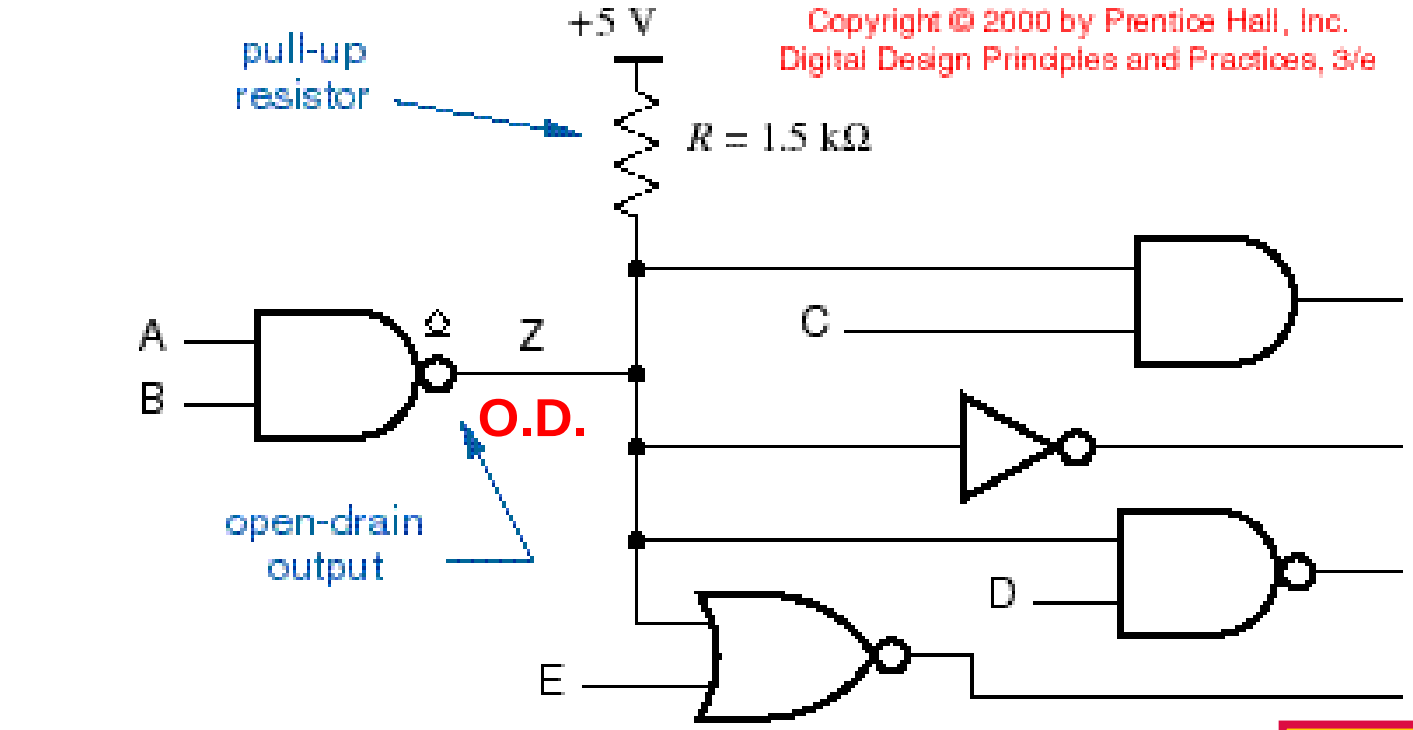
A	B	Q1	Q2	Z
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L

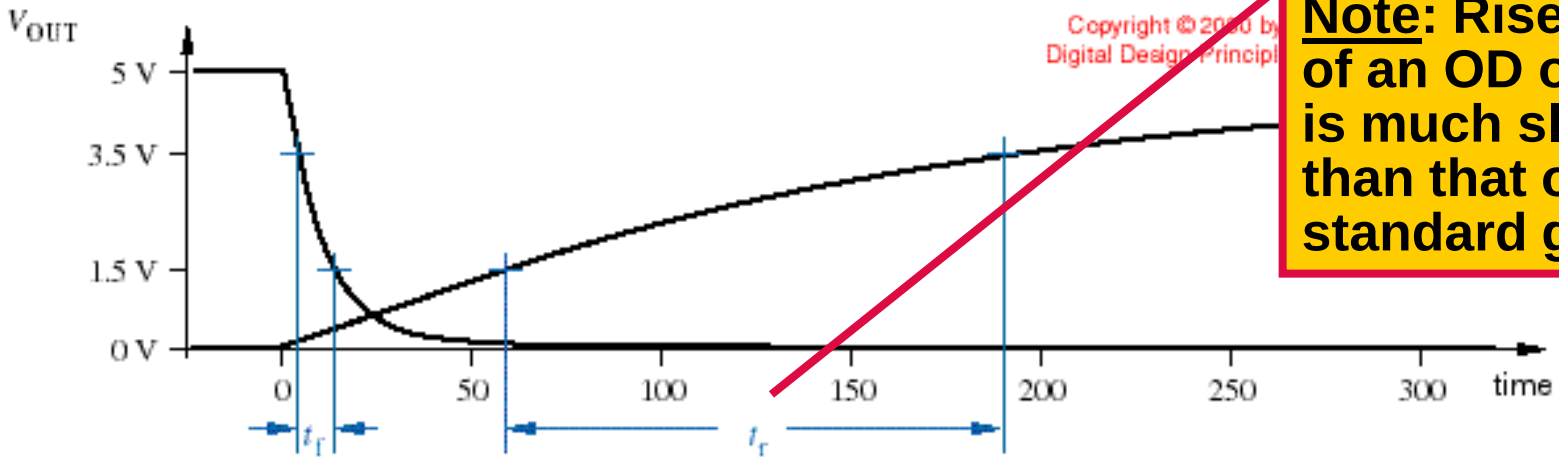
(c)



Symbol that denotes an open-drain output

Open-Drain Gate Driving a Load

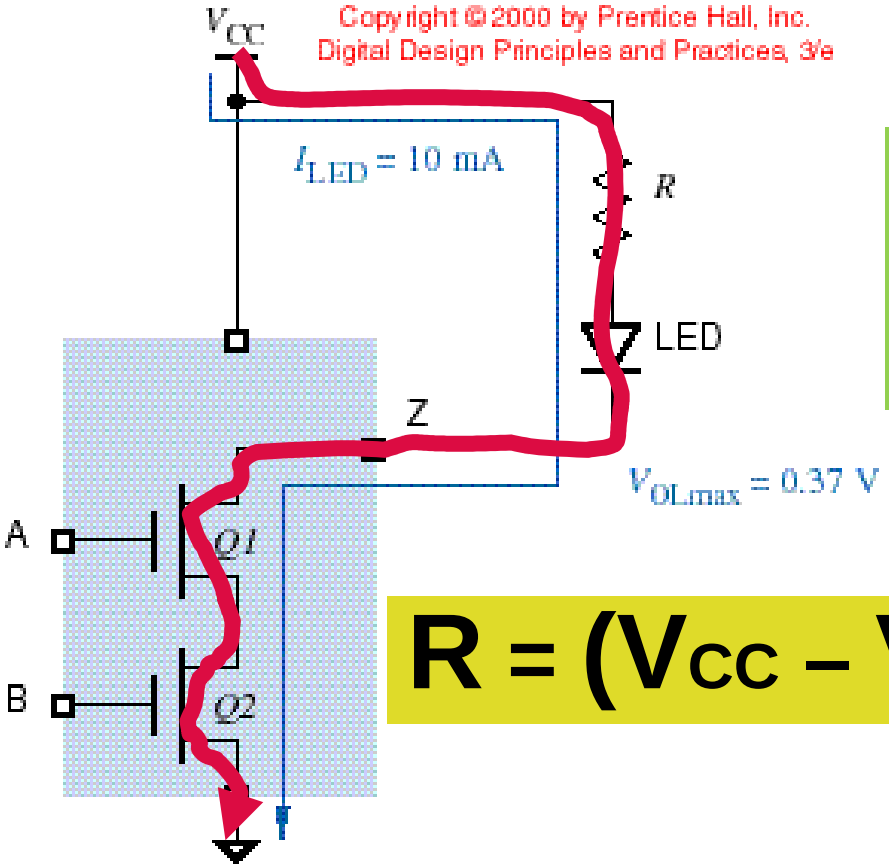




Note: Rise time of an OD output is much slower than that of a standard gate

Driving LEDs

- **One application for open-drain outputs is driving light-emitting diodes (LEDs)**

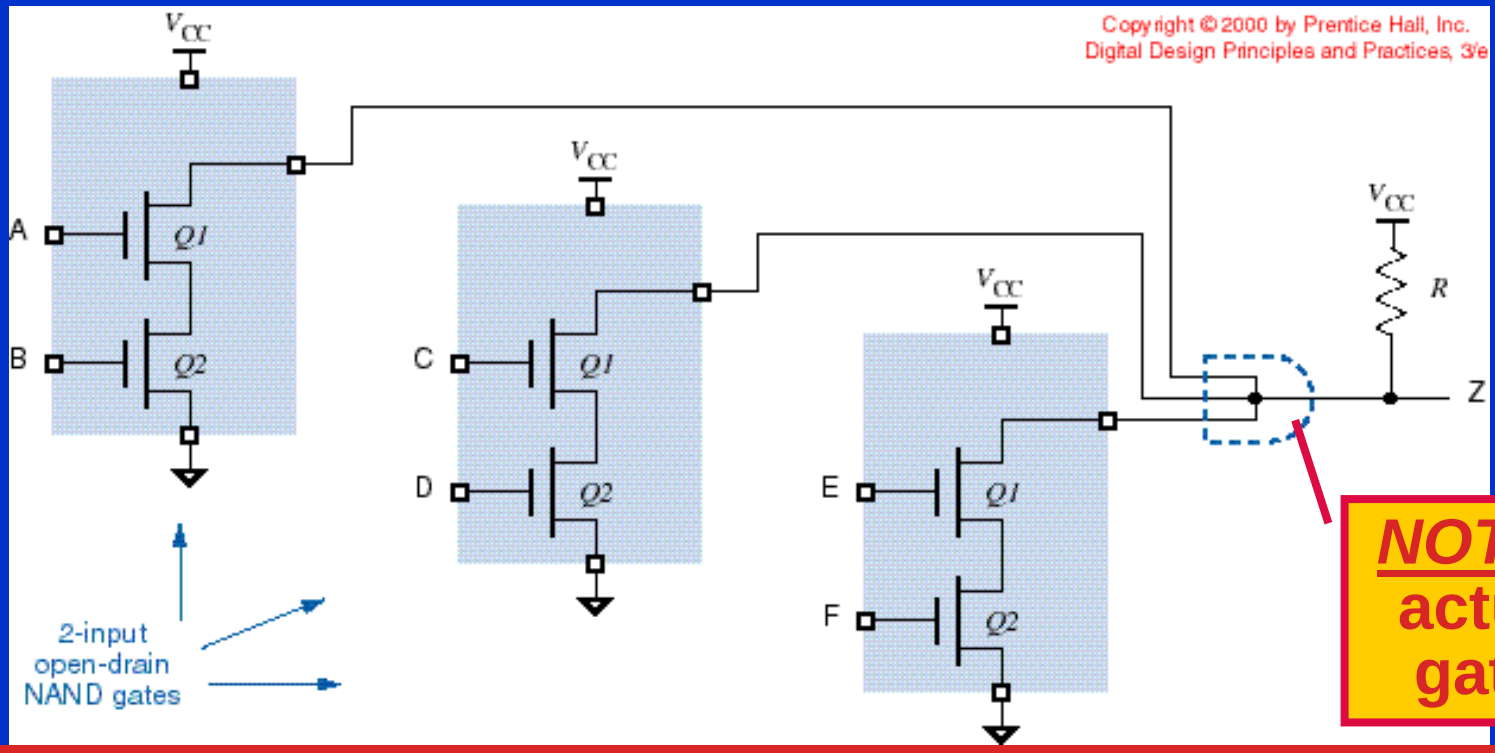


O.D. outputs can typically sink more current than conventional gates

$$R = (V_{CC} - V_{OL} - V_{LED}) / I_{LED}$$

Wired Logic

- **Definition: *Wired logic* is performed if the outputs of several open-drain gates are tied together with a single pull-up resistor**

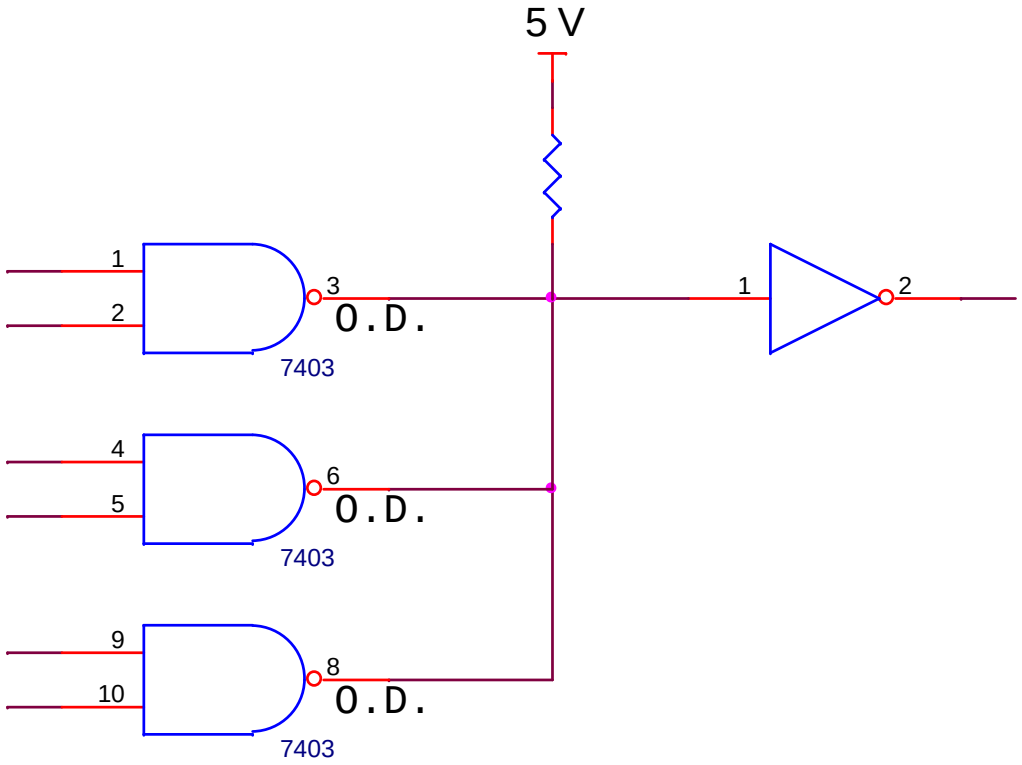


Caution: This ONLY works for open-drain outputs!

Pull-up Resistor Calculations

- **In open-drain applications, two calculations bracket the allowable values of the pull-up resistor R:**
  - **LOW The sum of the current through R plus the LOW state input currents of the gate inputs driven *must not exceed* the $I_{OL_{max}}$ of the active device**
  - **HIGH The voltage drop across R in the HIGH state *must not reduce* the output voltage below the $V_{IH_{min}}$ of the driven gate inputs**

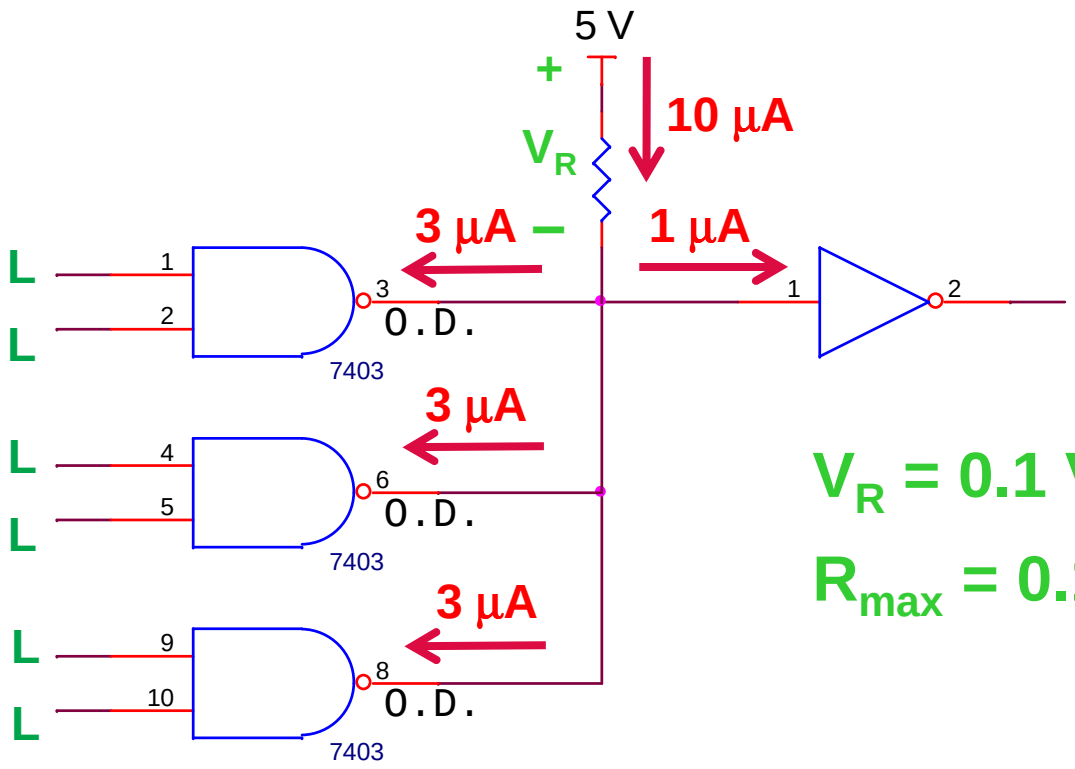
Example - Calculate a suitable value of pull-up resistor to use with the following circuit:



Specifications (hypothetical data):

- Off-state leakage current of O.D. NAND gate output: +3 μA
- I_{IH} and I_{IL} required by inverter input: ±1 μA
- V_{IH} desired for inverter input: 4.9 V
- $I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V

Solution, maximum R Value – based on V_{IH} desired



V_R = 0.1 V I_R = 10 μA

R_{max} = 0.1/0.00001 = 10,000 Ω

Specifications (hypothetical data):

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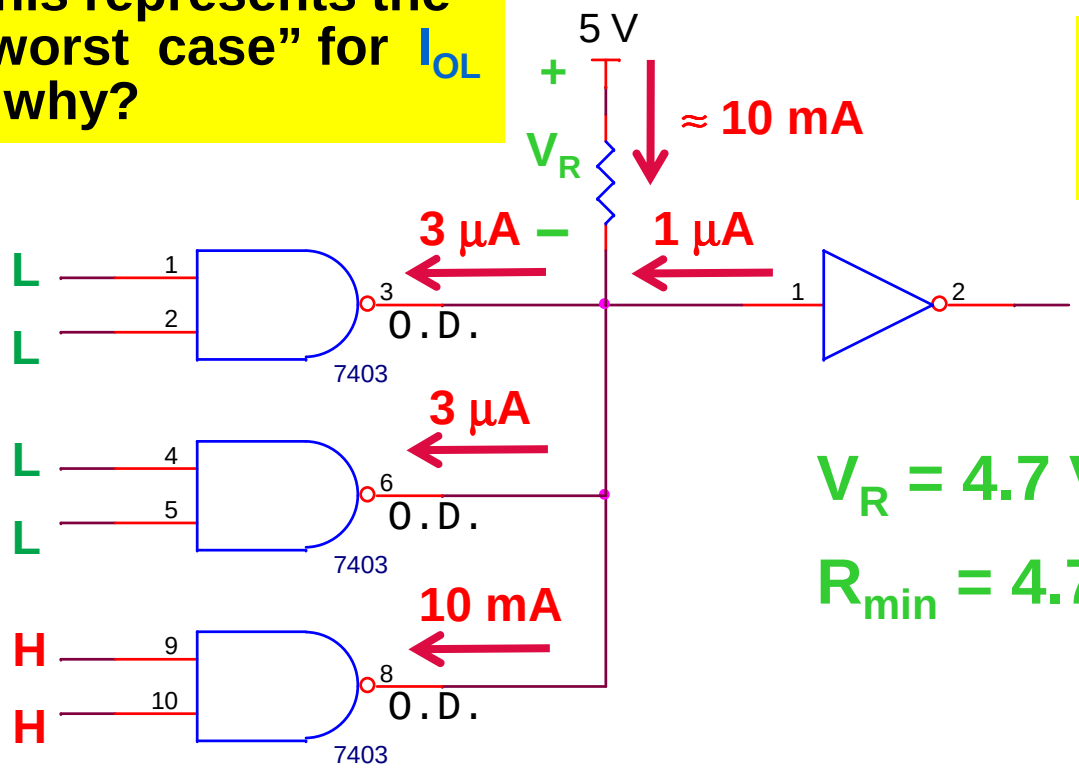
- V_{IH} desired for inverter input: 4.9 V
- $I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V

Solution, minimum R Value – based on $I_{OL\ max}$ of one gate

This represents the "worst case" for I_{OL} – why?



Here, can safely ignore leakage and I_{IL} currents – why?

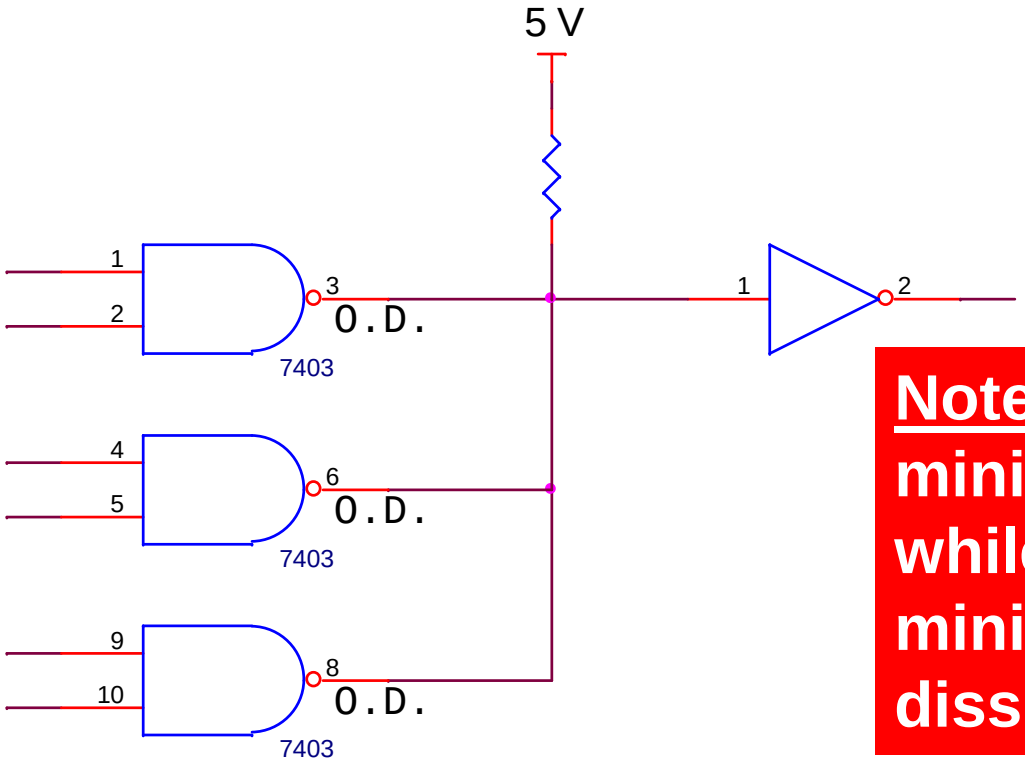
$V_R = 4.7\ V \quad I_R \approx 10\ mA$

$R_{min} = 4.7/0.01 = 470\ \Omega$

Specifications (hypothetical data):

- Off-state leakage current of O.D. NAND gate output: +3 μA
- I_{IH} and I_{IL} required by inverter input: ±1 μA
- V_{IH} desired for inverter input: 4.9 V
- $I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V

Conclusion – a pull-up resistor ranging from 470 Ω (R_{min}) to 10,000 Ω (R_{max}) will satisfy the specified constraints



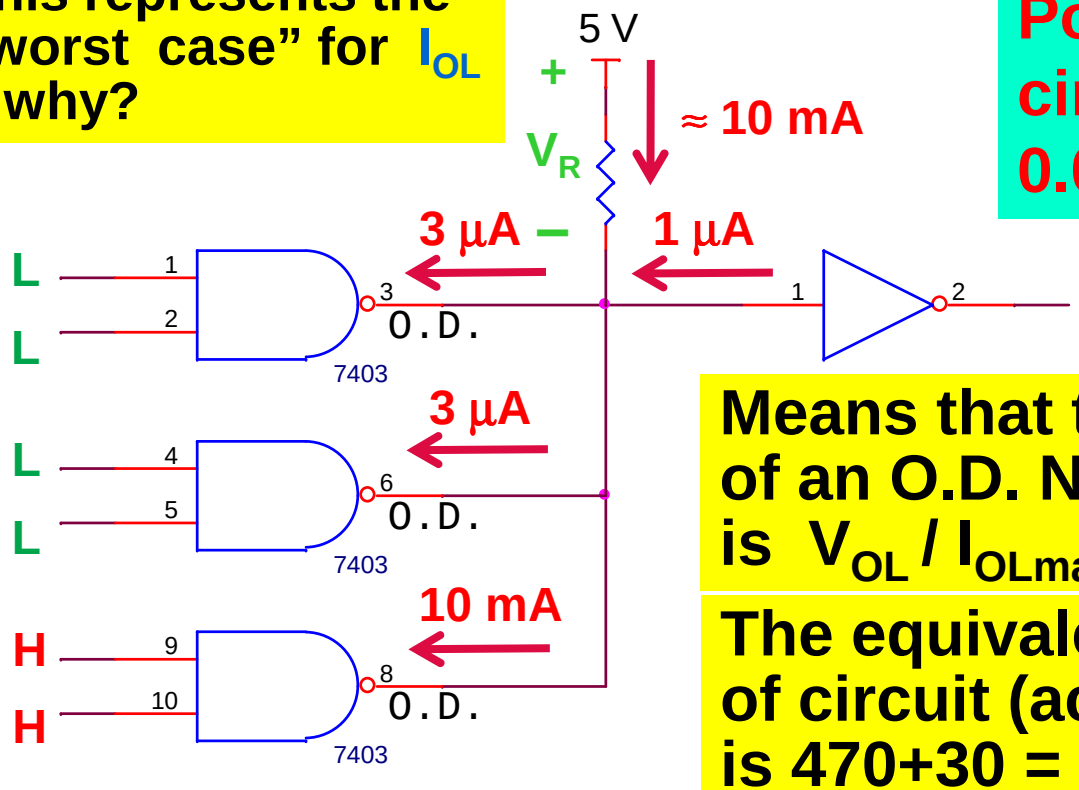
Note: Picking R_{min} will minimize the rise time, while picking R_{max} will minimize the power dissipation

Specifications (hypothetical data):

- Off-state leakage current of O.D. NAND gate output: +3 μA
- I_{IH} and I_{IL} required by inverter input: ±1 μA
- V_{IH} desired for inverter input: 4.9 V
- $I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V

Follow-up – "prove" the "worst case" scenario (R = 470 Ω)

This represents the "worst case" for I_{OL} – why?



Power dissipation of circuit is I_R^2 x R_{eq} = 0.01^2 x 500 ≈ 50 mW

Means that the "on" resistance of an O.D. NAND gate used here is V_{OL} / I_{OLmax} = 0.3/0.01 = 30 Ω

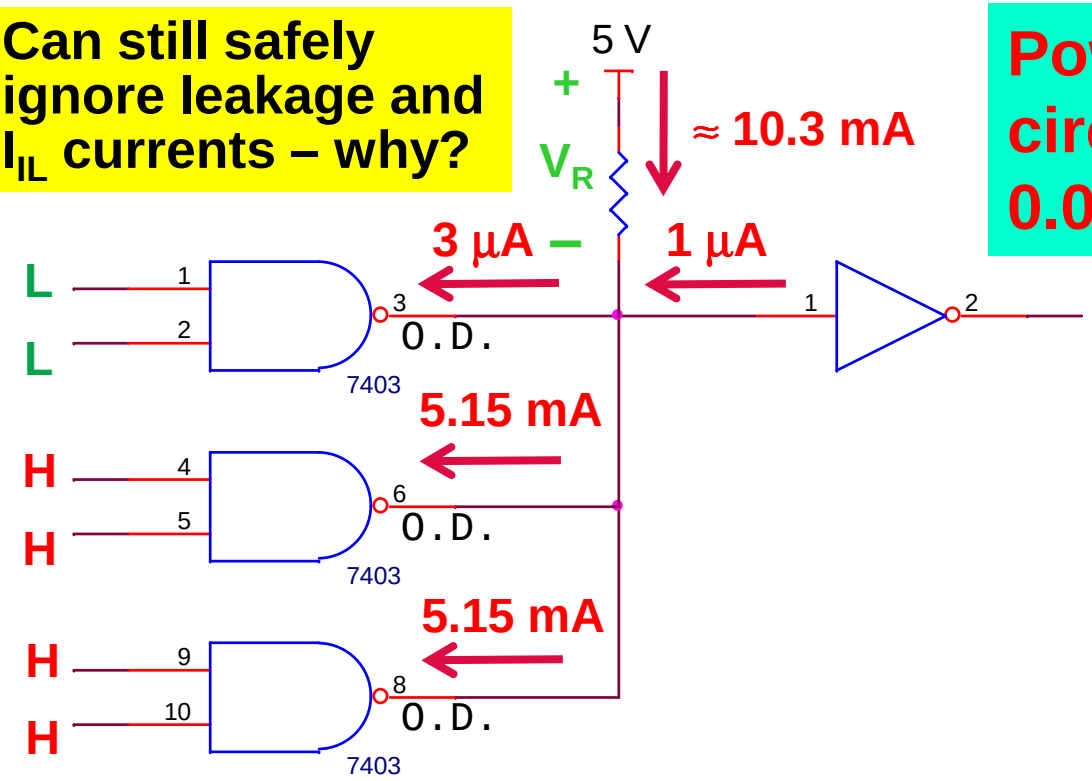
The equivalent load impedance of circuit (across power supply) is 470+30 = 500 Ω

Specifications (hypothetical data):

- Off-state leakage current of O.D. NAND gate output: +3 μA
- I_{IH} and I_{IL} required by inverter input: ±1 μA
- V_{IH} desired for inverter input: 4.9 V
- **$I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V**

Follow-up – "prove" the "worst case" scenario (R = 470 Ω)

Can still safely ignore leakage and I_{IL} currents – why?



Power dissipation of circuit is I_R^2 x R_{eq} = 0.0103^2 x 485 ≈ 51.5 mW

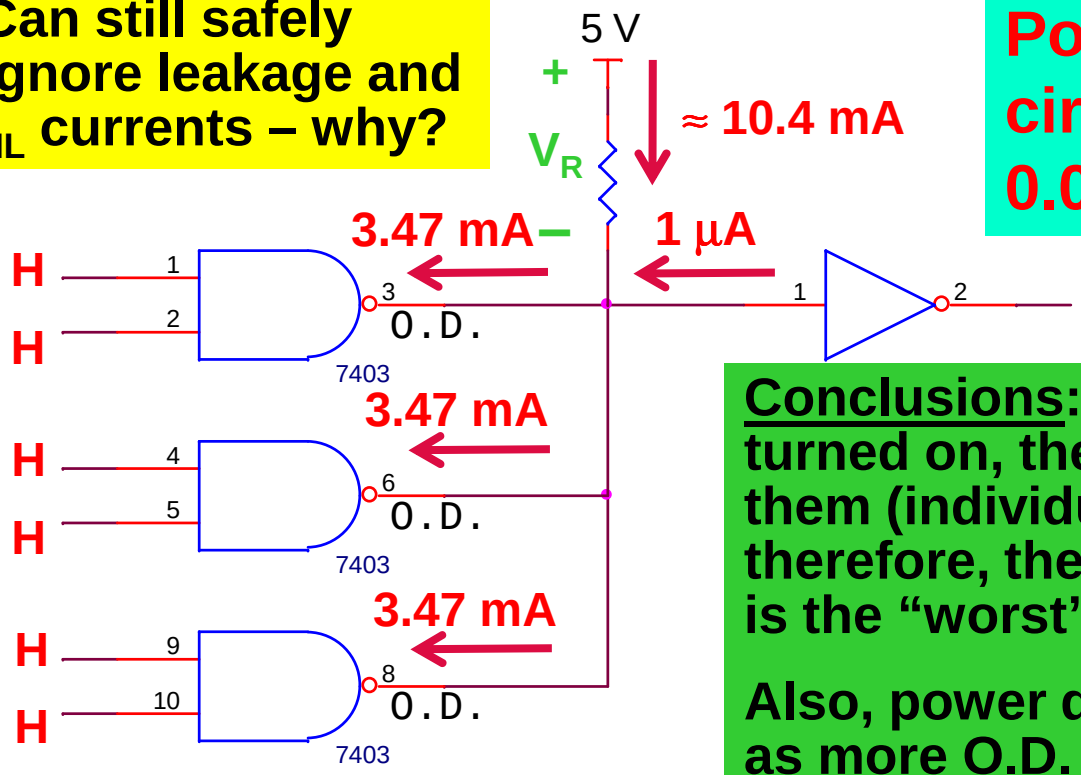
Next, turn on <u>two</u> O.D. gates

The equivalent load impedance of circuit is 470+15 = 485 Ω (because have two 30 Ω "on" resistances in parallel)

I_R is now 5 / 485 = 0.0103 A = 10.3 mA, which is <u>split</u> between the two gates that are "on"

Follow-up – "prove" the "worst case" scenario (R = 470 Ω)

Can still safely ignore leakage and I_{IL} currents – why?



Power dissipation of circuit is I_R^2 x R_{eq} = 0.0104^2 x 480 ≈ 52 mW

Conclusions: As more O.D. gates are turned on, the amount of current each of them (individually) has to sink is reduced; therefore, the first case (single gate "on") is the "worst" one with respect to I_{OL}.

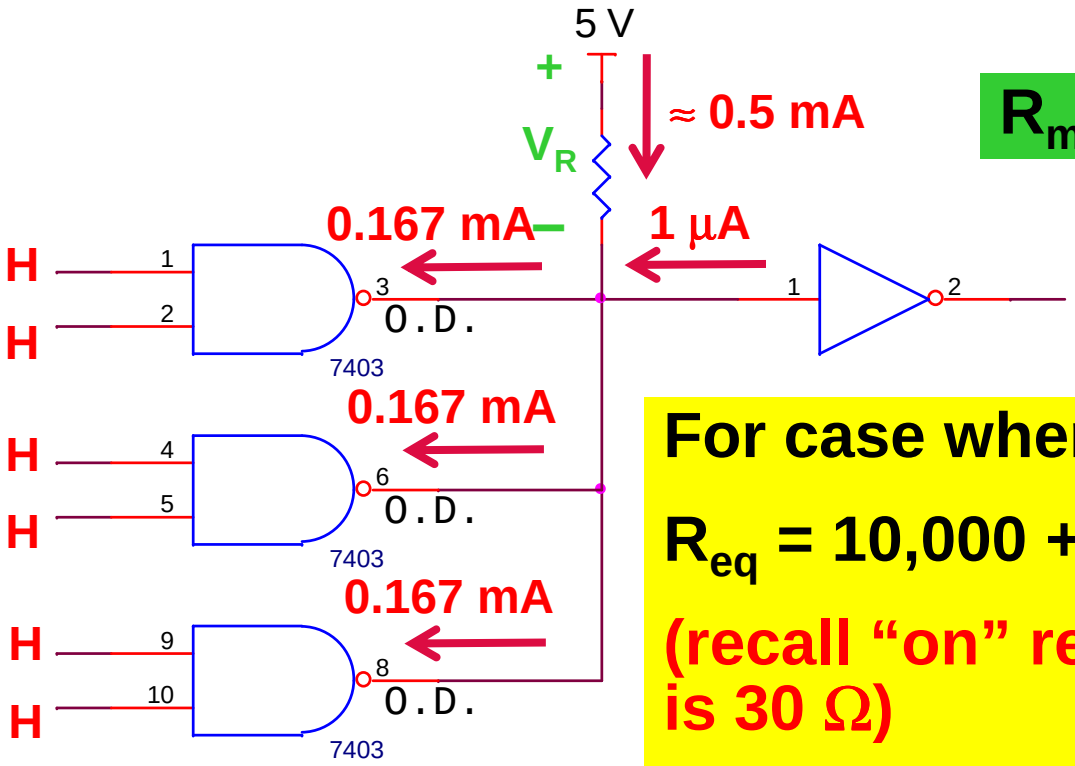
Also, power dissipation increases slightly as more O.D. gates are turned on.

Finally, turn on all three O.D. gates

The equivalent load impedance of circuit is 470+10 = 480 Ω (because have three 30 Ω "on" resistances in parallel)

I_R is now 5 / 480 = 0.0104 A = 10.4 mA, which is split among the three gates that are "on"

Follow-up – compare power dissipation of circuit using R_{min} vs. R_{max} as the pull-up resistor



R_{max} (10,000 Ω)

For case where all gates are <u>on</u>:

R_{eq} = 10,000 + 10 = 10,010 Ω

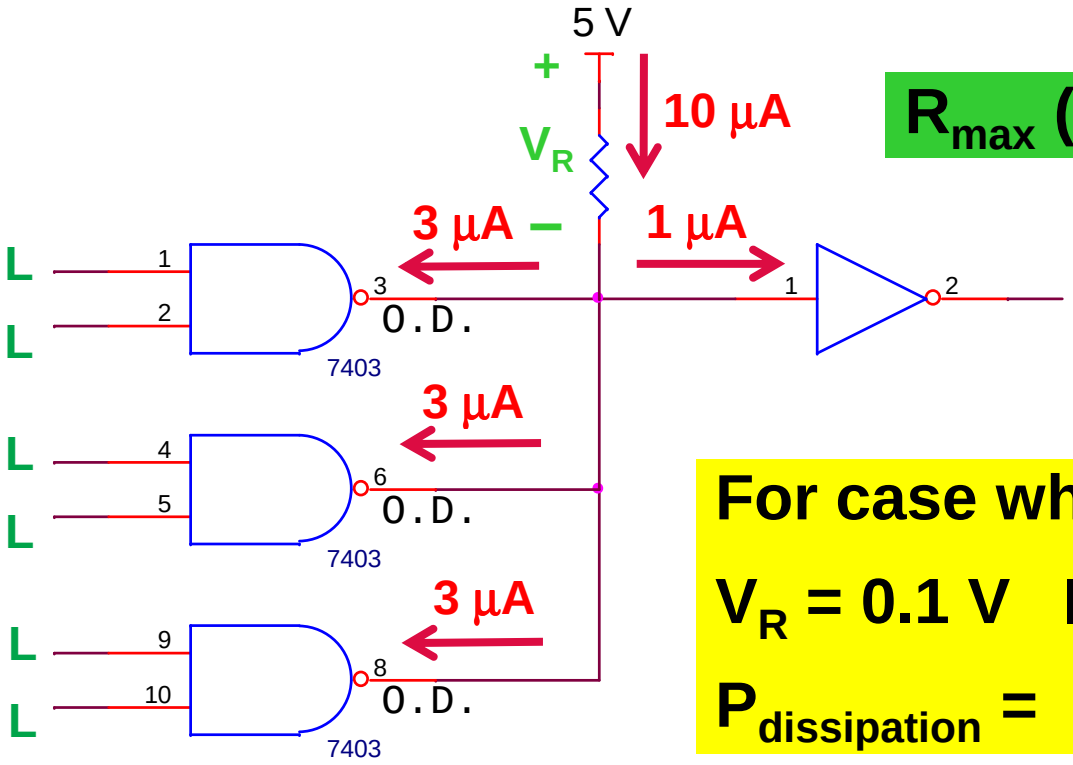
(recall "on" resistance of each gate is 30 Ω)

$I_R \approx 5 / 10{,}010 \approx 0.5$ mA (note - split among three gate outputs)

$P_{dissipation} = I_R^2 \times R_{eq} \approx 2.5$ mW

<u>Note</u>: V_{IL} of inverter is nearly 0 V

Follow-up – compare power dissipation of circuit using R_{min} vs. R_{max} as the pull-up resistor



R_{max} (10,000 Ω)

For case where all gates are <u>off</u>:

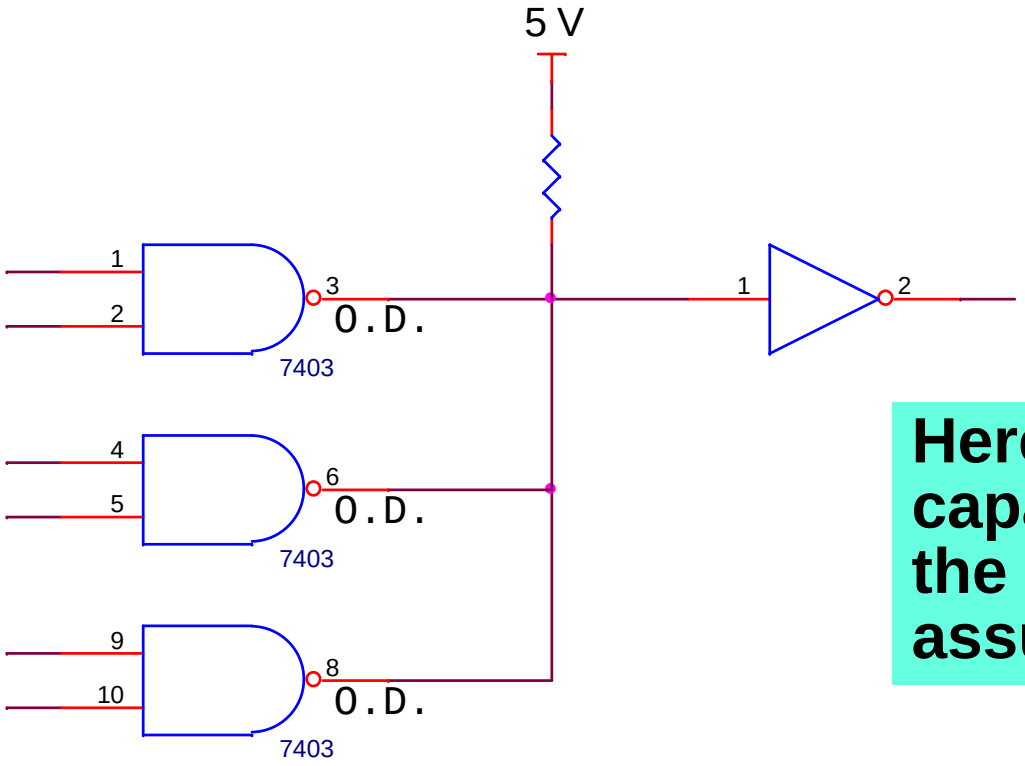
V_R = 0.1 V I_R = 10 μA

$P_{dissipation} = I_R^2 \times R = 1$ μW

<u>Note</u>: V_{IH} of inverter is 4.9 V

<u>Conclusion</u>: Power dissipation when R_{max} is used does not exceed 2.5 mW (vs. 52 mW for R_{min}); therefore, use of R_{max} minimizes the power dissipation

Follow-up – compare rise time estimates of circuit using R_{min} vs. R_{max} as the pull-up resistor

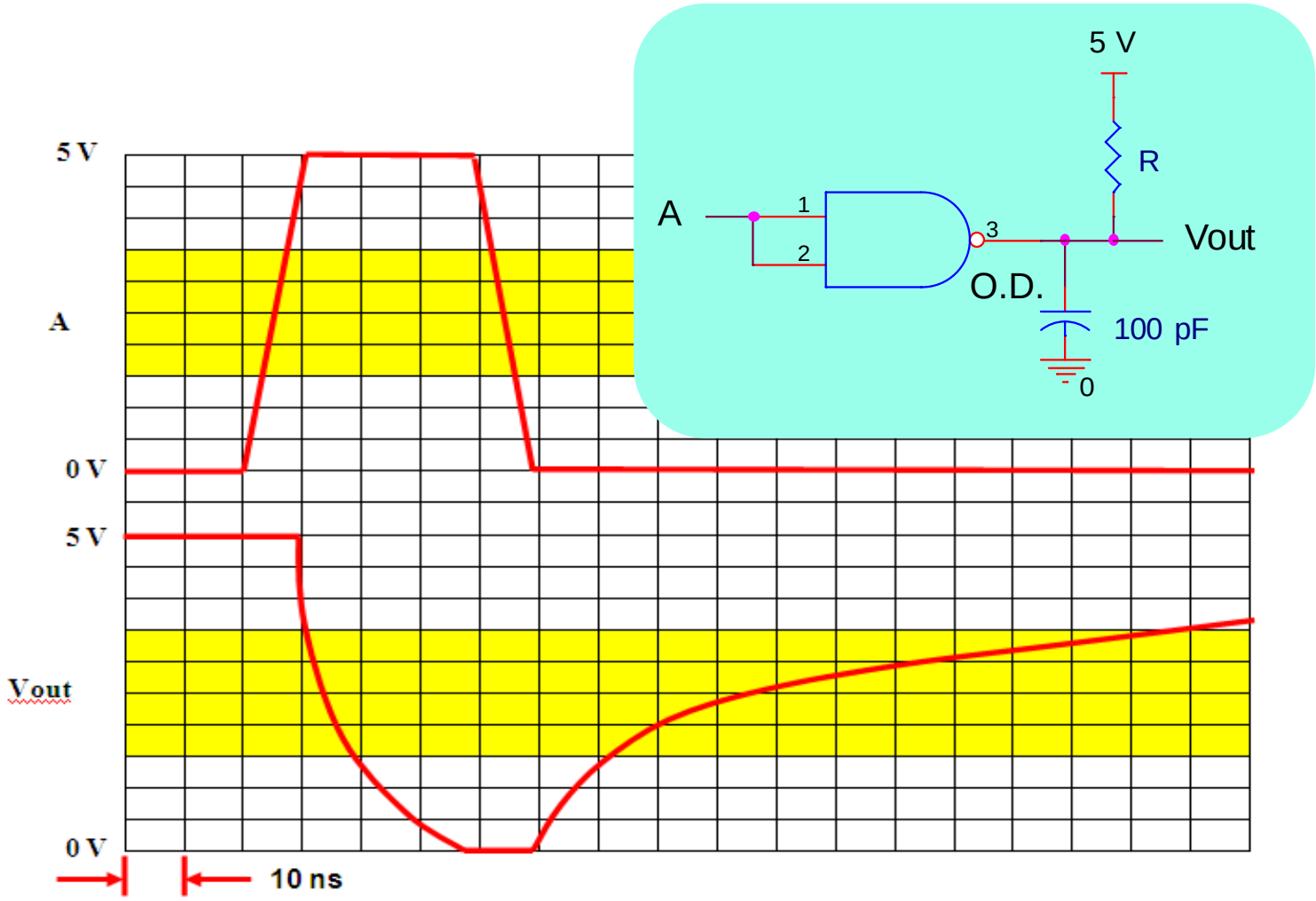


Here, need to know the capacitive load (C_L); for the sake of analysis, assume it is 100 pF

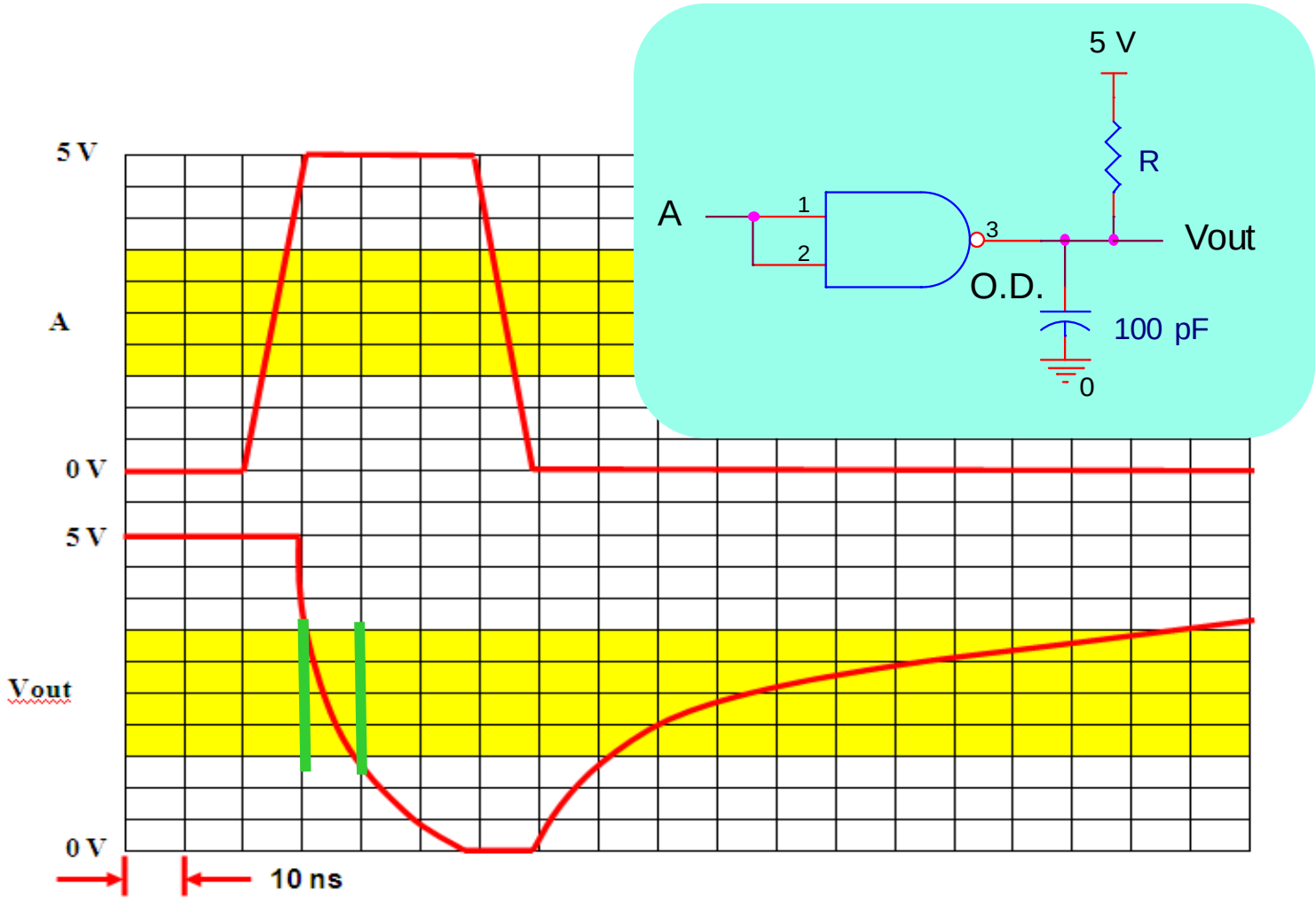
Comparison:

- **For $R_{min,}$ rise time estimate is 470 x 100 x 10^{-12} = 47 ns**
- **For $R_{max,}$ rise time estimate is 10,000 x 100 x 10^{-12} = 1000 ns**
- **Conclusion: rise time for R_{max} case is <u>considerably longer</u>**

Example – Estimate the "on" resistance of an O.D. gate and pull-up resistor value based on rise/fall times

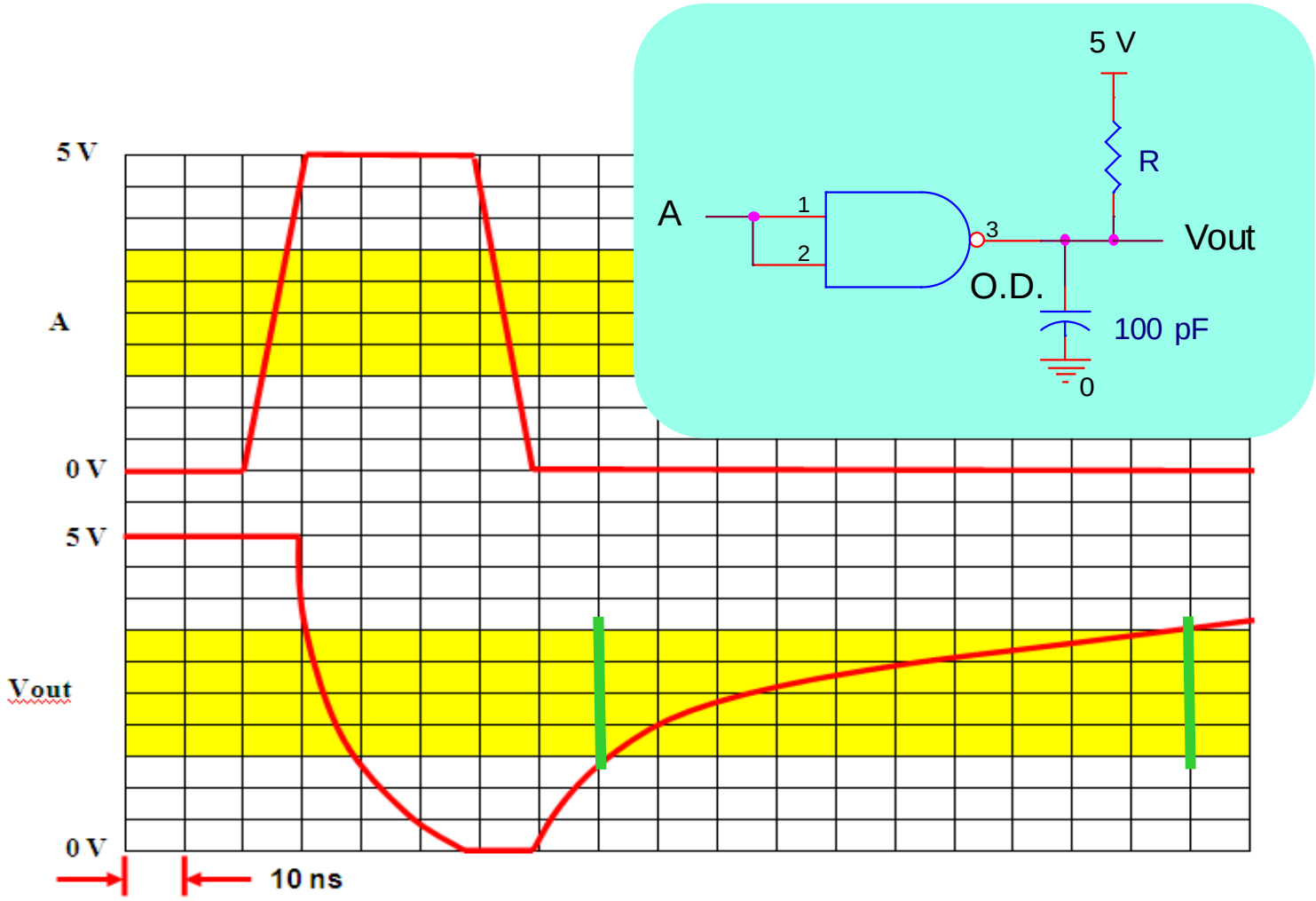


Example – Estimate the "on" resistance of an O.D. gate and pull-up resistor value based on rise/fall times



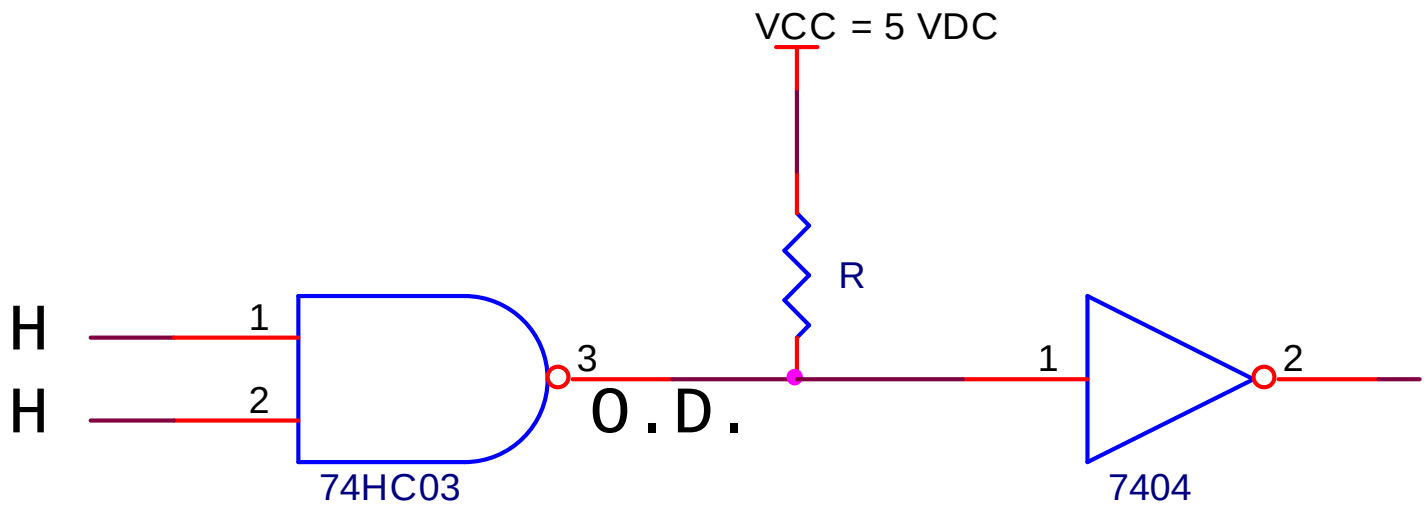
fall time = 10 ns = R_{on} x 100 pF $\rightarrow$ R_{on} = 100Ω

Example – Estimate the "on" resistance of an O.D. gate and pull-up resistor value based on rise/fall times



rise time = 100 ns = $R_{pull\text{-}up}$ x 100 pF → $R_{pull\text{-}up}$ = 1000 Ω

Clicker Quiz



Assume that measurements taken in laboratory reveal that a 74HC03 (open-drain CMOS NAND gate) will produce a V_{OL} = 0.2 V when sinking +2 mA of current. Also, assume that the I_{IL} required by a 7404 (standard-series TTL inverter) to recognize a logic "0" is -0.4 mA and that its I_{IH} (to recognize a logic "1") is +40 µA.

1. Based on the laboratory measurements cited in the figure, what is the "ON" resistance of the 74HC03's active output device?

A. 10 Ω

B. 20 Ω

C. 100 Ω

D. 1000 Ω

E. none of the above

2. If the capacitive load on the output of the NAND gate is 20 pF, *estimate* the *fall time* of the signal at the input to the inverter (assuming "ON" resistance calculated in previous problem):

A. **2 ns**

B. **16 ns**

C. **20 ns**

D. **160 ns**

E. **none of the above**

3. Calculate the value of the pull-up resistor that allows the open-drain NAND gate to produce a $V_{OL} = 0.2$ V when sinking 2 mA of current (i.e., $I_{OL} = +2$ mA) and pulling the input of the 7404 low.

A. 1000 Ω

B. 2000 Ω

C. 3000 Ω

D. 8000 Ω

E. none of the above

4. If the capacitive load on the output of the NAND gate is 20 pF, *estimate* the *rise time* of the signal at the input to the inverter assuming a pull-up resistor value of 3000Ω (calculated in previous problem):

A. 2 ns

B. 16 ns

C. 20 ns

D. 60 ns

E. none of the above

5. Assuming that the off-state leakage current of the 74HC03 is +10 μA, calculate the value of the pull-up resistor that produces a V_{IH} = 4.5 V at the 7404 input.

A. 4000 Ω

B. 9000 Ω

C. 10,000 Ω

D. 90,000 Ω

E. none of the above