Demand Paging

ECE595
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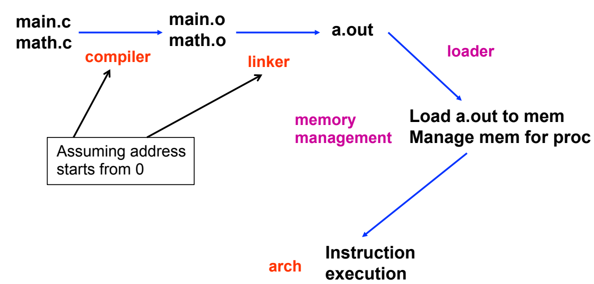
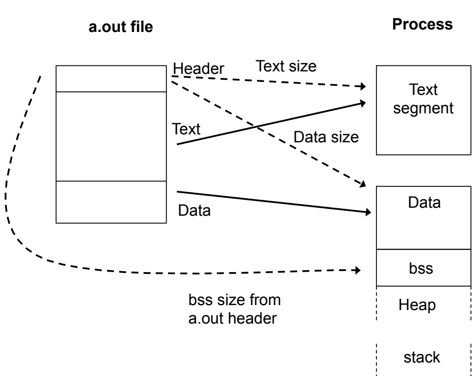
[lec13] The big picture – connecting the dots



[lec13] Loading

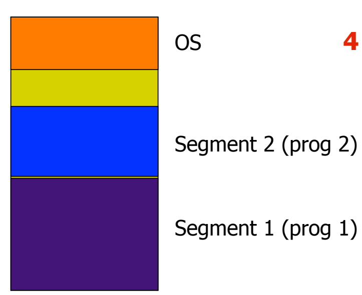


bss = block started by symbols (un-initialized data segment)

Review: sharing main memory

- Simple multiprogramming

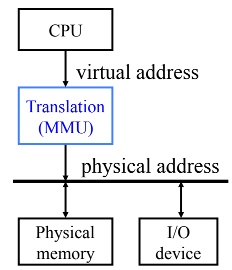
4 drawbacks?



[lec15] 3. Dynamic memory relocation

- Instead of changing the address of a program before it's loaded, change the address dynamically *during every reference*
  - Under dynamic relocation, each program-generated address (called a *logical address* or *virtual address*) is translated in hardware to a *physical* or *real address* at runtime

[week5] Translation overview



- Actual translation is in hardware (MMU)
- Controlled in software
- CPU view
  - what program sees, virtual memory
- Memory view
  - physical memory

What is the essence of going through MMU?

[lec15] Sharing main memory

- Simple multiprogramming – 4 drawbacks
  - Lack of protection
  - Cannot relocate dynamically
    → Base-and-bound
  - Single segment per process
    → Paging, segmentation, etc.
  - Entire address space needs to fit in mem

Dynamic Memory Relocation

[lec15] Sharing main memory

- Simple multiprogramming – 4 drawbacks
  - Lack of protection
  - Cannot relocate dynamically
    → dynamic memory relocation: base&bound
  - Single segment per process
    → dynamic memory relocation: segmentation, paging
  - Entire address space needs to fit in mem
    - More need for swapping
    - Need to swap whole, very expensive!

Tackling the last drawback

- Key observation:
  - a process often only needs a small amount of its total address space at any time (*reference locality!*)

[week1] What is an OS?

Extended (abstract) machine (answer 2)

- Much more ideal environment than the hardware
  - Ease to use
  - Fair (well-behaved)
  - Portable (back-compatible)
  - Reliable
  - Safe
- Illusion of infinite, private resources
  - Single processor → many separate processors
  - Single memory → many separate, larger memories

?

Virtual Memory

- Definition: *Virtual memory* permits a process to run with only some of its virtual address space loaded into physical memory
- Key idea: Virtual address space translated to either
  - Physical memory (small, fast) or
  - Disk (backing store), large but slow
- Deep thinking – what made above possible?
- Objective:
  - To produce the illusion of memory as big as necessary

Virtual Memory

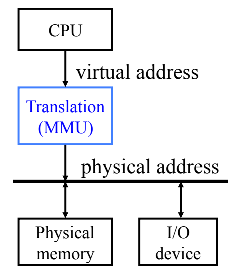
- "To produce the illusion of memory as big as necessary"
  - Without suffering a huge slowdown of execution
  - Why makes this possible?
  - *Principle of locality*
    - Knuth's estimate of 90% of the time in 10% of the code
    - There is also significant locality in data references

Virtual Memory Implementation

- Virtual memory is typically implemented via *demand paging*
- *Demand paging:* paging with swapping, e.g., physical pages are swapped in and out of memory

Demand Paging
(paging with swapping)

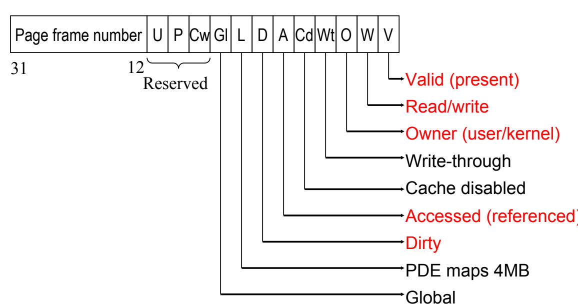
- If not all of a program is loaded when running, what happens when referencing a byte not loaded yet?
- How to detect this?
  - In software?



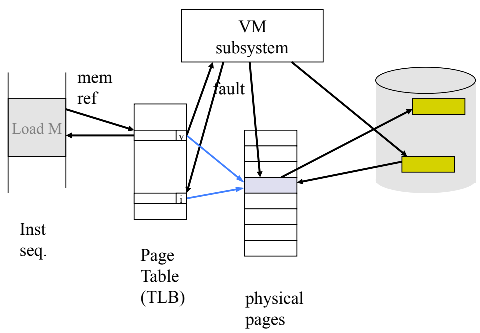
Demand Paging
(paging with swapping)

- If not all of a program is loaded when running, what happens when referencing a byte not loaded yet?
- Hardware/software cooperate to make things work
  - Extend PTEs with an extra bit "present"
  - Any page not in main memory right now has the "present" bit cleared in its PTE
  - If "present" isn't set, a reference to the page results in a trap by the paging hardware, called *page fault*
  - What needs to happen when page fault occurs?

x86 Page Table Entry



Page Fault Handling in Demand Paging



Page fault handling (cont)

- On a page fault
  - Find an unused phy. page or a used phy. page (how?)
  - If the phy. page is used
    - If it has been modified, write it to disk
    - Invalidate its current PTE and TLB entry (how?)
  - Load the new page from disk
  - Update the faulting PTE and its TLB entry
  - Restart the faulting instruction
- Supporting data structure
  - For speed: A list of unused physical pages (more later)
  - Data structure to map a phy. page to its pid and virtual address
    - Sounds faimiliar?

Page Fault Handling: Subtlety

- Page fault may have occurred in the middle of an instruction!
  - Suppose the instruction is restarted from the beginning
    - How is beginning located?
    - Side effects? MOVE (SP)+, R2
    - Require hardware support to keep track of side effects of instructions and undo them before restarting
  - You can make it easy when designing ISA
    - RISC (load-store) architecture make this relatively easy – only load/store can generate page faults

Miss handling: Hardware-controlled TLB

- On a TLB hit, MMU checks the valid bit
  - If valid, perform address translation
  - If invalid (e.g. page not in memory), MMU generates a page fault
    - OS performs fault handling
    - Restart the faulting instruction
- On a TLB miss
  - MMU parses page table and loads PTE into TLB
    - Needs to replace if TLB is full
    - PT layout is fixed
  - Same as hit …

Deep thinking: VM implementation

- Virtual memory is typically implemented via *demand paging*
- It can also be implemented via *demand segmentation*
  - Double drawbacks?

Deep thinking: Virtual Address vs. Virtual Memory

- Virtual address
  - Supported with dynamic memory relocation
    - Segmentation
    - Paging
- Virtual memory
  - Dynamic memory relocation + swapping
    - Demand paging
    - Demand segmentation

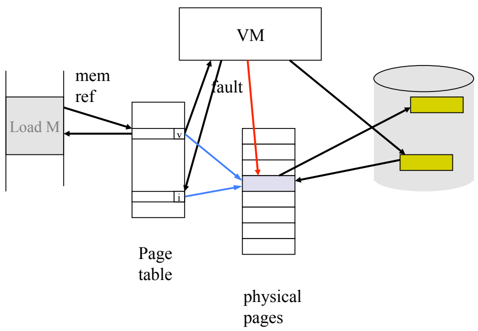
Tasks of the VM subsystem

- Once the hardware has provided basic capabilities for VM, OS must make two kinds of decisions
  - Page selection: when to bring pages into memory
  - Page replacement: which page(s) should be thrown out, and when

Page selection (when)

- Prepaging
  - Bring a page into memory before it is referenced
  - Hard to do without a “prophet"
- Request paging
  - Let user say which pages are needed when
  - Users don’t always know best
  - And aren’t always impartial
- Demand paging
  - Start up process with no pages loaded
  - Load a page when a page fault occurs, i.e., wait till it MUST be in memory
  - Almost all paging systems are demand paging

Page replacement algorithms? (which)



The BIG picture: Running at Memory Capacity

- Expect to run with all phy. pages in use
- Every "page-in" requires an eviction
- Goal of page replacement
  - Maximize hit rate → kick out the page that's least useful
- Challenge: how do we determine utility?
  - Kick out pages that aren't likely to be used again

- Page replacement is a difficult policy problem

Reading

- Chapter 8