Chapter 16
Analog Integrated Circuit Design Techniques

Microelectronic Circuit Design

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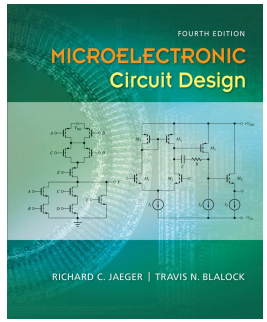
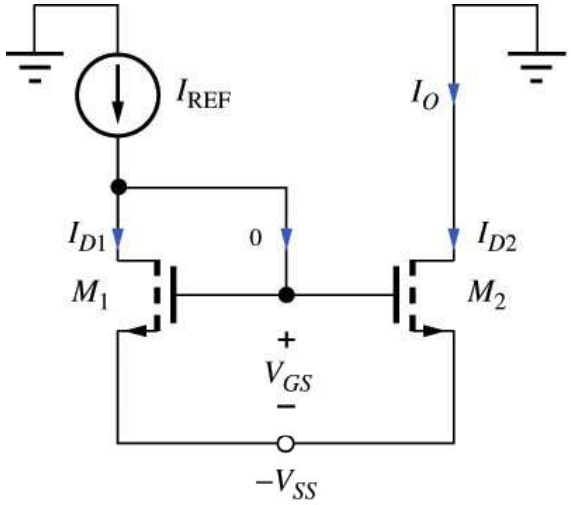


Chapter Goals

- Understand bipolar and MOS current mirror operation and mirror ratio errors.
- Explore high output resistance current sources.
- Design current sources for both discrete and integrated applications.
- Study reference current circuits such as V_{BE}-based reference, bandgap reference and Widlar current source.
- Use current mirrors as active loads in differential amplifiers to increase voltage gain of single-stage amplifiers.
- Study effects of device mismatch on amplifier performance.
- Analyze design of classic μA741 op amp.
- Increase understanding of SPICE simulation techniques.

MOS Current Mirrors: DC Analysis



MOSFETs M_1 and M_2 are assumed to have identical V_{TN}, K_n', λ, and W/L ratios.

I_{REF} provides operating bias to mirror.

$V_{DS1} = V_{GS1} = V_{GS2} = V_{GS}$

$$V_{GS1} = V_{TN} + \sqrt{\frac{2I_{REF}}{K_{n1}(1+\lambda V_{DS1})}}$$

$$I_O = I_{D2} = \frac{K_n}{2}\left(V_{GS2} - V_{TN}\right)^2\left(1+\lambda V_{DS2}\right)$$

$$\therefore I_O = I_{REF}\frac{\left(1+\lambda V_{DS2}\right)}{\left(1+\lambda V_{DS1}\right)} \cong I_{REF}$$

However, V_{DS1} is not equal to V_{DS2} and there is slight mismatch between output and reference currents. Mirror ratio is:

$$\text{MR} = \frac{I_O}{I_{REF}} = \frac{\left(1+\lambda V_{DS2}\right)}{\left(1+\lambda V_{DS1}\right)}$$

MOS Current Mirror (Example)

Problem: Calculate output current for given current mirror.

Given data: I_{REF} = 150 μA, V_{SS} = 10 V, V_{TN} = 1 V, K_n = 250 μA/V^2, λ = 0.0133 V^{-1}

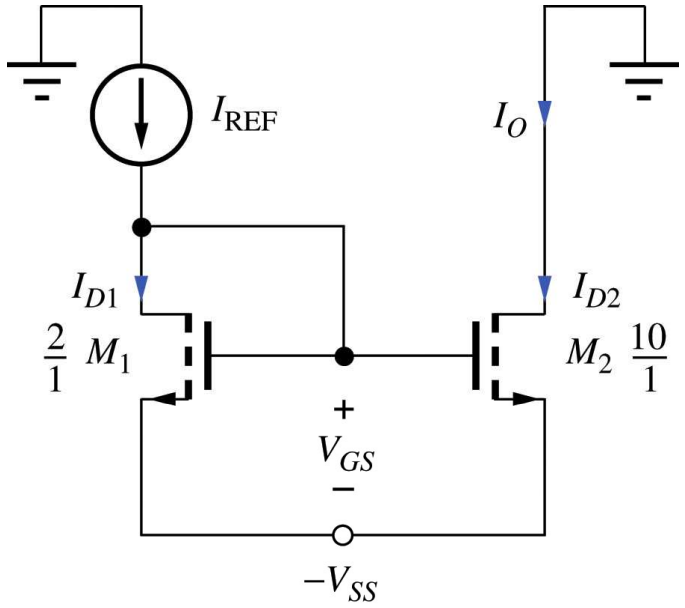
Analysis: $(1+\lambda V_{DS1})$ term is neglected to simplify dc bias calculation.

$$V_{DS1} = V_{GS1} = V_{TN} + \sqrt{\frac{2I_{REF}}{K_n}} = 1\text{V} + \sqrt{\frac{2(150\,\mu\text{A})}{250\,\frac{\mu\text{A}}{\text{V}^2}}} = 2.10\,\text{V}$$

$$\therefore I_O = (150\mu\text{A})\frac{\left(1+\frac{0.0133}{\text{V}}(10\text{V})\right)}{\left(1+\frac{0.0133}{\text{V}}(2.10\text{V})\right)} = 165\mu\text{A}$$

Actual currents are found to be mismatched by approximately 10%.

MOS Current Mirrors: Changing Mirror Ratio



Mirror ratio can be changed by modifying *W/L* ratios of the two transistors forming the mirror.

$$K_{n1} = K_n'\left(\frac{W}{L}\right)_1 \qquad K_{n2} = K_n'\left(\frac{W}{L}\right)_2$$

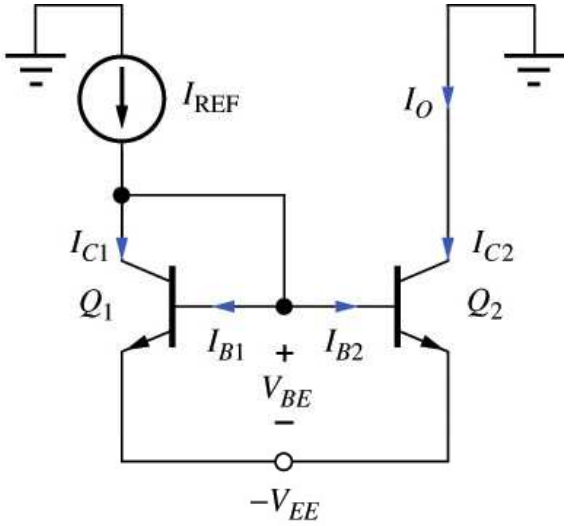
$$\therefore I_O = I_{REF}\frac{K_{n2}\left(1+\lambda V_{DS2}\right)}{K_{n1}\left(1+\lambda V_{DS1}\right)}$$

$$= I_{REF}\frac{\left(\frac{W}{L}\right)_2\left(1+\lambda V_{DS2}\right)}{\left(\frac{W}{L}\right)_1\left(1+\lambda V_{DS1}\right)}$$

$$\text{MR} = \frac{\left(\frac{W}{L}\right)_2\left(1+\lambda V_{DS2}\right)}{\left(\frac{W}{L}\right)_1\left(1+\lambda V_{DS1}\right)}$$

In given current mirror, $I_o = 5I_{REF}$. Again mismatch in V_{DS} causes error in MR.

Bipolar Current Mirrors: DC Analysis



$$I_{C1} = I_S \exp\left(\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE1}}{V_A}\right) \qquad I_{C2} = I_S \exp\left(\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE2}}{V_A}\right)$$

$$\beta_{F1} = \beta_{FO}\left(1+\frac{V_{CE1}}{V_A}\right) \qquad \beta_{F2} = \beta_{FO}\left(1+\frac{V_{CE2}}{V_A}\right)$$

$$I_{B1} = \frac{I_S}{\beta_{FO}}\exp\left(\frac{V_{BE}}{V_T}\right) \qquad I_{B1} = \frac{I_S}{\beta_{FO}}\exp\left(\frac{V_{BE}}{V_T}\right)$$

BJTs Q_1 and Q_2 are assumed to have identical I_S, V_A, β_{FO}, and W/L ratios.

$$\therefore I_O = I_{REF}\frac{\left(1+(V_{CE2}/V_A)\right)}{\left(1+\frac{V_{CE2}}{V_A}+\frac{2}{\beta_{FO}}\right)}$$

$I_o = I_{C2}$, $\quad I_{REF} = I_{C1} + I_{B1} + I_{B2}$

Finite current gain of BJT causes slight mismatch between I_o and I_{REF}.

$$V_{BE1} = V_{BE2} = V_{BE}$$

$$\text{MR} = \frac{I_O}{I_{REF}} = \frac{1}{1+(2/\beta_{FO})}$$

Current Mirror (Example)

Problem: Calculate and compare mirror ratios for BJT and MOS current mirror.

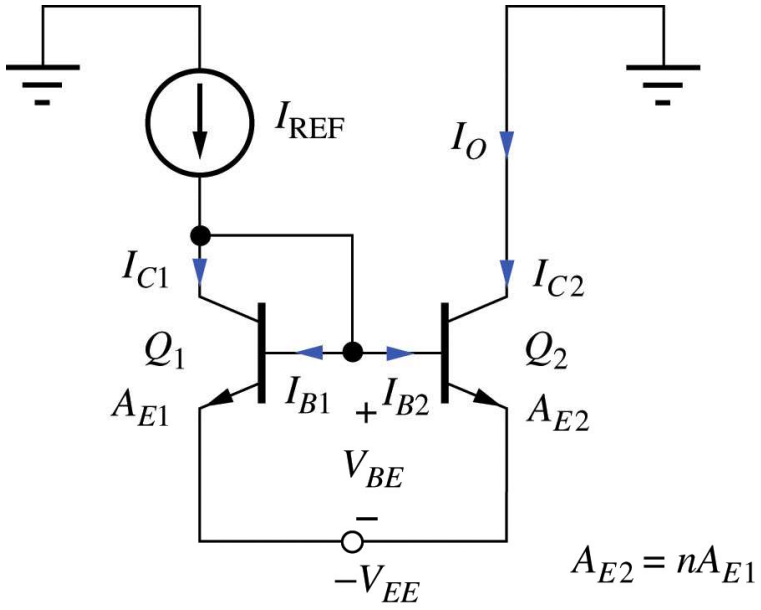
Given data: I_{REF} = 150 μA, V_{GS} = 2 V, $V_{DS2} = V_{CE2}$ = 10 V, λ = 0.02 V^{-1} V_A = 50 V, β_{FO} = 100, V_{SS} = 10 V, $M_1 = M_2$, $Q_1 = Q_2$.

Analysis:

$$\text{MR}_{\text{MOS}} = \frac{\left(1+\lambda V_{DS2}\right)}{\left(1+\lambda V_{DS1}\right)} = 1.15$$

$$\text{MR}_{\text{BJT}} = \frac{\left(1+(V_{CE2}/V_A)\right)}{\left(1+\dfrac{V_{CE2}}{V_A}+\dfrac{2}{\beta_{FO}}\right)} = 1.16$$

Bipolar Current Mirrors: Changing Mirror Ratio



Mirror ratio can be changed by modifying the emitter area of the transistor.

$$I_S = I_{SO}\frac{A_E}{A}$$

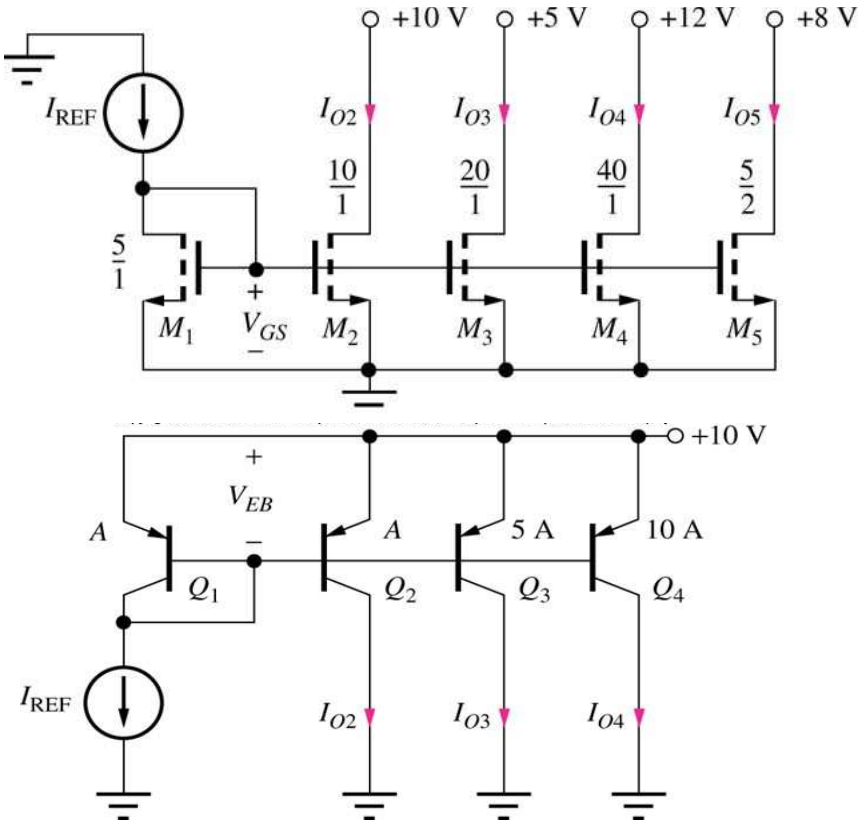
Emitter area scaling changes the transport equations using which,

$$I_O = nI_{REF}\frac{\left(1+(V_{CE2}/V_A)\right)}{\left(1+\frac{V_{CE2}}{V_A}+\frac{1+n}{\beta_{FO}}\right)} \qquad n=\frac{A_{E2}}{A_{E1}}$$

Ideally, MR = n, but for finite gain,

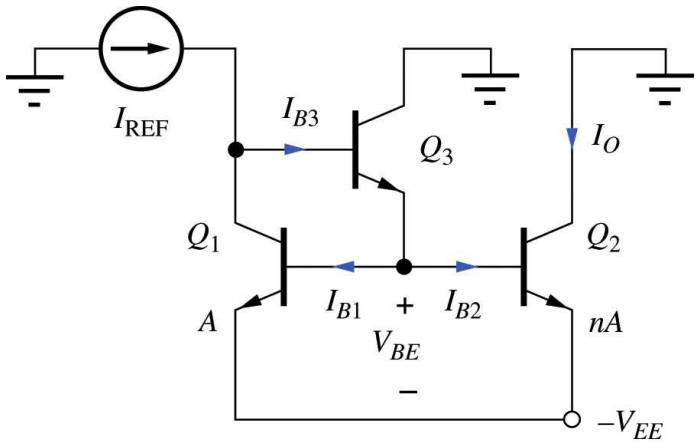
$$\text{MR} = \frac{n}{1+\frac{n}{\beta_{FO}}}$$

Multiple Current Sources



- Reference current enters diode-connected transistor M_1 establishing gate-source voltage to bias M_2 through M_5, each with different *W/L* ratio.
- Absence of current gain defect permits large number of MOSFETs to be driven by one reference transistor.
- Similar multiple bipolar sources can be built from one reference BJT.
- As base current error term worsens when more BJTs are added, umber of outputs of basic bipolar mirror are limited.

Buffered Bipolar Current Mirror



Assuming infinite Early voltage for simplicity,

$$I_{C1} = I_{REF} - I_{B3} = I_{REF} - \frac{(1+n)\dfrac{I_{C1}}{\beta_{FO1}}}{\left(1+\beta_{FO3}\right)}$$

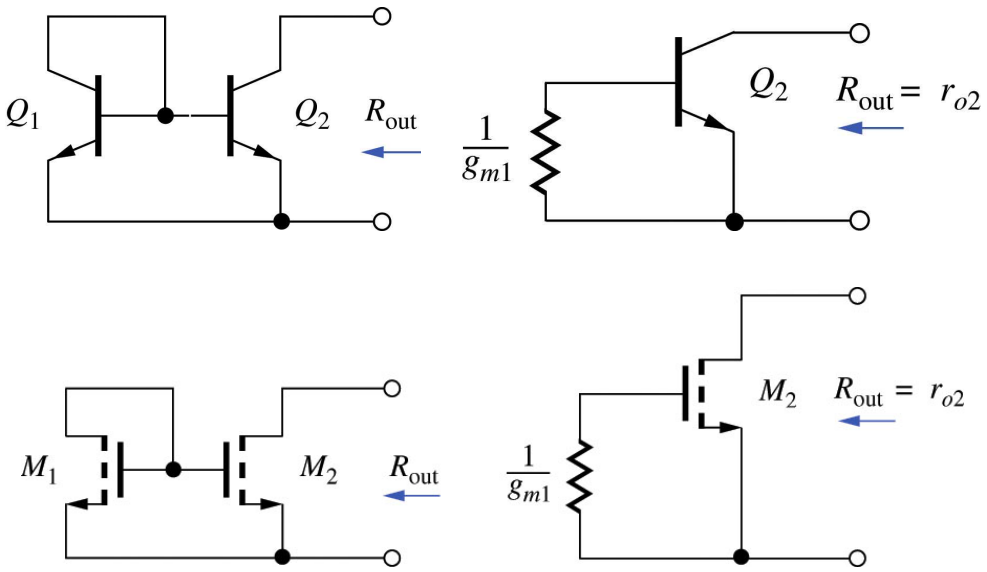
$$I_O = nI_{C1} = nI_{REF}\frac{1}{1+\dfrac{(1+n)}{\beta_{FO1}(1+\beta_{FO3})}}$$

When large mirror ratio is used or if many source currents are generated from one reference BJT, current gain defect worsens.

Current gain of Q_3 is used to reduce base current that is subtracted from reference current.

Thus error term in denominator is reduced.

Output Resistance of Current Mirrors



This simplifies the ac model of the current mirror. Similar analysis applies to MOSFET current mirror except that the current gain is infinite. Thus

$$R_{out} = r_{o2}$$

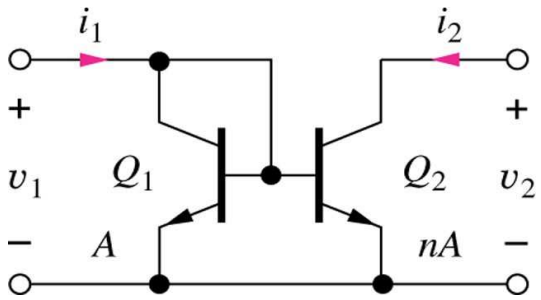
$$V_{CS} \cong V_{A2} \quad \text{or} \quad V_{CS} = \frac{1}{\lambda_2}$$

For diode connected BJT, from small-signal model,

$$\mathrm{i} = (g_m + g_o + g_\pi)\mathrm{v}$$

$$\therefore R = \frac{\mathrm{v}}{\mathrm{i}} \cong \frac{1}{g_m} \qquad \text{...If } \beta_o \text{ and } \mu_F >> 1$$

Two-port Model for Current Mirror



Since current mirror has a current input and current output, we use *h*-parameters.

$$v_1 = h_{11} i_1 + h_{12} v_2$$
$$i_2 = h_{21} i_1 + h_{22} v_2$$

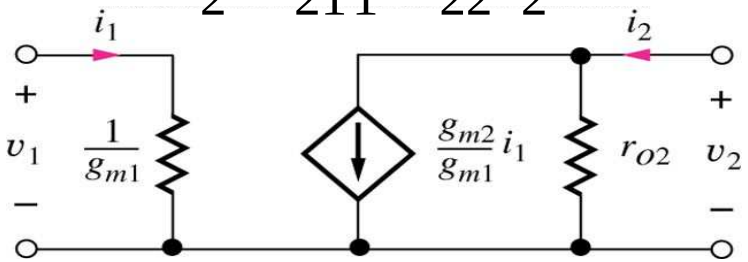
$$h_{11} = \left.\frac{v_1}{i_1}\right|_{v_2=0} = \frac{1}{g_{m1} + g_{\pi 2}} \cong \frac{1}{g_{m1}} \qquad h_{12} = \left.\frac{v_1}{v_2}\right|_{i_1=0} = 0$$

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2=0} = \frac{g_{m2} r_{\pi 2}}{1 + g_{m1} r_{\pi 2}} \cong \frac{g_{m2}}{g_{m1}} = n \qquad h_{22} = \left.\frac{i_2}{v_2}\right|_{i_1=0} = \frac{1}{r_{o2}}$$

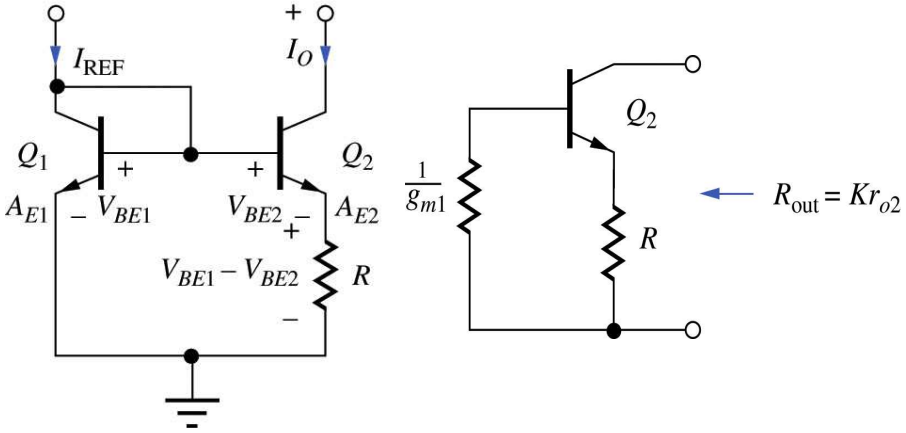
For MOS current mirrors,

$$h_{11} = \frac{1}{g_{m1}} \qquad h_{12} = 0$$

$$h_{21} \cong \frac{g_{m2}}{g_{m1}} \cong n \qquad h_{22} = \frac{1}{r_{o2}}$$



Bipolar Widlar Current Source



R in Widlar source allows adjustment of mirror ratio.

$$V_{BE1} = V_T \ln\left(1 + \frac{I_{REF}}{I_{S1}}\right) \cong V_T \ln\left(\frac{I_{REF}}{I_{S1}}\right)$$

$$V_{BE2} = V_T \ln\left(1 + \frac{I_O}{I_{S2}}\right) \cong V_T \ln\left(\frac{I_O}{I_{S2}}\right)$$

Current through *R* is given by:

$$I_{E2} = \frac{V_{BE1} - V_{BE2}}{R} = \frac{V_T}{R} \ln\left(\frac{I_{REF}}{I_O}\frac{I_{S2}}{I_{S1}}\right)$$

If transistors are matched,

$$I_O = \alpha_F I_{E2} = \frac{V_T}{R} \ln\left(\frac{I_{REF}}{I_O}\frac{A_{E2}}{A_{E1}}\right)$$

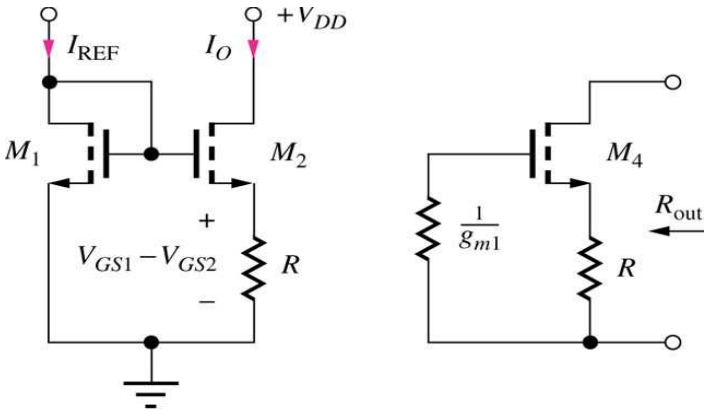
$$R_{out} \cong r_{o2}\left(1 + g_{m2}R\right)$$

$$= r_{o2}\left(1 + \ln\left(\frac{I_{REF}}{I_O}\frac{I_{S2}}{I_{S1}}\right)\right) = Kr_{o2}$$

$$V_{CS} \cong KV_{A2}$$

Typically $1 < K < 10$.

MOS Widlar Current Source



Current through R is given by:

$$I_O = \frac{V_{GS1} - V_{GS2}}{R} = \frac{\sqrt{\frac{2I_{REF}}{K_{n1}}} - \sqrt{\frac{2I_O}{K_{n2}}}}{R}$$

$$= \frac{1}{R}\sqrt{\frac{2I_{REF}}{K_{n1}}}\left(1 - \sqrt{\frac{I_O}{I_{REF}}\frac{(W/L)_1}{(W/L)_2}}\right)$$

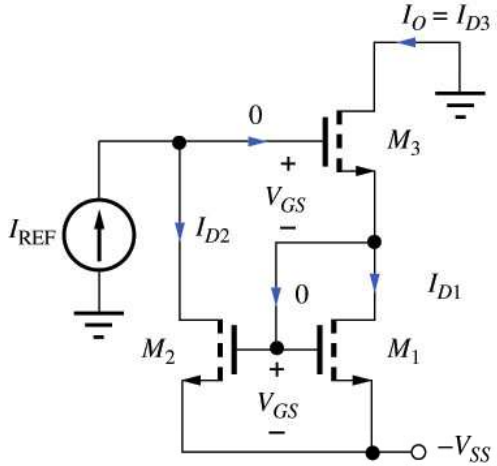
$$\frac{I_O}{I_{REF}} = \frac{1}{R}\sqrt{\frac{2}{I_{REF}K_{n1}}}\left(1 - \sqrt{\frac{I_O}{I_{REF}}\frac{(W/L)_1}{(W/L)_2}}\right)$$

If I_O is known, I_{REF} can be directly calculated. If I_{REF} , R and W/L ratios are known, we can write a quadratic equation in terms of $\sqrt{I_O / I_{REF}}$

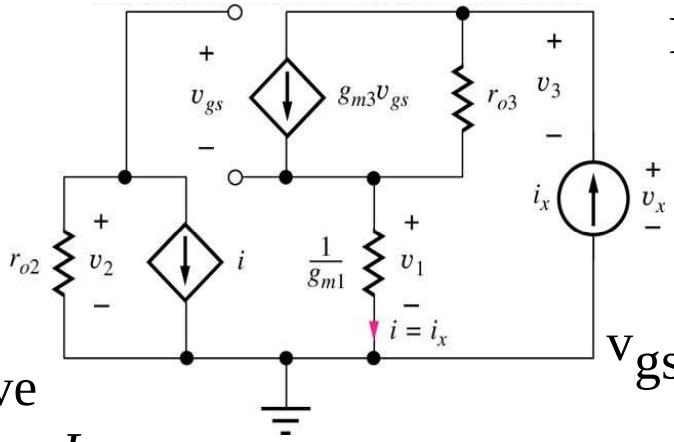
Small-signal model for MOS Widlar source represents a C-S stage with resistor R in its source.

$$\therefore R_{out} = r_{o2}\left(1 + g_{m2}R\right)$$

MOS Wilson Current Source



where $V_{GS} = V_{TN} + \sqrt{\dfrac{2I_{REF}}{K_{n1}}}$



From small-signal model,

$$v_x = v_3 + v_1$$

$$= \left(i_x - g_{m3}v_{gs}\right)r_{o3} + v_1$$

During operation, all transistors are in active region. $I_{D2} = I_{REF}$, $I_{D3} = I_{D1} = I_O$, $V_{GS3} = V_{GS1} = V_{GS}$

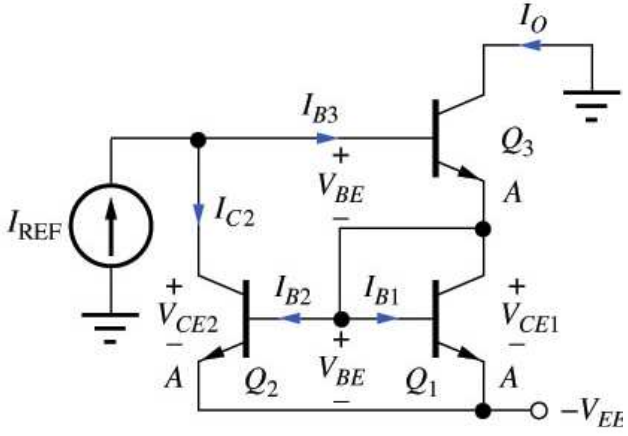
$$v_{gs} = v_2 - v_1 = \frac{i_x}{g_{m1}} - (-\mu_{f2}v_1)$$

$$\therefore R_{out} = \frac{v_x}{i_x} \cong r_{o3}\left(\mu_{f2} + 2 + \frac{1}{\mu_{f2}}\right) \cong \mu_{f2}r_{o3}$$

$$I_{D2} = I_{D1}\frac{\left(1+2\lambda V_{GS}\right)}{\left(1+\lambda V_{GS}\right)} \qquad I_O = I_{REF}\frac{\left(1+2\lambda V_{GS}\right)}{\left(1+\lambda V_{GS}\right)}$$

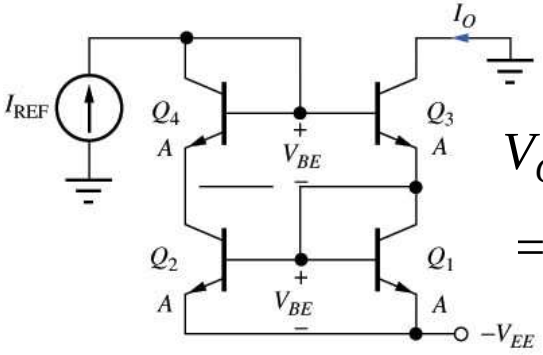
$$V_{CS} \cong \frac{\mu_{f2}}{\lambda_3}$$

Bipolar Wilson Current Source



$$I_O = I_{REF}\left(\frac{\left(1+(V_{BE}/V_A)\right)}{1+\frac{2}{\beta_{FO}(\beta_{FO}+2)}+\frac{2V_{BE}}{V_A}}\right)$$

Addition of extra BJT can balance the circuit and reduce errors.



During operation, all transistors are in active region. But some current is lost at base of Q_3 and current gain error is formed by Q_1 and Q_2.

$$I_{REF} = I_{C2} + I_{B3}$$

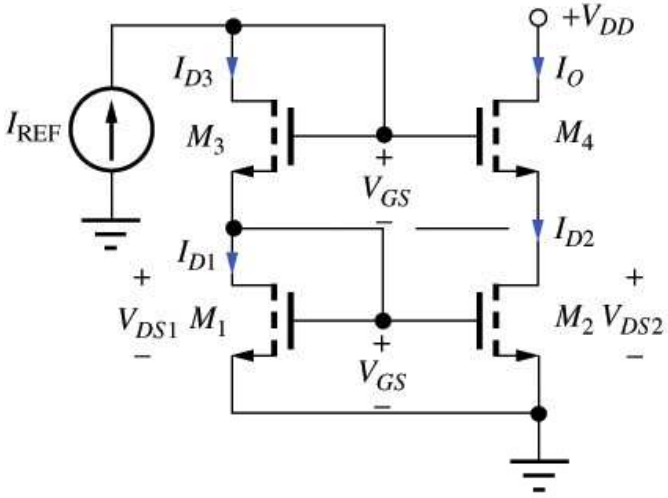
$$V_{CE1} = V_{BE} \qquad V_{CE2} = 2V_{BE}$$

$$V_{CE2} = V_{BE} + V_{BE3} - V_{BE4}$$

$$= V_{BE}$$

$$R_{out} \cong \frac{\beta_{o3} r_{o3}}{2} \qquad V_{CS} \cong \frac{\beta_o V_A}{2}$$

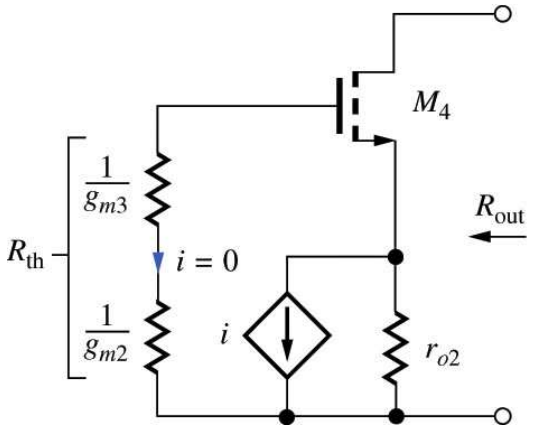
MOS Cascode Current Source

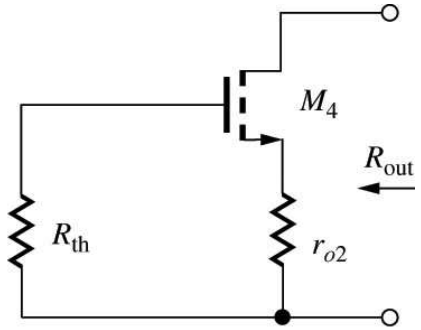


$I_{D1} = I_{D3} = I_{REF}$ Also $I_O = I_{D4} = I_{D2}$. So current mirror forces output current to be approximately equal to the reference current. If all transistors are matched with equal *W/L* ratios,

$$V_{DS2} = V_{GS1} + V_{GS3} - V_{GS4} = V_{GS} = V_{DS1}$$

From the small-signal model,

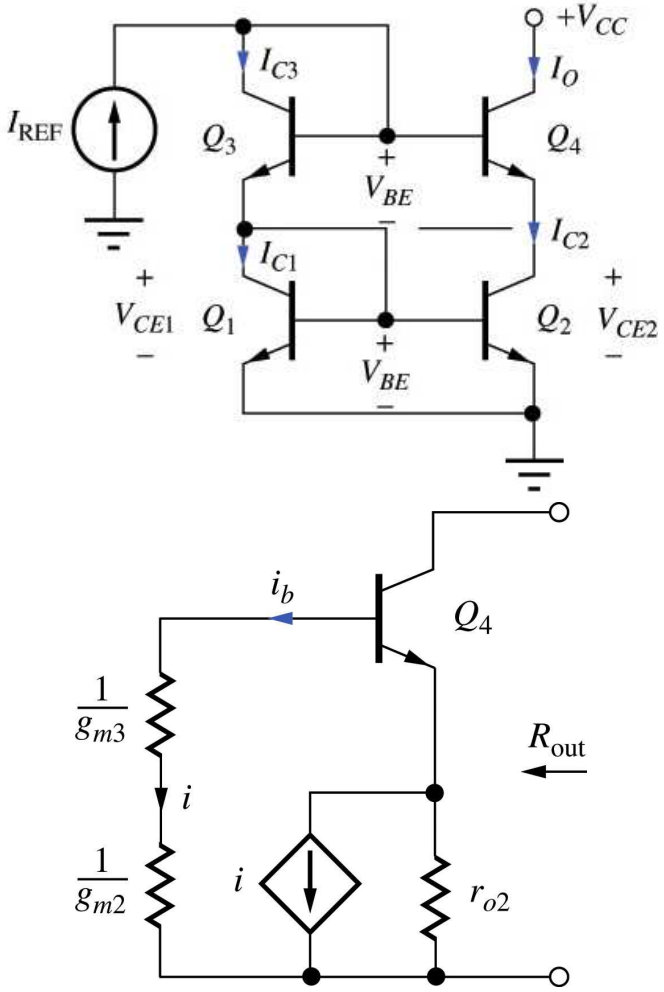




$$R_{out} = r_{o4}\left(1 + g_{m4}r_{o2}\right) \cong \mu_{f4} r_{o2}$$

$$V_{CS} \cong \frac{\mu_{f4}}{\lambda_2} \cong \frac{\mu_{f4}}{\lambda_4}$$

Bipolar Cascode Current Source



$I_{C1} = I_{C3} = I_{REF}$ Also $I_O = I_{C4} = I_{C2}$. So current mirror forces output current to be approximately equal to the reference current. If all transistors are matched,

$$V_{CE2} = V_{BE1} + V_{BE3} - V_{BE4} = V_{GS} = V_{CE1}$$

From the small-signal model,

$$R_{out} \cong \frac{\beta_{o4} r_{o4}}{2} \qquad V_{CS} \cong \frac{\beta_{o4} V_{A4}}{2}$$

Electronic Current Source Design Example

Problem: Design IC current source to meet given specifications.

Given data: I_{REF} = 25 μA, V_{SS} = 20 V, λ = 0.02 V^{-1} , V_{TN} = 0.75 V, K_n' = 50 μA/V^2, V_A = 50 V, β_{FO} = 100, I_{SO} = 0.5 fA

Analysis: MR <0.1 % requires output current of 25 μA±25 nA when output voltage is 20 V. Choose 1GΩ for safety margin.

$$R_{out} \geq \frac{20\,\text{V}}{25\,\text{nA}} = 800\,\text{M}\Omega \qquad \therefore V_{CS} = 25\,\mu\text{A}(1\text{G}\ \Omega) = 25{,}000\text{V}$$

Cascode or Wilson source's voltage-balanced MOS version must be used to meet this value of V_{CS} and for small MR. We can choose cascode source as it doesn't involve internal feedback loop.W/L ratios are all same as MR=1.

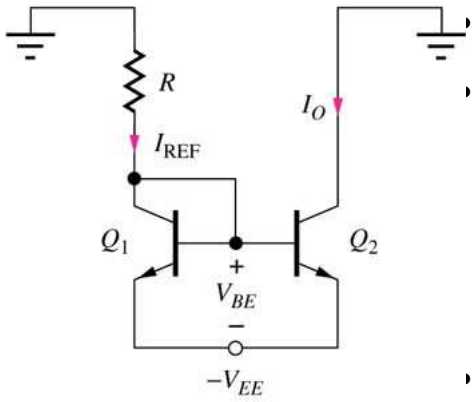
$$\mu_f = \lambda V_{CS} = \frac{0.02}{\text{V}}(25{,}000\text{V}) = 500 = g_m r_o \cong \sqrt{2K_n I_D}\,\frac{1}{\lambda I_D}$$

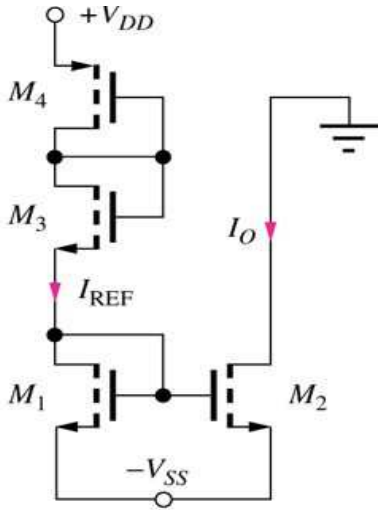
Using μ_f =500, λ =0.02/V and I_D =25 μA gives value of K_n=1.25 mS. Since K_n = K_n'*(W/L)* we need a *W/L* ratio of 25/1 for given technology.

Comparisons of the Basic Current Mirrors

TYPE OF SOURCE	R_{out}	V_{CS}	TYPICAL VALUES OF V_{CS}
Resistor	R	V_{EE}	15 V
Two-transistor mirror	r_o	V_A or $\frac{1}{\lambda}$	75 V
Cascode BJT	$\frac{\beta_o r_o}{2}$	$\frac{\beta_o V_A}{2}$	3750 V
Cascode FET	$\mu_f r_o$	$\frac{\mu_f}{\lambda}$	10,000 V
BJT Wilson	$\frac{\beta_o r_o}{2}$	$\frac{\beta_o V_A}{2}$	3750 V
FET Wilson	$\mu_f r_o$	$\frac{\mu_f}{\lambda}$	10,000 V

Reference Current Generation





- Reference current is required by all current mirrors.
- When resistor is used, source's output current is directly proportional to V_{EE}.

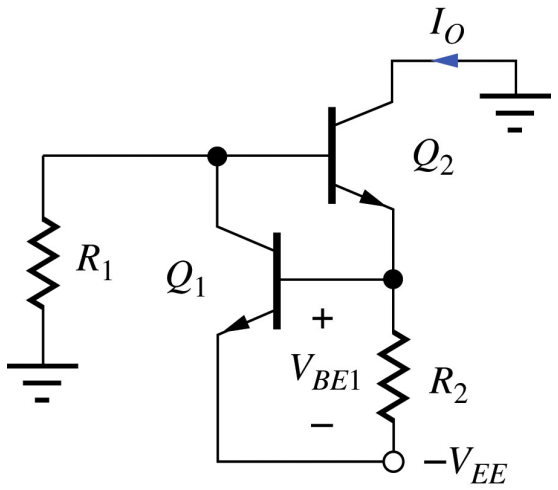
$$I_{REF} = \frac{V_{EE} - V_{BE}}{R}$$

- Gate-source voltages of MOSFETs can be large and several MOS devices can be connected in series between supplies to eliminate large resistors.

  $V_{DD} + V_{SS} = V_{SG4} + V_{GS3} + V_{GS1}$ and $I_{D3} = I_{D1} = I_4$

- Change in supply directly alters gate-source voltage of MOSFETs and the reference current.
- BJTs can't similarly be connected in series due to small fixed voltage developed across each diode and exponential relationship between voltage and current.

Supply-Independent Biasing: V_{BE} -based Reference and Widlar Current Source



$$I_O = \alpha_{F2} I_{E2} = \alpha_{F2}\left(\frac{V_{BE1}}{R_2} + I_{B1}\right) \cong \frac{V_{BE1}}{R_2} \cong \frac{0.7\text{V}}{R_2}$$

$$\therefore I_O \cong \frac{V_T}{R_2} \ln \frac{V_{EE} - 1.4\text{V}}{I_{S1} R_1}$$

- Output current is determined by base-emitter voltage of Q_1 . For high current gain,

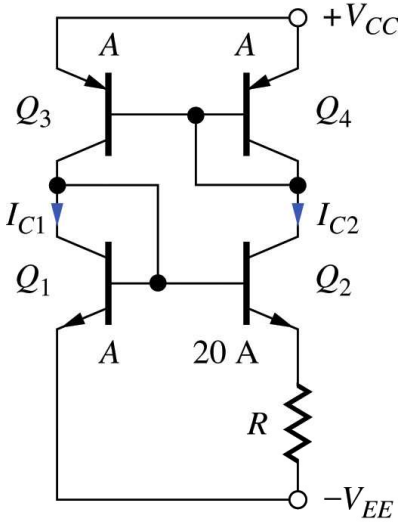
$$I_{C1} = \frac{V_{EE} - V_{BE1} - V_{BE2}}{R_1} \cong \frac{V_{EE} - 1.4\text{V}}{R_1}$$

Output current is now logarithmically dependent on supply voltage. However, it is temperature dependent due to temperature coefficients of both V_{BE} and R.

Widlar source also achieves similar supply independence of output current.

$$I_O = \alpha_F I_{E2} = \frac{V_T}{R} \ln\left(\frac{I_{REF}}{I_O}\frac{A_{E2}}{A_{E1}}\right)$$

Supply-Independent Biasing: Bias Cell Using Widlar Source and Current Mirror



Actual value of output current depends on temperature and absolute value of R. $I_{C1} = I_{C2} = 0$ is also a stable operating point and start-up circuits must be included in IC realizations to ensure that circuit reaches desires operating point.

Base-emitter voltages of Q_1 and Q_4 can be used as reference voltages for other current mirrors.

Assuming high current gain, *pnp* current mirror forces $I_{C1} = I_{C2}$. Emitter area ratio for Widlar source is shown to be 20.

$$\therefore I_{C2} = \frac{V_T}{R}\ln(20) = \frac{0.0749\ \text{V}}{R}$$

In MOS analog of the circuit, $I_{D3} = I_{D4}$ and so $I_{D1} = I_{D2}$.

$$R = \sqrt{\frac{2}{I_{D2}K_{n1}}}\left(1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}}\right)$$

Reference Current Design Example

Problem: Design supply-independent current source to meet given specifications.

Given data: output current = 45 μA, T=300 K, total current< 60 μA V_{CC} = V_{EE}= 5 V, V_A = 75 V, β_{FO} = 100, I_{SO} = 0.1 fA, V_T = 25.88 mV

Analysis:

$$\ln\left(\frac{I_{C1}}{I_{C2}}\frac{A_{E2}}{A_{E1}}\right)=\frac{I_{C2}R}{V_T}\le\frac{(45\mu\text{A})(1\text{k}\Omega)}{25.88\text{mV}}=1.739$$

$$\frac{I_{C1}}{I_{C2}}\frac{A_{E2}}{A_{E1}}\le 5.69$$

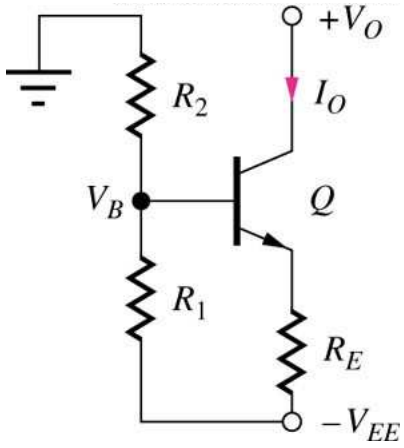
Also $\frac{I_{C2}}{I_{C1}}\ge\frac{45\mu\text{A}}{15\mu\text{A}}=3$. Choose I_{C2}=5 I_{C1}. Then A_{E2}/ A_{E1} <28.45 Choosing

A_{E2}/A_{E1} =20, $$R=\frac{25.88\text{mV}\ln(4)(45\mu\text{A})(1\text{k}\Omega)}{45\mu\text{A}}=797\Omega$$

Finally, A_{E1}=A, A_{E2}=20 A, A_{E3}=A, A_{E4}=5 A with 35.88 mV across R.

Bipolar Transistor Current Source Design Example

- **Problem:** Design a current source with the largest possible output voltage range that meets the given output resistance specification.
- **Given data**: V_{EE} = 15 V, I_o = 200 μA, I_{EE} < 250 μA, R_{out} > 2 MΩ, BJTs available with (β_o, V_A) = (80, 100 V) and (150, 75 V), V_B must be as low as possible.
- **Assumptions:** Active region and small-signal operating conditions. V_{BE} = 0.7 V, V_T = 0.025 V, choose V_o = 0 V as representative output value.



Analysis:

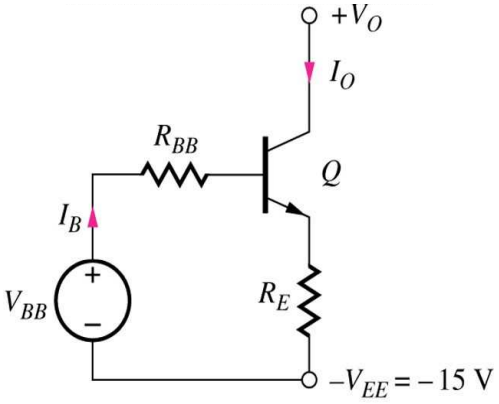
$$R_{out} = r_o\left(1+\frac{\beta_o R_E}{R_1 \| R_2 + r_\pi + R_E}\right) \le \beta_o r_o$$

$$V_{CS} = I_o R_{out} \le \beta_o V_A$$

$$\beta_o V_A = I_o R_{out} \ge (200\mu\text{A})(10\text{M}\Omega) = 2000\text{V}$$

Bipolar Transistor Current Source Design Example (contd.)

Both BJTs can satisfy these conditions. But, we choose BJT (150, 75V) with higher $\beta_o V_A$ product.



Total current < 250 μA. As output current is 200 μA, maximum of 50 μA can be used by base bias network. Current used by base bias network must be 5 to 10 times base current of BJT (1.33 μA for BJT with a current gain of 150). So bias network current =20 μA.

Large R_{BB} reduces output resistance and output compliance range (increase V_{BB}).Trading increased operating current for wider compliance range, choose bias network current of 40 μA.

$$\therefore R_1 + R_2 \cong \frac{15\text{V}}{40\mu\text{A}} = 375\text{k}\Omega$$

Bipolar Transistor Current Source Design Example (contd.)

- Following set of equations can be used in a spreadsheet analysis to determine design variables. Primary design variable is V_{BB} which can be used to determine other variables.

$$I_B = \frac{I_o}{\beta_F}$$

$$R_1 = (R_1 + R_2)\frac{V_{BB}}{15} = 375\text{k}\Omega\left(\frac{V_{BB}}{15}\right)$$

$$R_2 = (R_1 + R_2) - R_1 = 375\text{k}\Omega - R_1$$

$$R_{BB} = R_1 \| R_2$$

$$R_E = \alpha_F\left(\frac{V_{BB} - V_{BE} - I_B R_{BB}}{I_o}\right)$$

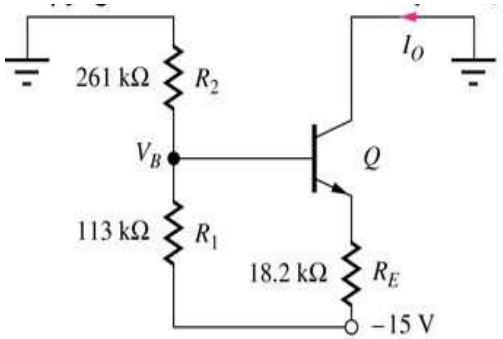
$$V_{CE} = V_{EE} - (V_{BB} - V_{BE} - I_B R_{BB})$$

$$r_o = \frac{V_A + V_{CE}}{I_o} \qquad r_\pi = \frac{\beta_o V_T}{I_o}$$

$$R_{out} = r_o\left(1 + \frac{\beta_o R_E}{R_1 \| R_2 + r_\pi + R_E}\right)$$

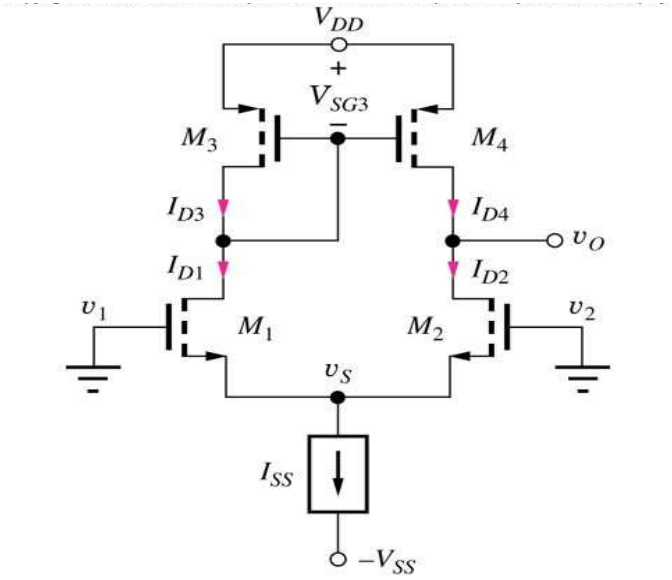
Bipolar Transistor Current Source Design Example (contd.)

- From spreadsheet, smallest V_{BB} for which output resistance > 10MΩ with some safety margin is 4.5 V, resulting output resistance is 10.7MΩ.
- Analysis of circuit with 1% resistor values gives I_o = 200 μA and supply current = 244 μA.
- Final current source design is as shown.



- MOSFET current source design can also be analyzed in similar manner.

CMOS Differential Amplifier with Active Load: DC Analysis



$$V_O = V_{DD} - V_{SD\,4} = V_{DD} - \left(\sqrt{\frac{I_{SS}}{K_p}} - V_{TP} \right)$$

$$V_{DS\,1} = V_{DD} + V_{TN} + V_{TP} + \sqrt{\frac{I_{SS}}{K_n}} - \sqrt{\frac{I_{SS}}{K_p}} \cong V_{DD}$$

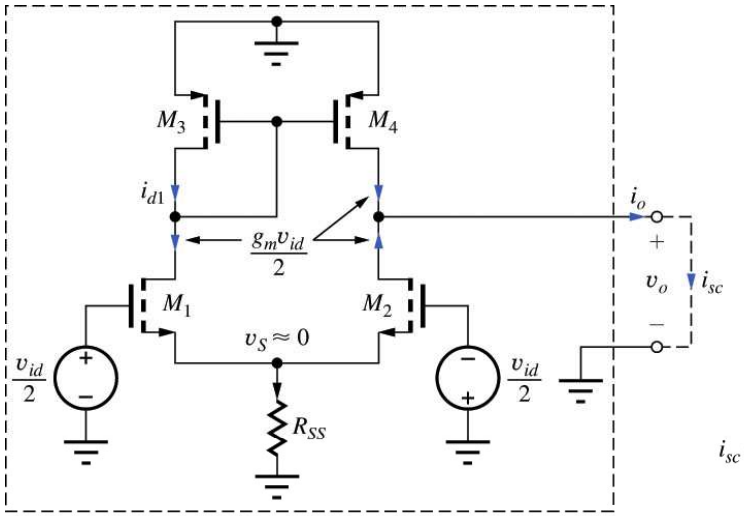
$$V_{SD\,3} = V_{SG\,3} = \sqrt{\frac{I_{SS}}{K_p}} - V_{TP}$$

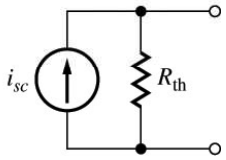
$I_{D3} = I_{D1} = I_{D2} = I_{D4} = I_{SS}/2$.

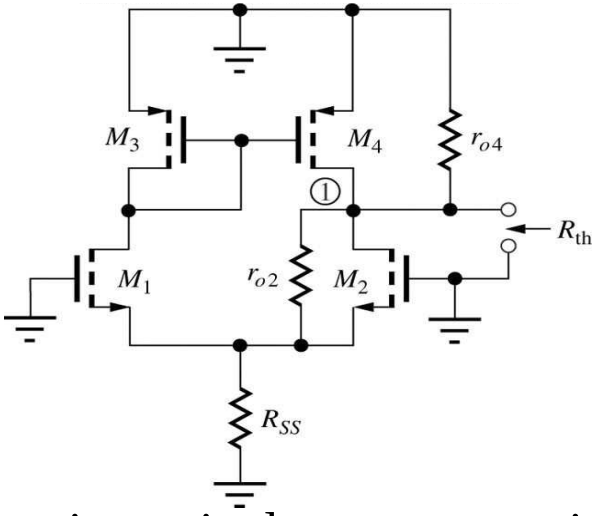
Mirror ratio is set by M_3 and M_4 and is exactly unity when $V_{SD4} = V_{SD3}$ and thus $V_{SD1} = V_{SD2}$.

Differential amplifier is completely balanced at dc when:

CMOS Differential Amplifier with Active Load: Differential-Mode Signal Analysis







The differential amplifier can be represented by its Norton equivalent.
Total short circuit output current:

$$i_o = 2\frac{g_{m2} v_{id}}{2} = g_{m2} v_{id}$$

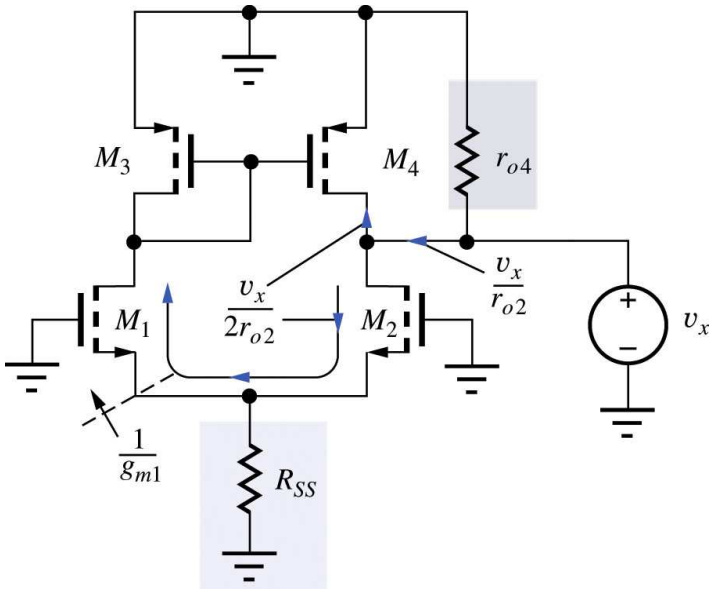
Thevenin equivalent output resistance:

$$R_{th} = r_{o2} \| r_{o4}$$

Differential-mode voltage gain:

$$A_{dm} = i_{sc} R_{th} = g_{m2}\left(r_{o2} \| r_{o4}\right) \cong \frac{\mu_{f2}}{2}$$

CMOS Differential Amplifier with Active Load: Output Resistance



Assume $R_{SS} >> 1/g_{m1}$.

Resistance looking into drain of M_2 (C-G transistor) is:

$$R_{o2} = r_{o2}\left(1 + g_{m2}R_S\right) = r_{o2}\left(1 + g_{m2}\frac{1}{g_{m1}}\right) = 2r_{o2}$$

Drain current of M_2 ($v_x/2r_{o2}$)is replicated by current mirror as drain current of M_4. Total current from source is $2(v_x/2r_{o2}) = v_x/r_{o2}$.

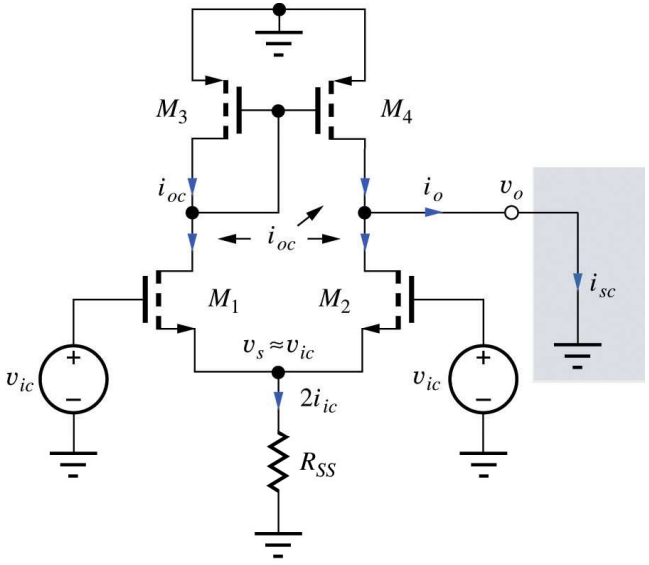
Total current is:

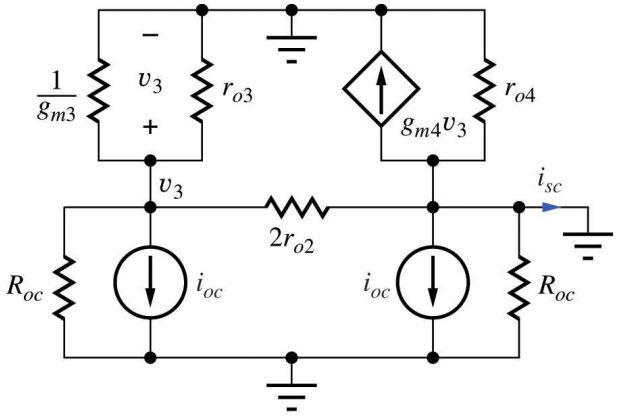
$$i_x^T = \frac{v_x}{r_{o2}} + \frac{v_x}{r_{o4}}$$

Output resistance is:

$$R_{od} = r_{o2} \| r_{o4}$$

CMOS Differential Amplifier with Active Load: Common-Mode Signal Analysis





From small-signal equivalent:

$$i_{oc} \cong \frac{v_{ic}}{2R_{ss}} \qquad R_{od} = 2r_{o2}$$

$$R_{oc} = 2\mu_f R_{SS}$$

$$v_3 = \frac{-i_{oc}}{g_{m3} + g_{o3} + \left(g_{o2}/2\right) + G_{oc}}$$

$$i_{sc} = -\left(i_{oc} + g_{m4}v_3 - \frac{g_{o2}}{2}v_3\right) \cong -\frac{\left(1 + \dfrac{r_{o3}}{r_{o2}}\right)}{\mu_{f3}}\left(\frac{v_{ic}}{2R_{SS}}\right)$$

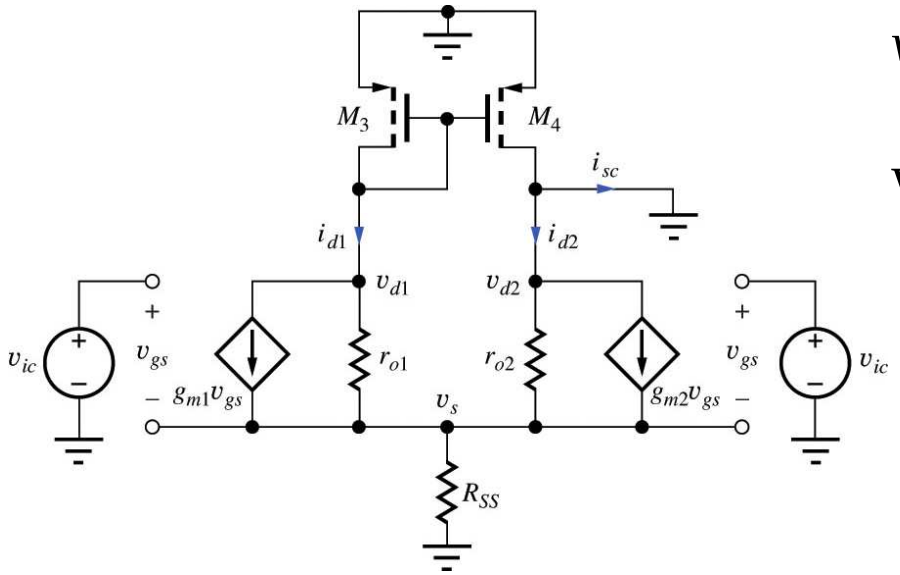
where it is assumed that $g_{m4} = g_{m3}$ and $G_{oc} << g_{m3}$.

Also

$$A_{cm} = \frac{i_{sc}R_{th}}{v_{ic}} = -\frac{\left(1 + \dfrac{r_{o3}}{r_{o2}}\right)}{2\mu_{f3}R_{SS}}\left(r_{o2} \| r_{o4}\right)$$

CMOS Differential Amplifier with Active Load: CMRR and Mismatch Contribution

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| = \frac{2\mu_{f3} g_{m2} R_{SS}}{1+\left(r_{o3}/r_{o2}\right)} \cong \mu_{f3} g_{m2} R_{SS} \qquad \text{for } r_{o3} = r_{o2}.$$



With mismatched transistors, assuming v_{d1}=0 and gate-source voltages are equal,

$$i_{sc} = i_{d1} - i_{d2} = \Delta g_m v_{gs} - \Delta g_o v_s$$

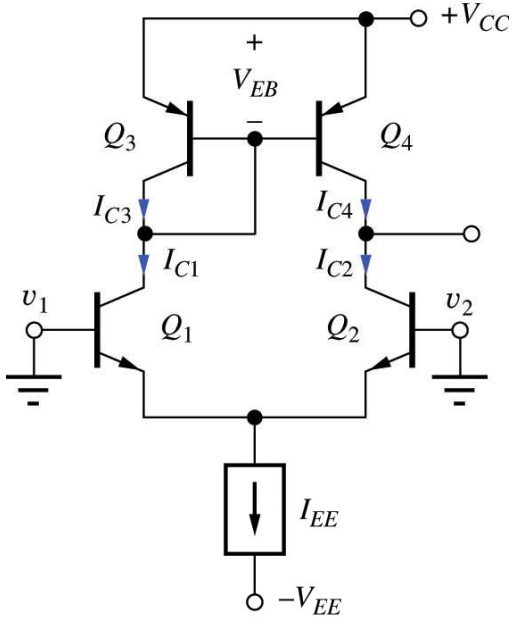
With $v_{gs} = v_{ic} - v_s$, v_{d1}=0 and v_{d2}=0,

$$v_s \cong \frac{2g_m R_{SS}}{1+2g_m R_{SS}} v_{ic} \cong v_{ic}$$

$$v_{gs} \cong \frac{1+2g_o R_{SS}}{1+2g_m R_{SS}} v_{ic} \cong \left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right) v_{ic}$$

$$\text{CMRR}^{-1} = \left|\frac{A_{cm}}{A_{dm}}\right| = \left|\frac{A_{cm}}{g_m\left(r_{o2} \| r_{o4}\right)}\right| = \left|\frac{\Delta g_m}{g_m}\left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right) - \frac{\Delta g_o}{g_o}\frac{1}{\mu_f}\right|$$

Bipolar Differential Amplifier with Active Load: DC Analysis



Differential amplifier is completely balanced at dc when:

$$V_O = V_{CC} - V_{EB}$$

$$V_{CE1} = V_{CE2} = V_C - V_E = (V_{CC} - V_{EB}) - (-V_{BE}) \cong V_{CC}$$

Current gain defect in current mirror upsets dc balance. As longs as BJTs are in forward-active region, V_{EC4} adjusts to make up for current-gain defect.

$$I_{C4} = I_{C1} \frac{\left(1+(V_{CE4}/V_A)\right)}{\left(1+\frac{V_{CE}}{V_A}+\frac{2}{\beta_{FO4}}\right)}$$

As $I_{C2} = I_{C4}$ and $I_{C2} = I_{C1}$, MR must be $I_{C3} = I_{C1} = I_{C2} = I_{C4} = I_{EE}/2$.

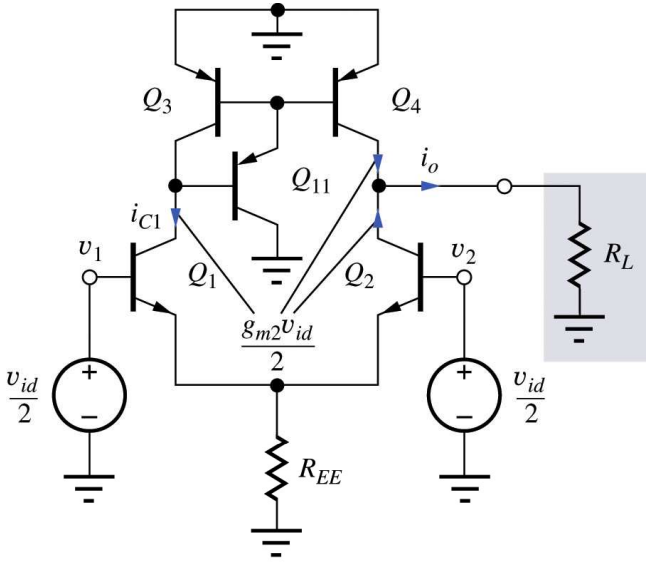
If β_{FO} is very large, current mirror ratio is set by Q_3 and Q_4 and is exactly 1 when $V_{EC4} = V_{EC3} = V_{EB}$.

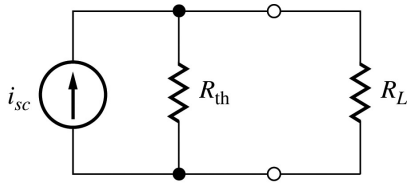
$$V_{EC4} = V_{EB} + \frac{2V_A}{\beta_{FO4}}$$

This causes an equivalent input offset voltage of

$$V_{OS} = \frac{V_{EC4} - V_{EC3}}{A_{dd}} = \frac{V_{EC4} - V_{EB}}{A_{dd}}$$

Bipolar Differential Amplifier with Active Load: Differential-Mode Signal Analysis





Thevenin equivalent output resistance:

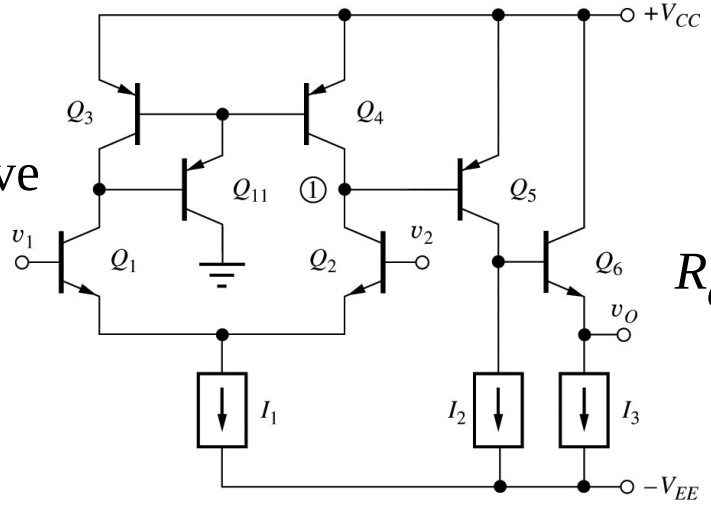
$$R_{th} = r_{o2} \| r_{o4}$$

Differential-mode voltage gain:

$$A_{dm} = \frac{i_{sc}\left(R_L \| R_{th}\right)}{v_{dm}} = g_{m2}\left(r_{o2} \| r_{o4} \| R_L\right) = g_{m2} R_L$$

To eliminate offset error, buffered current mirror active load is used. Total short circuit output current:

$$i_{sc} = 2\frac{g_{m2} v_{id}}{2} = g_{m2} v_{id}$$

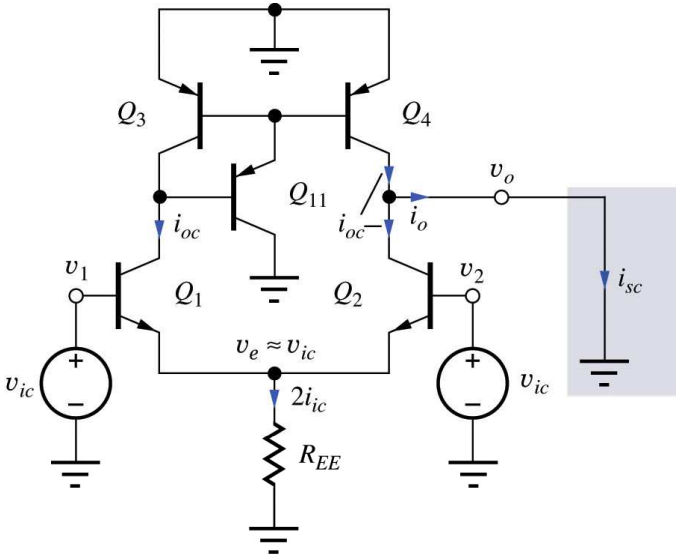


With added stages, the resistance at the output of the differential input stage is:

$$R_{eq} = r_{o2} \| r_{o4} \| r_{\pi 5} \cong r_{\pi 5}$$

$$A_{dm} = g_{m2} R_{eq} = \beta_{o5} I_{C2} / I_{C5}$$

Bipolar Differential Amplifier with Active Load: Common-Mode Signal Analysis



From small-signal equivalent:

$$i_{oc} = \frac{A_{cc} v_{ic}}{R_C} = v_{ic}\left(\frac{1}{2R_{EE}} - \frac{1}{\beta_o r_o}\right)$$

$$i_{sc} = v_{ic}\frac{2}{\beta_o}\left(\frac{1}{\beta_o r_o} - \frac{1}{2R_{EE}}\right)$$

Current forced in differential output resistance is doubled due to current mirror action.

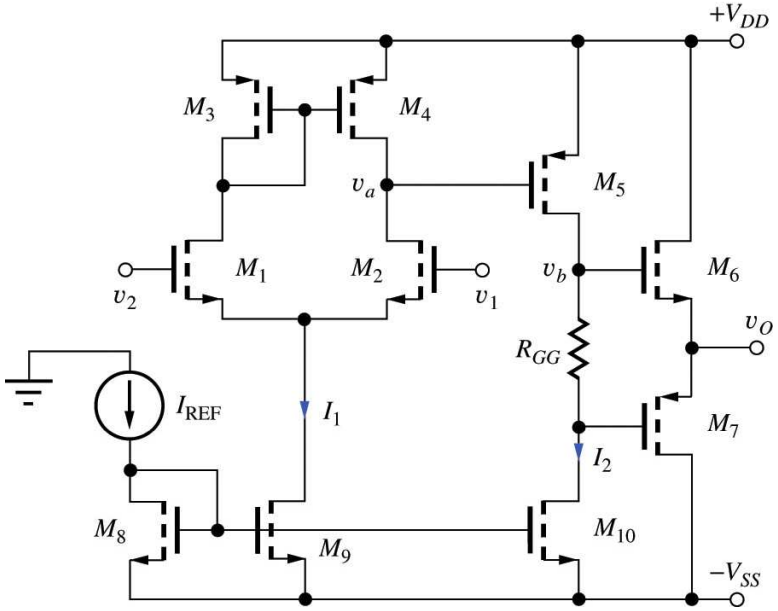
$$i_{sc} = 2v_{ic}\left(\frac{1}{\beta_o r_o} - \frac{1}{2R_{EE}}\right)\frac{1}{g_{m3}(2r_{o2})} \cong \frac{v_{ic}}{\mu_{f2}}\left(\frac{1}{\beta_o r_o} - \frac{1}{2R_{EE}}\right)$$

$$\text{CMRR} = \left|\frac{g_{m2} R_{th}}{i_{sc} R_{th} / v_{ic}}\right| \cong \left(\frac{2}{\beta_{o3}}\left(\frac{1}{\beta_o \mu_{f2}} - \frac{1}{2g_{m2} R_{EE}}\right)\right)^{-1}$$

Due to mismatches,

$$\text{CMRR}^{-1} = \left[\left(\frac{\Delta g_m}{g_m} + \frac{\Delta g_\pi}{g_\pi}\right)\left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right) - \frac{\Delta g_o}{g_o}\frac{1}{\mu_f}\right]$$

Active Loads in Op Amps: Voltage Gain



$$A_{dm} = \frac{v_a}{v_{id}}\frac{v_b}{v_a}\frac{v_o}{v_b} = A_{vt1}A_{vt2}(1) \cong A_{vt1}A_{vt2} = \frac{\mu_{f2}\mu_{f5}}{4}$$

If Wilson stage is used in first-stage active load, $A_{vt1} = \mu_{f2}$. If current source M_{10} is replaced by a Wilson or cascode source, $A_{vt2} = \mu_{f5}$.Overall gain can be raised to:

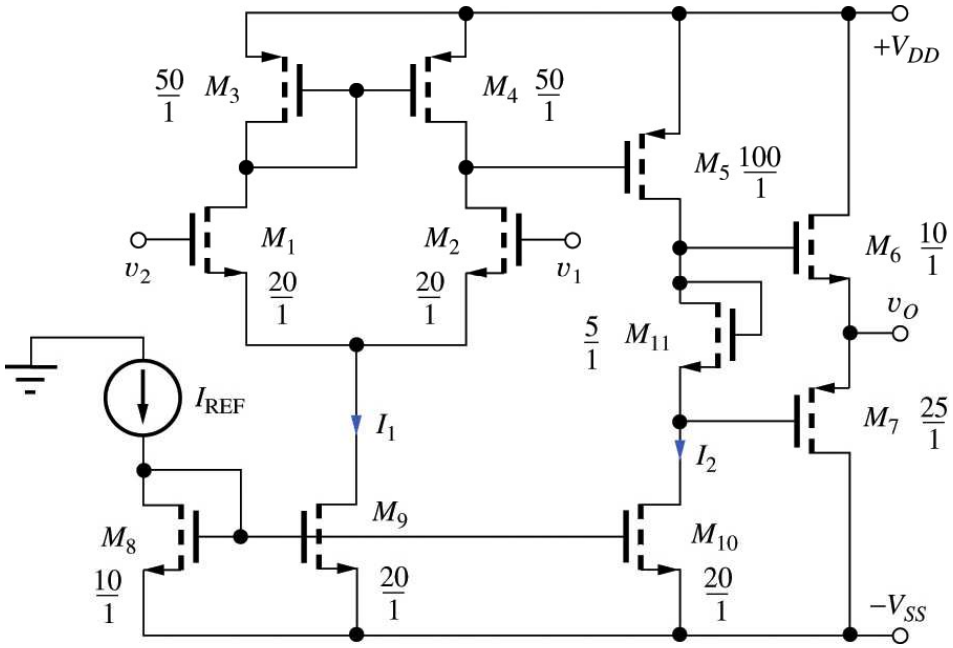
$$A_{dm} = \mu_{f2}\mu_{f5}$$

$$A_{vt1} = g_{m2}(r_{o2} \| r_{o4}) \cong \frac{\mu_{f2}}{2}$$

$$A_{vt2} = g_{m5}(r_{o5} \| (R_{GG} + r_{o10})) \cong g_{m2}(r_{o2} \| r_{o5}) = \frac{\mu_{f5}}{2}$$

Gain of output stage is approximately 1.

Active Loads in Op Amps: DC Design Considerations



- When op amp with active load is operated in closed-loop configuration, $I_{D5} = I_2$, the output current of source M_{10}.
- For minimum offset voltage, $(W/L)_5$ must be such that $V_{SG5} = V_{SD4} = V_{SG3}$ precisely sets $I_{D5} = I_2$ and accounts for V_{DS} and λ differences between M_5 and M_{10}.
- R_{GG}, $(W/L)_6$ and $(W/L)_7$ determine quiescent current in class-AB output stage.
- V_{GS11} can be used to bias output stage in place of R_{GG}.

CMOS Op Amp Analysis

Problem: Find small-signal characteristics of given CMOS op amp.

Given data: I_{REF} = 100 μA, $V_{DD} = V_{SS}$ = 5 V, V_{TN} = 1 V, V_{TP} = -0.75 V, K_n' = 25 μA/V^2, K_p' = 10 μA/V^2, λ = 0.0125 V^{-1}

Analysis:

$$I_{D2} = I_1/2 = I_{REF} = 100\,\mu\text{A}$$

$$I_{D5} = I_2 = 2I_{REF} = 200\,\mu\text{A}$$

$$A_{dm} = \frac{\mu_{f2}\mu_{f5}}{4}$$

$$= \frac{1}{4}\left(\frac{1}{\lambda_2}\sqrt{\frac{2K_{n2}}{I_{D2}}}\right)\left(\frac{1}{\lambda_5}\sqrt{\frac{2K_{p5}}{I_{D5}}}\right) = 16{,}000$$

$$R_{id} = R_{ic} = \infty$$

$$V_{GS11} = V_{TN11} + \sqrt{\frac{2I_{D11}}{K_{n11}}} = 2.54\,\text{V}$$

As $I_{D6} = I_{D7}$, $V_{GS6} = V_{SG7} = V_{GS11}/2$

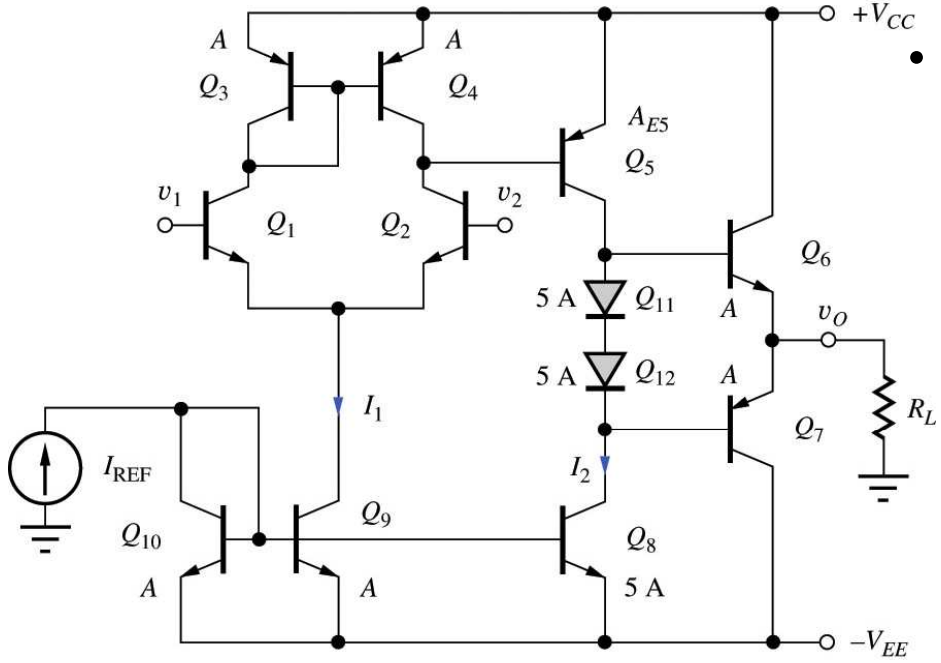
$$I_{D7} = I_{D6} = \frac{250}{2}\frac{\mu\text{A}}{\text{V}^2}(1.27\,\text{V} - 0.75\,\text{V})^2$$

$$= 33.7\,\mu\text{A}$$

$$g_{m7} = g_{m6} = 1.3\times10^{-4}\,\text{S}$$

$$R_{out} = \frac{1}{g_{m6}} \left\| \frac{1}{g_{m7}} \right. = 3.85\,\text{k}\Omega$$

Bipolar Op Amps



- Q_1 to Q_4 form differential input stage with active load.
- First stage is followed by high-gain C-E amplifier, Q_5 and its current source load, Q_8.

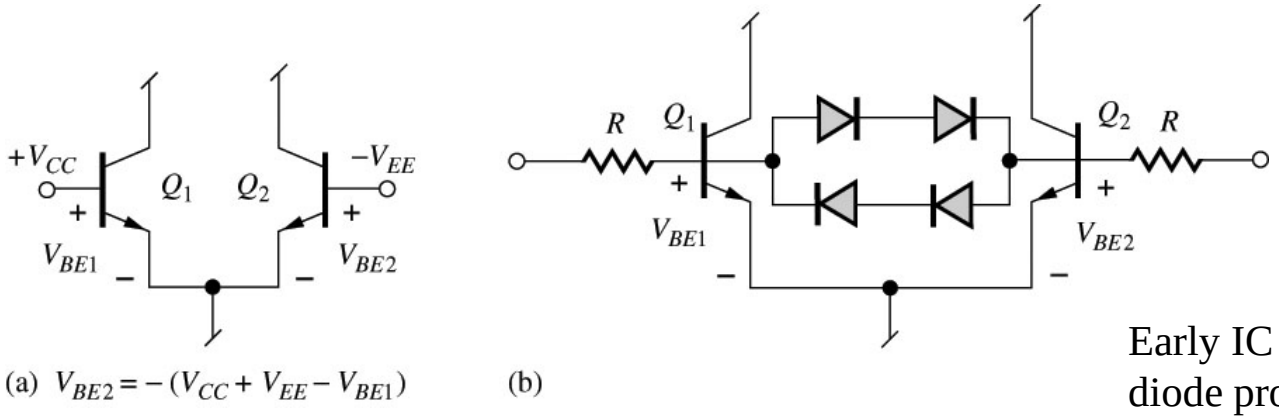
- Load resistance is driven by class-AB output stage formed by Q_6 and Q_7 , biased by I_2 and diodes Q_{11} and Q_{12}.

$$A_{dm} = A_{vt1}A_{vt2}A_{vt3}$$

$$\cong \left(g_{m2}r_{\pi 5}\right)\left(g_{m2}\left(r_{o5}\|r_{o8}\|(\beta_{o6}+1)R_L\right)\right) \quad (1)$$

$$\cong \frac{g_{m2}}{g_{m5}} g_{m5}r_{\pi 5}g_{m5}\frac{r_{o5}}{2} = \frac{I_{C2}}{I_{C5}}\beta_{o5}\frac{\mu_{f5}}{2}$$

Input Stage Breakdown in Bipolar Op Amps

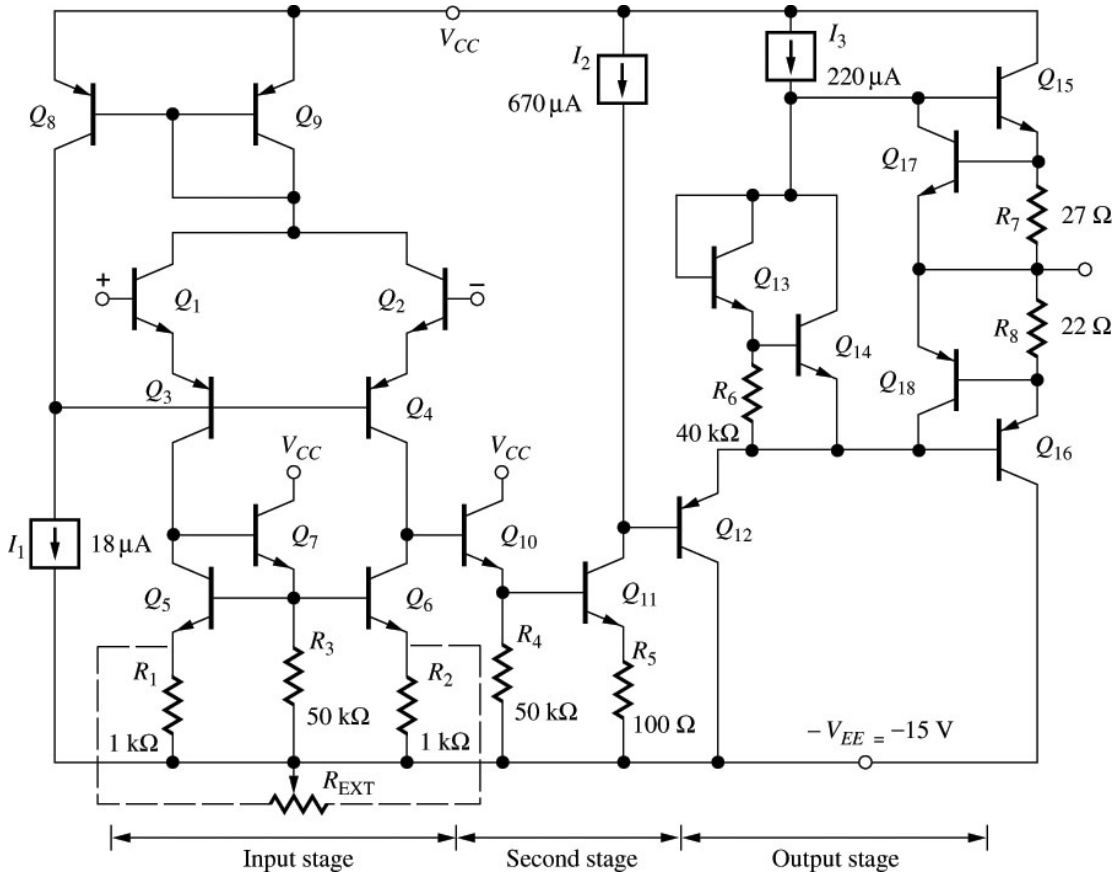


(a) $V_{BE2} = -(V_{CC} + V_{EE} - V_{BE1})$ (b)

- Input stage of bipolar op amp has no overvoltage protection and can easily be destroyed by large input voltage differences due to fault conditions or unavoidable transients, such as slew-rate limited recovery.
- In worst-case fault condition, B-E junction of Q_1 is forward-biased and that of Q_2 is reverse-biased by(V_{CC} + V_{EE} - V_{BE1}). If V_{CC} = V_{EE} =22 V, reverse voltage > 41 V.

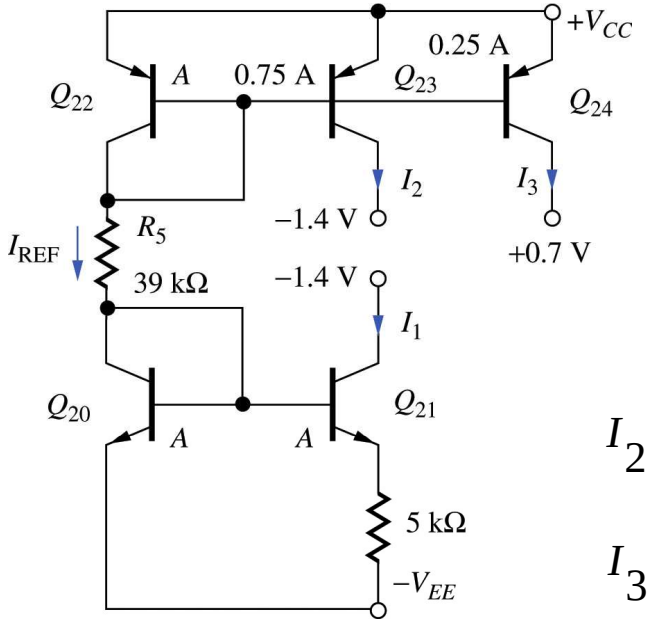
Early IC op amps used external diode protection across input terminals to limit differential input voltage to about 1.4 V at the cost of extra components.

μA741 Op Amp



- High gain, input resistance and CMRR, low output resistance and good frequency response.
- Fully protected input and output stages and offset adjustment port.
- Input stage is a differential amplifier with buffered current mirror active load.
- Two stages of voltage gain (emitter-follower driving C-E amplifier) followed by short-circuit protected class-AB output stage buffered from second gain stage by emitter follower.

μA741 Op Amp: Bias Circuitry



Assuming V_O =0, V_{CC} =15 V and neglecting drop across R_7 and R_8 ,

V_{EC23} = 15+1.4=16.4 V and V_{EC24} = 15-0.7 =14.3 V

Given V_A=60 V, β_{FO} =50,

$$I_2 = 0.75(0.733\,\text{mA})\,\frac{1+(16.4/60)}{1+(0.7/60)+(2/50)} = 666\,\mu\text{A}$$

$$I_3 = 0.25(0.733\,\text{mA})\,\frac{1+(14.4/60)}{1+(0.7/60)+(2/50)} = 216\,\mu\text{A}$$

$$I_{REF} = \frac{V_{CC} + V_{EE} - 2V_{BE}}{R_5} = 0.733\,\text{mA}$$

Solving iteratively,

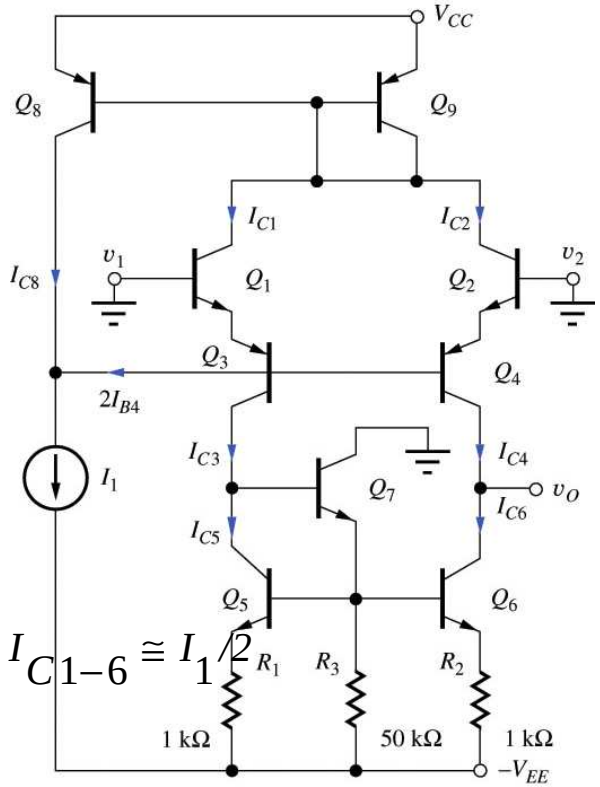
$$I_1 = \frac{V_T}{5000}\ln\left(\frac{I_{REF}}{I_1}\right)$$

I_1 =18.4 μA.

$$R_2 = \frac{V_{A23} + V_{EC\,23}}{I_2} = \frac{60\,\text{V} + 16.4\text{V}}{0.666\,\text{mA}} = 115\,\text{k}\Omega$$

$$R_3 = \frac{V_{A24} + V_{EC\,24}}{I_3} = \frac{60\,\text{V} + 14.3\text{V}}{0.216\,\text{mA}} = 344\,\text{k}\Omega$$

μA741 Op Amp:DC Analysis of Input Stage



$$I_{C1-6} \cong I_1/2$$

$$I_1 = 2I_{C2}\frac{1+(V_{EC8}/V_{A8})}{1+(2/\beta_{FO8})+(V_{EB8}/V_{A8})}+2I_{B4}$$

$$I_{C2} = \alpha_{F2}I_{E2} = \frac{\beta_{FO2}}{\beta_{FO2}+1}\left(\beta_{FO4}+1\right)I_{B4}$$

$$\therefore I_{C2} \cong \frac{I_1}{2}\times\left[\frac{1}{1+\dfrac{V_{EC8}-V_{EB8}}{V_{A8}}-\dfrac{2}{\beta_{FO8}}+\dfrac{1}{\beta_{FO4}}}\right]$$

$$I_{C4} = \alpha_{F4}I_{E4} = \frac{\beta_{FO2}+1}{\beta_{FO2}}\frac{\beta_{FO4}}{\beta_{FO4}+1}I_{C2}$$

$$V_{CE1} = V_{CE2} = V_{CC} - V_{EB9} + V_{BE2} \cong V_{CC}$$

$$V_{EC3} = V_{E3} - V_{C3} = -0.7\text{V} - (-V_{EE} + 1.4\text{V})$$
$$= V_{EE} - 2.1\text{V}$$

$$V_{EC8} = V_{CC} + 1.4\text{V}$$

$$V_{CE7} = V_{EE} - 0.7\text{V}$$

μA741 Op Amp: Input Stage Bias Currents Example

Problem: Calculate bias currents in the 741 input stage with given parameters.

Given data: $I_1 = 18\ \mu\text{A}, V_{CC} = V_{EE} = 15\ \text{V}, V_{Anpn} = 75\ \text{V}, \beta_{FOnpn} = 150, V_{Apnp} = 60\ \text{V}, \beta_{FOpnp} = 60$

Analysis:

$$V_{EC8} = V_{CC} + V_{BE1} + V_{EB3} \cong 16.4\text{V}$$

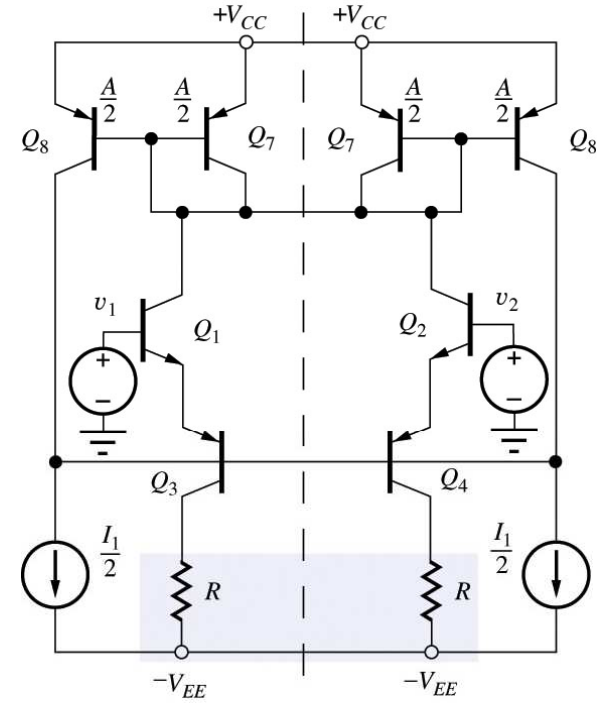
$$I_{C1} = I_{C2} = \frac{18\mu\text{A}}{2} \frac{1}{\dfrac{1+(16.4/60)}{1+(2/50)+(0.7/60)} + \dfrac{1}{(150/151)(60+1)}} = 7.32\mu\text{A}$$

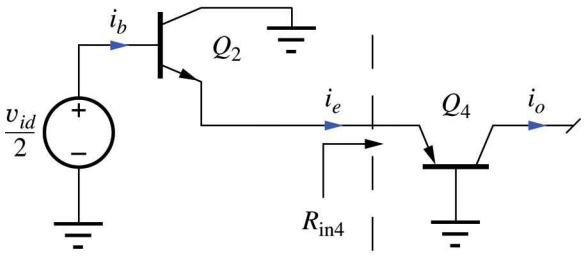
$$I_{C6} = I_{C3} = I_{C4} = \alpha_{F4} I_{E4} = \alpha_{F4} \frac{I_{C2}}{\alpha_{F2}} = \left(\frac{\beta_{FO2}+1}{\beta_{FO2}}\right) \frac{\beta_{FO4}}{\beta_{FO4}+1} I_{C2}$$

$$= \frac{60}{61}\left(\frac{150}{151}\right) I_{C2} = 7.25\mu\text{A}$$

$$I_{C5} \cong I_{C3} = 7.25\mu\text{A}$$

μA741 Op Amp: AC Analysis of Input Stage



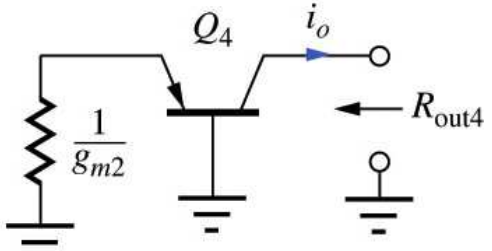


Using symmetry of the input stage differential-mode half circuit can be drawn.

$$i_o = \alpha_{o4} i_e = \alpha_{o4}(\beta_{o2}+1) i_b \cong \beta_{o2} i_b$$

$$i_b = \frac{v_{id}/2}{r_{\pi 2} + (\beta_{o2}+1) R_{in4}} = \frac{v_{id}/2}{r_{\pi 2} + (\beta_{o2}+1)\left(\frac{r_{\pi 4}}{\beta_{o4}+1}\right)} \cong \frac{v_{id}}{4 r_{\pi 2}}$$

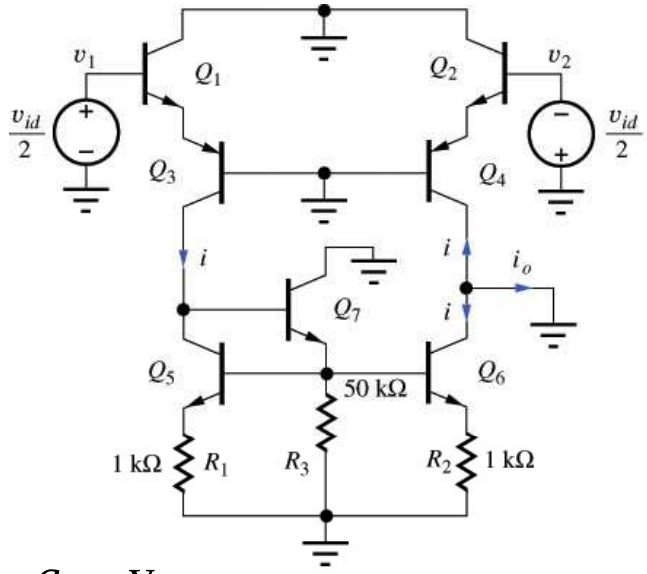
$$\therefore i_o \cong \beta_{o2} \frac{v_{id}}{4 r_{\pi 2}} = \frac{g_{m2}}{4} v_{id}$$

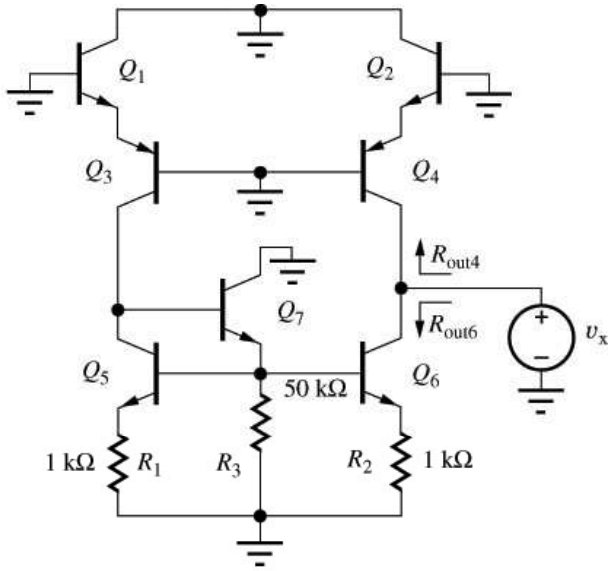


$$R_{id} = \frac{v_{id}}{i_b} = 4 r_{\pi 2}$$

$$R_{out} \cong r_{o4}\left(1 + g_{m4} R\right) = 2 r_{o4}$$

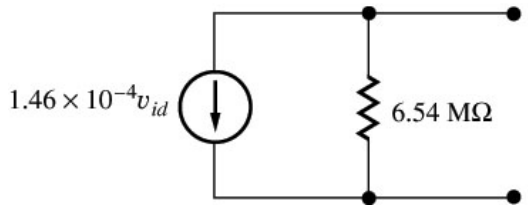
μA741 Op Amp: Voltage Gain (Input Stage Norton Equivalent)





$$i_o = -2i = -\frac{g_{m2} v_{id}}{2} = -20 I_{C2} v_{id}$$

$$= (-1.46 \times 10^{-4}\,\text{S}) v_{id}$$

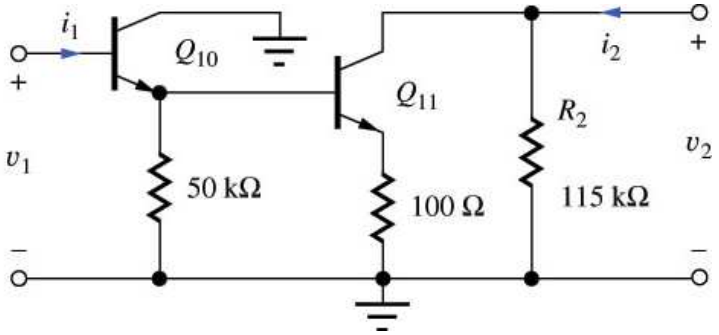


$$R_{th} = R_{out\,6} \| R_{out\,4} \cong r_{o6}\left(1 + g_{m6} R_2\right) \| 2r_{o4}$$

$$= 1.3 r_{o6} \| 2r_{o4} = 0.79 r_{o4} = 6.54\,\text{M}\Omega$$

Based on values in Norton equivalent, open-circuit voltage gain of first stage is -955.

μA741 Op Amp: Voltage Gain (Second Stage)



$$R_{in11} = r_{\pi 11} + (\beta_{o11} + 1)100 = 20.7\,\text{k}\Omega$$

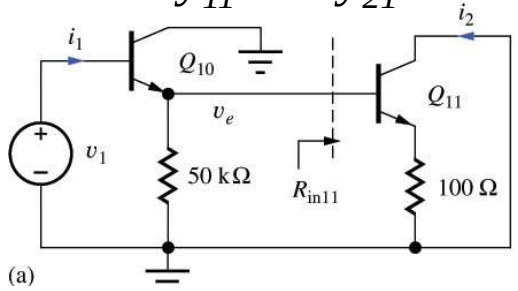
$$[y_{11}]^{-1} = r_{\pi 10} + (\beta_{o10} + 1)(50\,\text{k}\Omega \| R_{in11}) = 2.4\text{M}\,\Omega$$

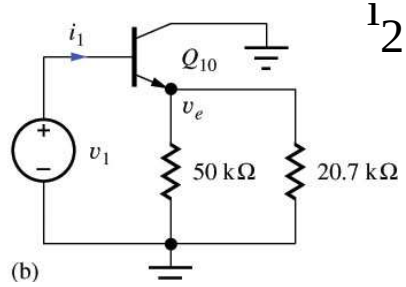
$$I_{C10} \cong I_{E10} = \frac{I_{C11}}{\beta_{F11}} + \frac{V_{B11}}{50\,\text{k}\Omega} = 19.8\mu\text{A}$$

$$v_e = v_1 \frac{(\beta_{o10} + 1)(50\text{k}\Omega \| R_{in11})}{r_{\pi 10} + (\beta_{o10} + 1)(50\text{k}\Omega \| R_{in11})} = 0.921 v_1$$

$$r_{\pi 10} = \frac{\beta_{o10}}{I_{C10}} = 189\,\text{k}\Omega \quad r_{\pi 11} = 5.63\text{k}\Omega$$

To find y_{11} and y_{21}:



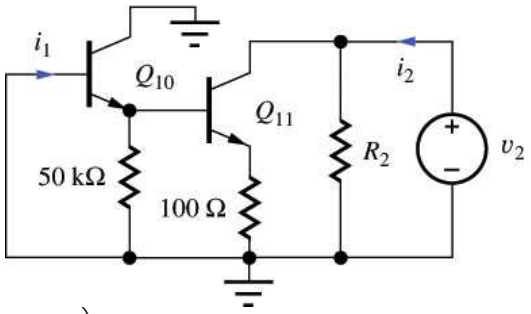


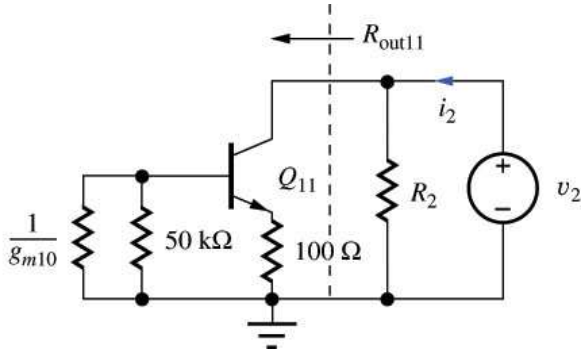
$$i_2 = \frac{v_e}{(1/g_{m11}) + 100\Omega} = 0.006701 v_1$$

$$\therefore y_{21} = 6.70\,\text{mS}$$

μA741 Op Amp: Voltage Gain (Second Stage cont.)

To find y_{12} and y_{22}:





$$R_{out11} = r_{o11}\left(1 + g_{m11}R_E\right)100 = 407\,\text{k}\Omega$$

$$\left[y_{22}\right]^{-1} = \left(R_2 \| R_{out11}\right) = 89.1\text{k}\Omega$$

Open-circuit voltage gain for the first two stages is:

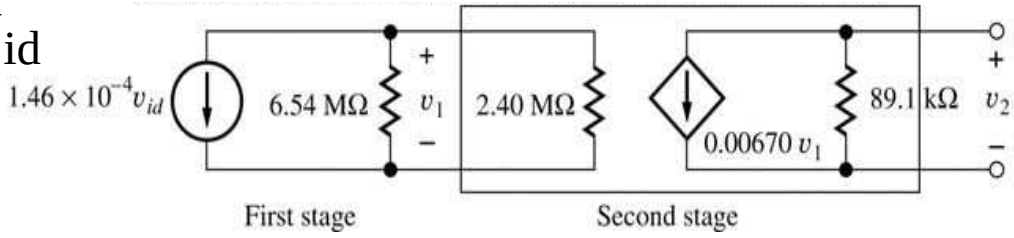
$$v_2 = -0.00670(89.1\text{k}\Omega)v_1 = -597v_1$$

$$v_1 = -1.46\times10^{-4}\left(6.54\text{M}\Omega \| 2.4\text{M}\Omega\right)v_{id}$$

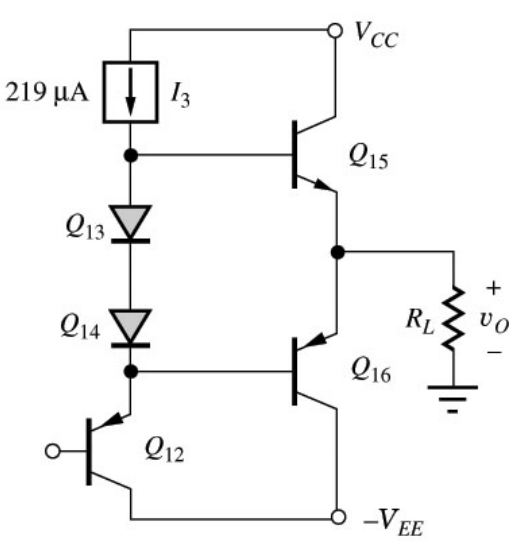
$$= -256v_{id}$$

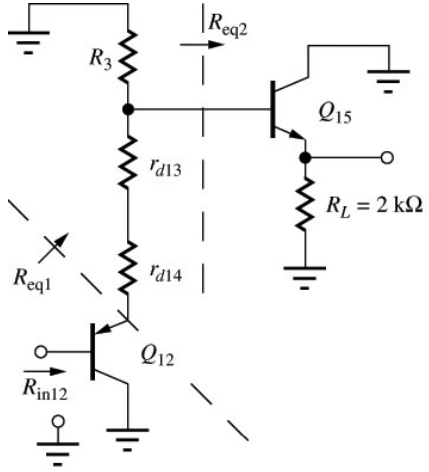
$$v_2 = -597(-256v_{id}) = 153{,}000v_{id}$$

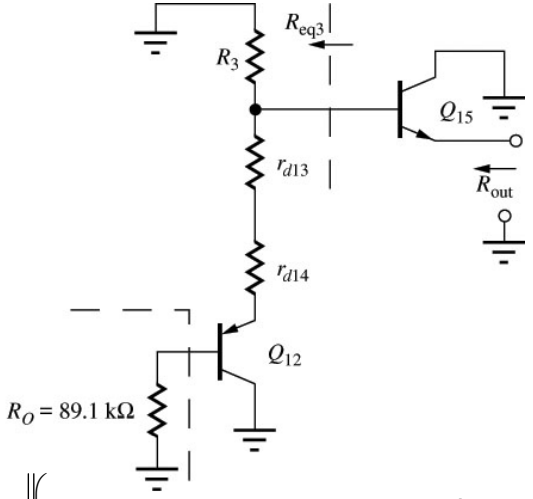
Combined model for first and second stages is:



μA741 Op Amp: Voltage Gain (Output Stage)







From simplified output stage without short-circuit protection:

$$R_{eq2} = r_{\pi 15} + \left(\beta_{o15} + 1\right) R_L = 304\ \text{k}\Omega$$

$$R_{eq1} = r_{d14} + r_{d13} + R_3 \left\| R_{eq2} \right. = 162\ \text{k}\Omega$$

$$R_{in12} = r_{\pi 12} + \left(\beta_{o12} + 1\right) R_{eq1} = 8.27\ \text{M}\,\Omega$$

$$R_{eq3} = R_3 \left\| \left(r_{d14} + r_{d13} + \frac{r_{\pi 12} + y_{22}^{-1}}{\beta_{o12} + 1} \right) \right.$$

$$= 2.08\ \text{k}\Omega$$

$$R_o = \frac{r_{\pi 15} + R_{eq3}}{\beta_{o15} + 1} = 26.2\,\Omega$$

Actual op amp output resistance is:

$$R_{out} = R_o + R_7 = 53\,\Omega$$

μA741 Op Amp Characteristics

	CALCULATION	TYPICAL VALUES
Voltage gain	153,000	200,000
Input resistance	2.05 MΩ	2 MΩ
Output resistance	53 Ω	75 Ω
Input bias current	49 nA	80 nA
Input offset voltage	—	2 mV

End of Chapter 16