Ziqi Wang

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EDUCATION

Carnegie Mellon University
Ph.D. in Computer Science
2017 - Present | PA, USA
Advised by Todd C. Mowry

Carnegie Mellon University
M.Sc. in Computer Science
2015 - 2016 | PA, USA
Major GPA: 3.9 / 4.0

Simon Fraser University
B.Sc. in Computer Science
2012 - 2015 | BC, Canada
Graduated with Distinction

Zhejiang University
B.Eng. in Computer Science
2010 - 2015 | Zhejiang, China
Major GPA: 4.46 / 5.0 (Avg. 89.2 / 100)

INTERESTS

Computer Architecture
Memory & Cache Subsystem Optimization
Database Concurrency Control
Concurrent Data Structures

AWARDS

Open Scholarship, SFU (Spring 2015)
Open Scholarship, SFU (Fall 2014)
Dean's Honor Roll, SFU (Spring 2014)
President's Honor Roll, SFU (Fall 2013)
Open Scholarship, SFU (Spring 2013)
Entrance Scholarship, SFU (Fall 2012)
National Scholarship of ZU (Fall 2012)
Department Scholarship of ZU (Fall 2011)

LINKS

Github
https://github.com/wangziqi2013/
https://github.com/wangziqi2016/

Homepage
https://wangziqi2013.github.io/ziqiw/

COMMUNITY

Contributed to stamp-rtm to add lock elision support.
Contributed to synchrobench to aid bug fixing.

DOCTORAL RESEARCH

Full System Persistence with Multiversioned Page Overlays

2018 – Present | Supervised by Todd Mowry and Michael Kozuch

- Applies multiversioned page overlays to support epoch-based full system persistence and crash recovery.
- Epoches are shadow-mapped to different versions. Processors run in local epoches without global coordination for most of the time.
- Integrates seamlessly with other page overlays applications, e.g. OverlayTM, overlay-on-write, fine-grained metadata, etc.
- Preliminary results show that, under certain circumstances, the overhead of persisting epochs can be reduced to less than 15%.
- By storing the mapping metadata compactly, we also expect less metadata usage compared with other shadow-mapping designs.

Main Memory Multiversioning and Hardware Transactional Memory with Reduced Abort Rates

2017 – 2018 | Supervised by Todd Mowry and Michael Kozuch

- Extended page overlays design by adding a version coherence protocol to support multiversioning on the virtual address space.
- Proposed OverlayTM, a hardware transactional memory running multiversioned backward Optimistic Concurrency Control.
- Extended zSim simulator and evaluated OverlayTM against previous proposals. Results show significant reduction in aborts and less wasted cycles.

MASTERS RESEARCH

Efficient In-Memory Indexing with Lock-Free B+Tree

Jun 2016 – Dec 2016 | Summer Internship | Supervised by Andrew Pavlo

- Worked on Peloton (renamed to terrier in 2018), a self-driving database management system. Responsible for implementing, profiling and tuning of the index subsystem.
- Implemented a highly optimized BwTree, a concurrent lock-free B+Tree index proposed by Microsoft Research. Currently deployed as Peloton's in-memory index.
- Benchmarked BwTree under YCSB workloads. Analyzed BwTree performance characteristics and compared it with Optimistic Lock Coupling and Masstree.
- Open-sourced the optimized BwTree as OpenBwTree and the index benchmarking framework.

Development of Flash Translation Layer Simulator for Grading

Jan 2016 – Apr 2016 | Independent Study | Supervised by Greg Ganger

- Developed a flash simulator for 15-746 Fall 2016 as the course project evaluation platform.

Analyzing a Million Apps from Android Store for Privacy Leakage

Jan 2017 – Jul 2017 | Research Scientist | Supervised by Sebastian Zimmeck

Static Analysis of Android Apps for Privacy Leakage

Sep 2015 – Dec 2015 | Research Assistant | Supervised by Norman Sadeh

- Developed a Python framework for static data-flow analysis of Android apps.
- Scaled the framework to be running on Amazon cloud platform for million-scale app analysis.

PUBLICATION

2019

Wang, Ziqi, Vivek Seshadri, Todd C. Mowry, and Michael Kozuch. "Multiversioned Page Overlays: Enabling Faster Serializable Hardware Transactional Memory." In 2019 28th International Conference on Parallel Architectures and Compilation Techniques (PACT). IEEE, 2019.

Zimmeck, Sebastian, Peter Story, Daniel Smullen, Abhilasha Ravichander, Ziqi Wang, Joel Reidenberg, N. Cameron Russell, and Norman Sadeh. "MAPS: Scaling privacy compliance analysis to a million apps." Proceedings on Privacy Enhancing Technologies 2019, no. 3 (2019): 66-86.

2018

Wang, Ziqi, Andrew Pavlo, Hyeontaek Lim, Viktor Leis, Huanchen Zhang, Michael Kaminsky, and David G. Andersen. "Building a bw-tree takes more than just buzz words." In Proceedings of the 2018 International Conference on Management of Data, pp. 473-488. ACM, 2018.

2017

Pavlo, Andrew, Gustavo Angulo, Joy Arulraj, Haibin Lin, Jiexi Lin, Lin Ma, Prashanth Menon et al. "Self-Driving Database Management Systems." In CIDR, vol. 4, p. 1. 2017. (Authors sorted by last name)

2016

Zimmeck, Sebastian, Ziqi Wang, Lieyong Zou, Roger Iyengar, Bin Liu, Florian Schaub, Shomir Wilson, Norman Sadeh, Steven Bellovin, and Joel Reidenberg. "Automated analysis of privacy requirements for mobile apps." In 2016 AAAI Fall Symposium Series. 2016.

TEACHING

Graduate Computer Architectures | CMU 15-740
Fall 2018 | with Nathan Backmann

Storage Systems | CMU 15-746
Fall 2016 | with Greg Ganger and Garth Gibson

Distributed Systems | CMU 15-440
Spring 2016 | with Mahadev Satyanarayanan

INDUSTRY

Ericsson Canada | Software Engineer Co-op
May 2014 - Dec 2014 | Burnaby, BC, Canada

- Added new feature to Ericsson's proprietary IP Operating System (IPOS) packet classifier
- Developed a Ternary Content Addressable Memory (TCAM) image rebuilder
- Developed a testing framework for PPPoE on routers

RESEARCH TALKS

Concurrency Control Methods for Hardware Transactions
Parallel reading group, Spring 2019

Hardware Transactional Memory
Guest speaker in 15-740 Computer Architecture, 2018 Fall

Building a Bw-Tree Takes More Than Just Buzz Words
SIGMOD 2018 Paper Presentation

Efficient Memory Indexing and Lock-Freedom
Oracle Research, 2017