



Agenda



Agenda: Day 1

08:50 – 09:00	Arrival and settle in period
09:00 – 09:10	Course Overview
09:15 – 09:30	Product Overview
09:30 – 10:10	Verix V Development Kit
10:10 – 10:30	Lab1 Exercise
10:30 – 12:00	Verix V OS
12:00 – 13:30	Lunch Break
13:30 – 16:00	User Interface
16:00 – 17:00	Lab2 Exercise
17:00 – 17:30	Q&A Session

There will be a 15 min break at convenient time during morning and the after noon session.



Agenda: Day 2

08:50 – 09:00	Arrival and settle in period
09:00 – 09:30	User Input
09:30 – 10:30	Lab3 Exercise
10:30 – 11:00	Printout
11:00 – 12:00	Lab4 Exercise
12:00 – 13:30	Lunch Break
13:30 – 16:00	Application Idle Engine
16:30 – 17:00	Lab5 Exercise
17:00 – 17:30	Q&A Session

There will be a 15 min break at convenient time during morning and the after noon session.



Agenda: Day 3

08:50 – 09:00	Arrival and settle in period
09:00 – 10:00	System Device
10:00 – 12:00	Lab6 Exercise
12:00 – 13:30	Lunch Break
13:30 – 16:00	File System
16:30 – 17:00	Lab7 Exercise
17:00 – 17:30	Q&A Session

There will be a 15 min break at convenient time during morning and the after noon session.



Agenda: Day 4

08:50 – 09:00	Arrival and settle in period
09:00 – 10:00	Modem Engine
11:00 – 12:00	Lab8 Exercise
12:00 – 13:30	Lunch Break
13:30 – 16:00	Debugging
16:00 – 17:00	Lab9 Exercise
17:00 – 17:30	Q&A Session

There will be a 15 min break at convenient time during morning and the after noon session.



Agenda: Day 5

08:50 – 09:00	Arrival and settle in period
09:00 – 10:00	UCL
10:00 – 12:00	TCP/IP
12:00 – 13:30	Lunch Break
13:30 – 17:00	Lab10 Exercise
17:00 – 17:30	Q&A Session

There will be a 15 min break at convenient time during morning and the after noon session.