JZ4775

Mobile Application Processor

Data Sheet

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1 Overview

JZ4775 is a mobile application processor targeting for multimedia rich and mobile devices like tablet computer, Ebook, mobile digital TV. This SOC introduces a kind of innovative architecture to fulfill both high performance mobile computing and high quality video decoding requirements addressed by mobile multimedia devices. JZ4775 provides high-speed CPU computing power and fluent 720p video replay.

The CPU (Central Processing Unit) core, equipped with 16kB instruction and 16kB data level 1 cache, and 256kB level 2 cache, operating at 1GHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included.

The VPU (Video Processing Unit) core is powered with another XBurst® processor engine. The SIMD instruction set implemented by XBurst® engine, in together with the on chip video accelerating engine and post processing unit, delivers high video performance. The maximum resolution of 720p in the formats of H.264, VC-1, MPEG-1/2, MPEG-4, RealVideo and VP8 are supported in decoding.
The memory interface supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory or up to 64-bit ECC MLC/TLC NAND flash memory and toggle NAND flash for cost sensitive applications. It provides the interface to DDR2, DDR3 and LPDDR memory chips with lower power consumption.

On-chip modules such as audio CODEC, multi-channel SAR-ADC, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. The LCD controller support regular RGB, 1280x720 output, WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. Other peripherals such as USB OTG and USB 1.1 host, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

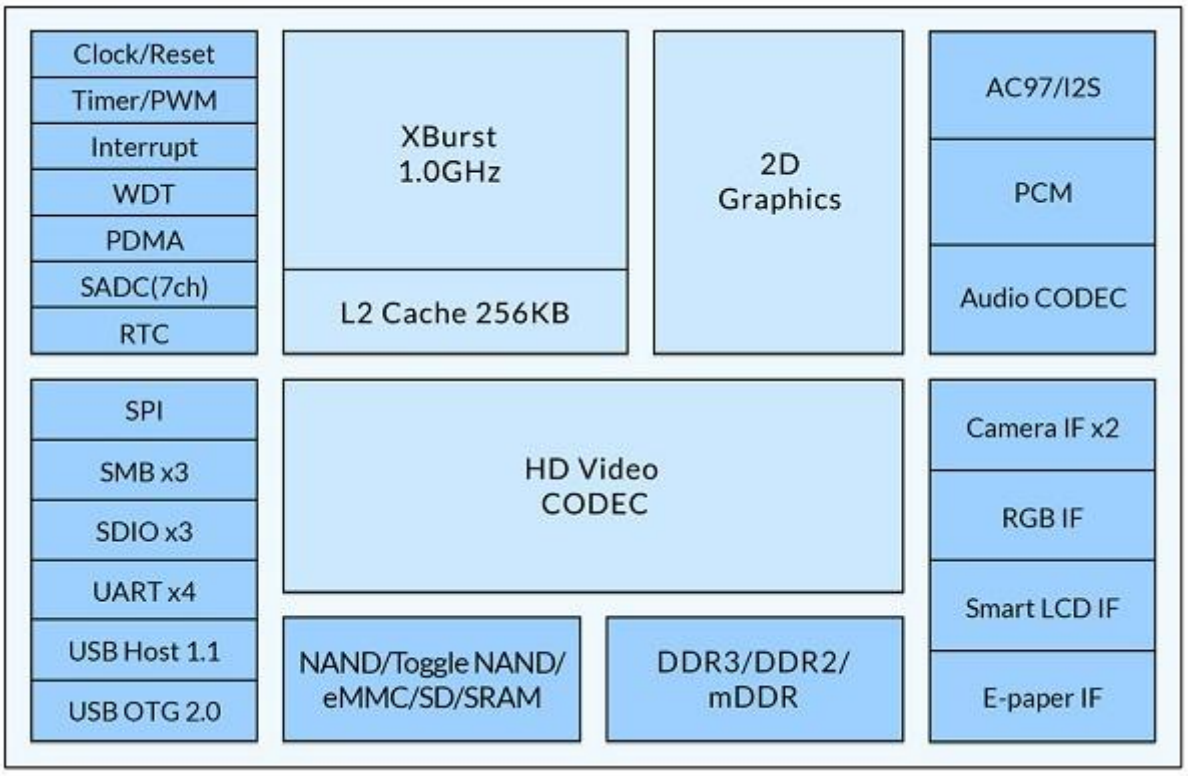


Figure 1-1 JZ4775 Diagram

1.2 Features

1.2.1 CPU

- XBurst® CPU
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the maximum frequency is 1G
- MMU
  - 32-entry joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- L1 Cache
  - 16kB instruction cache
  - 16kB data cache
- Hardware debug support
- 16kB tight coupled memory

- L2 Cache
  - 256kB unify cache

1.2.2 VPU

- MPEG-1/2 decoding up to 720P 30fps
- VC-1 decoding up to 720P 30fps
- H.264 decoding up to 720P 30fps
- VP8 decoding up to 720P 30fps
- MPEG-4 decoding up to 720P 30fps
- RV9 decoding up to 720P 30fps

1.2.3 GPU

- X2D
  - Location: AHB bus
  - Input format
    - Separate frame: YUV /YCbCr (4:2:0)
    - Packaged data: RGB888, RGB565, RGB555, NV12, NV21,TileYUV
  - Output data format
    - ARGB888，XRGB888, RGB555, RGB565
  - Color convention coefficient: configurable (CSC enable)
  - Minimum input image size (pixel): 4x4
  - Maximum input image size (pixel): 12288x12288 (12k x 12k)
  - Maximum output image size (pixel)
    - Width : up to 12288
    - Height: up to 12288
  - Image resizing
    - bi-cube zooming mode
  - Image Clockwise 90, 180, 270 rotation
  - Image horizontal and vertical mirror , same time with rotation
  - 5 layers OSD

1.2.4 Display/Camera/Audio

- LCD controller(compress must with IPU direct display)
  - Basic Features
    - Support panel(TFT, SLCD)
    - Display size up to 1280*720@60Hz(BPP24)
  - Colors Supports
    - Encoded pixel data of 16, 18 or 24 BPP in TFT mode
    - Support up to 16,777,216 (16M) colors in TFT mode
    - Support 24 BPP packed data

  - Panel Supports
    - Support 16-bit parallel TFT panel
    - Support 18-bit parallel TFT panel
    - Support 24-bit serial TFT panel with 8 data output pins
    - Support 24-bit parallel TFT panel
    - Support Delta RGB panel
    - Support SLCD panel
  - OSD Supports
    - Supports one single color background
    - Supports two foregrounds, and every size can be set for each foreground
    - Supports one transparency for the whole graphic
    - Supports one transparency for each pixel in one graphic
    - Supports color key and mask color key
    - Supports porter-duff blending
- EPD Controller
  - Supports multiple types of compatible EPD panels
  - Supports different size up to 4096x4096@20Hz
  - Supports 2/3/4 bits grayscale and color display
  - Pixel base updating
  - Supports hand-writing mode
  - Supports SW LUT algorithm
  - Supports AUTO-DU, AUTO-GC4 mode
- EPD Color Engine
  - Input data format is RGB565
  - Maximum image direction is 4096x4096
  - Includes CSC between RGB888 and YUV444
  - CSC supports 601 or 709, Wide or Narrow mode
  - Includes 3x3 Color Filter modules for RGB.R, RGB.B, RGB.B and YUV.Y.
  - Includes Color Linearization(VEE) for YUV.Y using 256-grade LUT
  - Supports Color Correction(HUE) for YUV.UV, and the coefficients are configurable
  - Supports Color Saturation for YUV.UV, and the coefficients are configurable
  - Supports Dither for RGB.R, RGB.B, RGB.B and YUV.Y. The output format is 2/3/4-bit configurable.
  - Supports Color Remapping for RGB.R, RGB.B, RGB.B and YUV.Y. If for RGB, there are two methods can be selected between individual CFA component and pixel array. And, the output order is configurable.
  - The EPDCE has a AXI master interface and a AHB slave interface.
- Camera interface module
  - Input image size up to 2048x2048 pixels
  - Max. VGA for image preview
  - Max. VGA for video record
  - Integrated DMA
  - Supported data format: YCbCr 4:4:4, YCbCr 4:2:2 and other formats

- Output format
  - csc mode: YCbCr 4:2:2 or YCbCr 4:2:0
  - bypass mode: the input data format
- Output frame format
  - Packaged : for all data format
  - Separated: for YCbCr 4:4:4, YCbCr 4:2:2 and YCbCr 4:2:0
- Supports ITU656 (YCbCr 4:2:2) input
- Configurable CIM_VSYNC and CIM_HSYNC signals: active high/low
- Configurable CIM_PCLK: active edge rising/falling
- 256x33 image data receive FIFO (RXFIFO)
- PCLK max. 80MHz
- Configurable output order

- AC97/I2S/SPDIF controller
  - AC-link (AC97) features
    - Up to 20 bit audio sample data sizes supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Support variable sample rate in AC-link format
    - Multiple channel output and double rated supported for AC-link format
    - Power Down Mode and two Wake-Up modes Supported for AC-link format
  - I2S features
    - 8, 16, 18, 20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Internal programmable or external serial clock and optional system clock supported for I2S or MSB-Justified format
    - Internal I2S CODEC supported
    - Two FIFOs for transmit and receive respectively
- SPDIF features
    - 8, 16, 18, 20 and 24 bit audio sample data sizes supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support IEC60958 two-channel PCM audio
    - Support IEC61937 multi-channel compressed audio
    - Support consumer mode and only support transmitter mode

  - Profession mode is not supported
  - The User data bit is ‘0’as it is not supported in the chip
  - Support sampling frequency from 32kHz to 192kHz
- PCM interface
  - Data starts with the frame PCMSYN or one PCMCLK later
  - Support three modes of operation for PCM
    - Short frame sync mode
    - Long frame sync mode
    - Multi-slot mode
  - Data is transferred and received with the MSB first
  - Support master mode and slave mode
  - The PCM serial output data, PCMDOUT, is clocked out using the rising edge of the PCMSCLK
  - The PCM serial input data, PCMDIN, is clocked in on the falling edge of the PCMSCLK
  - 8/16 bit sample data sizes supported
  - DMA transfer mode supported
  - Two FIFOs for transmit and receive respectively with 16 samples capacity in every direction
- Internal CODEC Interface
  - 24 bits ADC and DAC
  - Headphone load up to 16 Ohm
  - Sample frequency supported: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, and 96k
  - Stereo line input
  - DAC to HP path: Power consumption: 17.6mW, SNR: 95dB, THD: -65dB @17.6mW /16Ohm
  - DAC to stereo line output path @10kOhm: SNR: 95dB A-Weighted, THD: -80dB @FS-1dB
  - Line input to ADC path: SNR: 95dB A-Weighted, THD: -80dB @FS-1dB
  - Separate power-down modes for ADC and DAC path with several shutdown modes
  - Reduction of audible glitches systems: Pop Reduction system, Soft Mute mode
  - Output short circuit protection
  - Digital MIC supported.
  - Support Capacitor-coupled and Capacitor-less mode headphone connection
  - Advance SNR of recode.
  - Updata AGC system.
  - Add digital amplitude limiter use for remove the short when sound is very largely.
  - Add DAC digital amplifier the gain up to 32dB.

1.2.5 Memory Interface

- DDR Controller
  - Support DDR2, DDR3, DDR3L, mobile DDR (LPDDR), memory，up to 800Mbps

- Support x16 and x32 external DDR data width
- Asynchornize to system bus and each port.
- Support clock-stop mode
- Support auto-refresh and self-refresh
- Support power-down mode and deep-power-down mode
- Programmable DDR timing parameters
- Programmable DDR row and column address width and order

- Static memory interface
  - Support 3 external chip selection CS3~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8/16-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank
- NAND flash interface
  - Support on CS3~CS1#, sharing with static memory bank3~bank1
  - Support both of conventional NAND flash memory and Toggle NAND flash memory
  - Support most types of NAND flashes, 8/16-bit data access, 512B/2KB/4KB/8KB/16KB page size. For 512B page size, 3 and 4 address cycles are supported. For 2KB/4KB/8KB/16KB page size, 4 and 5 address cycles are supported
  - Support read/erase/program NAND flash memory
  - Support boot from NAND flash
- BCH Controller
  - Support up to 64-bit ECC encoding and decoding for NAND
- The XBurst® processor system supports little endian only

1.2.6 System Functions

- Clock generation and power management
  - On-chip 24/26MHZ oscillator circuit
  - On-chip 32.768KHZ oscillator circuit
  - One two-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - SSI clock supports 50M clock
  - MSC clock supports 100M clock
  - Functional-unit clock gating
  - Shut down power supply for J1, VPU, L2CC, X2D
- Timer and counter unit with PWM output and/or input edge counter
  - Provide eight channels, four channels 0~3 can generate PWM, two of them have input

signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer
  - One channel
  - 32-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
    - PCLK, EXTAL and RTCCLK can be used as the clock for counter
    - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- PDMA Controller
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SOC
  - A simple Xburst®-1 CPU supports smart transfer mode controlled by programmable firmware
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - A dedicated bus interface - BIF interconnects with on-chip BCH
  - A dedicated bus interface - NIF interconnects with on-chip NEMC or off-chip NEMC.
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - 7 Channels
  - Resolution: 12-bit
  - Integral nonlinearity: ±1 LSB
  - Differential nonlinearity: ±0.5 LSB
  - Resolution/speed: up to 2Msps

- Max Frequency: 200k
- Low power dissipation: 1.5mW(worst)
- Support 4-wire and 5-wire touch panel measurement (Through pin XP, XN, YP, YN and AUX2)
- Support multi-touch detect
- Support write control command by software
- Support voltage measurement (Through pin VBAT)
- Support two auxiliary input (Through pin AUX1, AUX2)
- Single-end and Differential Conversion Mode
- Auto X/Y, X/Y/Z1/Z2 and X/Y/Z1/Z2/X2/Y2 position measurement
- Support external touch screen controller

- RTC (Real Time Clock)
  - RTCLK selectable from the oscillator or from the divided clock of EXCLK, so that 32k crystal can be absent if the hibernating mode is not needed
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter

1.2.7 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 7 interrupts, 1 for every group, to INTC
- SMB Controller
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - -level transmit and receive FIFOs
  - Interrupt operation

  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 3 independent SMB channels (SMB0, SMB1, SMB2)
- Synchronous serial interfaces (SSI0)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI_CE0_ / SSI_CE1_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing
- Four UARTs (UART0, UART1, UART2, UART3)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification
- Three MMC/SD/SDIO controllers (MSC0, MSC1, MSC2)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit ,4bit and 8bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands
  - Support Command Completion Signal and interrupt to CPU

  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes
- USB 1.1 host interface
  - Open Host Controller Interface OHCI-compatible and USB Revision 1.1-compatible
  - Full speed and low speed
  - Embedded USB 1.1 PHY
- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints:
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer
- GMAC controller
  - 10/100/1000 Mbps operation
  - Supports MII、RMII、GMII and RGMII PHY interfaces
  - Supports VLAN and CRC
  - Station Management Agent (SMA)
  - remote wake-up frame and magic packet frame processing
- OTP Slave Interface
  - Total 256 bits. Higher 128bits are read-able and write-able, Lower 128bits are read only

1.2.8 Boot

16kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	65nm CMOS low power
Power supply voltage	General purpose I/O: 1.6~3.6V DDR I/O for DDR2: 1.8V± 0.1V DDR I/O for DDR3: 1.5V± 0.075V DDR I/O for DDR3L: 1.35V± 0.1V DDR I/O for LPDDR: 1.8V± 0.15V RTC I/O: 1.8V~3.6V EFUSE programming: 2.5V± 10% Analog power supply 1: 2.5V± 10%

	Analog power supply 2: 3.3V± 10% Core: 1.2 -0.1/+0.2 V
Package	BGA314 14mm x 14mm x 1.4mm, 0.65mm pitch
Operating frequency	1GHz

2 Packaging and Pinout Information

2.1 Overview

JZ4775 processor is offered in 314-pin BGA package, which is 14mm x 14mm x 1.4mm outline, 21 x 21 matrix ball grid array and 0.65mm ball pitch, show in Figure 2-1. The JZ4775 pin to ball assignment is show in Figure 2-2.

The detailed pin description is listed in Table 2-1~Table 2-24.

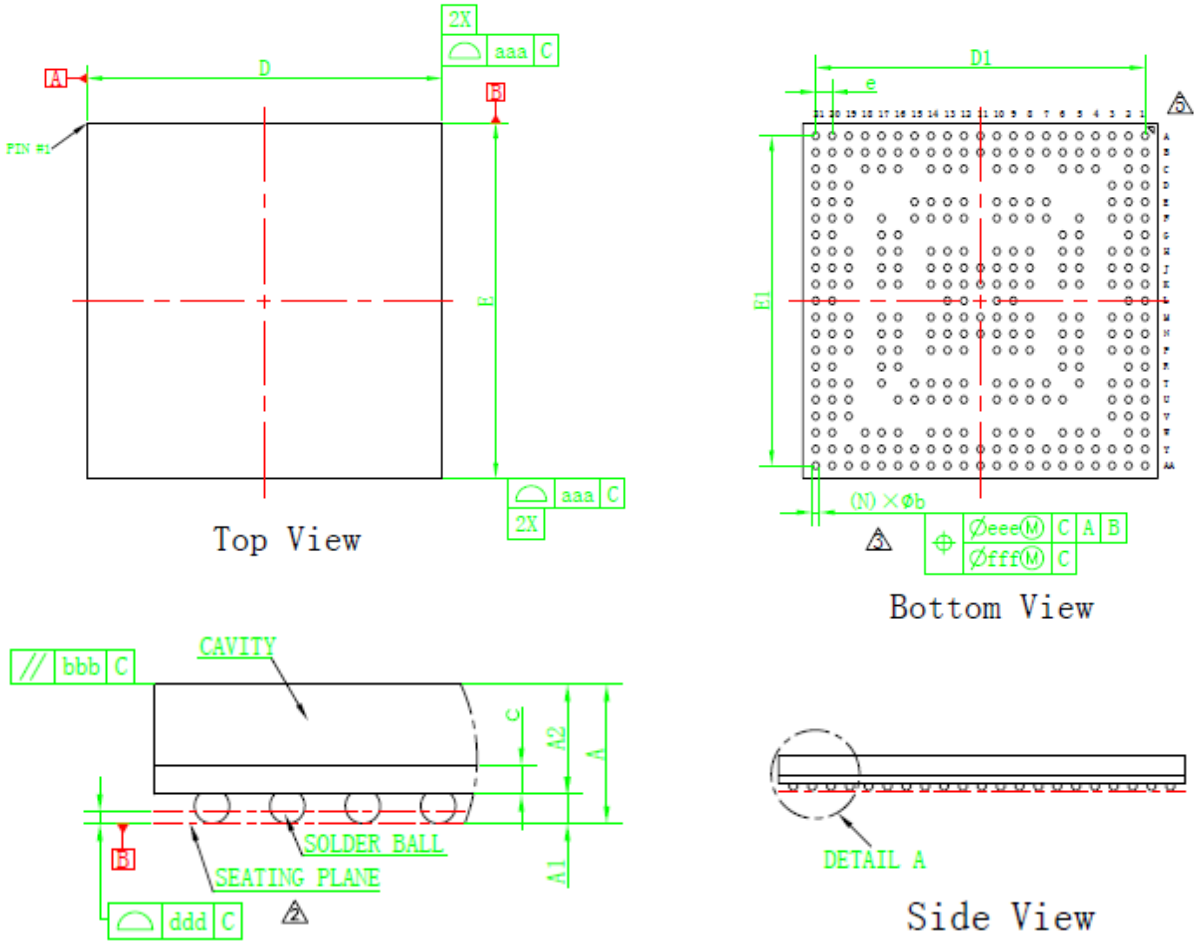
2.2 Solder Process

JZ4775 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

JZ4775 package moisture sensitivity is level 3.

2.4 JZ4775 Package



DETAIL A

20:1

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.300	—	—	0.051
A1	0.200	0.250	0.300	0.008	0.010	0.012
A2	0.900	0.950	1.000	0.035	0.037	0.039
c	0.210	0.250	0.290	0.008	0.010	0.011
D	13.900	14.000	14.100	0.547	0.551	0.555
E	13.900	14.000	14.100	0.547	0.551	0.555
D1	—	13.000	—	—	0.512	—
E1	—	13.000	—	—	0.512	—
e	—	0.650	—	—	0.026	—
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.150			0.006		
bbb	0.200			0.008		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
N	314			314		
MD/ME	21/21			21/21		

Figure 2-1 JZ4775 package outline drawing

Notes:

1. All units are in millimeter;
2. Primary datum C and seating plane are the solder balls;
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C;
4. Special characteristics C class: bbb, ddd;
5. The pattern of Pin 1 fiducial is for reference only;
6. Ball pad opening: 0.280mm;

JZ4775 Ball Assignment Ver1.0
BGA314, 14mm X 14mm X 1.4mm, 0.65pitch, top view

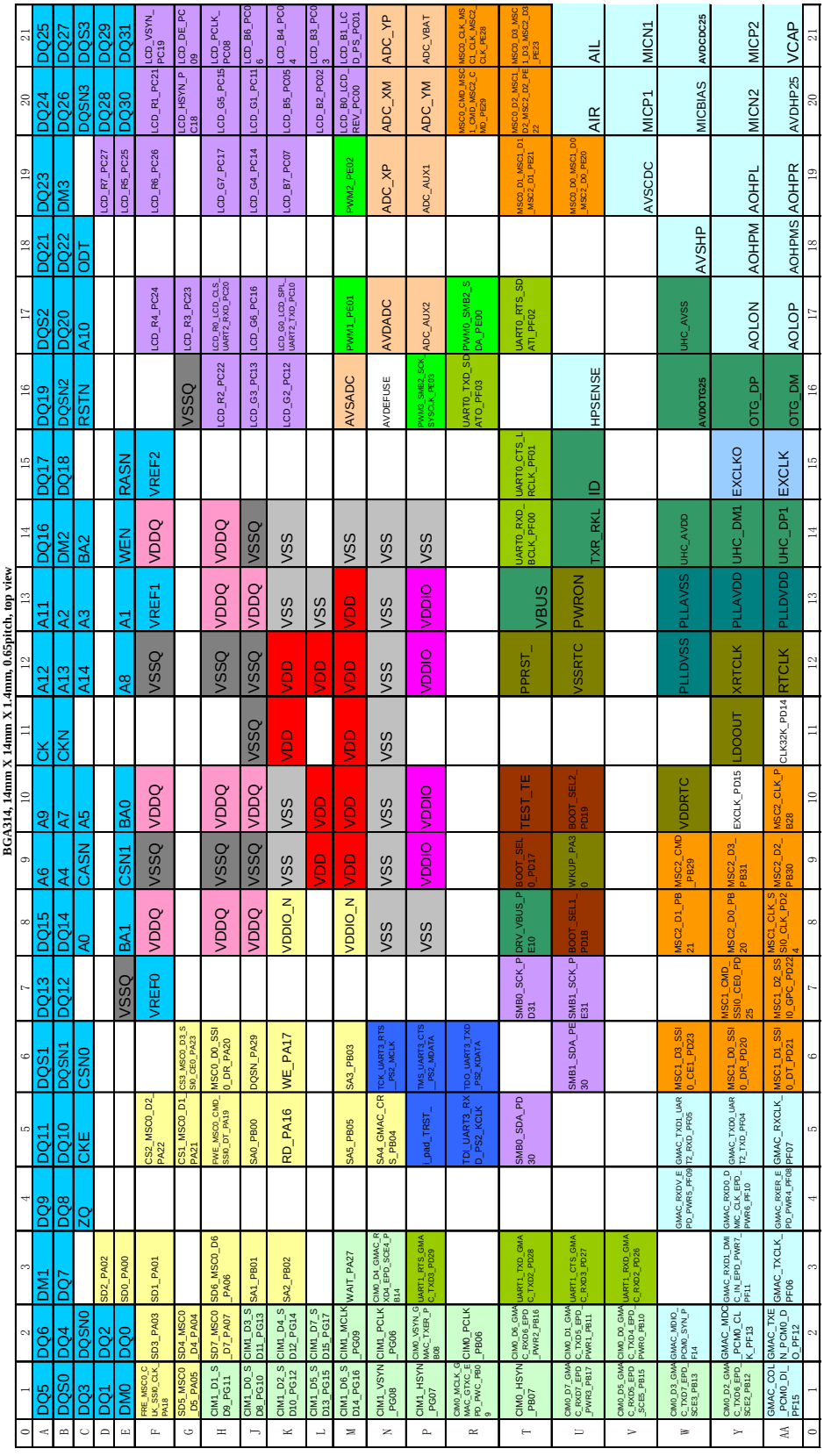


Figure 2-2 JZ4775 pin to ball assignment

2.5 Pin Description [1][2]

2.5.1 DRAM

Table 2-1 Port 0 DDR(mDDR, DDR2, DDR3) Pins (76)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DQ0	IO	E2	Bi-dir, Single-end	DQ0: DDR data bus bit 0	VDDQ
DQ1	IO	D1	Bi-dir, Single-end	DQ1: DDR data bus bit 1	VDDQ
DQ2	IO	D2	Bi-dir, Single-end	DQ2: DDR data bus bit 2	VDDQ
DQ3	IO	C1	Bi-dir, Single-end	DQ3: DDR data bus bit 3	VDDQ
DQ4	IO	B2	Bi-dir, Single-end	DQ4: DDR data bus bit 4	VDDQ
DQ5	IO	A1	Bi-dir, Single-end	DQ5: DDR data bus bit 5	VDDQ
DQ6	IO	A2	Bi-dir, Single-end	DQ6: DDR data bus bit 6	VDDQ
DQ7	IO	B3	Bi-dir, Single-end	DQ7: DDR data bus bit 7	VDDQ
DQ8	IO	B4	Bi-dir, Single-end	DQ8: DDR data bus bit 8	VDDQ
DQ9	IO	A4	Bi-dir, Single-end	DQ9: DDR data bus bit 9	VDDQ
DQ10	IO	B5	Bi-dir, Single-end	DQ10: DDR data bus bit 10	VDDQ
DQ11	IO	A5	Bi-dir, Single-end	DQ11: DDR data bus bit 11	VDDQ
DQ12	IO	B7	Bi-dir, Single-end	DQ12: DDR data bus bit 12	VDDQ
DQ13	IO	A7	Bi-dir, Single-end	DQ13: DDR data bus bit 13	VDDQ
DQ14	IO	B8	Bi-dir, Single-end	DQ14: DDR data bus bit 14	VDDQ
DQ15	IO	A8	Bi-dir, Single-end	DQ15: DDR data bus bit 15	VDDQ
DQ16	IO	A14	Bi-dir, Single-end	DQ16: DDR data bus bit 16	VDDQ
DQ17	IO	A15	Bi-dir, Single-end	DQ17: DDR data bus bit 17	VDDQ
DQ18	IO	B15	Bi-dir, Single-end	DQ18: DDR data bus bit 18	VDDQ
DQ19	IO	A16	Bi-dir, Single-end	DQ19: DDR data bus bit 19	VDDQ
DQ20	IO	B17	Bi-dir, Single-end	DQ20: DDR data bus bit 20	VDDQ
DQ21	IO	A18	Bi-dir, Single-end	DQ21: DDR data bus bit 21	VDDQ
DQ22	IO	B18	Bi-dir, Single-end	DQ22: DDR data bus bit 22	VDDQ
DQ23	IO	A19	Bi-dir, Single-end	DQ23: DDR data bus bit 23	VDDQ
DQ24	IO	A20	Bi-dir, Single-end	DQ24: DDR data bus bit 24	VDDQ
DQ25	IO	A21	Bi-dir, Single-end	DQ25: DDR data bus bit 25	VDDQ
DQ26	IO	B20	Bi-dir, Single-end	DQ26: DDR data bus bit 26	VDDQ
DQ27	IO	B21	Bi-dir, Single-end	DQ27: DDR data bus bit 27	VDDQ
DQ28	IO	D20	Bi-dir, Single-end	DQ28: DDR data bus bit 28	VDDQ
DQ29	IO	D21	Bi-dir, Single-end	DQ29: DDR data bus bit 29	VDDQ
DQ30	IO	E20	Bi-dir, Single-end	DQ30: DDR data bus bit 30	VDDQ
DQ31	IO	E21	Bi-dir, Single-end	DQ31: DDR data bus bit 31	VDDQ
A0	O	C8	Output, Single-end	A0: DDR address bus bit 0	VDDQ
A1	O	E13	Output, Single-end	A1: DDR address bus bit 1	VDDQ
A2	O	B13	Output, Single-end	A2: DDR address bus bit 2	VDDQ
A3	O	C13	Output, Single-end	A3: DDR address bus bit 3	VDDQ
A4	O	B9	Output, Single-end	A4: DDR address bus bit 4	VDDQ
A5	O	C10	Output, Single-end	A5: DDR address bus bit 5	VDDQ
A6	O	A9	Output, Single-end	A6: DDR address bus bit 6	VDDQ
A7	O	B10	Output, Single-end	A7: DDR address bus bit 7	VDDQ
A8	O	E12	Output, Single-end	A8: DDR address bus bit 8	VDDQ
A9	O	A10	Output, Single-end	A9: DDR address bus bit 9	VDDQ

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
A10	O	C17	Output, Single-end	A10: DDR address bus bit 10	VDDQ
A11	O	A13	Output, Single-end	A11: DDR address bus bit 11	VDDQ
A12	O	A12	Output, Single-end	A12: DDR address bus bit 12	VDDQ
A13	O	B12	Output, Single-end	A13: DDR address bus bit 13	VDDQ
A14	O	C12	Output, Single-end	A14: DDR address bus bit 14	VDDQ
CSN0	O	C6	Output, Single-end	CSN0: DDR chip select 0	VDDQ
CSN1	O	E9	Output, Single-end	CSN1: DDR chip select 1	VDDQ
RASN	O	E15	Output, Single-end	RASN: DDR row address strobe	VDDQ
CASN	O	C9	Output, Single-end	CASN: DDR column address strobe	VDDQ
WEN	O	E14	Output, Single-end	WEN: DDR write enable	VDDQ
DQS0	IO	B1	Bi-dir, Differential	DQS0: DDR data byte 0 strobe positive	VDDQ
DQSN0	IO	C2	Bi-dir, Differential	DQS0N: DDR data byte 0 strobe negative for differential. Use this pin for differential DQS signal.	VDDQ
DQS1	IO	A6	Bi-dir, Differential	DQS1: DDR data byte 1 strobe positive	VDDQ
DQSN1	IO	B6	Bi-dir, Differential	DQS1N: DDR data byte 1 strobe negative for differential.	VDDQ
DQS2	IO	A17	Bi-dir, Differential	DQS2: DDR data byte 2 strobe positive	VDDQ
DQSN2	IO	B16	Bi-dir, Differential	DQS2N: DDR data byte 2 strobe negative for differential.	VDDQ
DQS3	IO	C21	Bi-dir, Differential	DQS3: DDR data byte 3 strobe positive	VDDQ
DQSN3	IO	C20	Bi-dir, Differential	DQS3N: DDR data byte 3 strobe negative for differential.	VDDQ
DM0	O	E1	Output, Single-end	DM0: DDR data byte 0 mask	VDDQ
DM1	O	A3	Output, Single-end	DM1: DDR data byte 1 mask	VDDQ
DM2	O	B14	Output, Single-end	DM2: DDR data byte 2 mask	VDDQ
DM3	O	B19	Output, Single-end	DM3: DDR data byte 3 mask	VDDQ
BA0	O	E10	Output, Single-end	BA0: DDR address bus bank 0	VDDQ
BA1	O	E8	Output, Single-end	BA1: DDR address bus bank 1	VDDQ
BA2	O	C14	Output, Single-end	BA2: DDR address bus bank 2	VDDQ
CK	O	A11	Output, Differential	CK: DDR clock	VDDQ
CKN	O	B11	Output, Differential	CKN: DDR inverse clock	VDDQ
CKE	O	C5	Output, Single-end	CKE: DDR clock enable	VDDQ
ODT	O	C18	Output, Single-end	ODT: DDR rank 0 On-die termination	VDDQ
RSTN	O	C16	Output, Single-end	RSTN: DDR3 reset pin	VDDQ
VREF0	AI	F7		VREF0: DDR/DDR2/DDR3 input reference voltage	
VREF1	AI	F13		VREF1: DDR/DDR2/DDR3 input reference voltage	
VREF2	AI	F15		VREF2: DDR/DDR2/DDR3 input reference voltage	
ZQ	AIO	C4		ZQ: DDR3 External reference which is connected to a 240ohm resister to VSSIOm	

2.5.2 BOOT and storage

Implementation	BOOT pin/signal used
NAND flash 8-bit	SD0~SD7, FRE_, FWE_, FRB, CS1_~CS2_, CL(SA0), AL(SA1),
NAND flash 8/16-bit	SD0~SD15, FRE_, FWE_, FRB, CS1_~CS2_, CL(SA0), AL(SA1),
MMC/SD card	MSC0_D0~D3, MSC0_CLK, MSC0_CMD
SPI	SSI0_CLK, SSI0_DT, SSI0_DR, SSI0_CE0_

Implementation	Storage pin/signal used
EBOOK/EPEN	Static memory: SD0~SD7, SA0~SA5, CS1_~CS3_, RD_, WE_, WAIT_

Table 2-2 Static-Memory/MSC0/SPI0 Pins (24)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD0 PA00	IO IO	E3	8mA, pullup-pe	SD0: Static memory data bus bit 0 PA0: GPIO group A bit 0	VDDIO_N
SD1 PA01	IO IO	F3	8mA, pullup-pe	SD1: Static memory data bus bit 1 PA1: GPIO group A bit 1	VDDIO_N
SD2 PA02	IO IO	D3	8mA, pullup-pe	SD2: Static memory data bus bit 2 PA2: GPIO group A bit 2	VDDIO_N
SD3 PA03	IO IO	F2	8mA, pullup-pe	SD3: Static memory data bus bit 3 PA3: GPIO group A bit 3	VDDIO_N
SD4 **MSC0_D4** PA04	IO IO IO	G2	8mA, pullup-pe	SD4: Static memory data bus bit 4 MSC0_D4: MSC (MMC/SD) 0 data bit 4 PA4: GPIO group A bit 4	VDDIO_N
SD5 **MSC0_D5** PA05	IO IO IO	G1	8mA, pullup-pe	SD5: Static memory data bus bit 5 MSC0_D5: MSC (MMC/SD) 0 data bit 5 PA5: GPIO group A bit 5	VDDIO_N
SD6 **MSC0_D6** PA06	IO IO IO	H3	8mA, pullup-pe	SD6: Static memory data bus bit 6 MSC0_D6: MSC (MMC/SD) 0 data bit 6 PA6: GPIO group A bit 6	VDDIO_N
SD7 **MSC0_D7** PA07	IO IO IO	H2	8mA, pullup-pe	SD7: Static memory data bus bit 7 MSC0_D7: MSC (MMC/SD) 0 data bit 7 PA7: GPIO group A bit 7	VDDIO_N
SA0 (CL) PB00	O IO	J5	8mA, pulldown-pe, **rst-pe**	SA1: Static memory address bus bit 0 If NAND flash is used, this pin is used as NAND CL (command latch) pin PB0: GPIO group B bit 0	VDDIO_N
SA1 (AL) PB01	O IO	J3	8mA, pulldown-pe, **rst-pe**	SA1: Static memory address bus bit 1 If NAND flash is used, this pin is used as NAND AL (address latch) pin PB1: GPIO group B bit 1	VDDIO_N
SA2 PB02	O IO	K3	8mA, pullup-pe	SA2: Static memory address bus bit 2 PB2: GPIO group B bit 2	VDDIO
SA3 PB03	O IO	M6	8mA, pullup-pe	SA3: Static memory address bus bit 3 PB3: GPIO group B bit 3	VDDIO
SA4 GMAC_CRS PB04	O I IO	N5	**4mA(~SL)** pullup-pe	SA4: Static memory address bus bit 4 GMAC_ CRS: Ethernet carrier sense for GMAC PB4: GPIO group B bit 4	VDDIO
SA5 PB5	O IO	M5	8mA, pullup-pe	SA5: Static memory address bus bit 5 PB5: GPIO group B bit 5. NAND flash FRB input 1 candidate	VDDIO
RD_ PA16	O IO	K5	8mA, pullup-pe, **rst-pe**	RD_: Static memory read strobe PA16: GPIO group A bit 16	VDDIO
WE_ PA17	O IO	K6	8mA, pullup-pe, **rst-pe**	WE_: Static memory write strobe PA17: GPIO group A bit 17	VDDIO
FRE_ MSC0_CLK SSI0_CLK PA18	O O O IO	F1	8mA, pullup-pe, **rst-pe**	FRE_: NAND read enable MSC0_CLK: MSC (MMC/SD) 0 clock output SSI0_CLK: SSI 0 clock output PA18: GPIO group A bit 18	VDDIO_N
FWE_ MSC0_CMD SSI0_DT PA19	O O O IO	H5	8mA, pullup-pe, **rst-pe**	FEW_: NAND write enable MSC0_CMD: MSC (MMC/SD) 0 command SSI0_DT: SSI 0 data output PA19: GPIO group A bit 19	VDDIO_N

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_D0 SSI0_DR PA20(FRB0)	IO I IO	H6	8mA, pullup-pe **rst-pe**	MSC0_D0: MSC (MMC/SD) 0 data bit 0 SSI0_DR: SSI 0 data input PA20: GPIO group A bit 20. NAND flash FRB (ready/busy) input 0	VDDIO_N
CS1_ MSC0_D1 PA21	O IO IO	G5	8mA, pullup-pe, **rst-pe**	CS1_: NAND/NOR/SRAM chip select 1 MSC0_D1: MSC (MMC/SD) 0 data bit 1 PA21: GPIO group A bit 21	VDDIO_N
CS2_ MSC0_D2 PA22	O IO IO	F5	8mA, pullup-pe, **rst-pe**	CS2_: NAND/NOR/SRAM chip select 2 MSC0_D2: MSC (MMC/SD) 0 data bit 2 PA22: GPIO group A bit 22	VDDIO_N
CS3_ MSC0_D3 **SSI0_CE0_** PA23	O IO O IO	G6	8mA, pullup-pe, **rst-pe**	CS3_: NAND/NOR/SRAM chip select 3 MSC0_D3: MSC (MMC/SD) 0 data bit 3 **SSI0_CE0_: SSI 0 chip enable 0** PA23: GPIO group A bit 23. NAND flash FRB input 1 candidate	VDDIO_N
WAIT_ PA27(FRB1)	I IO	M3	8mA, pullup-pe	WAIT_: Slow static memory/device wait signal PA27: GPIO group A bit 27. NAND flash FRB input 1 candidate	VDDIO
DQSN PA29	IO IO	J6	8mA pullup-pe	DQSN: Toggle nand DQS pin. PA29: GPIO group A bit 29.	VDDIO_N

2.5.3 LCD/EPD

Table 2-3 LCDC Pins (28; all GPIO shared: PC0~27)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_B0 LCD_REV PC00	O O IO	M20	8mA, pullup-pe	LCD_B0: LCD Blue data bit 0 LCD_REV: LCD REV output for special TFT PC0: GPIO group C bit 0	VDDIO
LCD_B1 LCD_PS PC01	O O IO	M21	8mA, pullup-pe	LCD_B1: LCD Blue data bit 1 LCD_PS: LCD PS output for special TFT PC01: GPIO group C bit 1	VDDIO
LCD_B2 PC02	O IO	L20	8mA, pullup-pe	LCD_B2: LCD Blue data bit 2 PC02: GPIO group C bit 2	VDDIO
LCD_B3 PC03	O IO	L21	8mA, pullup-pe	LCD_B3: LCD Blue data bit 3 PC03: GPIO group C bit 3	VDDIO
LCD_B4 PC04	O IO	K21	8mA, pullup-pe	LCD_B4: LCD Blue data bit 4 PC04: GPIO group C bit 4	VDDIO
LCD_B5 PC05	O IO	K20	8mA, pullup-pe	LCD_B5: LCD Blue data bit 5 PC05: GPIO group C bit 5	VDDIO
LCD_B6 PC06	O IO	J21	8mA, pullup-pe	LCD_B6: LCD Blue data bit 6 PC06: GPIO group C bit 6	VDDIO
LCD_B7 PC07	O IO	K19	8mA, pullup-pe	LCD_B7: LCD Blue data bit 7 PC07: GPIO group C bit 7	VDDIO
LCD_PCLK PC08	O IO	H21	16mA, pullup-pe	LCD_PCLK: LCD pixel clock PC8: GPIO group C bit 8	VDDIO
LCD_DE PC09	O IO	G21	8mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PC09: GPIO group C bit 9	VDDIO
LCD_G0 LCD_SPL UART2_TxD PC10	O O O IO	K17	8mA, pullup-pe, **rst-pe**	LCD_G0: LCD Green data bit 0 LCD_SPL: LCD SPL output UART2_TxD: UART 2 transmitting data PC10: GPIO group C bit 10	VDDIO
LCD_G1 PC11	O IO	J20	8mA, pullup-pe	LCD_G1: LCD Green data bit 1 PC11: GPIO group C bit 11	VDDIO
LCD_G2 PC12	O IO	K16	8mA, pullup-pe	LCD_G2: LCD Green data bit 2 PC12: GPIO group C bit 12	VDDIO
LCD_G3 PC13	O IO	J16	8mA, pullup-pe	LCD_G3: LCD Green data bit 3 PC13: GPIO group C bit 13	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_G4 PC14	O IO	J19	8mA, pullup-pe	LCD_G4: LCD Green data bit 4 PC14: GPIO group C bit 14	VDDIO
LCD_G5 PC15	O IO	H20	8mA, pullup-pe	LCD_G5: LCD Green data bit 5 PC15: GPIO group C bit 15	VDDIO
LCD_G6 PC16	O IO	J17	8mA, pullup-pe	LCD_G6: LCD Green data bit 6 PC16: GPIO group C bit 16	VDDIO
LCD_G7 PC17	O IO	H19	8mA, pullup-pe	LCD_G7: LCD Green data bit 7 PC17: GPIO group C bit 17	VDDIO
LCD_HSYN PC18	IO IO	G20	8mA, pullup-pe	LCD_HSYN: LCD line clock/horizonal sync PC18: GPIO group C bit 18	VDDIO
LCD_VSYN PC19	IO IO	F21	8mA, pullup-pe	LCD_VSYN: LCD frame clock/vertical sync PC19: GPIO group C bit 19	VDDIO
LCD_R0 LCD_CLS UART2_RxD PC20	O O I IO	H17	8mA, pullup-pe	LCD_R0: LCD Red data bit 0 LCD_CLS: LCD CLS output UART2_RxD: UART 2 Receiving data PC20: GPIO group C bit 20	VDDIO
LCD_R1 PC21	O IO	F20	8mA, pullup-pe	LCD_R1: LCD Red data bit 1 PC21: GPIO group C bit 21	VDDIO
LCD_R2 PC22	O IO	H16	8mA, pullup-pe	LCD_R2: LCD Red data bit 2 PC22: GPIO group C bit 22	VDDIO
LCD_R3 PC23	O IO	G17	8mA, pullup-pe	LCD_R3: LCD Red data bit 3 PC23: GPIO group C bit 23	VDDIO
LCD_R4 PC24	O IO	F17	8mA, pullup-pe	LCD_R4: LCD Red data bit 4 PC24: GPIO group C bit 24	VDDIO
LCD_R5 PC25	O IO	E19	8mA, pullup-pe	LCD_R5: LCD Red data bit 5 PC25: GPIO group C bit 25	VDDIO
LCD_R6 PC26	O IO	F19	8mA, pullup-pe	LCD_R6: LCD Red data bit 6 PC26: GPIO group C bit 26	VDDIO
LCD_R7 PC27	O IO	D19	8mA, pullup-pe	LCD_R7: LCD Red data bit 7 PC27: GPIO group C bit 27	VDDIO

2.5.4 MAC/EPD/UART2

Table 2-4 MAC-GMAC/RGMAC/PCM0 Pins (12; all GPIO shared: PF4~15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
GMAC_TXD0 UART2_TxD PF04	O O IO	Y5	**4mA(~SL)**, pulldown-pe	GMAC_TXD0: Ethernet transmit data bit 0 for RMII、MII、RGMII and GMII UART2_TxD: UART 2 transmitting data PF04: GPIO group F bit 4. Pull-down not enabled at and after reset	VDDIO
GMAC_TXD1 UART2_RxD PF05	O I IO	W5	**4mA(~SL)** pulldown-pe	GMAC_TXD1: Ethernet transmit data bit 1 for RMII、MII、RGMII and GMII UART2_RxD: UART 2 Receiving data PF05: GPIO group F bit 5. Pull-down not enabled at and after reset	VDDIO
GMAC_TXCLK (RGMAC_CLK) PF06	I IO	AA3	**4mA(~SL)** pulldown-pe	GMAC_TXCLK: Ethernet 25MHz transmit clock for GMAC or (RGMAC_CLK) ethernet 50MHz reference clock for RGMAC input PF06: GPIO group F bit 6. Pull-down not enabled at and after reset	VDDIO
GMAC_RXCLK PF07	I IO	AA5	**4mA(~SL)** pulldown-pe	GMAC_RXCLK: Ethernet receive clock for GMAC (25MHz) PF07: GPIO group F bit 7. Pull-down not enabled at and after reset	VDDIO
GMAC_RXER EPD_PWR4 PF08	I O IO	AA4	**4mA(~SL)** pulldown-pe	GMAC_RXER: Ethernet receive error EPD_PWR7: EPD power control bit4 PF08: GPIO group F bit 8. Pull-down not enabled at and after reset	VDDIO
GMAC_RXD	I	W4	**4mA(~SL)**	GMAC_RXDV: Ethernet receive data valid	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
V EPD_PWR5 PF09	O IO		pulldown-pe	EPD_PWR7: EPD power control bit5 PF09: GPIO group F bit 9. Pull-down not enabled at and after reset	
GMAC_RXD0 DMIC_CLK EPD_PWR6 PF10	I O O IO	Y4	**4mA(~SL)** pulldown-pe	GMAC_RXD0: Ethernet receive data bit 0 for RMII、MII、RGMII and GMII DMIC_CLK: Digital MIC clock output EPD_PWR7: EPD power control bit6 PF10: GPIO group F bit 10. Pull-down not enabled at and after reset	VDDIO
GMAC_RXD1 DMIC_IN EPD_PWR7 PF11	I O I IO	Y3	**4mA(~SL)** pulldown-pe	GMAC_RXD1: Ethernet receive data bit 1 for RMII、MII、RGMII and GMII DMIC_IN: Digital MIC input EPD_PWR7: EPD power control bit7 PF11: GPIO group F bit 11. Pull-down not enabled at and after reset	VDDIO
GMAC_TXEN PCM0_DO PF12	O O IO	AA2	**4mA(~SL)** pullup-pe	GMAC_TXEN: Ethernet transmit enable PCM0_DO: PCM 0 data out PF12: GPIO group F bit 12	VDDIO
GMAC_MDC PCM0_CLK PF13	O IO IO	Y2	**4mA(~SL)** pullup-pe	GMAC_MDC: Ethernet management clock for GMAC and RGMAC PCM0_CLK: PCM 0 clock PF13: GPIO group F bit 13	VDDIO
GMAC_MDIO PCM0_SYN PF14	IO IO IO	W2	**4mA(~SL)** pullup-pe	GMAC_MDIO: Ethernet management data for GMAC and RGMAC PCM0_SYN: PCM 0 sync PF14: GPIO group F bit 14	VDDIO
GMAC_COL, PCM0_DI F15	I IIO	AA1	**4mA(~SL)** pullup-pe	GMAC_COL: Ethernet collision for GMAC PCM0_DI: PCM 0 data in F15: GPIO group F bit 15	VDDIO

2.5.5 CIM0/EPD/GMAC

Table 2-5 CIM/EPD/GMAC Pins (12; all GPIO shared: PB6~17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM0_PCLK PB06	I IO	R2	8mA, pullup-pe	CIM_PCLK: CIM pixel clock input PB06: GPIO group B bit 6	VDDIO
CIM0_HSYN PB07	I O	T1	8mA, pullup-pe	CIM_HSYN: CIM horizonal sync input PB07: GPIO group B bit 7	VDDIO
CIM0_VSYN GMAC_TXER PB08	I O IO	P2	**4mA(~SL)** pullup-pe, **rst-pe**	CIM_VSYN: CIM vertical sync input GMAC_TXER: PHY Transmit Error PB08: GPIO group B bit 8	VDDIO
CIM0_MCLK**(** **GMAC_GTXC)** EPD_PWC PB09	O O IO	R1	**8mA(~SL)** pullup-pe	CIM_MCLK: CIM master clock output **()** EPD_PWC: EPD power control common PB09: GPIO group B bit 9	VDDIO
CIM0_D0 GMAC_TXD4 EPD_PWR0 PB10	I O O IO	V2	**4mA(~SL)** pulldown-pe	CIM_D0: CIM data input bit 0. When use 8-bit data, use CIM_D0~D7 GMAC_TXD4: PHY Transmit Data bit 4 for GMII EPD_PWR0: EPD power control bit 0 PB10: GPIO group B bit 10	VDDIO
CIM0_D1 GMAC_TXD5 EPD_PWR1 PB11	I O O IO	U2	**4mA(~SL)** pulldown-pe	CIM_D1: CIM data input bit 1 GMAC_TXD5: PHY Transmit Data bit 5 for GMII EPD_PWR1: EPD power control bit 1 PB11: GPIO group B bit 11	VDDIO
CIM0_D2 GMAC_TXD6 EPD_SCE2_ PB12	I O O IO	Y1	**4mA(~SL)** pullup-pe	CIM_D2: CIM data input bit 2 GMAC_TXD6: PHY Transmit Data bit 6 for GMII EPD_SCE2_: EPD source driver chip select 2 PB12: GPIO group B bit 12	VDDIO
CIM0_D3 GMAC_TXD7 EPD_SCE3_ PB13	I O O IO	W1	**4mA(~SL)** pullup-pe	CIM_D3: CIM data input bit 3 GMAC_TXD7: PHY Transmit Data bit 7 for GMII EPD_SCE3_: EPD source driver chip select 3 PB13: GPIO group B bit 13	VDDIO
CIM0_D4	I	N3	**4mA(~SL)**	CIM_D4: CIM data input bit 4	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
GMAC_RXD4 EPD_SCE4_ PB14	O I IO		pullup-pe	GMAC_RXD4: PHY Receive Data bit 4 for GMII EPD_SCE4_: EPD source driver chip select 4 PB14: GPIO group B bit 14	
CIM0_D5 GMAC_RXD5 EPD_SCE5_ PB15	I O I IO	V1	**4mA(~SL)** pullup-pe	CIM_D5: CIM data input bit 5 GMAC_RXD5: PHY Receive Data bit 5 for GMII EPD_SCE5_: EPD source driver chip select 5 PB15: GPIO group B bit 15	VDDIO
CIM0_D6 GMAC_RXD6 EPD_PWR2 PB16	I O I IO	T2	**4mA(~SL)** pulldown-pe	CIM_D6: CIM data input bit 6 GMAC_RXD6: PHY Receive Data bit 6 for GMII EPD_PWR2: EPD power control bit 2 PB16: GPIO group B bit 16	VDDIO
CIM0_D7 GMAC_RXD7 EPD_PWR3 PB17	I O I IO	U1	**4mA(~SL)** pulldown-pe	CIM_D7: CIM data input bit 7 GMAC_RXD7: PHY Receive Data bit 7 for GMII EPD_PWR3: EPD power control bit 3 PB17: GPIO group B bit 17	VDDIO

2.5.6 CIM1/Storage

Table 2-6 CIM1/ Static-Memory Pins (12; all GPIO shared: PG6~17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM1_PCLK PG06	I IO	N2	8mA, pullup-pe	CIM_PCLK: CIM pixel clock input PG06: GPIO group G bit 6	VDDIO
CIM1_HSYN PG07	I IO	P1	8mA, pullup-pe	CIM_HSYN: CIM horizonal sync input PG07: GPIO group G bit 7	VDDIO
CIM1_VSYN PG08	I IO	N1	8mA, pullup-pe, rst-pe	CIM_VSYN: CIM vertical sync input PG08: GPIO group G bit 8	VDDIO
CIM1_MCLK PG09	O IO	M2	8mA, pullup-pe	CIM_MCLK: CIM master clock output PG09: GPIO group G bit 9	VDDIO
CIM1_D0 SD8 PG10	I IO IO	J1	8mA, pulldown-pe	CIM_D0: CIM data input bit 0. When use 8-bit data, use CIM_D0~D7 SD8: Static memory data bus bit 8 PG10: GPIO group G bit 10	VDDIO_ N
CIM1_D1 SD9 PG11	I IO IO	H1	8mA, pulldown-pe	CIM_D1: CIM data input bit 1 SD9: Static memory data bus bit 9 PG11: GPIO group G bit 11	VDDIO_ N
CIM1_D2 SD10 PG12	I IO IO	K1	8mA, pullup-pe	CIM_D2: CIM data input bit 2 SD10: Static memory data bus bit 10 PG12: GPIO group G bit 12	VDDIO_ N
CIM1_D3 SD11 PG13	I IO IO	J2	8mA, pullup-pe	CIM_D3: CIM data input bit 3 SD11: Static memory data bus bit 11 PG13: GPIO group G bit 13	VDDIO_ N
CIM1_D4 SD12 PG14	I IO IO	K2	8mA, pullup-pe	CIM_D4: CIM data input bit 4 SD12: Static memory data bus bit 12 PG14: GPIO group G bit 14	VDDIO_ N
CIM1_D5 SD13 PG15	I IO IO	L1	8mA, pullup-pe	CIM_D5: CIM data input bit 5 SD13: Static memory data bus bit 13 PB15: GPIO group B bit 15	VDDIO_ N
CIM1_D6 SD14 PG16	I IO IO	M1	8mA, pulldown-pe	CIM_D6: CIM data input bit 6 SD14: Static memory data bus bit 14 PG16: GPIO group G bit 16	VDDIO_ N
CIM1_D7 SD15 PG17	I IO IO	L2	8mA, pulldown-pe	CIM_D7: CIM data input bit 7 SD15: Static memory data bus bit 15 PG17: GPIO group G bit 17	VDDIO_ N

2.5.7 UART0

Implementation	Pin/signal used
UART	UART0_TxD, UART0_RxD, UART0_CTS_, UART0_RTS_

Table 2-7 UART0/I2S Pins (4; all GPIO shared: PF0~3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RxD BCLK PF00	I IO IO	T14	8mA, pullup-pe	UART0_RxD: UART 0 Receiving data I2S unified or DAC bit clock PF00: GPIO group F bit 0	VDDIO
UART0_CTS_ LRCLK PF01	I IO IO	T15	2/4mA, pullup-pe,	UART0_CTS_: UART 0 CTS_ input LRCLK: I2S unified or DAC Left/Right clock PF01: GPIO group F bit 1	VDDIO
UART0_RTS_ SDATI PF02	O I IO	T17	2/4mA, pullup-pe,	UART0_RTS_: UART 0 RTS_ output SDATI: I2S serial data input PF02: GPIO group F bit 2	VDDIO
UART0_TxD SDATO PF03	O O IO	R16	2/4mA, pullup-pe,	UART0_TxD: UART 0 transmitting data SDATI: I2S serial data output PF03: GPIO group F bit 3	VDDIO

2.5.8 UART1(DEBUG)

Table 2-8 UART1/GMAC Pins (4; all GPIO shared: PD26~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART1_RxD GMAC_RXD2 PD26	I I IO	V3	**4mA(~SL)** pullup-pe	UART1_RxD: UART 1 Receiving data GMAC_RXD2: Ethernet receive data bit 2 for MII、RGMII and GMII PD26: GPIO group D bit 26	VDDIO
UART1_CTS_ GMAC_RXD3 PD27	I I IO	U3	**4mA(~SL)** pullup-pe	UART1_CTS_: UART 1 CTS_ input GMAC_RXD3: Ethernet receive data bit 3 for MII、RGMII and GMII PD27: GPIO group D bit 27	VDDIO
UART1_TxD GMAC_TXD2 PD28	O O IO	T3	**4mA(~SL)** pullup-pe, rst-pe	UART1_TxD: UART 1 transmitting data GMAC_TXD2: Ethernet transmit data bit 2 for MII、RGMII and GMII PD28: GPIO group D bit 28	VDDIO
UART1_RTS_ GMAC_TXD3 PD29	O O IO	P3	**4mA(~SL)** pullup-pe, **rst-pe**	UART1_RTS_: UART 1 RTS_ output GMAC_TXD3: Ethernet transmit data bit 3 for MII、RGMII and GMII PD29: GPIO group D bit 29	VDDIO

2.5.9 System/JTAG/UART3(DEBUG Used)

Table 2-9 JTAG/UART3/PS2 Pins (5, GPIO PA30~31 are used to control)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST_	I	P5	Schmitt, pull-down **rst-pe**	TRST_: JTAG reset	VDDIO
TCK UART3_RTS_ PS2_MCLK	I O	N6	8mA, Schmitt, pulldown-pe, **rst-pe**	TCK: JTAG clock UART3_RTS_: UART 3 RTS_ output	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TMS UART3_CTS_ PS2_MDATA	I I	P6	8mA, Schmitt, pullup-pe, **rst-pe**	TMS: JTAG mode select UART3_CTS_: UART 3 CTS_ input	VDDIO
TDI UART3_RxD PS2_KCLK	I I	R5	8mA, Schmitt, pullup-pe, **rst-pe**	TDI: JTAG serial data input UART3_RxD: UART 3 Receiving data	VDDIO
TDO UART3_TxD PS2_KDATA	O O	R6	8mA, Schmitt, pullup-pe, **rst-pe**	TDO: JTAG serial data output UART3_TxD: UART 3 transmitting data	VDDIO

2.5.10 SMB0/1

Table 2-10 SMB0/SMB1 Pins (4; all GPIO shared: PD30~31, PE30~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SMB0_SDA PD30	IO IO	T5	8mA, pullup-pe	SMB0_SDA: SMB 0 serial data PD30: GPIO group D bit 30	VDDIO
SMB0_SCK PD31	IO IO	T7	8mA, pullup-pe	SMB0_SCK: SMB 0 serial clock PD31: GPIO group D bit 31	VDDIO
SMB1_SDA PE30	IO IO	U6	8mA, pullup-pe	SMB1_SDA: SMB 1 serial data PE30: GPIO group E bit 30	VDDIO
SMB1_SCK PE31	IO IO	U7	8mA, pullup-pe	SMB1_SCK: SMB 1 serial clock PE31: GPIO group E bit 31	VDDIO

2.5.11 MSC1

Implementation	Pin/signal used
SDIO	MSC1_D0~MSC1_D3, MSC1_CLK, MSC1_CMD
SPI	SSI_CLK, SSI_DT, SSI_DR, SSI_CE0_, SSI_CE1_

Table 2-11 MSC1/SSI0, Pins (6; all GPIO shared: PD20~25)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC1_D0 SSI0_DR PD20	IO I IO	Y6	8mA, pullup-pe	MSC1_D0: MSC (MMC/SD) 1 data bit 0 SSI0_DR: SSI 0 data input PD20: GPIO group D bit 20	VDDIO
MSC1_D1 SSI0_DT PD21	IO O IO	AA6	8mA, pullup-pe	MSC1_D1: MSC (MMC/SD) 1 data bit 1 SSI0_DT: SSI 0 data output PD21: GPIO group D bit 21	VDDIO
MSC1_D2 SSI0_GPC PD22	IO O IO	AA7	8mA, pullup-pe	MSC1_D2: MSC (MMC/SD) 1 data bit 2 SSI0_GPC: SSI 0 general-purpose control signal PD22: GPIO group D bit 22	VDDIO
MSC1_D3 SSI0_CE1_ PD23	IO O IO	W6	8mA, pullup-pe, **rst-pe**	MSC1_D3: MSC (MMC/SD) 1 data bit 3 SSI0_CE1_: SSI 0 chip enable 1 PD23: GPIO group D bit 23	VDDIO
MSC1_CLK SSI0_CLK	O O	AA8	8mA, pullup-pe	MSC1_CLK: MSC (MMC/SD) 1 clock output SSI0_CLK: SSI 0 clock output	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PD24	IO			PD24: GPIO group D bit 24	
MSC1_CMD SSI0_CE0_ PD25	IO O IO	Y7	8mA, pullup-pe, **rst-pe**	MSC1_CMD: MSC (MMC/SD) 1 command SSI0_CE0_: SSI 0 chip enable 0 PD25: GPIO group D bit 25	VDDIO

2.5.12 MSC2

Implementation	Pin/signal used
SDIO	MSC2_D0~MSC2_D4, MSC2_CLK, MSC2_CMD

Table 2-12 MSC2 Pins (6; all GPIO shared: PB20~21,PB28~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC2_D0 PB20	IO IO	Y8	8mA, pullup-pe	MSC2_D0: MSC (MMC/SD) 2 data bit 0 PB20: GPIO group B bit 20	VDDIO
MSC2_D1 PB21	IO IO	W8	8mA, pullup-pe	MSC2_D1: MSC (MMC/SD) 2 data bit 1 PB21: GPIO group B bit 21	VDDIO
MSC2_CLK PB28	O IO	AA10	8mA, pullup-pe	MSC2_CLK: MSC (MMC/SD) 2 clock output PB28: GPIO group B bit 28	VDDIO
MSC2_CMD PB29	O IO	W9	8mA, pullup-pe, **rst-pe**	MSC2_CMD: MSC (MMC/SD) 2 command PB29: GPIO group B bit 29	VDDIO
MSC2_D2 PB30	IO IO	AA9	8mA, pullup-pe	MSC2_D2: MSC (MMC/SD) 2 data bit 2 PB30: GPIO group B bit 30	VDDIO
MSC2_D3 PB31	IO IO	Y9	8mA, pullup-pe, **rst-pe**	MSC2_D3: MSC (MMC/SD) 2 data bit 3 PB31: GPIO group B bit 31	VDDIO

2.5.13 MSCx

Table 2-13 MSCx (6; all GPIO shared: PE20~23, PE28~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_CLK MSC1_CLK MSC2_CLK PE28	O O O IO	R21	4/8mA, pullup-pe	MSC0_CLK: MSC (MMC/SD) 0 clock output MSC1_CLK: MSC (MMC/SD) 1 clock output MSC2_CLK: MSC (MMC/SD) 2 clock output PE28: GPIO group E bit 28	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_CMD MSC1_CMD MSC2_CMD PE29	O O O IO	R20	8mA, pullup-pe	MSC0_CMD: MSC (MMC/SD) 0 command MSC1_CMD: MSC (MMC/SD) 1 command MSC2_CMD: MSC (MMC/SD) 2 command PE29: GPIO group E bit 29	VDDIO
MSC0_D0 MSC1_D0 MSC2_D0 PE20	IO IO IO IO	U19	4/8mA, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 MSC1_D0: MSC (MMC/SD) 1 data bit 0 MSC2_D0: MSC (MMC/SD) 2 data bit 0 PE20: GPIO group E bit 20	VDDIO
MSC0_D1 MSC1_D1 MSC2_D1 PE21	IO IO IO IO	T19	4/8mA, pullup-pe	MSC0_D1: MSC (MMC/SD) 0 data bit 1 MSC1_D1: MSC (MMC/SD) 1 data bit 1 MSC2_D1: MSC (MMC/SD) 2 data bit 1 PE21: GPIO group E bit 21	VDDIO
MSC0_D2 MSC1_D2 MSC2_D2 PE22	IO IO IO IO	T20	4/8mA, pullup-pe	MSC0_D2: MSC (MMC/SD) 0 data bit 2 MSC1_D2: MSC (MMC/SD) 1 data bit 2 MSC2_D2: MSC (MMC/SD) 2 data bit 2 PE22: GPIO group E bit 22	VDDIO
MSC0_D3 MSC1_D3 MSC2_D3 PE23	IO IO IO IO	T21	4/8mA, pullup-pe	MSC0_D3: MSC (MMC/SD) 0 data bit 3 MSC1_D3: MSC (MMC/SD) 1 data bit 3 MSC2_D3: MSC (MMC/SD) 2 data bit 3 PE23: GPIO group E bit 23	VDDIO

2.5.14 PWM/SMB2

Table 2-14 PWM/AIC/UART3 Pins (4; all GPIO shared: PE0~3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 SMB2_SDA PE00	IO IO	R17	8mA, **pullup-pe**	PWM0: PWM output or pulse input 0 SMB2_SDA: SMB 2 serial data PE00: GPIO group E bit 0. Pull-down not enabled at and after reset	VDDIO
PWM1 PE01	O IO	M17	8mA, pulldown-pe	PWM1: PWM 1 output. This PWM can run in sleep mode in RTCLK clock PE01: GPIO group E bit 1. Pull-down not enabled at and after reset	VDDIO
PWM2 PE02	O IO	M19	8mA, pullup-pe	PWM2: PWM 2 output. This PWM can run in sleep mode in RTCLK clock PE02: GPIO group E bit 2. Pull-up not enabled at and after reset	VDDIO
PWM3 SMB2_SCK SYSCLK PE03	IO O O IO	P16	8mA, pullup-pe, **rst-pe**	PWM3: PWM output or pulse input 3 SMB2_CLK: SMB 2 serial clock SYSCLK: I2S system clock output PE03: GPIO group E bit 5	VDDIO

Table 2-15 System Pins (3, all GPIO shared: PD17~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PD17 (BOOT_SEL0)	IO I	T9	8mA, pullup-pe	PD17: GPIO group D bit 17 It is taken as BOOT select bit 0 by Boot ROM code	VDDIO
PD18 (BOOT_SEL1)	IO I	U8	8mA, pullup-pe	PD18: GPIO group D bit 18 It is taken as BOOT select bit 1 by Boot ROM code	VDDIO
PD19 (BOOT_SEL2)	IO I	U10	8mA, pullup-pe	PD19: GPIO group D bit 19 It is taken as BOOT select bit 2 by Boot ROM code	VDDIO

Table 2-16 USB OTG Digital Pins (1, all GPIO shared: PE10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DRV_VBUS PE10	O IO	T8	8mA, pulldown-pe, **rst-pe**	DRVVBUS: USB OTG VBUS driver control signal PE10: GPIO group E bit 10	VDDIO

Table 2-17 EXCLK output Pins (1, all GPIO shared: PD15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLKO_ PD15	O IO	Y10	8mA, pulldown-pe, **rst-pe**	EXCLKO_: output external clock PD15: GPIO group D bit 15	VDDIO

2.5.15 Digital power/ground

Table 2-18 IO/Core power supplies for FBGAs (51)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDQ	P	J8 J10 J13 H8 H10 H13 H14 F8 F10 F14		VDDQ: IO digital power for DRAM, 1.8V~3.3V	-
VSSQ	P	J9 J11 J12 J14 H9 F9 E7 H12 F12 G16		VSSQ: IO digital ground for DRAM, 0V	-
VDDIO_N	P	K8 M8		VDDIO_N: IO digital power for NAND power domain, 1.8V~3.3V	-
VDDIO	P	P9 P10 P12 P13		VDDIO: IO digital power for none DRAM/NAND, 3.3V	-
VSS	P	K9 K10 K13 K14 L13 M14 N8 N9 N10 N11 N12 N13 N14 P8 P14		VSS: IO digital gound for none DRAM and CORE digital ground, 0V	-
VDD	P	K11 K12 L9 L10 L12 M9 M10 M11 M12 M13		VDD: CORE digital power, 1.2V	-

2.5.16 Analog

Table 2-19 Audio CODEC Pins (19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MICP1	AI	V20		Microphone mono differential analog input 1 (MIC1), positive pin.	AVDCD C25
MICN1	AI	V21		Microphone mono differential analog input 1 (MIC1), negative pin.	AVDCD C25

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MICP2	AI	Y21		Microphone mono differential analog input 2 (MIC2), positive pin.	AVDCDC25
MICN2	AI	Y20		Microphone mono differential analog input 2 (MIC2), negative pin.	AVDCDC25
MICBIAS	AO	W20		Microphone bias.	AVDCDC25
AIL	AI	U21		Left line single-ended analog input.	AVDCDC25
AIR	AI	U20		Right line single-ended analog input.	AVDCDC25
AOLOP	AO	AA17		Differential line output, positive pin.	AVDCDC25
AOLON	AO	Y17		Differential line output, negative pin.	AVDCDC25
AOHPL	AO	Y19		Left headphone single-ended analog output.	AVDHP
AOHPR	AO	AA19		Right headphone single-ended analog output.	AVDHP
AOHPM	AO	Y18		Headphone common mode output.	AVDHP
AOHPMS	AI	AA18		Headphone common mode sense input.	AVDHP
VCAP	AO	AA21		Voltage Reference Output. An 10μF ceramic or tantalum capacitor in parallel with a 0.1μF ceramic capacitor attached from this pin to AVSCDC eliminates the effects of high frequency noise.	AVDCDC25
AVDHP25	P	AA20		Headphone amplifier power, 2.5V.	-
AVSHP	P	W18		Headphone amplifier ground.	-
AVDCDC25	P	W21		CODEC analog power, 2.5V, inter signal VREFP.	-
AVSCDC	P	V19		CODEC analog ground, inter signal VREFN.	-
HPSENSE	AI	U16		Headphone jack sense.	AVDHP

Table 2-20 USB 2.0 OTG, USB 1.1 host (10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
OTG_DP	AIO	Y16		OTG_DP: USB OTG data plus	UHC_AVDD
OTG_DM	AIO	AA16		OTG_DM: USB OTG data minus	UHC_AVDD
VBUS	AIO	T13		VBUS: USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin	5V
ID	AI	U15		ID: USB mini-receptacle identifier. It differentiates a mini-A from a mini-B plug. If this signal is not used, internal resistance pulls the signal's voltage level to AVDOTG25.	AVDOTG25
TXR_RKL	AIO	U14		TXR_RKL: Transmitter resister tune. It connects to an external resistor of 43.2Ω with 1% tolerance to analog ground, that adjusts the USB 2.0 high-speed source impedance	AVDOTG25
UHC_DP1	AIO	AA14		UHC_DP1: USB 1.1 host data plus	UHC_AVDD
UHC_DM1	AIO	Y14		UHC_DM1: USB 1.1 host data minus	UHC_AVDD
UHC_AVDD	P	W14		UHC_AVDD: USB analog power.3.3V	-
UHC_AVSS	P	W17		UHC_AVSS: USB analog ground.	
AVDOTG25	P	W16		AVDOTG25: USB OTG analog power, 2.5V	-

Table 2-21 SAR ADC Pins (9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_XP	AIO	N19		ADC_XP: Touch screen input, X+ for 4-wire, bottom-right for 5-wire	AVDADC
ADC_XM	AIO	N20		ADC_XM: Touch screen input, X- for 4-wire, top-left for 5-wire	AVDADC
ADC_YP	AIO	N21		ADC_YP: Touch screen input Y+ for 4-wire, top-right for 5-wire	AVDADC
ADC_YM	AIO	P20		ADC_YM: Touch screen input Y- for 4-wire, bottom-left for 5-wire	AVDADC
ADC_AUX1	AI	P19		ADC_AUX1: ADC general purpose input	AVDADC
ADC_AUX2	AI	P17		ADC_AUX2: Top sheet connection for 5-wire touch screen or ADC general purpose input	AVDADC
ADC_VBAT	AI	P21		ADC_VBAT: Battery voltage input with external resistance divider or ADC general purpose input	AVDADC
AVDADC	P	N17		AVDADC: ADC analog power, 3.3 V	-
AVSADC	P	M16		AVSADC: ADC analog ground	-

Table 2-22 EFUSE Pins for Two EFUSE (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AVDEFUSE	P	N16		AVDEFUSE: EFUSE programming power, 0V/2.5V	AVDADC

Table 2-23 CPM Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK	AI	AA15	2~30 MHz Oscillator, OSC on/off	EXCLK: OSC input.	VDDIO
EXCLKO	AO	Y15		EXCLKO: OSC output.	VDDIO
PLLDVDD	P	AA13		PLLDVDD:PLL digital power, 1.2V	-
PLLDVSS	P	W12		PLLDVSS:PLL digital ground	-
PLLAVDD	P	Y13		PLLAVDD: PLL analog power, 1.2V	-
PLLAVSS	P	W13		PLLAVSS: PLL analog ground	-

Table 2-24 RTC Pins (10, 2 with GPIO input: PA30, PD14)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	AA12	32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
XRTCLK	AO	Y12		XRTCLK: OSC output or 32768Hz clock input	VDD_{RTC}
PWRON	O	U13	8mA	PWRON: Power on/off control of main power	VDD_{RTC}
CLK32K PD14	O IO	AA11	8mA, pullup-pe	CLK32K: 32768Hz clock output PD14: GPIO group D bit 14. When main power down, this pin is controlled by RTC register: CLK32K or PD14, pull-up enable/disable, input/output if it is PD14, 0/1 if it is PD14 output	VDD_{RTC}
WKUP PA30	I I	U9	Schmitt	WKUP: Wakeup signal after main power down PA30: GPIO group A bit 30, input/interrupt only	VDD_{RTC}

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PPRST_	I	T12	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
TEST_TE	I	T10	Schmitt, pull-down	TEST_TE: Manufacture test enable, program readable	VDD_{RTC}
VDDRTC	P	W10		VDDRTC: power for RTC and hibernating mode controlling that never power down	-
VSSRTC	P	U12		VSSRTC:	
LDOOUT	AIO	Y11		LDOOUT: capacitor pin for RTC LDO need a 1nF decoupling capacitor to ground	

2.5.17 Summary

BGA314 14mm x 14mm x 1.4mm, 0.65 pitch, 21 x 21 matrix

Blocks	Pin Number			Notes
	BGA8	mA	GPIO	
DRAM	76		-	Include VREFmem
Boot & storage: Static/NAND /MSC0/SPI0	24	8	PA0~7, PA16~29, PB0~5	
LCDC/EPD/UART2	28	8	PC0~27	PCLK 8mA
MAC/SPI/UART/EPD	12	8	PF4~15	GMAC-TXD0~1 4mA
CIM0/EPD	12	8		
CIM1/SRAM8~15	12	8		
MSC1/SPI0,1	6	8	PD20~25	
MSC2/SPI0,1	6	8	PB20~21 PB28~31	
MSC0/MSC1/MSC2	6	8	PE20~23, PE28~29	
SMB0/SMB1	4	8	PD30~31, PE30~31	
UART0	4	8	PF0~3	
UART1	4	8	PD26~29	
UART3/JTAG	5			
PWM/SMB	4	8	PE0~3	
BOOT_SEL	3	8	D17~19	
OTG DRVVBUS	1	8	PE10	
EXCLK_O	1	8	PD15	EXCLK output pin
CODEC	19		-	
USB OTG + USB 2.0 host	10		-	
ADC	9		-	
EFUSE	1		-	
OSC12M + PLL			-	

RTC	10		PA30, PD14	PA30 is only input/int
Core power(VDD)	10			
Ground for core/IO	15			
IO power/ground for DRAM	20		-	
IO power for NAND	2		-	
IO P/G for PLL0/1(digital)	2		-	
IO P/G for PLL0/1(analog)	2		-	
IO power for other none DRAM	4		-	IO 3.3 (mainly LCD and others)
EXCLK	1			
EXCLKO	1			
NC	0			
SUM	**314**			

NOTES:

1 The meaning of phases in IO cell characteristics are:
   a Bi-dir, Single-end: bi-direction and single-ended DDR IO are used.
   b Output, Single-end: output and single-ended DDR IO are used.
   c Output, Differential: output and differential signal DDR IO are used.
   d Bi-dir, Differential: bi-direction and differential signal DDR IO are used.
   e 4mA,8mA,16mA out: The IO cell's output driving strength is about 4mA,8mA,16mA.
   4/8mA means the IO cell's output driving strength is selected, can be set as 4mA or 8mA.
   2/4mA means the IO cell's output driving strength is selected, can be set as 2mA or 4mA.
   f Pull-up: The IO cell contains a pull-up resistor.
   g Pull-down: The IO cell contains a pull-down resistor.
   h Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
   i Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.
   j rst-pe: these pins are initialed (during reset and after reset) to IO internal pull (up or down) enabled. Otherwise, the pins are initialed to pull disabled
   k Schmitt: The IO cell is Schmitt trig input.
   l ~SL: The IO cell do not limited slew rate.
2 All GPIO shared pins are reset to GPIO input

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDQ power supplies voltage	-0.5	1.98	V
VDDIO power supplies voltage	-0.5	3.6	V
VDDIO_N power supplies voltage	-0.5	3.6	V
VDDcore power supplies voltage	-0.2	1.32	V
AVDPLL power supplies voltage	-0.2	1.32	V
AVDEFUSE power supplies voltage	-0.5	2.75	V
VDDRTC power supplies voltage	-0.5	3.63	V
AVDOTG25 power supplies voltage	-0.5	2.75	V
UHC_AVDD power supplies voltage	-0.5	3.63	V
AVDADC power supplies voltage	-0.5	3.63	V
AVDCDC25 power supplies voltage	-0.5	2.75	V
Input voltage to VDDQ supplied non-supply pins	-0.3	1.98	V
Input voltage to VDDIO supplied non-supply pins with 5V tolerance	-0.5	6.0	V
Input voltage to VDDIO supplied non-supply pins without 5V tolerance	-0.5	3.6	V
Input voltage to VDDIO_N supplied non-supply pins	-0.5	3.6	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	3.6	V
Input voltage to AVDCDC25 supplied non-supply pins	-0.5	2.75	V
Input voltage to AVDOTG25 supplied non-supply pins	-0.5	2.75	V
Input voltage to UHC_AVDD supplied non-supply pins	-0.5	3.63	V
Input voltage to AVDADC supplied non-supply pins	-0.5	3.63	V
Output voltage from VDDQ supplied non-supply pins	-0.5	1.98	V
Output voltage from VDDIO supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDIO_N supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDOTG25 supplied non-supply pins	-0.5	2.75	V
Output voltage from UHC_AVDD supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDADC supplied non-supply pins	-0.5	2.75	V
Output voltage from AVDCDC25 supplied non-supply pins	-0.5	2.75	V
Maximum ESD stress voltage, Human Body Model; Any pin to any		2000	V

supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.			

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VMEM	VDDQ voltage for LPDDR	1.65	1.8	1.95	V
	VDDQ voltage for SSTL18 (DDR2)	1.7	1.8	1.9	V
	VDDQ voltage for DDR3	1.425	1.5	1.575	V
	VDDQ voltage for DDR3L	1.28	1.35	1.45	V
VIO	VDDIO voltage	1.62	-	3.6	V
VION	VDDIO_N voltage	1.62	-	3.6	V
VCORE	VDDcore voltage	1.08	1.2	1.32	V
VPLL	AVDPLL analog voltage	1.08	1.2	1.32	V
VEFUSE	AVDEFUSE voltage	2.25	2.5	2.75	V
VRTC	VDDRTC voltage	1.8	1.8	3.63	V
VUSB25	AVDOTG25 voltage	2.25	2.5	2.75	V
VUSB33	UHC_AVDD voltage	3.0	3.3	3.6	V
VADC	AVDADC voltage	3.0	3.3	3.6	V
VCDC	AVDCDC25 voltage	2.25	2.5	2.75	V

Table 3-3 Recommended operating conditions for VDDQ supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
VI18	Input voltage for DDR2/LPDDR applications	0		1.9	V
VO18	Output voltage for DDR2/LPDDR applications	0		1.9	V
VI15	Input voltage for DDR3 application	0		1.575	V
VO15	Output voltage for DDR3 application	0		1.575	V
VI135	Input voltage for DDR3L application	0		1.45	V
VO135	Output voltage for DDR3L application	0		1.45	V

Table 3-4 Recommended operating conditions for VDDIO/VDDIO_N/VDDRTC supplied pins

Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Unit**
V_{IH18}	Input high voltage for 1.8V I/O application	1.17		3.6	V
V_{IL18}	Input low voltage for 1.8V I/O application	–0.3		0.63	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7		3.6	V
V_{IL25}	Input low voltage for 2.5V I/O application	–0.3		0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2		3.6	V
V_{IL33}	Input low voltage for 3.3V I/O application	–0.3		0.8	V

Table 3-5 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	–20		85	°C

Table 3-6 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
Vbat	VBAT input voltage range	0		1.15	V
V_{IADC}	ADC_XP/ADC_XM/ADC_YP/ADC_YM/ADC_AUX1/ADC_AUX2 input voltage range	0		AVDADC	V

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-7 DC characteristics for V_{REFMEM} and V_{TT}

Symbol	Parameter	Min	Typical	Max	Unit
VREFM	Reference voltage supply	0.49	0.5	0.51	VMEM
VTT	Terminal Voltage	VREFM – 0.4	VREFM	VREFM + 0.4	V

Table 3-8 DC characteristics for VDDQ supplied pins in DDR3 application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	VREFMEM + 0.1		VMEM	V
VIL(DC)	DC input voltage Low	-0.3		VMEM -0.1	V
VOH	DC output logic High	0.8 * VMEM			V
VOL	DC output logic LOW			0.2 * VMEM	V
RTT	Input termination resistance (ODT) to VMEM/2	100 54 36	120 60 40	140 66 44	Ω
IOHL(DC)	PAD pin, 34Ω Output source/sink DC current, RTT=120		5.07	5.48	mA
IOHL(DC)	PAD pin, 34Ω Output source/sink DC current, RTT=60		8.45	9.28	mA
IOHL(DC)	PAD pin, 34Ω Output source/sink DC current,		10.80	11.97	mA

	RTT=40				
IOHL(DC)	PAD pin, 50Ω Output source/sink DC current, RTT=120		4.53	5.13	mA
IOHL(DC)	PAD pin, 50Ω Output source/sink DC current, RTT=60		6.97	8.24	mA
IOHL(DC)	PAD pin, 50Ω Output source/sink DC current, RTT=40		8.42	10.21	mA
IMEM	VMEM standby current; ODT OFF		0.02	14.47	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		9.49	10.68	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.74	1.31	mA
IMEM	Input Low ODT/Drv=60/34, IMEM DC current		6.51	7.65	mA
IMEM	Input High ODT/Drv=60/34, IMEM DC current		12.45	15.31	mA
ILS	Input leakage current, SSTL mode, unterminated		0.02	5.06	uA

Table 3-9 DC characteristics for VDDQ supplied pins in DDR3L application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	VREF + 0.09		VMEM	V
VIL(DC)	DC input voltage Low	-0.3		VREF -0.09	V
VOH	DC output logic High	0.8 * VMEM			V
VOL	DC output logic Low			0.2 * VMEM	V
RTT	Input termination resistance (ODT) to VMEM/2	100 54 36	120 60 40	140 66 44	ohm
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=120		4.55	4.99	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=60		7.58	8.36	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=40		9.66	10.70	mA

IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=120		4.17	4.65	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=60		6.50	7.37	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=40		7.93	9.05	mA
IMEM	VMEM standby current; ODT OFF		0.02	13.48	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		8.25	9.40	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.48	1.02	mA
IMEM	Input Low ODT/Drv=60/34, IMEM DC current		5.41	6.35	mA
IMEM	Input High ODT/Drv=60/34, IMEM DC current		11.29	13.28	mA
ILS	Input leakage current, SSTL mode, unterminated		0.01	4.80	uA

Table 3-10 DC characteristics for VDDQ supplied pins in LPDDR application

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IH(DC)}$	Input logic threshold High	0.7* VMEM		VMEM+0.3	V
$V_{IL(DC)}$	Input logic threshold Low	VMEM-0.3		0.3* VMEM	V
VIH(AC)	AC Input logic High	0.8* VMEM		VMEM+0.3	V
VIL(AC)	AC Input logic Low	VMEM-0.3		0.2* VMEM	V
VOH	DC output logic High (IOH=-0.1mA)	0.9*VMEM			V
VOL	DC output logic Low (IOL=0.1mA)			0.1 *VMEM	V
ILL	Input leakage current		0.01	6.45	uA
IMEM	VMEM quiescent current		0.02	15.03	uA

Table 3-11 DC characteristics for VDDIO/VDDIO_N/VDDRTC supplied pins for 1.8V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	0.79	0.86	0.94	V
V_{T+}	Schmitt trig low to high threshold point	0.95	1.06	1.16	V
V_{T-}	Schmitt trig high to low threshold point	0.58	0.69	0.79	V

V_{TPU}	Threshold point with pull-up resistor enabled		0.79	0.86	0.94	V
V_{TPD}	Threshold point with pull-down resistor enabled		0.79	0.86	0.94	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.95	1.06	1.16	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.58	0.68	0.78	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.96	1.07	1.17	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.59	0.69	0.79	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		66	114	211	kΩ
R_{PD}	Pull-down Resistor		58	103	204	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	5.3	9.8	15.8	mA
		16mA	10.8	19.7	31.8	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	3.3	8.3	16.6	mA
		16mA	6.6	16.5	33.2	mA

Table 3-12 DC characteristics for VDDIO/VDDIO_N/VDDRTC supplied pins for 2.5V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.06	1.17	1.27	V
V_{T+}	Schmitt trig low to high threshold point	1.27	1.40	1.50	V
V_{T-}	Schmitt trig high to low threshold point	0.86	0.98	1.09	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.05	1.16	1.25	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.06	1.17	1.27	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.27	1.39	1.48	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	0.85	0.97	1.08	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.27	1.41	1.50	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	0.88	0.99	1.10	V
I_L	Input Leakage Current @ V_I=1.8V or 0V			±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V			±10	μA
R_{PU}	Pull-up Resistor	43	69	120	kΩ
R_{PD}	Pull-down Resistor	41	66	124	kΩ
V_{OL}	Output low voltage			0.7	V

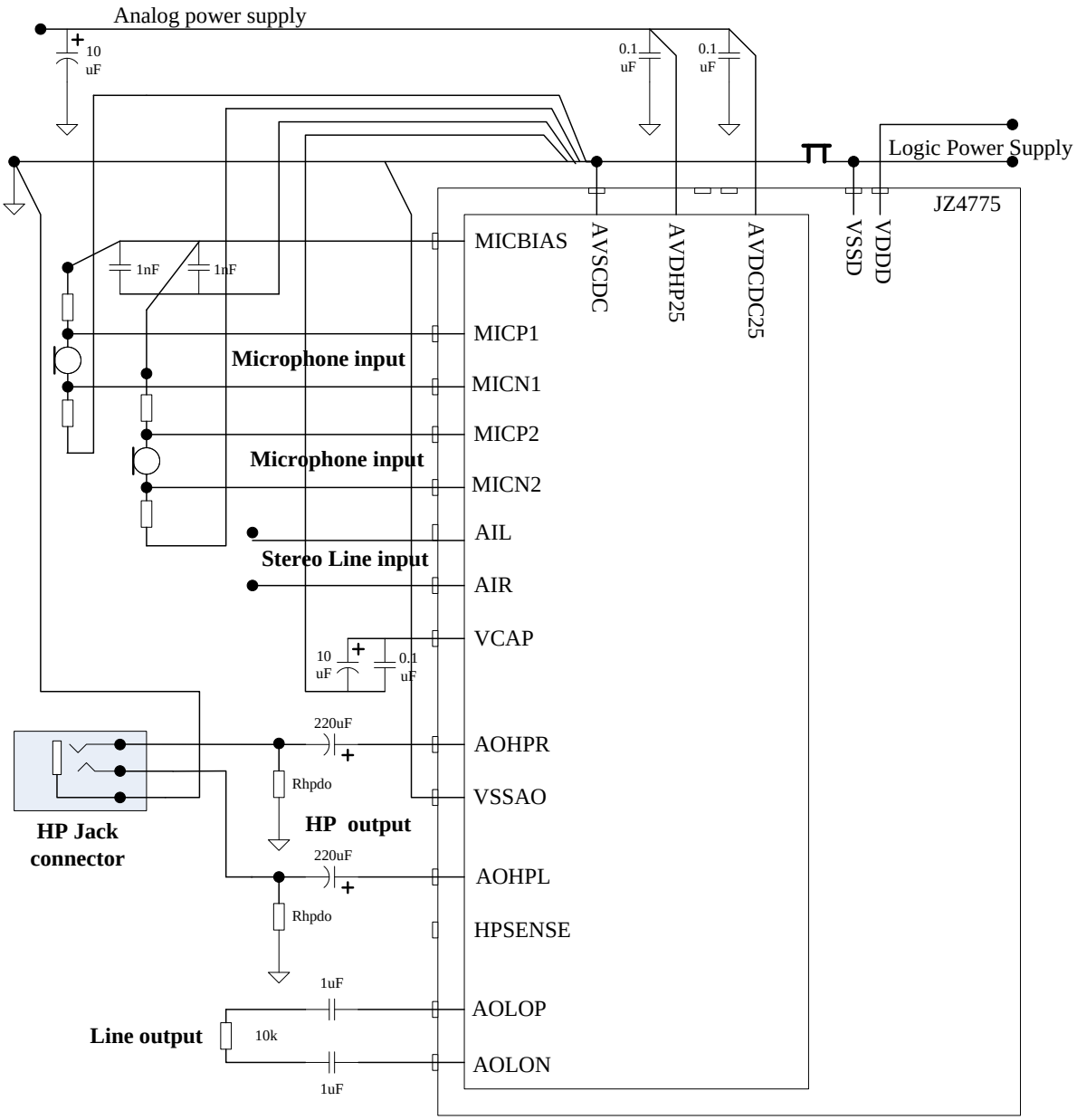
V_{OH}	Output high voltage		1.7			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	11.6	19.4	28.4	mA
		16mA	23.3	39.1	57.2	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	9.3	19.4	34.6	mA
		16mA	18.6	38.7	69.2	mA

Table 3-13 DC characteristics for VDDIO/VDDIO_N/VDDRTC supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.39	1.50	1.65	V
V_{T+}	Schmitt trig low to high threshold point		1.62	1.75	1.90	V
V_{T-}	Schmitt trig high to low threshold point		1.18	1.29	1.44	V
V_{TPU}	Threshold point with pull-up resistor enabled		1.36	1.48	1.64	V
V_{TPD}	Threshold point with pull-down resistor enabled		1.40	1.52	1.66	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.62	1.75	1.89	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		1.16	1.28	1.43	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.64	1.77	1.91	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		1.19	1.31	1.45	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		34	51	81	kΩ
R_{PD}	Pull-down Resistor		35	51	88	kΩ
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		2.4			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	10.0	15.2	20.2	mA
		16mA	20.2	30.6	40.6	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	13.9	28.0	48.2	mA
		16mA	27.8	56.0	96.3	mA

3.4 Audio codec

3.4.1 Application schematic



Note: 1. The Rhpdo value is 470 Ohm, it use to prevent pop-up noise.

2. AVDCDC25 / AVDHP25 / VCAP each of them requires connecting decoupling capacitors (0.1uF) between the pads AVDCDC25 / AVDHP25 / VCAP and AVSCDC. This ceramic capacitor has to be kept as close as possible to IC package (closer than 0.2 inch)

3.4.2 Line input to audio ADC path

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GIDL, GIDR = 0dB (note 1)	1.89	2.12	2.39	Vpp
Input resistance		8.5			kOhm
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF

NOTE: The Full Scale input voltage scales with AVDCDC25, equals to 0.85*VREF (typ).

3.4.3 Microphone input to audio ADC path

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GIDL, GIDR = 0dB, boost gain GIM1,GIM2 = 20dB (note 1)	0.189	0.212	0.239	Vpp
Input resistance (Differential mic configuration)	Boost gain GIM1,GIM2 = 0 dB	66	80	100	kOhm
	Boost gain GIM1,GIM2 = 20 dB	10	13	15	
Input resistance (single-ended mic configuration)	Boost gain GIM1,GIM2 = 0 dB	92	115	138	kOhm
	Boost gain GIM1,GIM2 = 20 dB	19	24	29	
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF

NOTE: The Full Scale input voltage scales with AVDCDC25, equals to 0.085*VREF (typ).

3.4.4 Audio DAC to headphone output path

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96 kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
DAC playback on 16 Ohm HeadPhone					
Output level	Full Scale, Gain GOL, GOR = -3 dB, GODL, GODR=0dB, 16 Ohm load	1.33	1.5	1.69	Vpp
Maximum output power	Rl = 16 Ohm		17.6		mW
Output resistance	R1	16			Ohm
Output bypass capacitor	Cl (Rl = 16 Ohm)			220	uF
DAC playback to 10k Ohms lineout single					
Output level	Full Scale, Gain GOL, GOR = 0 dB, GODL, GODR=0dB (note 1)	1.89	2.12	2.39	Vpp
Output resistance	R1	10k			Ohm
Output bypass capacitor	Cl (Rl = 10 kOhm)			1	uF
Common characteristics					
Output capacitance (note 2)	Cp			200	pF

NOTES:

1 The Full Scale output voltage scales with AVDCDC25, equals to 0.85*VREF. The minimum and maximum output levels are given with gain accuracy.

2 Output may oscillate above specified load capacitances. The capacitance is equivalent to a 2-meter cable.

3.4.5 Audio DAC to mono line output path

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Output level	Full Scale, Gain GODL, GODR = 0dB (note 1)	3.78	4.25	4.78	Vpp
Output resistance		10			kOhm
Output capacitance	Cp			100	pF
Output bypass capacitor	Cl (Rl = 10 kOhm)			1	uF

NOTE: The Full Scale output voltage scales with AVDCDC25, equals to 1.7*VREF (typ).

3.4.6 Line input to headphone output path (analog bypass)

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96 kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale	1.89	2.12	2.39	Vpp
Input resistance		8.5			kOhm
bypass on 16 Ohm HeadPhone					
Output level	Full Scale, Gain GOL, GOR = -3 dB, GIL, GIR=0dB, 16 Ohm load	1.33	1.5	1.69	Vpp
Output resistance	R1	16			Ohm
bypass to 10k Ohms lineout single					
Output level	Full Scale, Gain GOL, GOR = 0 dB, GIL, GIR=0 dB (note 1)	1.89	2.12	2.39	Vpp
Common characteristics					
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF

NOTE: The Full Scale output voltage scales with AVDCDC25, equals to 1.7*VREF (typ).

3.4.7 Microphone input to headphone output path (analog sidetone)

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GOL, GOR = 0dB, boost gain GIM1,GIM2 = 20dB (note 1)	0.189	0.212	0.239	Vpp
Output level	Full Scale, Gain GOL,GOR= 0dB, boost gain GIM1,GIM2 = 0 to 20dB, 10kOhm load (note 2)	1.89	2.12	2.39	Vpp
	Full Scale, Gain GOL,GOR= -3 dB, boost gain GIM1,GIM2 = 0 to 20dB, 16Ohm load (note 2)	1.33	1.5	1.69	Vpp

NOTES:

1 The Full Scale input voltage scales with AVDCDC25, equals to 0.085*VREF (typ).

2 The Full Scale output voltage scales with AVDCDC25, equals to 0.85*VREF (typ).

3.4.8 Micbias and reference

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Micbias output level	(note 1)		2.08 1.66		V
Micbias output current				4	mA
Micbias decoupling capacitor	Cmic	0.75	1	1.25	nF
VCAP voltage	(note 2)		2		V

NOTES:

1 Micbias output voltage scales with AVDCDC25, equals to 5/6*VREF or 4/6*VREF (typ).

2 VCAP output voltage scales with AVDCDC25, equals to 0.8*VREF (typ).

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the JZ4775 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-11 gives the timing parameters. Following are the name of the power.

- VDDRTC
- AVDAUD: AVDCDC25, AVDHP
- VDD11: all 1.2V power supplies, include VDDCORE, AVDPLL
- VDD: all other digital IO, include DDR power supplies: VDDQ, VDDIO, VDDIO_N
- AVD: all other analog power supplies: AVDADC, AVDOTG25, UHC_AVDD
- AVDEFUSE

Table 3-11 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDDRTC}	VDDRTC rise time[1]	0	5	ms
t_{R_VDD}	VDD rise time[1]	0	5	ms
t_{D_VDD}	Delay between VDDRTC arriving 50% (or 90%) to VDD33 arriving 50% (or 90%)	0	–	ms
t_{R_VDD11}	VDD11 rise time[1]	0	5	ms
t_{D_VDD11}	Delay between VDD arriving 50% (or 90%) to VDD11	–1	1	ms

	arriving 50% (or 90%)			
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms
t_{D_AVDAUD}	Delay between VDD11 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%)	0.01	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms
t_{D_AVDA}	Delay between VDD arriving 50% to AVD arriving 50%	-1	1	ms
$t_{D\_PPRST\_}$	Delay between VDDAUD stable and PPRST_ deasserted	TBD[3]	–	ms[2]
$t_{D\_VPEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

1 The power rise time is defined as 10% to 90%.

2 The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

3 It must make sure the EXCLK is stable and all power(except AVDEFUSE) is stable.

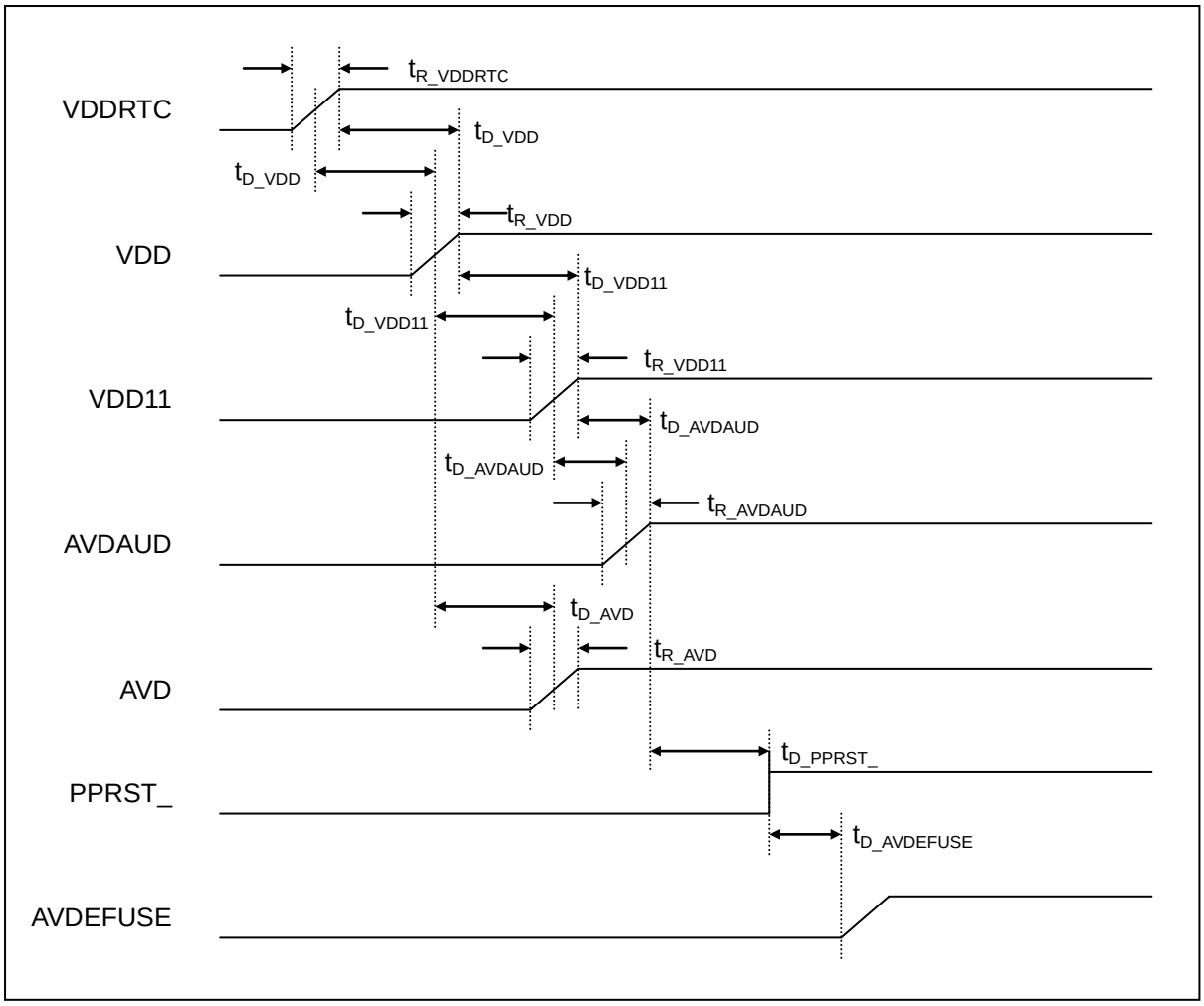


Figure 3-1 Power-On Timing Diagram

3.5.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.
2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.
3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see "2.5Pin Description [1][2]" for details. The PWRON is output 1. The oscillators are on. The USB 2.0 OTG PHY and USB 1.1 PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.5.3 BOOT

JZ4775 supports 7 different boot sources depending on BOOT_SEL0, BOOT_SEL1 and BOOT_SEL2 pins values. Table 3-12 lists them.

Table 3-12 Boot from 3 boot sources

boot_sel[2:0]	Boot method
110	NAND boot @ CS1
101	SD boot @ MSC0 (MMC/SD use GPIO Port A)
011	eMMC boot @ MSC0 (use GPIO Port A)
000	SPI boot @ SPI0/CE0
010	NOR boot @ CS4 (just for FPGA testing)
111	USB boot @ USB 2.0 device, EXTCLK=24MHz
100	SD boot @ MSC1 (MMC/SD use GPIO Port E)
001	USB boot @ USB 2.0 device, EXTCLK=26MHz

The boot procedure is showed in the following flow chart:
After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[2:0] to determine the boot method.
2 If it is boot from NAND flash, 4 flags at the beginnig of NAND are read to know the NAND

information including nand type, page cycle(2 or 3 cycles) and its page size(512B, 2KB, 4KB 8KB or 16KB). Then 14KB code are read out from NAND to tcsm, if the 14KB reading failed, the next 14KB backup in NAND will be read. Then branch to tcsm at 192 bytes offset.

3 There 14KB backup reading failed, the 14KB backup at 128th, 256th , …, and finally 1024th page will be tried in consecutive order.

4 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 14KB code from MMC/SD card to tcsm and jump to it. Only one data bus which is MSC0_D0 is used. The clock EXTCLK/128 is used initially. When reading data, the clock EXTCLK/4 is used.

5 If it is boot from eMMC boot partition1 at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 14KB code from eMMC boot partition1 to tcsm and jump to it. Only one data bus which is MSC0_D0 is used. The clock EXTCLK/4 is used.

6 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in tcsm. Then branch to this area in tcsm.

7 If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0,D1,D2,D3, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the 14KB code from MMC/SD card to tcsm and jump to it.

NOTE: The JZ4775's tcsm is 16KB, its address is from 0xf4000000 to 0xf4004000.