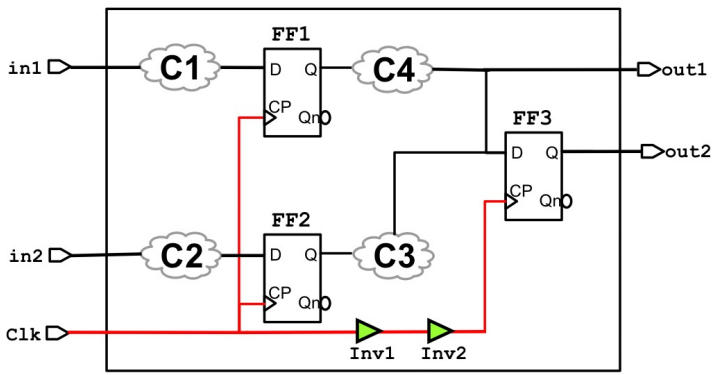
Homework 1



1. How many timing paths are there?
2. How many path groups are there?
3. Assume (FF2,C3) is the critical path, given T(setup), T(hold), T(cp-q), T(inv-delay), T(c3), T(c4)
    1. What's the minimum requirement of T(hold)?
    2. What's the maximum clock frequency of the circuit?

1. 6

2. 2

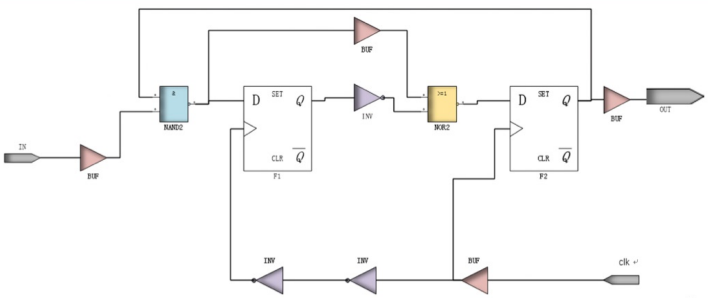
3. (1) $\begin{cases} T(cp\text{-}q) + T(C3) > T(hold) + 2T(inv\text{-}delay) \\ T(cp\text{-}q) + T(C4) > T(hold) + 2T(inv\text{-}delay) \end{cases}$

$\therefore \begin{cases} T(hold) < T(cp\text{-}q) + T(C3) - 2T(inv\text{-}delay) \\ T(hold) < T(cp\text{-}q) + T(C4) - 2T(inv\text{-}delay) \end{cases}$

(2) $\begin{cases} T(cp\text{-}q) + T(C3) < T(CLK) - T(setup) + 2T(inv\text{-}delay) \\ T(cp\text{-}q) + T(C4) < T(CLK) - T(setup) + 2T(inv\text{-}delay) \\ f = \frac{1}{T(CLK)} \end{cases}$

$$\therefore \begin{cases} f_c \dfrac{1}{T(setup)+T(cq-q)+T(c3)-2T(inv\text{-}delay)} \\ f_c \dfrac{1}{T(setup)+T(cq-q)+T(cq4)-2T(inv\text{-}delay)} \end{cases}$$

Homework 2



Input delay：T(in_delay)=1ns
INV delay：T(inv_max)=1ns T(inv_min)=0.5ns
Buffer delay：T(buf_max)=2ns T(buf_min)=1ns
NAND2 delay：T(nan_max)=1.8ns T(nan_min)=0.9ns
NOR2 delay：T(nor_max)=2ns T(nor_min)=1ns
Transfer time of Flip-Flop：T(cq_max)=4ns T(cq_min)=1ns
Setup time：T(setup)=3ns hold time：T(hold)=1ns

Question:
1. Is there any timing violation in the circuit? (the setup time and hold time of F1 and F2)
2. What's the maximum clock frequency of the circuit?

1. Yes 从 F_2 至 F_1，会出现数据在 F_1 hold 阶段变化的情况

2. $$\begin{cases} 2\times1+4+1+2<T-3 \\ 4+1.8<T-3+2\times0.5 \\ 2+4+1.8+2+2<T-3+1 \end{cases} \Rightarrow \begin{cases} T>13 \\ T>7.8 \\ T>13.8 \end{cases} \Rightarrow \begin{cases} f<76.92MHz \\ f<28.21MHz \\ f<72.46MHz. \end{cases}$$

$\therefore$ maximum clock frequency is 72.46MHz