Result:

```
xilinx@pynq:~/wanhch$ sudo python3 run.py
[sudo] password for xilinx:
[INFO ] Collected bit file is ee216.bit
[INFO ] Collected hwh file is ee216.hwh
[INFO ] Collected elf file is proj2.elf
[INFO ] Start to download bitstream ./ee216.bit to PL
[INFO ] Finish downloading
[INFO ] Start to run your code: ./proj2.elf
[INFO ] Running round 0
[INFO ] Running round 1
[INFO ] Running round 2
[INFO ] Running round 3
[INFO ] Running round 4
[INFO ] Running round 5
[INFO ] Running round 6
[INFO ] Running round 7
[INFO ] Running round 8
[INFO ] Running round 9
[INFO ] The time of exp r0.txt is 271.0us, status pass
[INFO ] The time of exp r6.txt is 269.0us, status pass
[INFO ] The time of exp r7.txt is 272.0us, status pass
[INFO ] The time of exp r8.txt is 271.0us, status pass
[INFO ] The time of exp r2.txt is 269.0us, status pass
[INFO ] The time of exp r1.txt is 270.0us, status pass
[INFO ] The time of exp r4.txt is 269.0us, status pass
[INFO ] The time of exp r5.txt is 270.0us, status pass
[INFO ] The time of exp r9.txt is 271.0us, status pass
[INFO ] The time of exp r3.txt is 270.0us, status pass
[INFO ] Total time of all exps are: 2702.0us
[INFO ] Average time of all exps are: 270.2
[INFO ] Dump result csv file to ./result/result.csv
[INFO ] Finish running your code: ./proj2.elf
[INFO ] Exit ...
```

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.750	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
21757	21757	2073	2073	dataflow

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	122	-
FIFO	-	-	-	-	-
Instance	88	1109	43672	87697	-
Memory	40	-	0	0	0
Multiplexer	-	-	-	180	-
Register	-	-	20	-	-
Total	128	1109	43692	87999	0
Available	624	1728	460800	230400	96
Utilization (%)	20	64	9	38	0

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../src/fft_test.cpp in debug mode
   Compiling ../../../../src/fft.cpp in debug mode
   Generating csim.exe
This is EE216 FFT Project Testbench
fft_hw 1000 us
-----------------------------------------------
   RMSE(R)           RMSE(I)
0.046909254044294 0.013719381764531
-----------------------------------------------
***********************************************
PASS: The output matches the golden output!
***********************************************
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************

```

Code structure:
在 baseline 基础上进行修改，主要修改是将原先 fft_stage 中的双重循环展开成了一重循环。

Optimization strategies:
首先在 baseline 代码中加入 dataflow，并将 fft_hw 中的循环进行 unroll 展开，对 X_R. OUT_R, X_I. OUT_I, Stage_R, Stage_I 进行 partition，其中 Stage_R, Stage_I 在 dim=1 处进行 partition。然后再对 fft_stage 中循环进行优化，对其中的 dft_loop 加 PIPELINE II=2 的限制。
此时发现每个 stage 间的 latency 与 Interval 差别很大，分析原因是因为每个 stage 中，butterfly_loop 与 dft_loop 循环的次数不同造成的。stage1 中，butterfly_loop 循环 1 次，dft_loop 循环 512 次，而在 stage10 中，butterfly_loop 循环 512 次，dft_loop 循环 1 次。当 butterfly_loop 数量增加时，因为执行一次循环需要多个周期，所以 latency 与 Interval 数大大增加。所以考虑将双重循环展开成一重循环，并经过计算给其加最小 II=4，将新函数命名为 fft_stage1。
经过测试，stage1 与 stage2 运用原始 fft_stage，其他 stage 使用展开后的 fft_stage1，不同 stage 间的 latency 与 interval 最为平衡，可以得到最佳的优化效果，如下图所示。

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
21757	21757	2073	2073	dataflow

Detail

Instance

		Latency		Interval		
Instance	Module	min	max	min	max	Type
fft_stage82_U0	fft_stage82	1049	1049	1049	1049	none
fft_stage191_U0	fft_stage191	2072	2072	2072	2072	none
fft_stage1_187_U0	fft_stage1_187	2072	2072	2072	2072	none
fft_stage1_188_U0	fft_stage1_188	2072	2072	2072	2072	none
fft_stage1_189_U0	fft_stage1_189	2072	2072	2072	2072	none
fft_stage1_190_U0	fft_stage1_190	2072	2072	2072	2072	none
fft_stage1_185_U0	fft_stage1_185	2072	2072	2072	2072	none
fft_stage1_186_U0	fft_stage1_186	2072	2072	2072	2072	none
fft_stage1_184_U0	fft_stage1_184	2072	2072	2072	2072	none
fft_stage1_183_U0	fft_stage1_183	2072	2072	2072	2072	none
bit_reverse81_U0	bit_reverse81	2050	2050	2050	2050	none