Section A

Question 1

(i) a

(ii) 2 1
1 2

(iii) The pages will increase.

(iv) a

(v) 7

(vi) the hitting ratio are h_1, h_2, h_3 for shared cache, RAM and disk.
time are t_1, t_2, t_3 for shared cache, RAM and disk.
$T_{eff}: h_1t_1 + (1-h_1)h_2t_2 + (1-h_1)(1-h_2)h_3t_3$

(vii) (a). $\log_2(1024) = 10 \rightarrow$ access a block
$\log_2(4) = 2 \rightarrow$ specific byte

(b). remaining bits are used for tag.

(viii) $\sqrt{4m}$

(ix) False
$H_k = \frac{S_k}{k \cdot t} = \frac{1}{k \cdot t} \cdot S_k$ linear relationship

(x) 1 False

(xi) False

(xii) the memory could be accessed concurrently.

Question 2

(i). For sequential:

```
Load y
Load a
Load b
Load c
Load x
MUL b,b,x // b=b*x
MUL x,x,x // x=x*x
MUL a,a,x // a=a*x
ADD y,a,b,c // y=a+b+c
```

For VLIW:

```
Load b   Load x
Load a   Load c   MUL b,b,x
MUL x,x,x   ADD b,b,c
MUL a,a,x
ADD y,a,b.
```

(ii). $\frac{5}{9}$

(iii) $y = a_n x^n + a_{n-1} x^{n-1} + \ldots + a_1 x + a_0$

~~$y = ax^2 + bx + c$~~

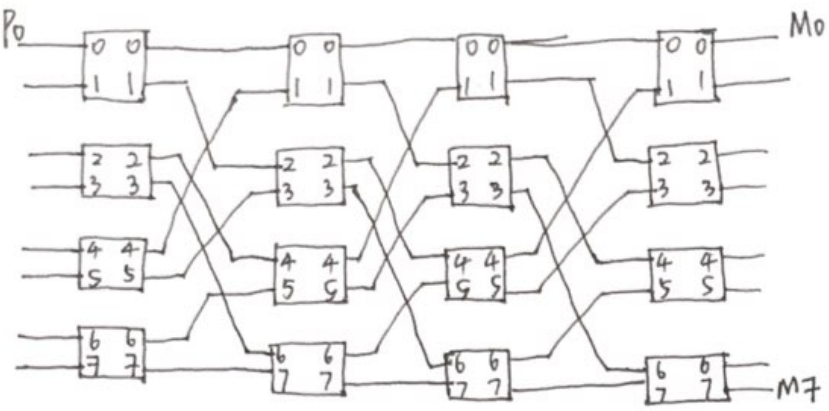
~~$O\log(ax^2+bx+c) = O\log($~~

Polynominal Time Complexity: $T(n) = O(n^k)$ for all positive k.

Here, we have the upper bound of the time complexity, which is $T(n) = O(x^n)$ for all positive n.

Question 4

(i).



(ii) P_0 to M_0 : 1

P_0 to M_7 : 1 Yes, it is hold for all pairs.

(iii) suppose switch 1 fails.

(P_0, M_0) (P_4, M_2) fails.

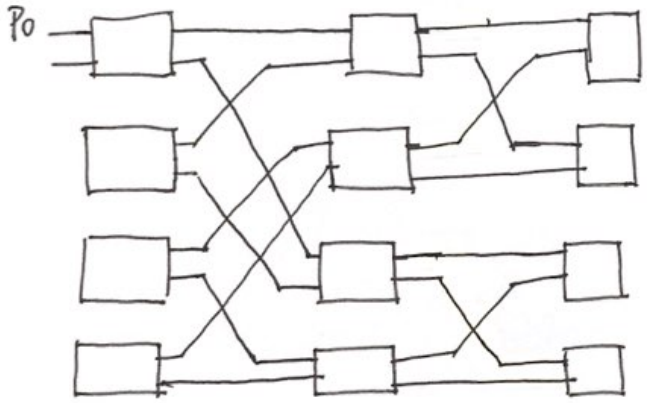
(iv) (P_0, M_0) fails.

(v) If only the top link ~~is~~ fails, the upper link still can use, and (P_4, M_2) will not fail.

(vi) Yes, it will increase.

The base-line network has self-routing ability.

Base Line.



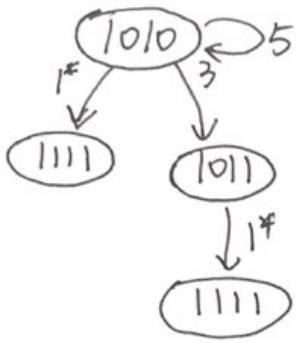
Question 5

i). IL = (4, 2)

PL = (1, 3, 5, 6)

(ii) (1010)

(iii)



(iv) (1)
(3, 1)

(v) MAL = 2

(vi) True

(vii) True