Order of questions may not follow chapter order

1. Multiprocessors are parallel processors (T/F) T

2. Multicomputers are distributed systems (T/F) T

3. Multiprocessors, using a strict definition, are otherwise called as loosely connected computer systems (T/F) F

4. Parallelism can be exploited at algorithm design time, program time, compile time and also at run time (T/F) T

5. MISD architecture, under a pipelined execution, is otherwise referred to as Systolic arrays

6. Memory-to-memory architecture is a Vector processor

7. Argue whether this statement is right or wrong.
In a multi-programmed computer, the I/O system overheads of a given program are not allowed to overlap with the CPU time required in other programs because I/O systems require CPU intervention predominantly.

Wrong! These overheads are allowed to overlap as CPU time is not needed. These I/O systems use other means to transfer any data that may be required to and fro from Memory. DMA is one such example.

8. MIPS rate is inversely proportional to the total number of clock cycles needed to execute a program (T/F) T

9. Identify incorrect statements in the following.

S1: CPU time can be used as a basis to estimate the execution rate of a processor.
S2: One of the key performance factors in the design of cache and memory hierarchy is the number of memory references per instruction.
S3: An explicit approach to achieve parallelism is to design a concurrency preserving compiler.
S4: UMA model is a general-purpose multiprocessor System
S5: In a NUMA architecture, all processors in a cluster have non-uniform access to shared-memory modules.

Ans: S2 and S5 are incorrect.

10. In a MIMD computer, all processors must execute the same instruction at the same time simultaneously (T/F). F

11. For a particular reservation table that is defined, the greedy cycles are found to be (5) and (4,6). The MAL is given by 5

12. For a linear pipeline unit, the maximum throughput will be equal to the pipeline frequency f when

Ek -> 1 as n -> infinity.

13. A CISC instruction set has a large number of instructions and uses large register files to execute when compared to a RISC instruction set (T/F) F

14. Consider the following loop: *We have done this before…*

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For j = 0 to (log n)-1
        For i = 2^j to (n-1) do in parallel
        S[i] = S[i-2^j] + S[i];
        End For
End For
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i). What is the complexity of the algorithm? O(log n)

ii). What does the algorithm do? Assume that the array is filled with some arbitrary positive numbers.

iii). Can you identify the type of PRAM used to implement The above algorithm with a time complexity obtained in (ii) ? CREW type PRAM

15. AN SIMD computer exploits spatial parallelism rather Than temporal parallelism (T/F) T

16. A vector processor is equipped with multiple vector pipelines that can be concurrently used under a hardware control (T/F) T

17. Loop-level parallelism is the most optimized program construct to execute on a vector processor.

18. Number of links in an n-dimensional hypercube with N nodes (i.e., $n = \log_2 N$) is nN/2

19. The ideal execution time required by an m-issue superscalar machine is k+(N-1)/m (T/F). F

20. If C = (1011010) is a collision vector for a reservation Table, then the latencies 6 and 3 are permissible.

21. The cache memory technique provides a fast store for the program on RISC machine and therefore compensates for the increased number of instructions in the program (T/F) T

22. A location monitor module, which is one of the key modules in a set of functional modules in any hardware board, monitors possible collisions on interrupt and synchronization bus in the backplane (T/F) F

23. || relationship is a transitive relationship but not an equivalence relationship (T/F) F

24. Control parallelism, appearing in the form of pipelining is limited by the pipeline length.

25. For parallel programming purposes, one of the important forms of parallelism considered is data parallelism (T/F). T

26. Fine-grain partition of a program may not demand more inter-processor communication if data dependency is less.

27. A write-invalidate protocol will essentially invalidate all the copies when the local copy is being updated (T/F) T

28. For full-mapped directories, the size of the total memory overhead increases as the square of the number of processors, i.e., O(N^2) (T/F). T

29. Two-way lower order interleaving design is more fault-tolerant than a four-way lower order interleaving design, for a shared-memory organization (T/F). T

30. If 15% of conditional branches are present and 80% of conditional branches are taken in a program, the average delay caused is 3 * 0.15 * 0.8 = 0.36. Assume that 3 clock cycles time will be spent if a conditional branch is taken.

31. Super-scaling implies that a processor is a is a k-issue processor, with k > 1 (T/F) T

32. If m is the number of instructions and n is the number of clock cycles per instruction, the speed-up achieved for a system that uses pipelining technique is $\underline{mn / (n+m-1)}$.

33. If speed-up of a parallel processing system is given by Bonus problem!

$$S(n) = 1 / (x + (1-x)/n)$$

where n is the number of processors and 0 <= x <= 1, plot the variation of S(n) w.r.t x, for a given n.

34. In the above problem, plot the variation of S(n) w.r.t number of processors n, for a fixed x. Bonus problem!

35. If x is interpreted as the fraction of the program that is to be executed in sequential form, interpret your observations from the plots in questions (33) and (34). Bonus problem!

36. Because associative cache mapping technique searches the entire cache memory to locate the requested word, the disadvantage in using direct cache mapping technique can be tolerated (T/F) F

37. Because of excessive overheads in implementing associative mapping technique, set-associative mapping

Cont'd….

uses direct mapping technique to reduce the overheads involved (T/F) T

38. In a TLB, set-associative mapping will always work better than associative mapping technique (T/F) F

39. In transferring data from a disk to main memory, direct memory mapping technique will deliver a poor performance than associative memory technique (T/F) T

40. Destination tag routing in the case of self-routing networks is meaningful only when each switch is of dimension 2 x 2 (T/F) T

41. Node degree in a graph representing a multiprocessor system is a measure of the number of I/O ports at that node (T/F)? T

42. If you are given a matrix of size n x n, how many processors would you expect if you wish to achieve a time complexity of O(log n) for A x A operation ? n^3

43. Space complexity is a measure of the amount of space occupied by a program in the main memory (T/F)? F

44. In a SIMD architecture, the routing function and the set of instructions that are to be executed by the control unit must be explicitly specified (T/F)? T

45. A statement such as Add R2, R1, implying R2 <- (R1) + (R2) is a flow dependent statement on itself (T/F)? T

46 .To double the speed-up of a linear pipeline, one of the ways is to double the clock speed (T/F)? F

47. If probability of finding a desired word is 0.5 in cache and main memory systems, the effective access time of the desired word in this memory hierarchy is 0.5 Tc + 0.25 Tm. Assume that Tc and Tm are the time to access the respective memory systems.

48. Collision free non-linear pipeline scheduling is equivalent to determining all the simple cycles that leads to MAL (T/F) T [Note: The statement is correct, as greedy cycles are members of simple cycles. Therefore, it is correct to say that "we determine simple cycles to determine MAL", as determining greedy cycles is an intermediate step . The above statement does not mean that MAL belongs to Simple cycles]

49. Identify what can be wrong in the following specifications?

A computer system has the following memory characteristics.

Level	Access time	Capacity	cost	bandwidth
	nano secs	KBytes	cents/KB	MB/sec
Cache	25	256	80	260
Main Memory	20	256	70	300
Disk Storage	20	2000	0.7	10

Soln : Respective relationships can be compared across each level

50. (a) In Pentium series machines, the number of Concurrent operations in the execution stage is 2 .

(b) The above operations could be Data fetch / ALU/ FPU

51. What is the complexity of recursion involved in the ROR model we have seen in the lecture for resource allocation problem? $O(n^2)$ Express in terms of n, the demand at each stage.

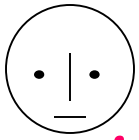
52. If $X = (\log^2 n + \log n)/2$ for an algorithm, this is equivalent to saying that the complexity of this algorithm is $O(\log n)$.

53. A shared memory multiprocessor system has 256 nodes. It uses directory based protocol to resolve any incoherence and has 2GB of main memory with block size of 256 bytes. What is the size of the directory? Assume that each cache is 1MB.

Soln : Num of bits for directory = 256 Mbytes; Num of bits for directory in each cache = 8192bits

54. If C is the capacity of a cache memory, then space allocation for I and D type streams depends on miss rate behavior with respect to C .

I wish you all the best for your exam
Good Luck !



- Bharadwaj V