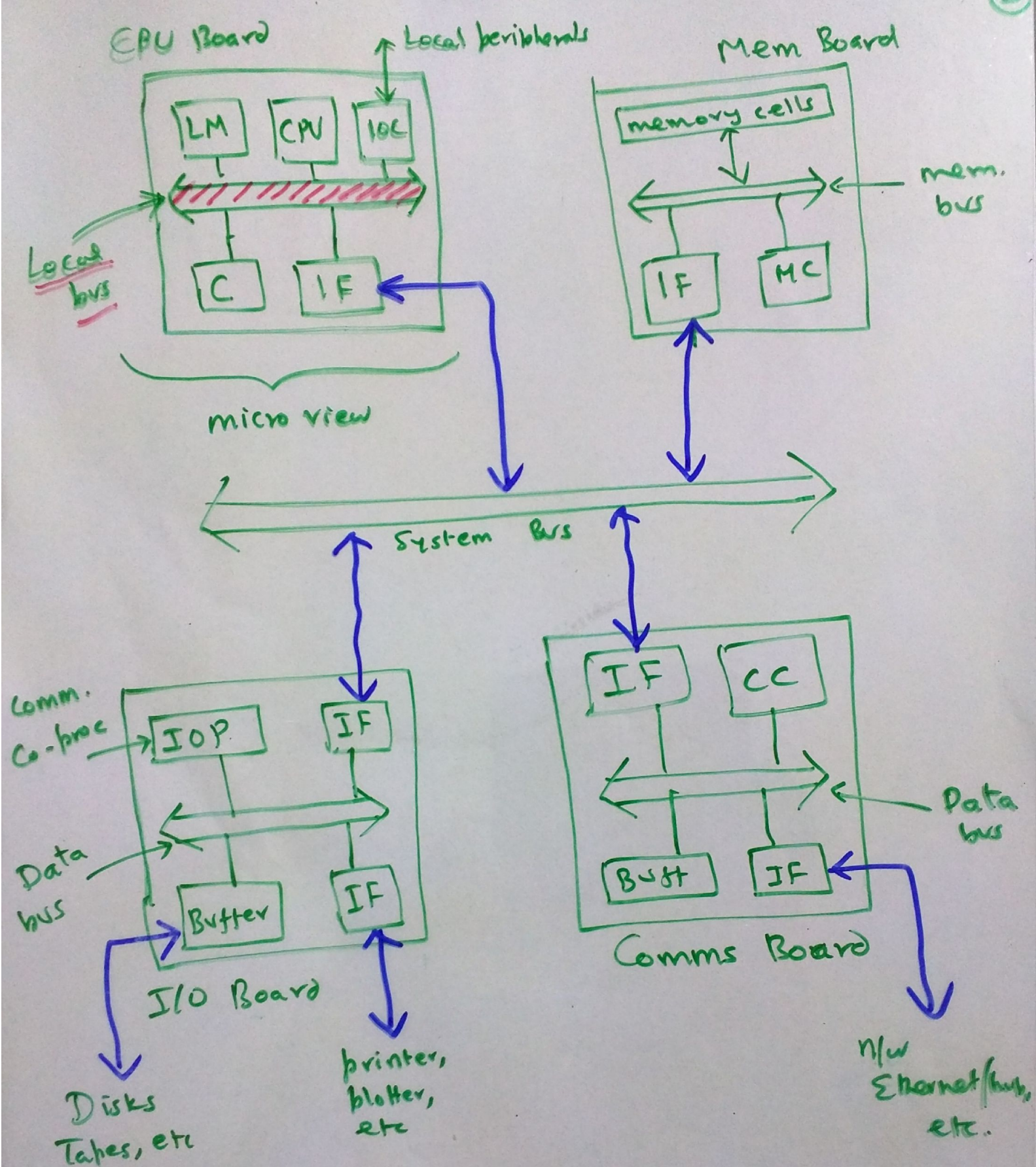


Generalized MP System

Shared I/O
+
peripherals

- Combines features from UMA, NUMA & COMA (chapter 1)

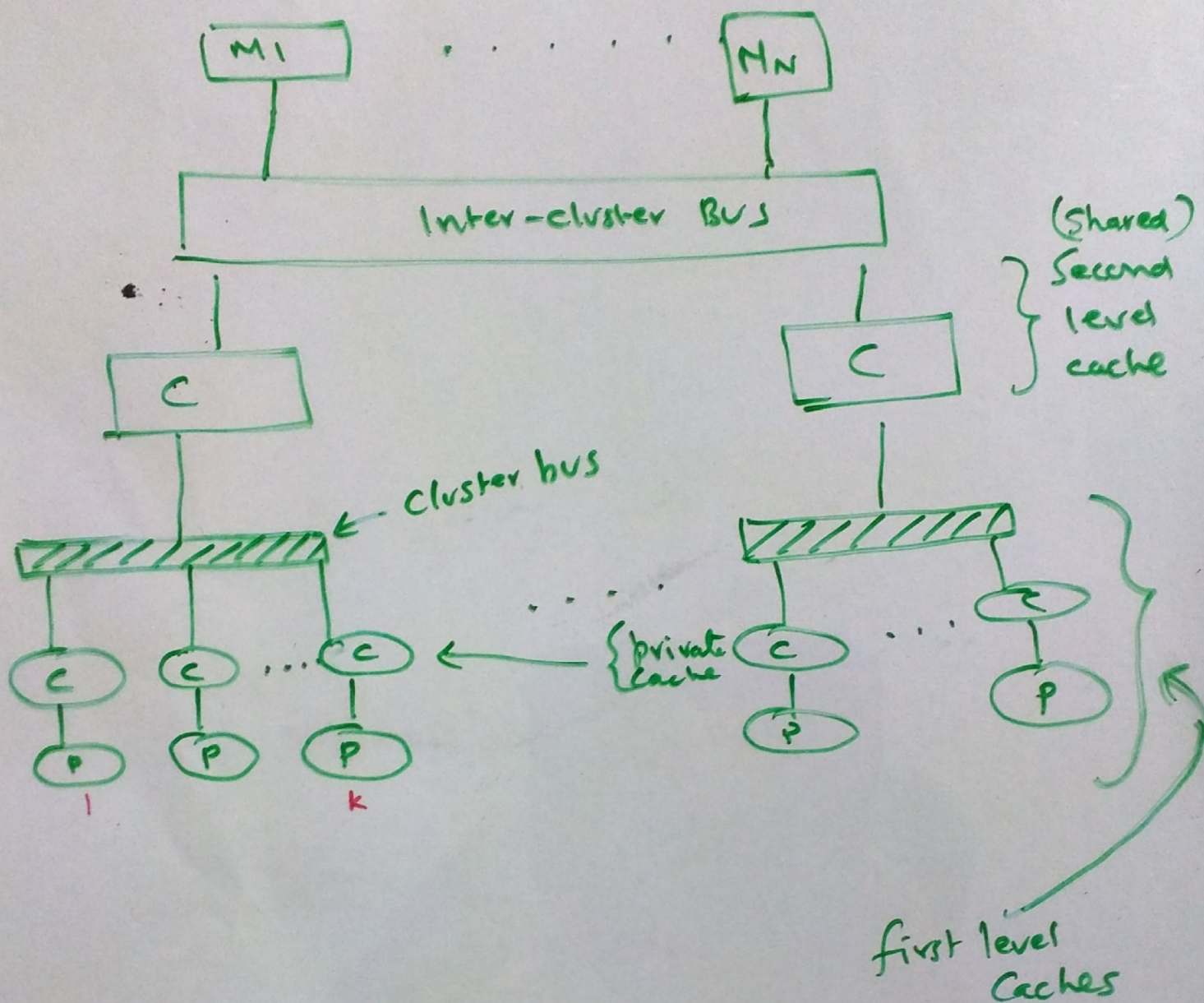
- Direct IP comms via optional IPCN instead of a SM.



Bus Systems

- Local Buses on board
- back-plane buses
- I/O buses

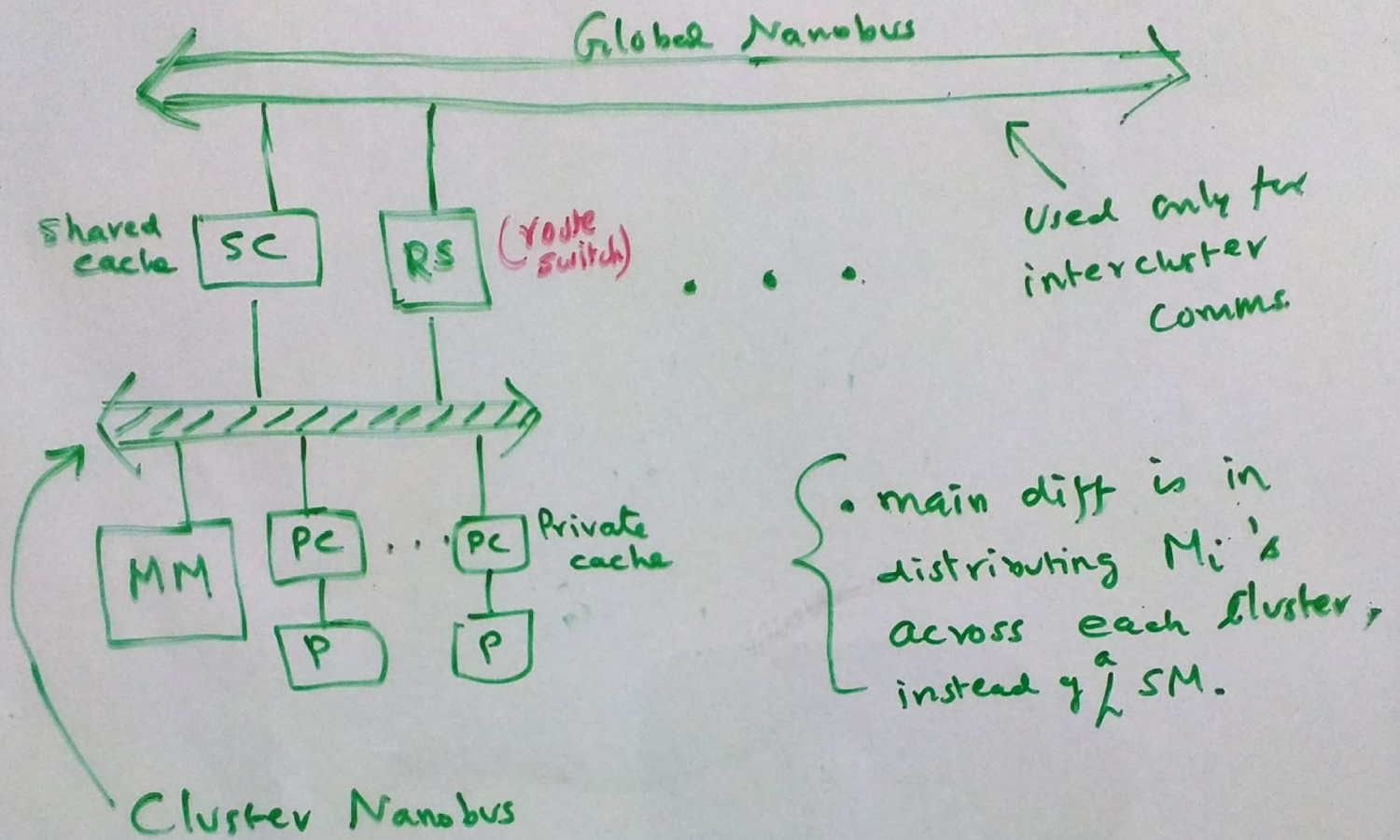
WILSON's HIERARCHICAL MODEL



- Capacity of ^{each} 2nd level cache \geq Sum of all the Capacities of 1st level caches beneath it.
- for every i : $C_{2,i}$
- $\sum_{j=1}^n C_{1,j}$

Encore's Ultramax MP architecture

④



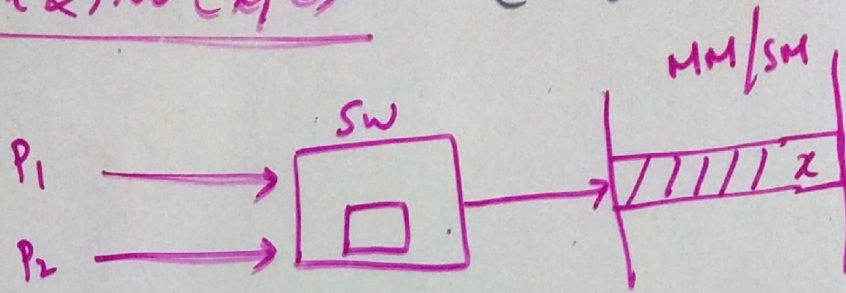
• Bridges are used to interface clusters

- protocol conversion
- interrupt handling in split transactions

Fetch & Add (x, e)

(fig 7.11 ; page: 346)

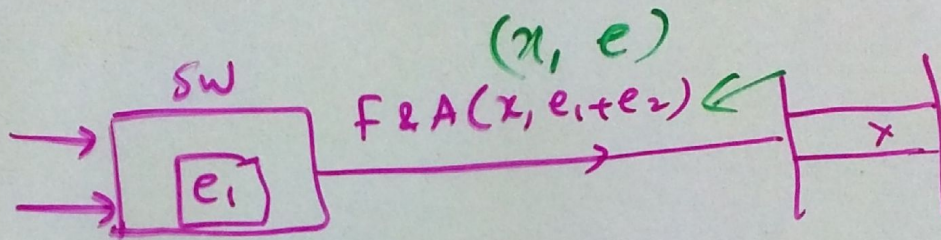
①



$P_1: F\&A(x, e_1)$
 $P_2: F\&A(x, e_2)$

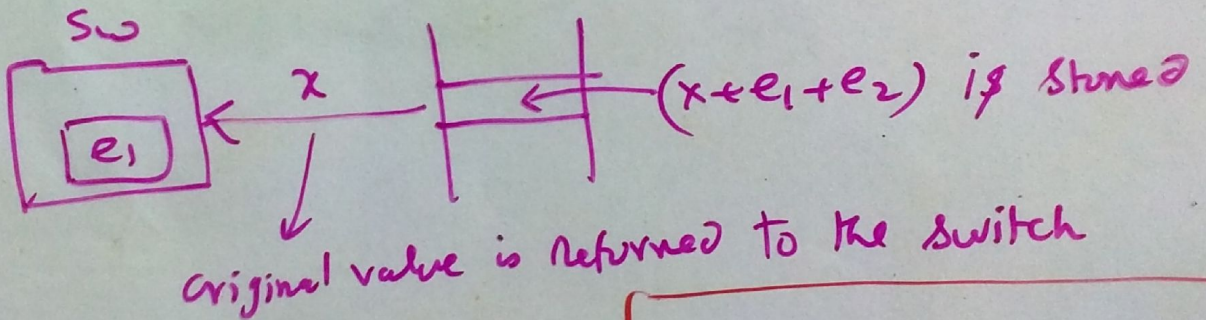
Result: $x \rightarrow P_1$
 $x + e_1 \rightarrow P_2$

②

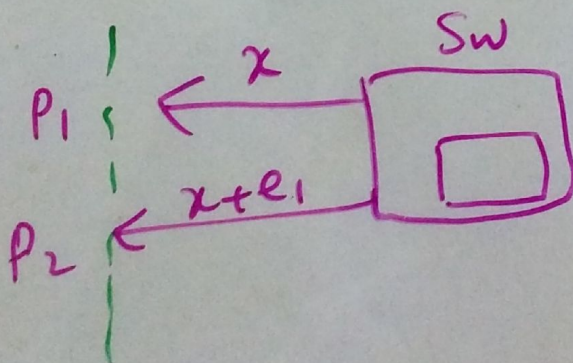


Switch forms the sum $(e_1 + e_2)$,
 stores e_1 & forwards the combined val to MM.

③



④



Suppose
 $P_2 \rightarrow P_1$
 $Ans_2 \leftarrow x$
 $Ans_1 \leftarrow x + e_2$

Regardless of the executing order, we have $(x + e_1 + e_2)$
 is stored at that loc. in MM.