Consider an interleaved memory access design as shown in Fig. 1. Observe that there are 4 DRAMs in each bank. When a bank is selected, all the words in the same row can be retrieved from all DRAMs in that bank sequentially. Ignore the switching time between the DRAMs within a bank to read or write data. Assume that a hardware based pipelined mechanism is implemented to facilitate accessing the words that reside in different banks in the same row. Use the following data and answer all the parts.

The loading time of the n-bit memory address register(MAR) \neq 2 cycles

Access time to a specific row in a bank = 1 cycle; Access time for a word from a DRAM = 1.5 cycles; Time to return 1 word = 0.5 cycle.

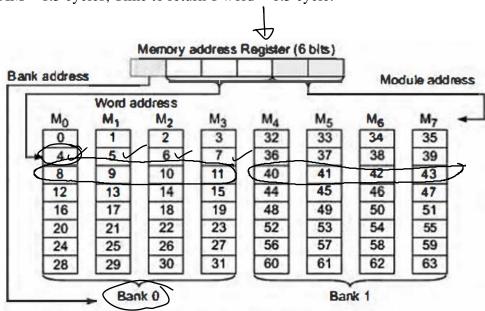
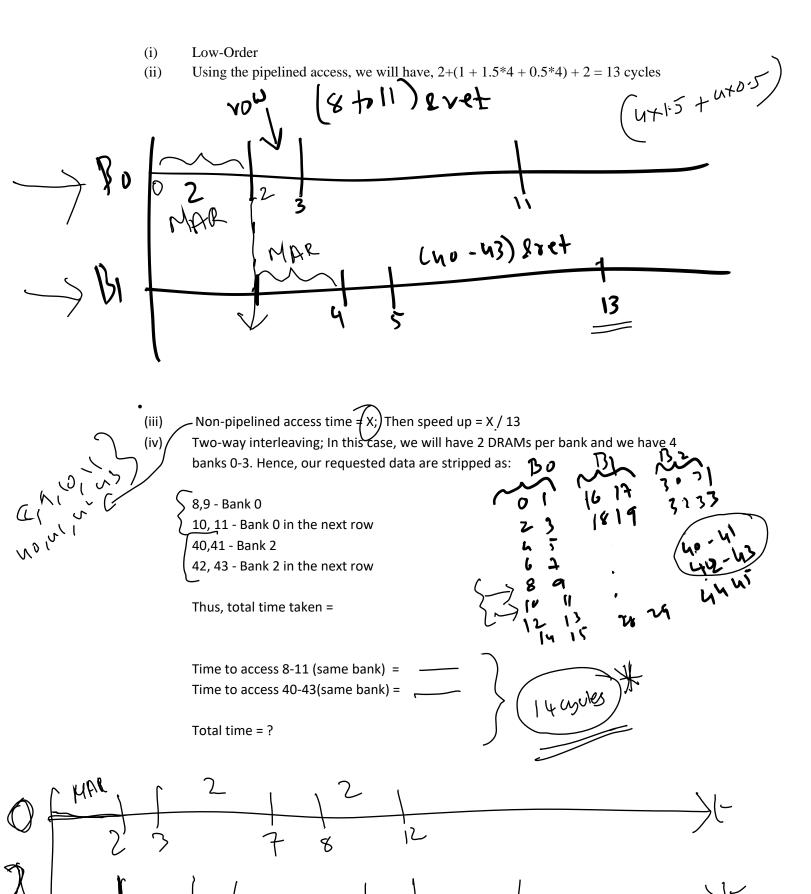


Fig. 1: Four-way interleaved shared-memory design

- (i) The interleaved architecture shown in Fig. 1 is ______ interleaving design.
- (ii) Compute the total time taken to access the words 8,9, 10,11, 40, 41, 42, and 43. Initial MAR contents are zero. Clearly mark all the timing events in your diagram.
- (iii) Compare the result obtained in (ii) using a non-pipelined way of accessing all the data in the same architecture. Compute the speed up. Within a bank, all accesses remain sequential as before.
- (iv) Following the same interleaved design shown in Fig. 1, repeat (ii) by drawing a timing diagram to capture the total time if a two-way interleaving within each memory bank is used. Initial MAR contents are zero. Comment on your result. Clearly mark all the timing events in your diagram.

(2+1+1·5+05)



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