EE5902 AY21/22 Exam syllabus

Prepare the following for your exam.

Nomenclature:

Slides - power-point slides

Book - The recommended text book (Kai Hwang's book)

It is important that you be thorough with all the material above, as we have taught everything listed below in the class.

Chapter 1

- **Book Ref**: Pages 3 to 39 (before Bisection Communication Bound)
- **Slides**: Go through all the slides as a revision process + Examples we have seen in the class (such as matrix multiplication, prefix-sum computation, for calculating the time-complexity of an algorithm, etc)
- Practice some simple (not overly complex!) problems on computing time-complexity;
- Amdhal's law and its implications using fundamental definition;

CONCEPTS & POINTS TO PONDER: Definitions of fundamental metrics like MIPS, throughput, etc; different class of architectures; Flynn's taxonomy – identifying architectures for different class of problems; time-space complexity – definitions and problems (matrix vector multiplication on parallel machines; prefix-sum computation, ***etc***); Given a code segment, you must be able to compute the time-complexity; Basic Amdahl's law and its interpretation;

Chapter 2

- **Book Ref**: Pages 51 to 71(before "A Dataflow Architecture" on Page 71)

- **Slides**: All the slides in Chapter 2 + Slides on the topic "Effect of granularity on the time performance" ; Multistage Interconnection Networks - all types of MINS discussed in the class - CLOS, Shuffle-Exchange, Baseline network; ~~Max-Flow Min-Cut theorem and applicability to multiprocessor scheduling;~~ Effect of Granularity – time non-overlapped model;

CONCEPTS & POINTS TO PONDER: Identifying all flow dependencies in a code; Bernstein's conditions- given a specific hardware and a program, we must be able to compute and identify the mismatch; KL procedure on a given program graph; **[**code segment -> Bernstein's conditions -> Mapping on a hardware using KL approach with a given granularity**];** ~~Max-Flow Min-Cut theorem and its implications identifying a feasible schedule and an optimal schedule for a given graph;~~ MINS – all MINS we have dealt in the class – Crossbar switch analysis, CLOS network non-blocking analysis, Processing Time versus Granularity – time ~~overlapped and~~ non-overlapped models - their performance w.r.t R/C ratio;

Chapter 3 [This is Chapter 4 in your book]

- **Book Ref**: Pages 157 to 165; 177 to 184(before Section 4.2.3); 188 to 196(before Section 4.4)

- **Slides**: All the slides are important; ~~Case Study - Pentium Processor (block diagram and description;~~ Multi-core basics; Multi-threaded Programming Example – Using Shared memory and MPI; GPU architecture and process involving code execution (code re-targeting on a GPU) in a CPU-GPU system;

CONCEPTS & POINTS TO PONDER: Distinguishing CISC/RISC architectures given a specs; definitions and timing diagrams for Superscalar/Super-pipelining and hybrid architectures; VLIW architecture – motivation, advantages, disadvantages; example of writing a simple code for a given expression on a VLIW processor; What makes CISC/RISC special? ~~Pentium series machine core descriptions~~; Basic multi-core and multi-threaded concepts; GPU architecture and programming example; Shared memory & MPI on an application example (heat-wave propagation); You may refer to Superscalar workings via Chap 6.

Chapter 4 [This is Chapter 5 in your book]

- **Book Ref**: 213-222; 238-244 (exclude Section 5.3.2); Pay attention to Example 5.7 which we have dealt in the lecture;

- **Slides**: All slides of this chapter;

CONCEPTS & POINTS TO PONDER: All about Bus and timing controls; arbitration policies we have seen in the class; basic problem solving using Direct/associative/set-associative caches; LRU and its variants (if defined any); Belady's anomaly; Working sets – Problem – given a trace/application, you must be able to identify the LRU blocks and show the memory map when using any of the above 3 mapping techniques; Understanding of the concept of VM & TLB use; shared memory organizations – higher/lower order interleaving techniques – concept and their use;

Chapter 5 [This is Chapter 7 in your book]

- **Book**: Pages 331- 335 + Example 7.1; 345-350; 358-359(before full-map directories)
- **Slides**: Use the lecture slides for Snoopy bus protocols and for directory-based protocols; Example demonstrated in the lecture; fetch&add()
- CONCEPTS & POINTS TO PONDER: Cache coherence – methods to resolve using Snoopy/Directory based methods; Hot-spot problem and given an architecture, you must be able to show the flow of responses for ***fetch&add()*** procedure at every stage;

Chapter 6

- **Book Ref**: Relevant pages w.r.t the slides indicated below;
- **Slides – All:** Linear pipeline, Non-Linear Pipeline, determining the state-space for a given non-linear pipeline, deriving the MAL for a given CV and/or a NL pipeline, Out of order and in-order execution examples, Speed-up loss calculations for single cache memory (for data and instruction) systems; Speed-up for Superscalar, Super-pipeline, and superscalar-super pipeline derivations);

CONCEPTS & POINTS TO PONDER: Linear, Non-linear pipeline analysis, instruction pipeline – basic concepts, in-order execution and out-of-order execution examples, loss of speed-up calculation using same memory for instructions and data,

different types of hazards, dependences, speed-up derivations of different class of multiprocessors (superscalar, super pipeline, superscalar-super pipeline – compare their performances),

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Note: As Section A of the Question paper involves objective/multiple-choice type of questions, it is recommended that you visit all the above contents carefully.

EXAM PAPER FORMAT AND SOME IMPORTANT POINTS

- Class will be split into 3 groups in this term; Separate examiner for each; Separate zoom login sessions for exams;
- Cheat Sheet – 1 Page A4 size handwritten sheet (both sides)
- Use your phone to login to Zoom;
- Use your computer to login to luminous (to QP download and answer sheet upload actions)
- Get ready with a screen recorder (OBS – recommended - (*1 fps can be set to consume low memory* - https://obsproject.com/download)

Exam Paper Format

Time: 2 hours

Section A – 12 x 2 = 24 Marks

Section B – 3 x 12 = 36 Marks

Total Final (written exam) = 60 Marks

CA = 40 Marks