Welcome! So, you are ready for the exam. Good luck!

- **Take this 1.5 hour (90 minutes) self-test and judge your preparation. You may give a score of 1 point for each question.**

Suggestion: This test will be helpful as a process of revision and it would be better if you take two or three days before the exam.

Request: In the exam, for questions that ask you to answer either TRUE/FALSE, please just answer TRUE/FALSE and I do not need any reason.

Answer the following questions. (T: True; F: False)

1. Non-linear pipeline line analysis using the state diagram approach may generate an optimal MAL (**T/F**)
2. A set of processes can be executed in parallel if P(i) || P(j), for all i not equal to j (**T/F**)
3. In the case of explicit parallelism, a parallelizing compiler translates the source code to a parallel object code before execution (**T/F)**.
4. The node degree of network must be as small as possible to keep the cost low (**T/F**)
5. Consider a non-overlapped communication and computation time model for a two processor system. Assume that the two processors are identical. The total execution time for executing M tasks by the two processors is given by _____. Assume that R is the length of a run-time quantum and C is the length of communications overhead produced by that quantum.
6. Let the number of jobs be n and time to process a job is p. Let each job be divisible into k tasks and let each task be done by a different processor. Also, let the time for processing each task is p/k. The speed-up achieved with a k stage pipeline organization of the processors is k/(1 +(k-1)/n) (**T/F**).
7. Because of the fact that every read/write reference PT is used by the memory unit, the entire PT is kept inside the MMU (**T/F**).
8. The throughput of a pipeline amidst branch instruction execution will be a maximum when a branch instruction occurs at the last stage of the pipeline (**T/F**).
9. For a CISC computer, in general, the CPI is very low as a result of long microcodes used to control the execution (**T/F**).
10. For contiguous access in a _____m-way interleaved memory system with m modules, all the m modules can be kept busy at a time.
11. Diameter of a network is defined as: _____ _____
12. A fetch&add call returns the most recent value stored in the memory location (**T/F**).
13. Draw a two-stage CLOS-based interconnection network with r switches in the input stage and s switches in the output stage, let p x r = M and s x q = N, where p is the number of input pins per switch in the i/p stage and q is the number of output pins per switch in the o/p stage.
14. Draw a two stage network when M = N in the above question.

15. A shuffle-exchange network has a self-routing ability (**T/F**).
16. Different realizations of the same VLIW design may not be binary-compatible with each other (**T/F**)
17. The number of switches in the middle stage of a three-stage CLOS network does not affect the non-blocking property of the network (**T/F)**.
18. The advantage of duplicating a node in a grain packing phase in a static multiprocessor scheduling scheme is ---------- (choose from the following) (a). to decrease the idle time and to further reduce the communication delays (b). to evenly balance the load
19. Bernstein's conditions for a parallel execution of a code includes anti-dependent property(T/F).
20. RISC processor although uses larger register files it gains speed due to faster decoding ability and easy management of register window functions. What is wrong with this statement?
21. The throughput of a linear pipeline with k stages will equal to the clock frequency (f) when _____.
22. Out of n instructions, if f is the fraction of the instructions that are either conditional or unconditional branches, using a non-pipelined system, the finish time of the n instructions will be _____. Assume that each instruction takes 1 clock cycle and k additional cycles for every conditional and unconditional branch instruction.
23. The number of input points for a switch in the middle stage of a three-stage CLOS network is equal to _____ and the number of output points for that switch is equal to _____.
24. Pentium Processor is a _____ architecture.
25. The idle execution time of required by an m-issue superscalar machine is given by, k + ((N-1)/m) (**T/F**)
26. As number of instructions increases in a superpipeline-superscalar machine, the speed-up will eventually tend to _____.
27. Given a collision vector C = 1000, possible evaluation times of the reservation table are____. Assume that no stage is left unutilized in any clock cycle and only one stage is used in a clock cycle.
28. Out of all four possible PRAM variants, the most uncommon type is _____.
29. Given a collision vector C = 1000, the number of stages in this pipeline is ____. Assume that no stage is left unutilized in any clock cycle.
30. Given a particular state, say X, in the state-transition diagram for a reservation table of a pipeline, the maximum number of states that can be visited is _____.
31. In a VLIW machine, all the functional units share a common register file (**T/F**).
32. NUMA multiprocessor system is a shared memory system with variable access times for every word (**T/F**).
33. Given a collision vector C = 1000, the forbidden latency is ____.
34. The mismatch between software parallelism and hardware parallelism can also be minimized by using a single m-issue processor, as opposed to using several processors (**T/F**).
35. If the complexity of a program is stated as $O(\log_2(M / \log_2 M))$, then for very large values of M, we refer to this algorithm as "order of complexity _____".
36. The rate at which the instructions are issued is also called as the degree of a superscalar processor (**T/F**).
37. Routing in a MIN depends on the interconnection pattern of the MIN (**T/F**).
38. The number of windows that can be supported by an overlapping register window mechanism is dependent on the number of registers utilized per process (**T/F**).

39. I/O dependence is indeed a flow-dependence (**T/F**).
40. In super-pipelined processors, since multiphase clocks are used, the effective CPI is very high (**T/F**).
41. Super-scaling does not imply that a processor is a k-issue processor (**T/F**).
42. Memory-to-Memory is usually viewed as a vector computer (**T/F**).
43. All processors need not be executing an instruction concurrently in a MIMD machine **(T/F).**
44. In the state-transition diagram capturing a non-linear pipeline execution, every CV of a state has Cm=1 (**T/F**).
45. Super-pipelining and Super-Scalar computers are not general purpose computers (**T/F).**

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Interpretation of your score !

35 and above: Fantastic, you will have a cake-walk in the exam!!

28 to 34: Good show! One more revision will boost you to a higher range

20 to 27: You may be bit careless in deciding the answers. I believe you are nervous and sometimes you attempt multiple times. Identify the questions that disappointed you, and scroll through that chapter.

15 to 20: Absolutely probabilistic in approach, and most of the correct answers for you would be of general type questions. So, work hard!

Below 15: I truly sympathize! Group discussion and at least two times reading is a must.

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My general observation:

In the above spectrum, with my so far experience in looking at the performance (in the last six years), persons in the range 20 to 27 will do better in the final exam, for sure.

GOOD LUCK FOR YOUR EXAMS !