Multiprocessor System Interconnects

Parallel processing demands the use of efficient system interconnects for fast communication among multiple processors and shared memory , I/O and other devices.

Hierarchical buses, crossbar switches, and multi-stage networks are often used for this purpose.

Refer to Fig. 7.1 on page 332. This figure shows a generalized multiprocessor system, having the following features.

• This architecture combines the features from UMA, NUMA, and COMA models.

• Each processor is attached to its own local memory and local cache

• Multiple processors are connected to shared-memory modules through an inter-processor memory network (IPMN)

• The processors share the access of I/O and peripheral devices through a processor-I/O network (PION)

• Both IPMN and PION are necessary in a shared-memory multiprocessor

• For direct communications, an optional inter-processor communication network (IPCN) is provided instead of through the shared memory

Network characteristics:Each of the above networks IPMN, PION, and IPCN can be designed with many choices - topology, timing protocol, switching method, and control strategy.

• Dynamic interconnection networks can also be used - the interconnections are under a program control

• Timing, switching and control are the three major operational characteristics that determine the space of all switching networks.

• Synchronous and asynchronous timing controls are possible

• Circuit, packet switching are also possible

• Control strategy - centralized or decentralized

Refer to our notes on MINS - Chapter 2

Hierarchical Bus Systems

A bus system consists of a hierarchy of buses connecting various system and sub-system components in a computer.

Each bus is formed with a number of signal, control, and power lines.

Different buses are used to perform different interconnection functions.

Refer to Fig. 7.2 on page 333, showing the hierarchy of bus systems at different levels

The set of buses include - local busses on boards, back-plane buses, and I/O buses

Local Bus:

• These are the buses implemented on the printed-circuit boards

• On a processor board, this local bus provides a common communication path for most of the chips mounted on the board

• A memory board uses a memory bus to connect the memory with the interface logic

• An I/O board or a network interface board uses a data bus. Each of these board buses consists of signal and utility lines

Back-plane Bus: This is a printed circuit on which there are many connectors are provided to plug in functional boards. A system bus, consisting of shared signal and utility lines is built on the back-plane.

The system bus provides a common communication among all plug-in boards

I/O Bus: Input/Output devices are connected to the system through an I/O bus - SCSI(small computer systems interface) BUS.

Wilson's model (1987) [Refer to Fig. 7.3 on page 335]

• Each processor has a local (private) cache

• A set of processors are grouped to form clusters and these cache memories are referred to as first level caches

• Processors within a cluster can communicate between themselves using the cluster bus, which inter-connects these processors

• The clusters communicate between themselves by using another bus, referred to as inter-cluster bus

• A second level cache is also provided between each cluster bus and the inter-cluster bus.

• Each second-level cache must have a capacity that is at least an order of magnitude larger than the sum of the capacities of all first-level caches connected beneath it.

• Each single cluster operates as a single bus system. Snoopy cache coherence protocols are used to establish consistency among the first level caches belonging to the same cluster.

• Second-level caches are used to extend consistency from each local cluster to the upper level