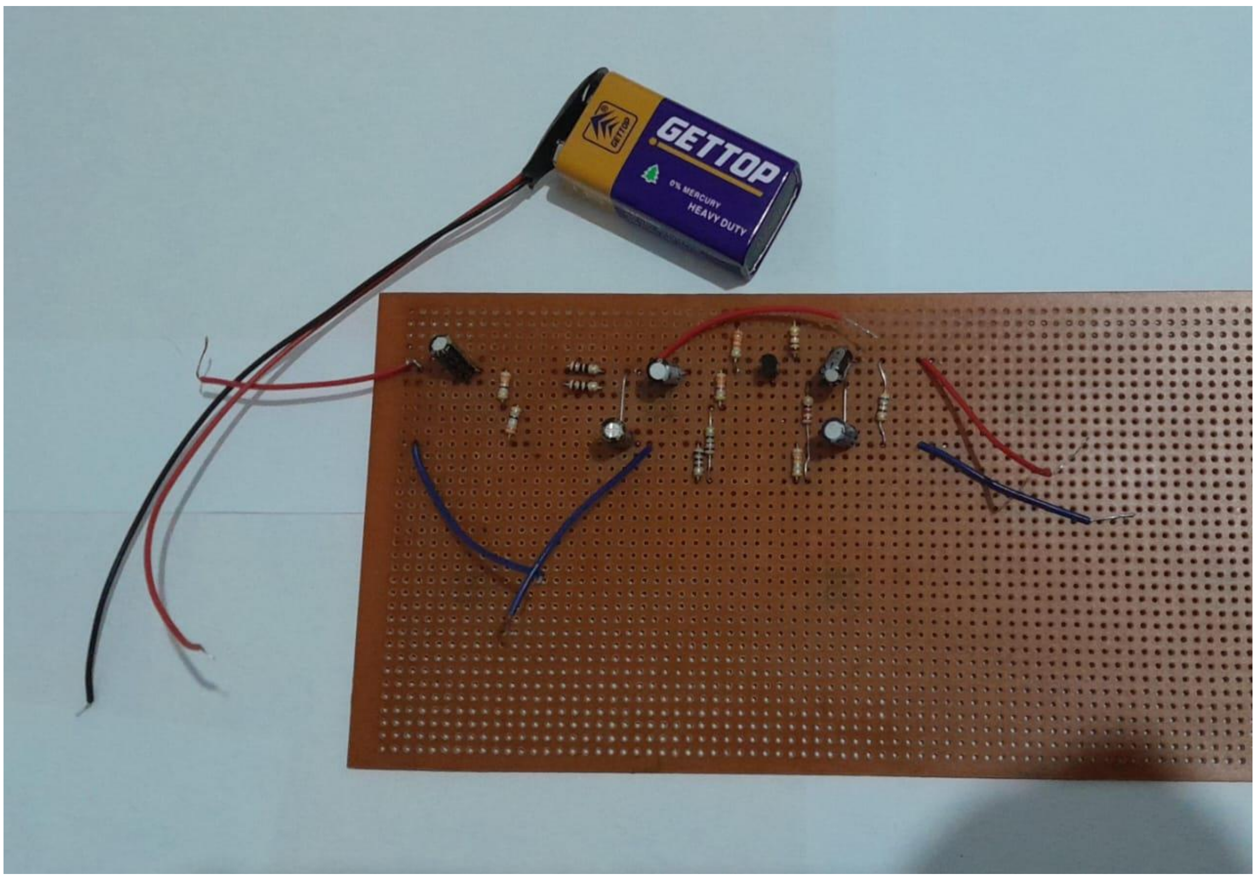
Analog Electronics

Assignment

Title: Design and Implementation of a Multi-stage Amplifier and Filtering circuit	
Batch Number: CSNE Y2S1 (WE)	Group Number: WE_03



Declaration:

We hold a copy of this assignment that we can produce if the original is lost or damaged.

We hereby certify that no part of this assignment has been copied from any other group's work or from any other source. No part of this assignment has been written / produced for our group by another person except where such collaboration has been authorized by the subject lecturer/tutor concerned.

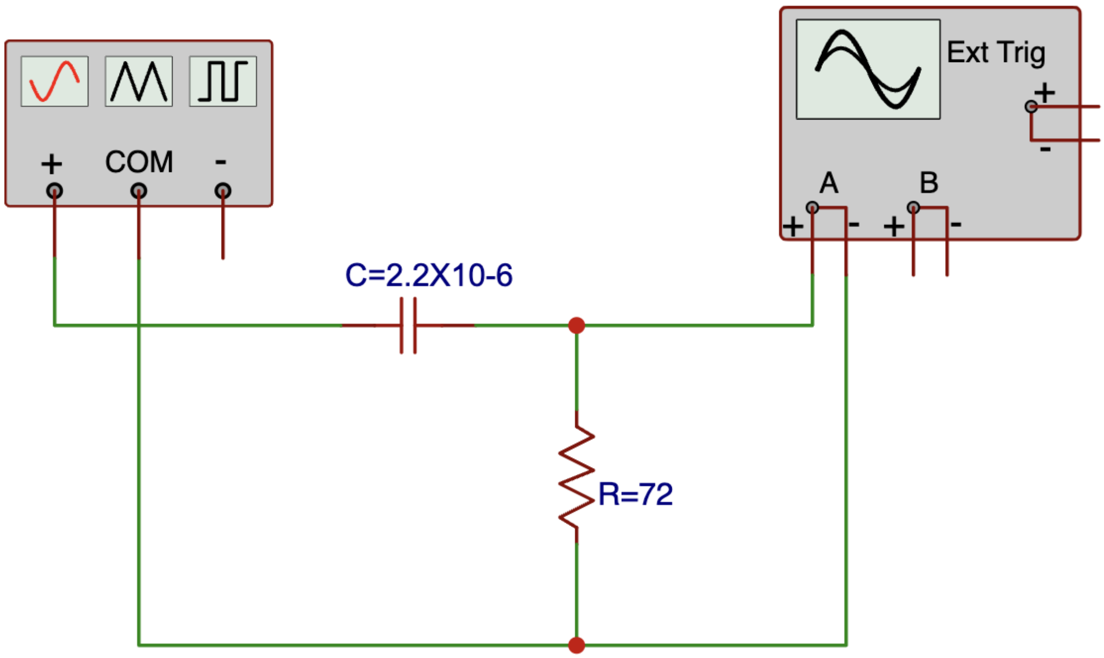
Group Members:

IT23184176 Wanniarachchi C P ………………………… signature 

IT21258176 Fernando W.W.S.M ………………………… signature 

Submitted on: <06/10/2024>

High Pass Filter



The cutoff frequency of fc for a high-pass filter is determined by the resistor R and capacitor C in the circuit. The formula is,

$$f_c = \frac{1}{2\pi RC}$$

$$RC = \frac{1}{2\pi f_c}$$

$$= \frac{1}{2\ X\ \pi\ X\ 1000}$$

$$= 1.592\ X\ 10^{-6}$$

$$\approx (72)\ X\ (2.2\ X\ 10^{-6})$$

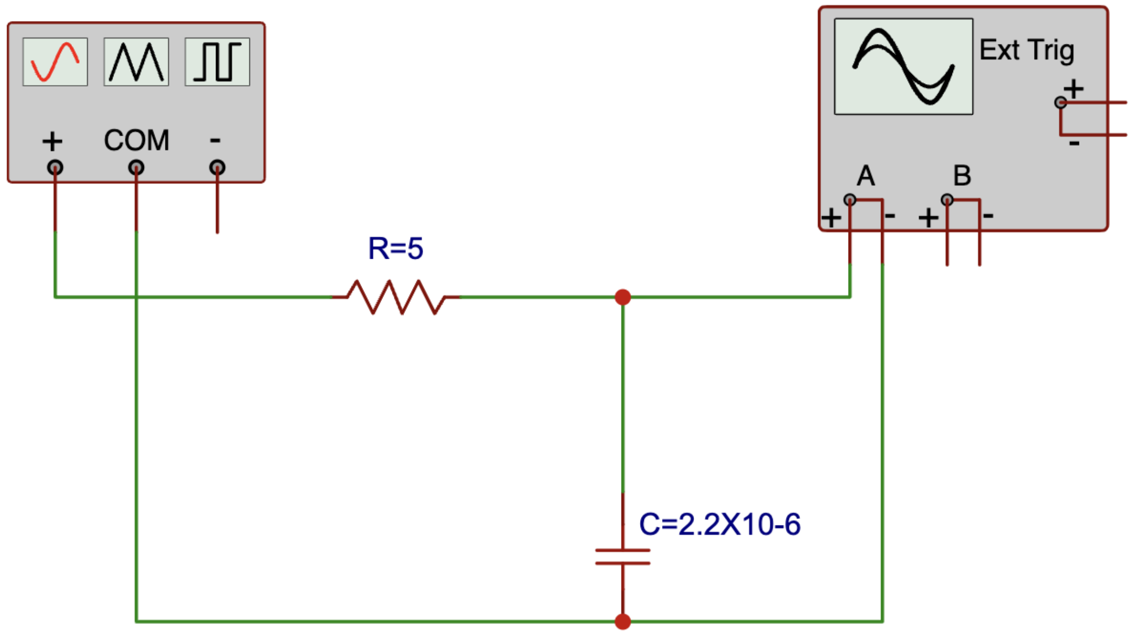
$$Let\ R = 72\Omega$$

$$Therefore, C = 2.2\mu F$$

f_c – High Pass cut off frequency = 1KHz

This ensures that signals with frequencies below 1 kHz are attenuated, while signals above 1 kHz pass through.

Low Pass Filter



For a low-pass filter, the cutoff frequency of fc is also determined by the resistor R and capacitor C

$$f_c = \frac{1}{2\pi RC}$$

$$RC = \frac{1}{2\pi f_c}$$

$$= \frac{1}{2\ X\ \pi\ X\ 15000}$$

$$= 1.061\ X\ 10^{-6}$$

$$\approx (5)\ X\ (2.2\ X\ 10^{-6})$$

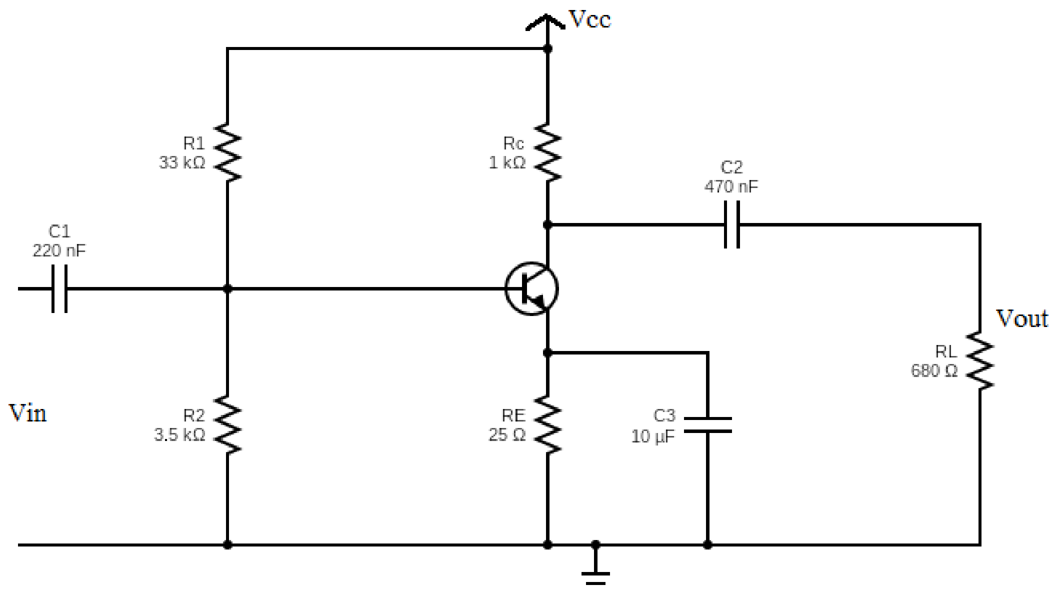
$Let\ R = 5\Omega$

$Therefore, C = 2.2\mu F$

f_c – Low Pass cut off frequency = 15KHz

This allows signals with frequencies below 15 kHz to pass through, while frequencies above 15 kHz are attenuated.

Transistor-Based Common Emitter Amplifier

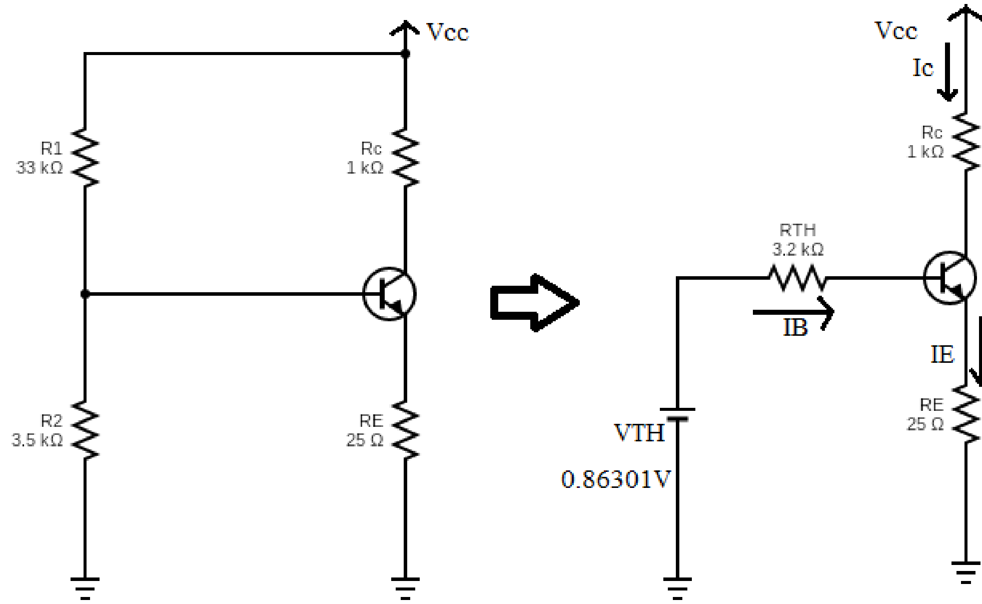


*Vcc=9V

Transistor- BC547 – Low current amplification

- High current gain
- Low noise

(DC stage analysis)



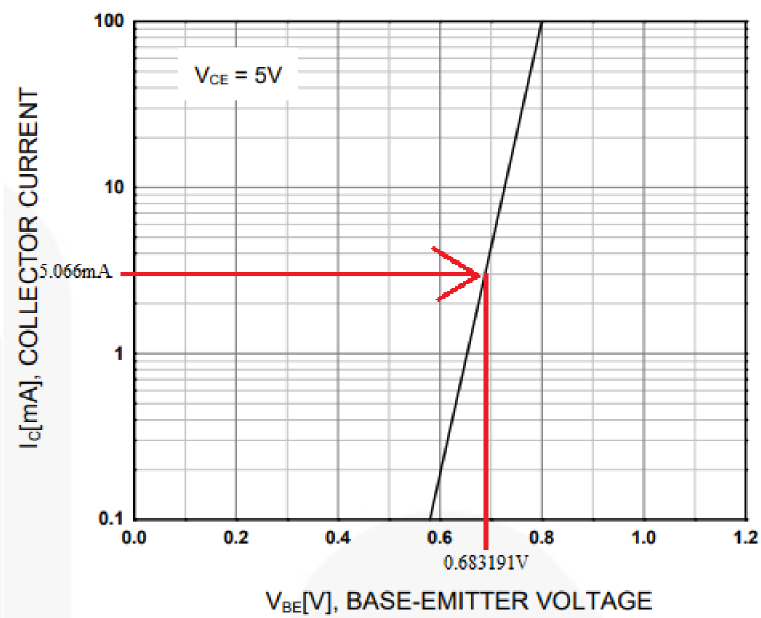


Figure 2. Transfer Characteristic

3C547 / BC548 / BC549 / BC550

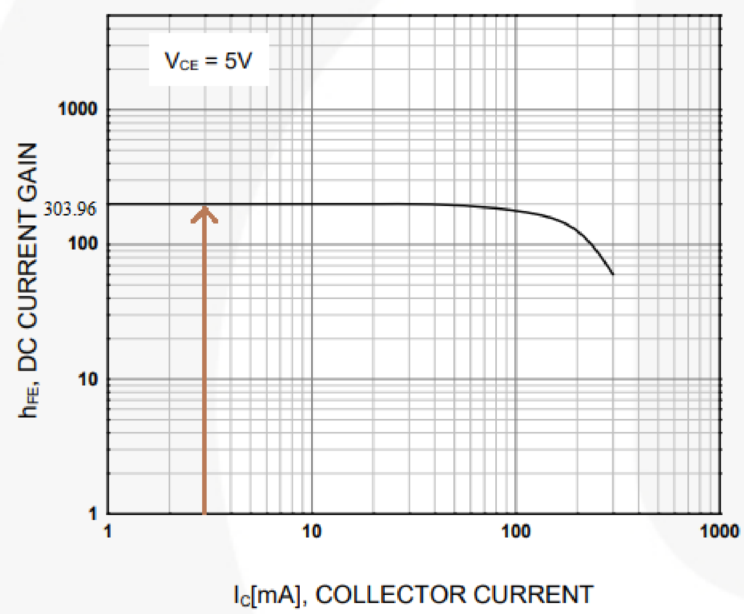


Figure 3. DC Current Gain

Thevenin Resistance (RTH):

When resistors R1 and R2 are arranged in parallel, the Thevenin equivalent resistance RTH is calculated using:

$$R_{TH} = R1||R2 = \frac{R1R2}{R1 + R2} = \frac{33k\ X3.5k}{33k + 3.5k} = 3.16438356164\ kohm$$

This resistance reflects the equivalent resistance seen by the transistor base, simplifying the biasing network

Thevenin Voltage (VTH)

The Thevenin equivalent voltage VTH across R2 and R1 is given by:

$$V_{TH} = \frac{R2}{R1+R2} Vcc = \frac{3.5k}{3.5k+33k}.9V = 0.8630136$$

This voltage is used to set the bias point of the transistor.

$$V_{TH} = R_{TH}I_H + V_{BE} + R_E I_E;\ I_E = (\beta + 1)I_B$$

$$Therefore\ V_{TH} = R_{TH}I_H + V_{BE} + R_E I_E;\ I_E = (\beta + 1)I_B$$

$$V_{TH} = R_{TH}I_B + V_{BE} + R_E(\beta + 1)I_B$$

Base Current

The base current IB is calculated using the following formula.

VBE - Base-Emitter voltage

RE Emitter resistance

β - transistor's current gain(which is got from the data sheet):

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + R_E(\beta + 1)I_B} \; ; \beta = 303.9615846(from\ data\ sheet)$$

$$= \frac{0.8630136 - 0.683191}{3016438356164\ X\ 10^4 + 25(303.9615846 + 1)} = 16.668\mu A$$

From this calculated base current, we can calculate the collector and emitter current

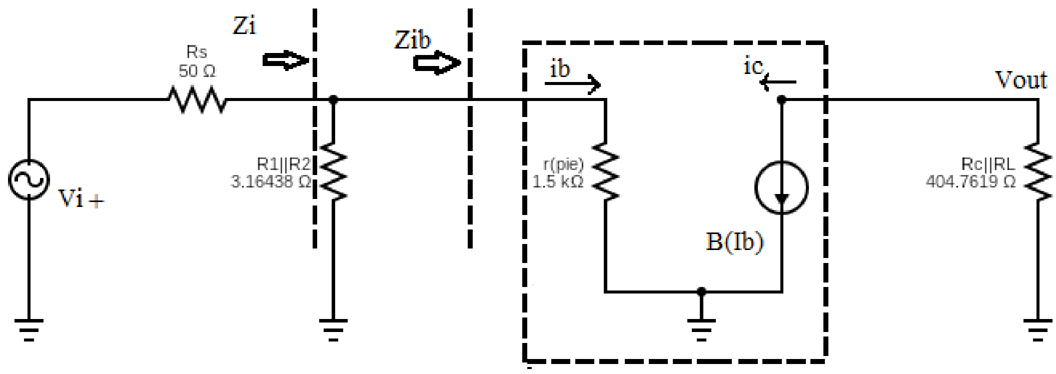
Collector currrent

Collector current and base current is related through current gain β,

$$I_c = \beta I_B = 5.0664mA$$

Emitter Current

$$I_E = (\beta + 1)I_B = 5.083mA$$



Input Resistance (rπ) and Zib:

In small signal model of the transistor input resistance rπ = Zib, (The dynamic resistance looking into the base.)

(VT = thermal voltage-nearly 25mV at room temperature)

$$r_\pi = Z_{ib} = \frac{V_T}{I_B} = \frac{25mV}{16.66\mu A} = 1.5006002\ k\Omega$$

Input Impedance (Zi):

The overall input impedance Zi of the circuit is the resistances R1, R2, and Zib (or rπ).

Simply the total impedance seen by the input signal at the base of the transistor.

$$Z_i = R1|R2|Z_{ib}$$

$$\frac{1}{Z_i} = \frac{1}{R1} + \frac{1}{R2} + \frac{1}{Z_{ib}}$$

$$Z_i = 998.432562\ \Omega$$

Voltage Gain (Av):

The voltage gain of the common emitter amplifier can be calculated by,

(RC||RL is the parallel combination of the collector resistor RC and the load resistor RL)

$$A_v = \frac{V_0}{V_i} = \frac{V_b}{V_i} . \frac{V_0}{V_b}\ ;\ \frac{V_b}{V_i} = \frac{Z_i}{R_E + Z_i}\ ;\ V_b = r_\pi i_b\ ;\quad V_o = -\beta I_b(Rc||RL)$$

$$therefore\ \frac{V_0}{V_b} = \frac{-\beta I_b(Rc||RL)}{r_\pi i_b} = \frac{-\beta(Rc||RL)}{r_\pi}$$

$$Rc||RL = (1k\Omega||680\Omega) = 404.761904\Omega$$

$$A_v = \frac{V_b}{V_i} . \frac{V_0}{V_b}$$

$$= \frac{Z_i}{R_E + Z_i} . \frac{-\beta(Rc||RL)}{r_\pi}$$

$$= \frac{(303.9615846\ X\ \ 404.761904)}{1.5006002\ X\ 1000} = -81.988573$$

The negative sign indicates a 180-degree phase shift between the input and output signals, typical of common emitter amplifiers

Calculating cutoff frequency of C1 coupling capacitor

$$f_c = \frac{1}{2\pi X_c}$$

$$\frac{1}{2\pi Z_i} = \frac{1}{2 * \frac{22}{7} * 0.22\mu * 998.43\Omega} = 724.569\ Hz$$

Calculating cutoff frequency of C2 coupling capacitor

$$f_c = \frac{1}{2\pi X_c} \qquad ; Xc = Z_o = Rc||RL = 404.76\Omega$$

$$= \frac{1}{2\pi Z_i} = \frac{1}{2 * \frac{22}{7} * 0.47\mu * 404.76\Omega} = 836.61 Hz$$

Choosing bypass capacitor value

Our target to effectively bypass the emitter resistor RE at the desired frequency(fc).

Fc - > The frequency at which we want the capacitor to start bypassing RE.

(Typically this is chosen to be around the lower cut off frequency of the amplifier)

For 1kHz -> let’s select fc=835.27Hz(in parallel to get the cap value from market).

So, $C_E \geq \frac{1}{2\pi fcRE}$

$$\geq \frac{1}{2\pi * 835.27Hz * 25\Omega} = 7.62172\ \mu F$$

So we selected 10μF which is >= 7.62172 μF

IC Range for Common-Emitter Amplifiers(for small signal amplifiers)

For **small-signal** amplifiers, it typically ranges from **1 mA to 10 mA**.

Our calculated current level (5.066 mA) is high enough to drive the output without compromising on gain, but not too high to cause thermal issues.

Keeping VC=VCC/2 in a common-emitter amplifier

1.To maximize Voltage Swing (Signal Handling Capacity)

The signal can swing equally in both directions (positive and negative) before it hits the supply voltage rail (saturation) or ground (cutoff).

2. To avoid Saturation and Cutoff

3. To ensure linearity

4. To Bias Stability:

Because of that any **temperature variations** or **parameter changes** (like in β) do not push the transistor too close to saturation or cutoff.

Concept of Bypass capacitor

RE is used to provide negative feedback and stabilize the DC operaring point(Q-point).

But RE reduce AC-gain. (because the presence of emitter resistance limits the voltage drop across the collector load Rc.)

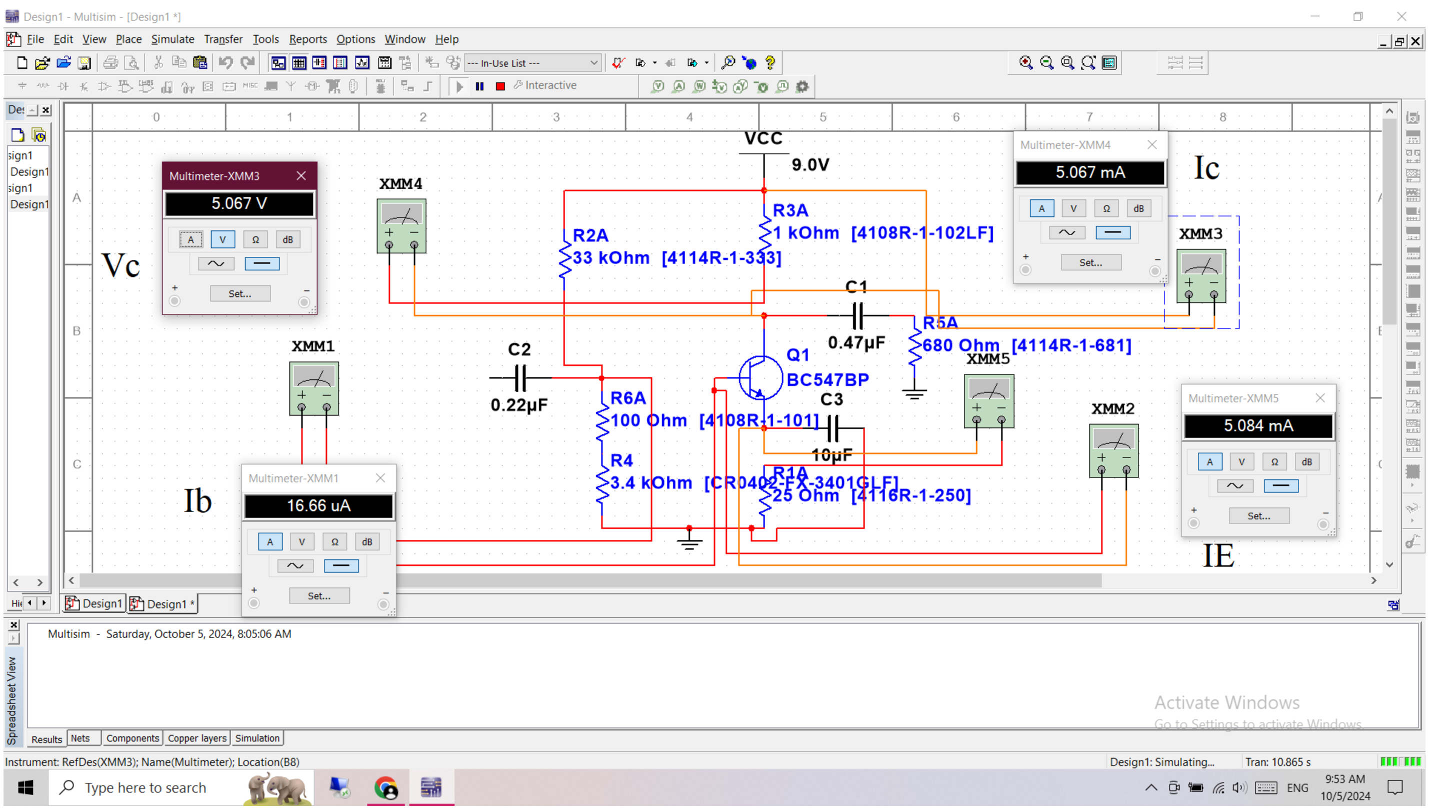
So to bypass the effect of AC signal(but still keeping RE to do his task at DC stage) we are using a capacitor in parallel with RE emitter resistor. So that AC signals wil bypass the emitter resistance and go through the capacitor. And it still allows RE to control the DC bias stage.

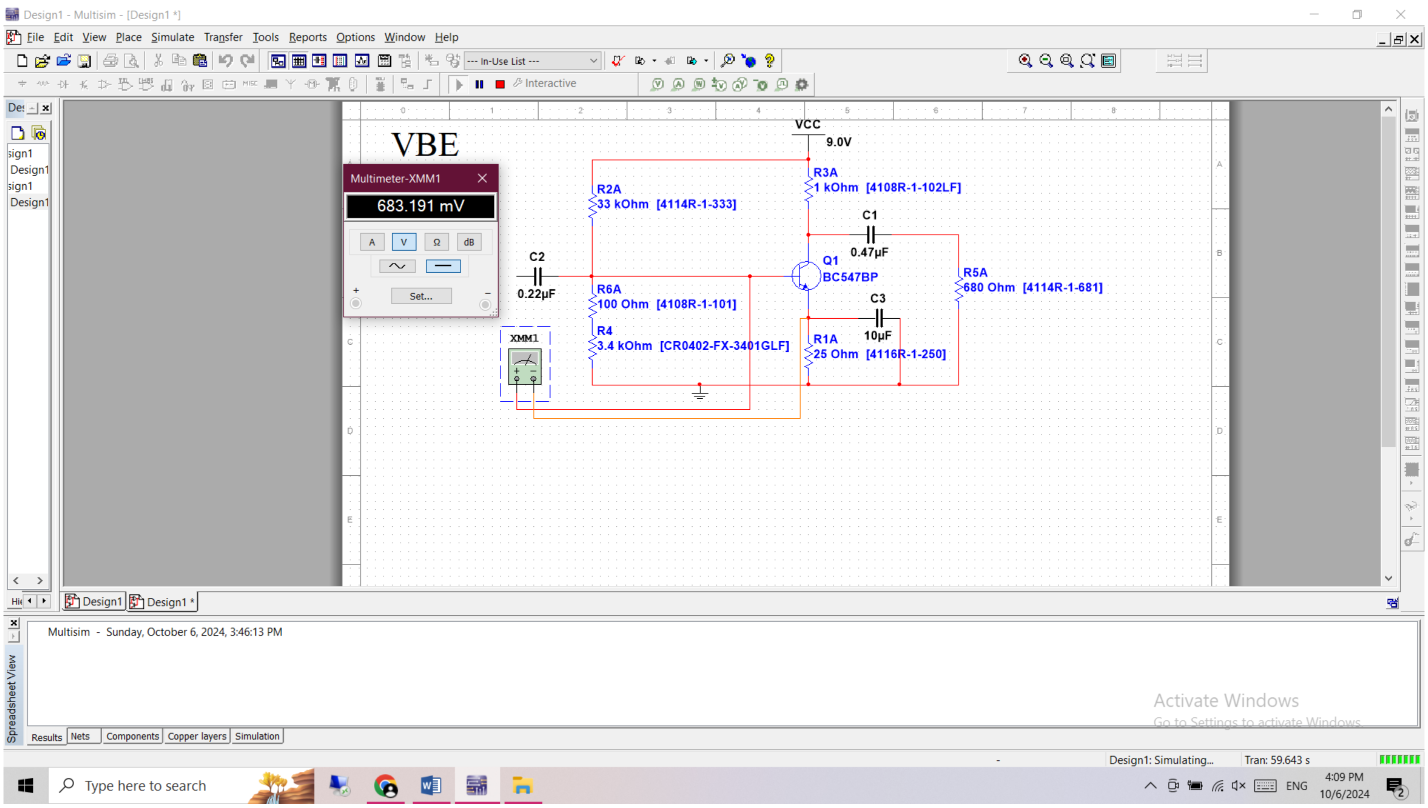
Simply,

1.For DC bias stage it acts like a open circuit by not allowing DC current to pass through it.

2. For AC signals it(bypass capacitor) acts as a short circuit by allowing AC signals to pass through it.

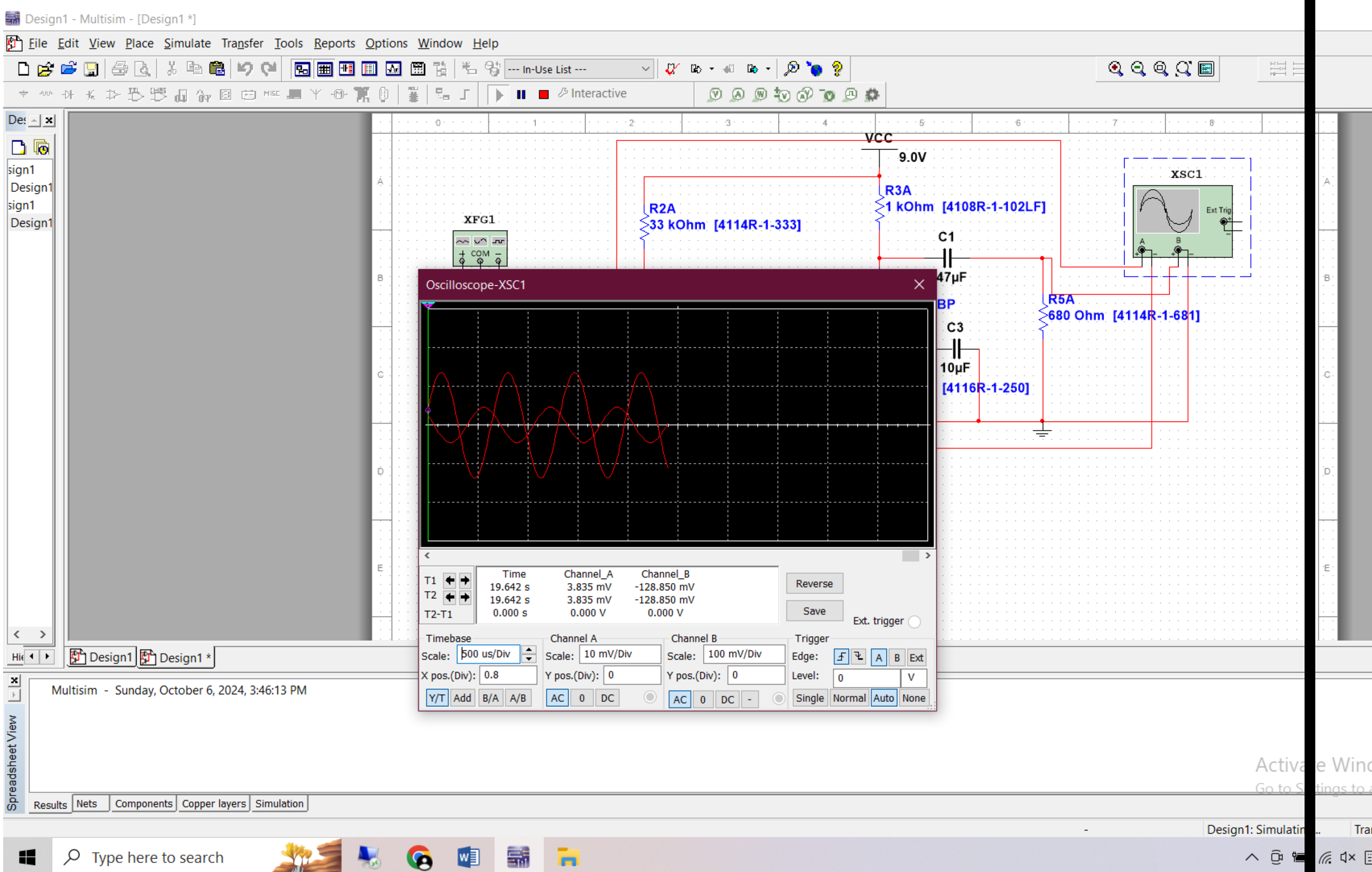
At DC bias stage readings for each calculated currents and voltage values



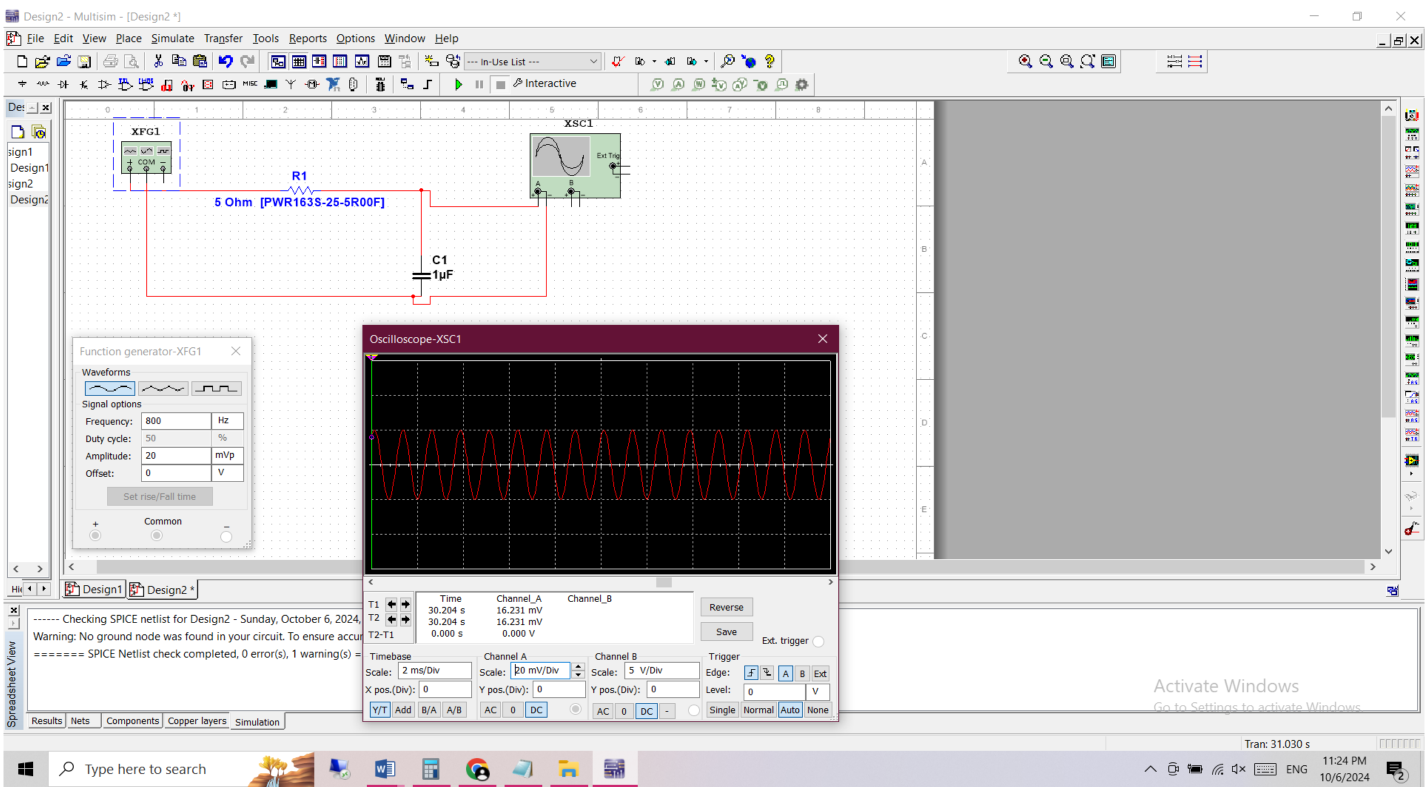


Design1 - Multisim - [Design1 *]
File Edit View Place Simulate Transfer Tools Reports Options Window Help
VBE
Multimeter-XMM1
683.191 mV
VCC
9.0V
R3A
1 kOhm [4108R-1-102LF]
R2A
33 kOhm [4114R-1-333]
C1
0.47µF
C2
0.22µF
Q1
BC547BP
R5A
680 Ohm [4114R-1-681]
R6A
100 Ohm [4108R-1-101]
C3
10µF
R4
3.4 kOhm [CR0402-FX-3401GLF]
R1A
25 Ohm [4116R-1-250]
XMM1
Multisim - Sunday, October 6, 2024, 3:46:13 PM
Design1: Simulating...
Tran: 59.643 s
4:09 PM
10/6/2024

AC signal given to the amplifier circuit (without filters)

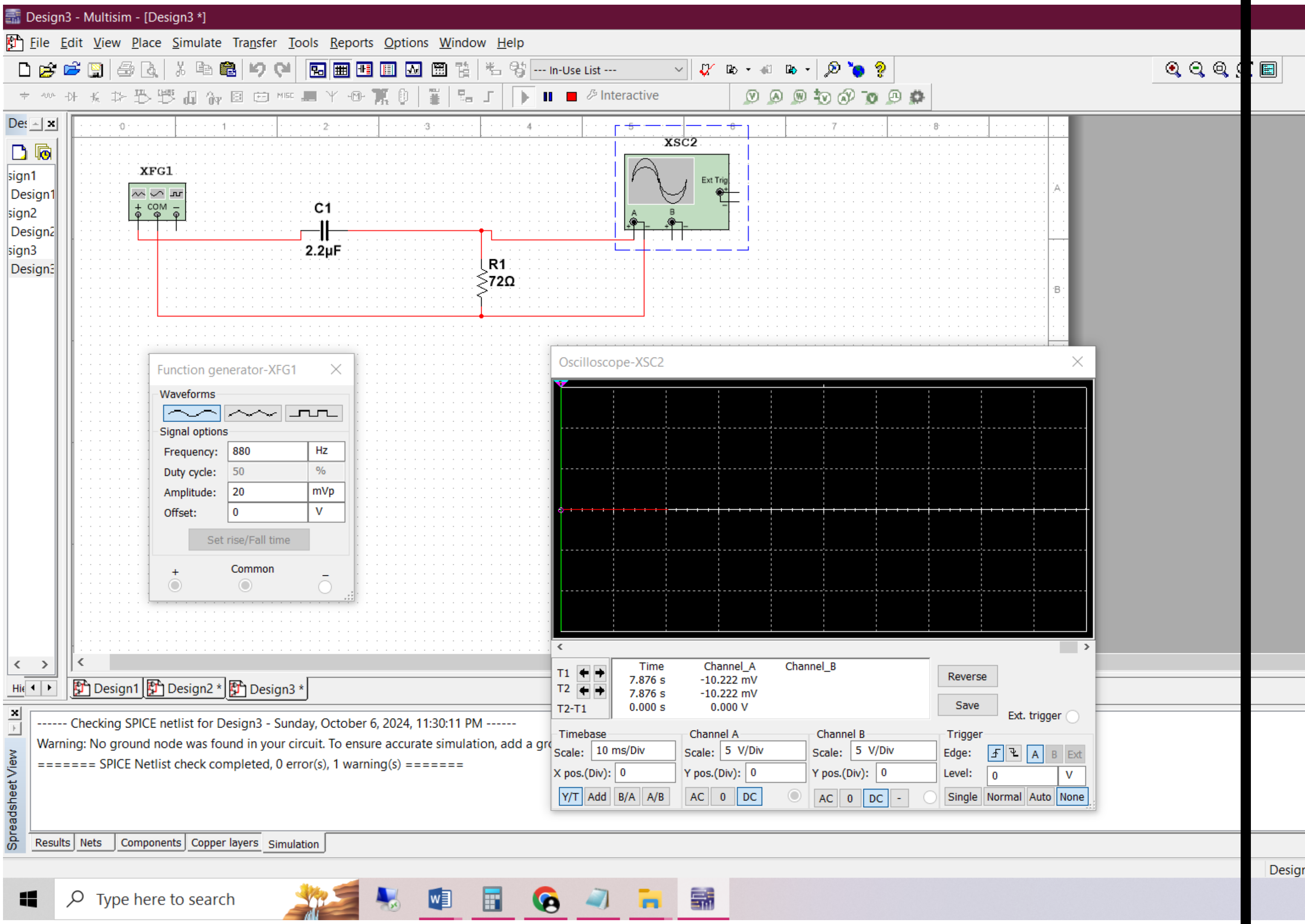


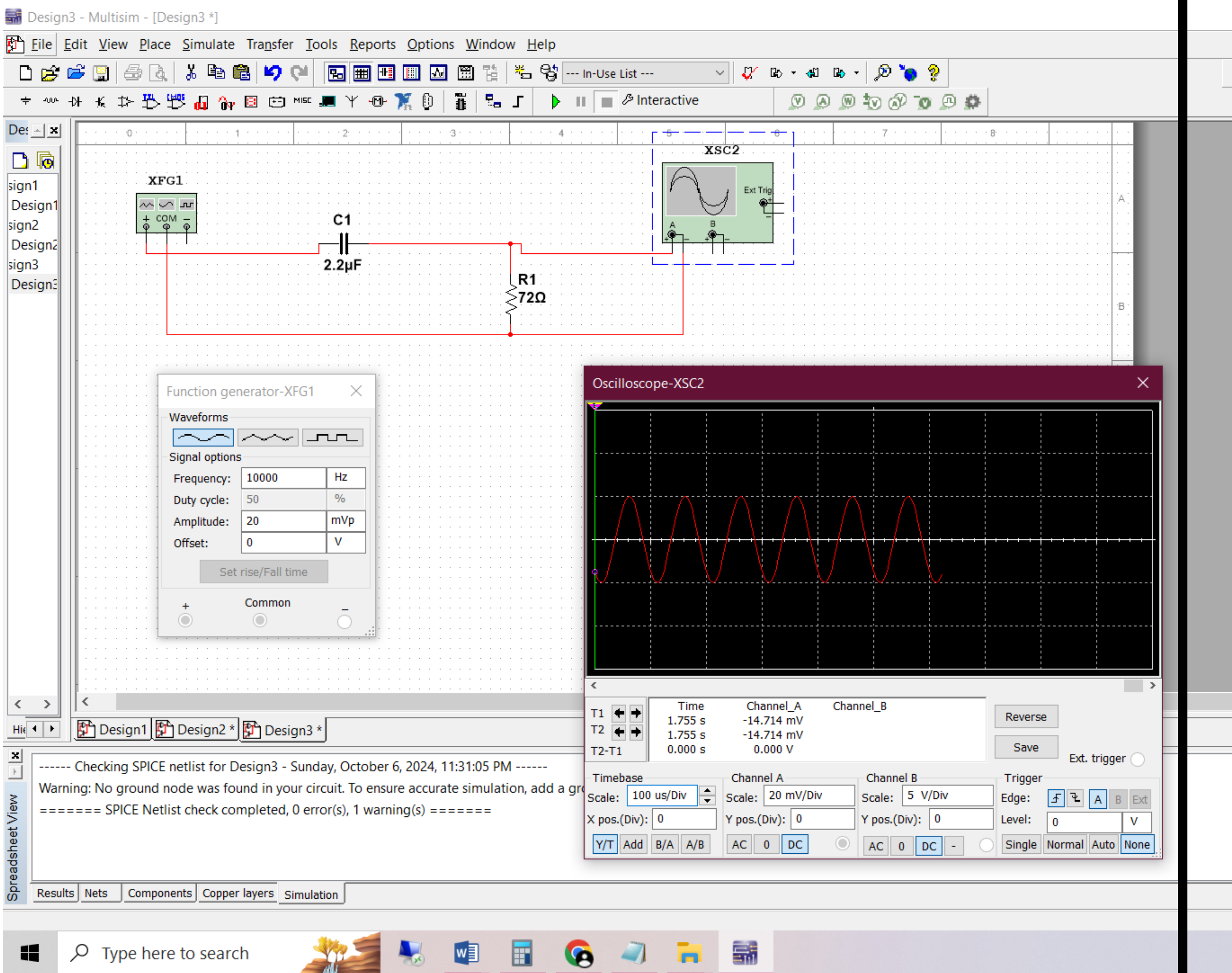
Low Pass



Design2 - Multisim - [Design2 *]
XFG1
R1
5 Ohm [PWR163S-25-5R00F]
C1
1µF
XSC1
Function generator-XFG1
Frequency: 800 Hz
Amplitude: 20 mVp
Offset: 0 V
Oscilloscope-XSC1
Timebase Scale: 2 ms/Div
Channel A Scale: 20 mV/Div
Channel B Scale: 5 V/Div
------ Checking SPICE netlist for Design2 - Sunday, October 6, 2024,
Warning: No ground node was found in your circuit. To ensure accur
======= SPICE Netlist check completed, 0 error(s), 1 warning(s) =
Tran: 31.030 s

High pass




Design3 - Multisim - [Design3 *]
File Edit View Place Simulate Transfer Tools Reports Options Window Help
--- In-Use List ---
Interactive
XFG1
C1
2.2µF
R1
72Ω
XSC2
Function generator-XFG1
Waveforms
Signal options
Frequency: 10000 Hz
Duty cycle: 50 %
Amplitude: 20 mVp
Offset: 0 V
Set rise/Fall time
Common
Oscilloscope-XSC2
Time Channel_A Channel_B
T1 1.755 s -14.714 mV
T2 1.755 s -14.714 mV
T2-T1 0.000 s 0.000 V
Reverse
Save
Ext. trigger
Timebase Scale: 100 us/Div X pos.(Div): 0
Channel A Scale: 20 mV/Div Y pos.(Div): 0
Channel B Scale: 5 V/Div Y pos.(Div): 0
Trigger Edge: Level: 0 V
Y/T Add B/A A/B AC 0 DC AC 0 DC - Single Normal Auto None
Design1 Design2 * Design3 *
------ Checking SPICE netlist for Design3 - Sunday, October 6, 2024, 11:31:05 PM ------
Warning: No ground node was found in your circuit. To ensure accurate simulation, add a gr
======= SPICE Netlist check completed, 0 error(s), 1 warning(s) =======
Results Nets Components Copper layers Simulation
Spreadsheet View
Type here to search


0% MERCURY
HEAVY DUTY

Thank you!

(for all those who supported)