Fundamental of Digital Design

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Active and Inactive States

ACTIVE – a descriptor denoting an action condition

INACTIVE – a descriptor denoting a condition which in NOT ACTIVE

ACTIVE = Logic ‘1’

INACTIVE = Logic ‘0’

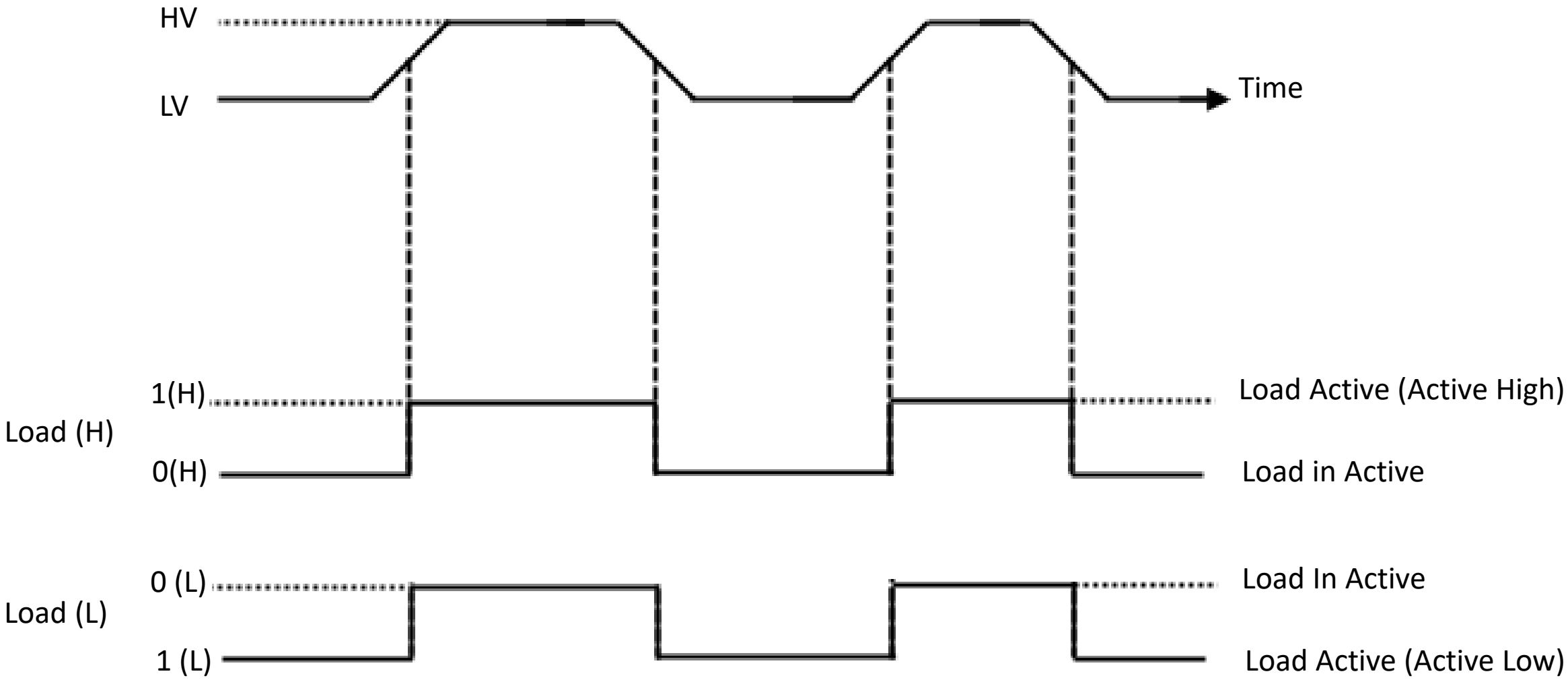
Activation Level Indicators

(H) Meaning ACTIVE HIGH

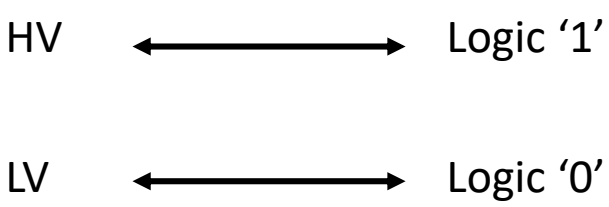
(L) Meaning ACTIVE LOW

Ex : Reset (L)
Load (H)

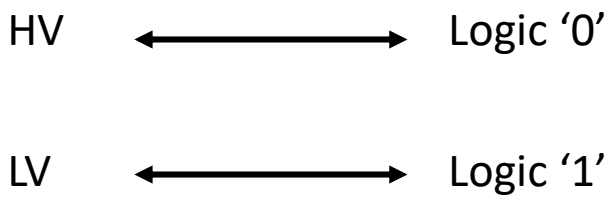
Positive and Negative Logic



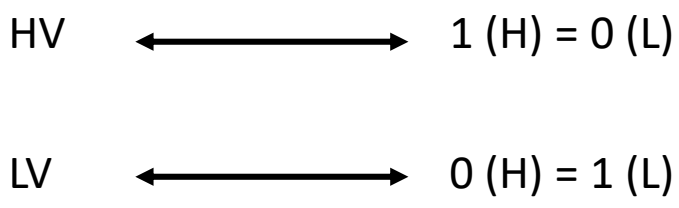
Positive and Negative Logic



Positive Logic System

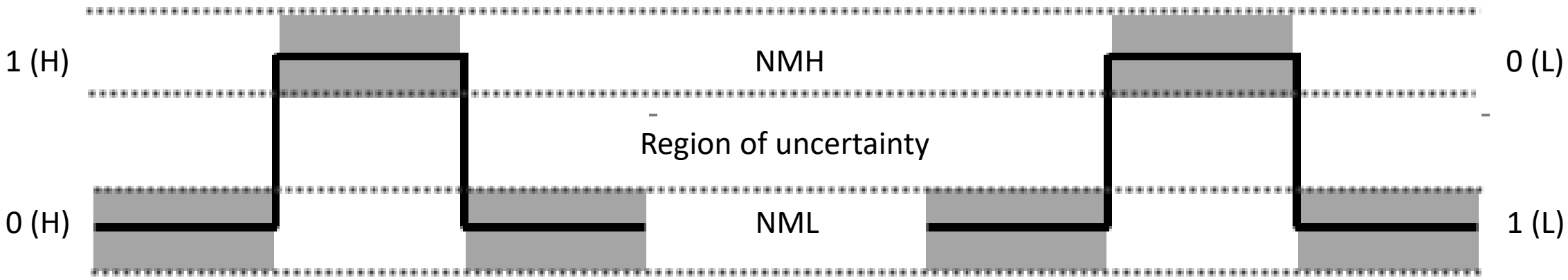


Negative Logic System

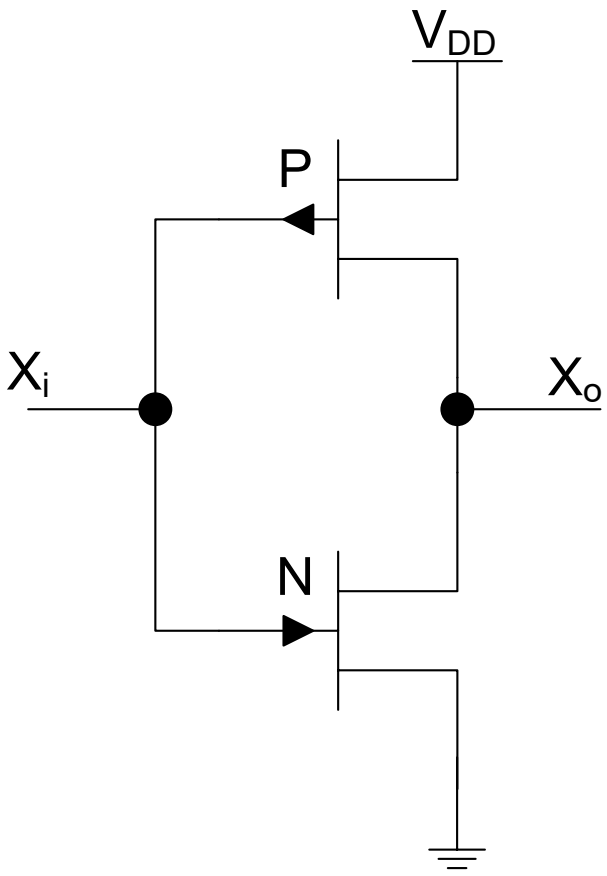


Implication

Positive and Negative Logic



Logic Level Conversion – The Inverter

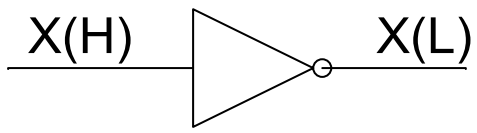


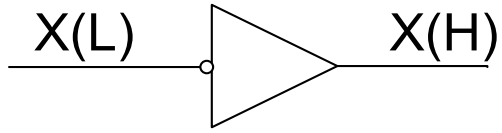
X_i	X_o
0	VDD
VDD	0

X_i	X_o
LV	HV
HV	LV

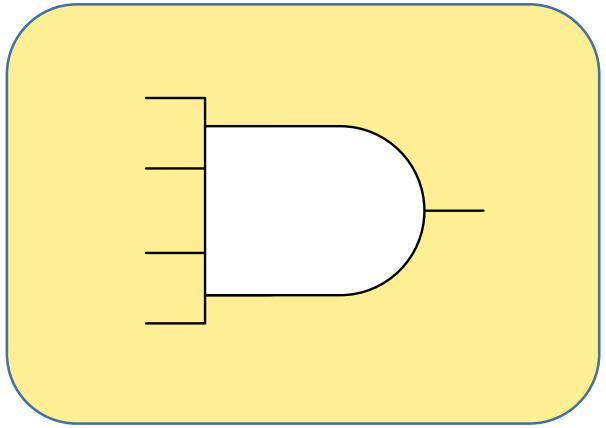
X(H)	X(L)
0	0
1	1

X(L)	X(H)
1	1
0	0



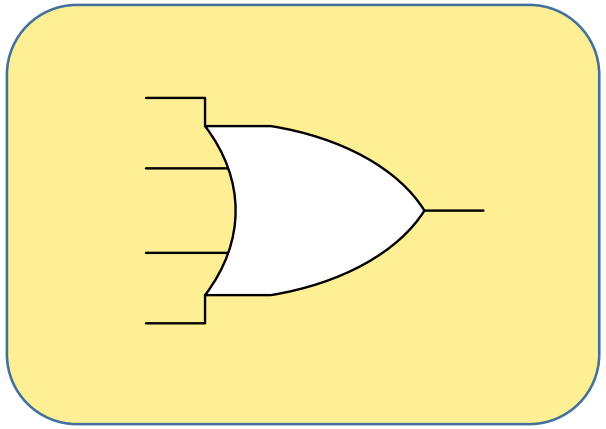


AND and OR



The outputs of a logic AND circuit is ACTIVE if, and only if, ALL inputs are ACTIVE

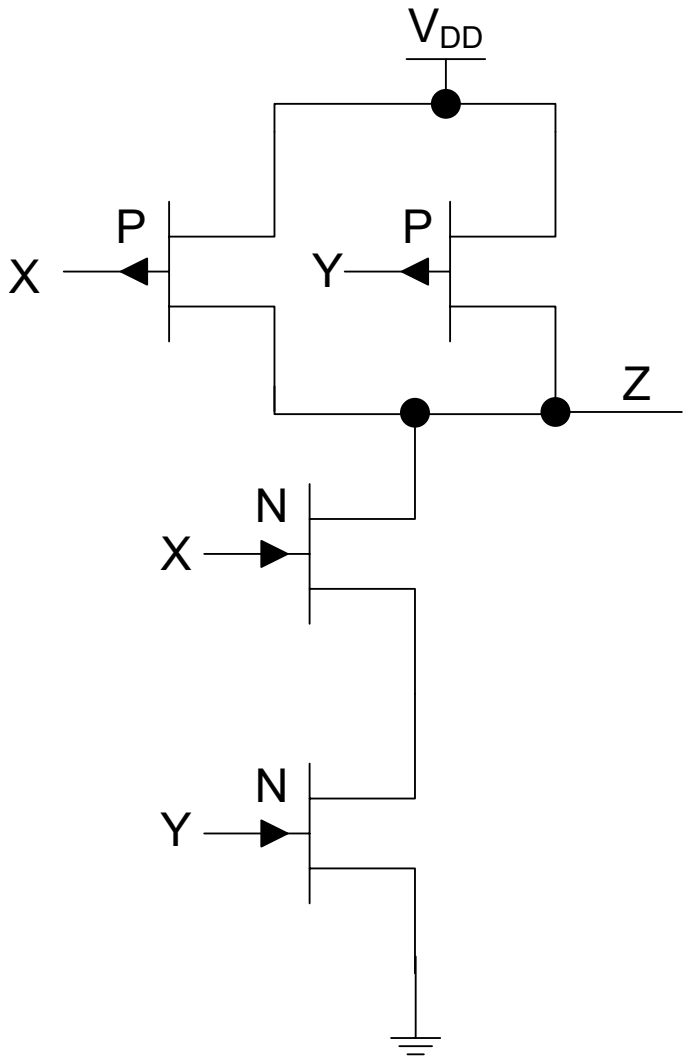
$$Y = A \cdot B \cdot C \cdot \ \ldots \cdot Z$$



The outputs of a logic OR circuit is ACTIVE if, one or more of the inputs are ACTIVE

$$Y = A + B + C + \ \ldots + Z$$

NAND gate realization of AND and OR (1)



X	Y	Z
0	0	5
0	5	5
5	0	5
5	5	0

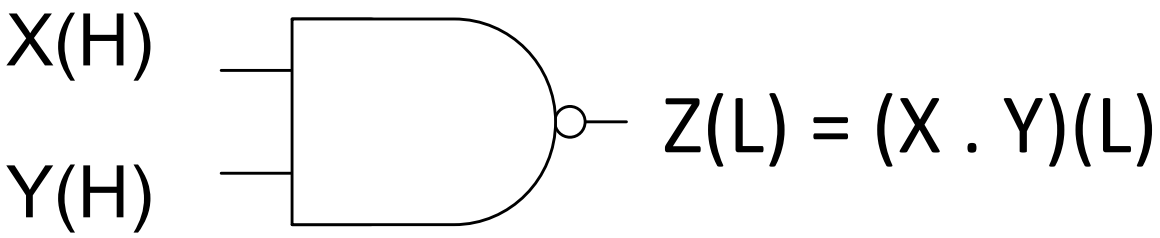
X	Y	Z
LV	LV	HV
LV	HV	HV
HV	LV	HV
HV	HV	LV

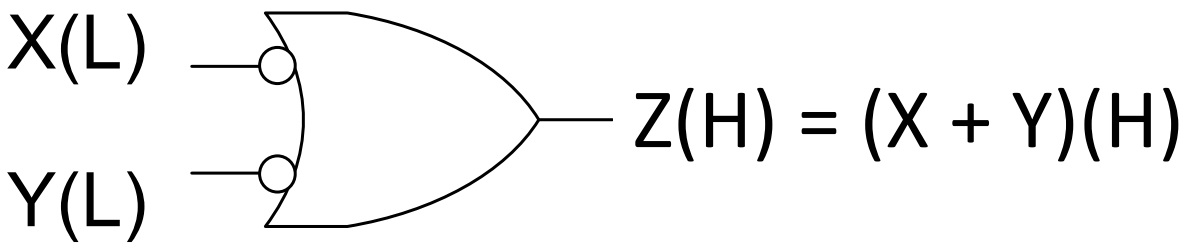
NAND gate realization of AND and OR (2)

X(H)	Y(H)	Z(L)
0	0	0
0	1	0
1	0	0
1	1	1

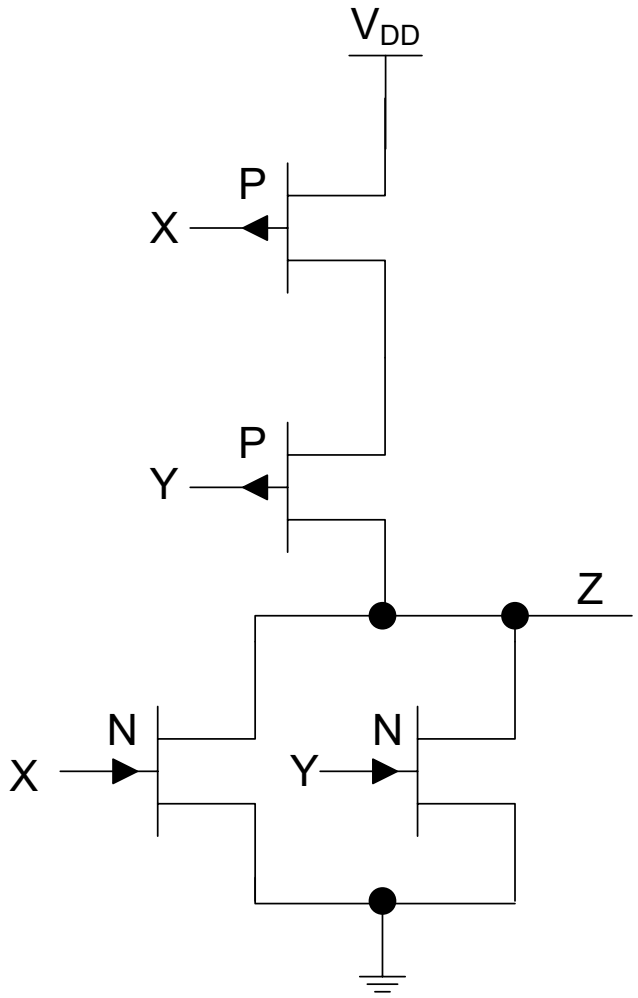
X	Y	Z
LV	LV	HV
LV	HV	HV
HV	LV	HV
HV	HV	LV

X(L)	Y(L)	Z(H)
1	1	1
1	0	1
0	1	1
0	0	0





NOR gate realization of AND and OR (1)



X	Y	Z
0	0	5
0	5	0
5	0	0
5	5	0

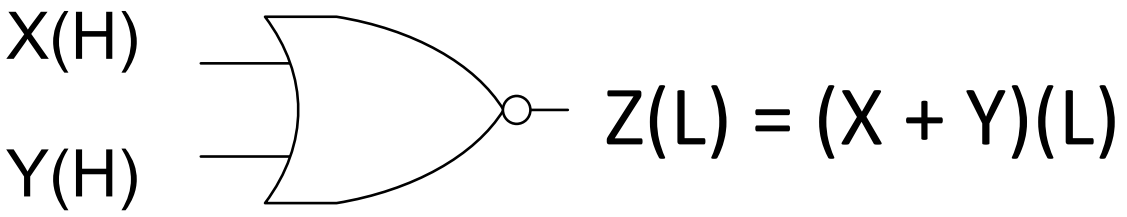
X	Y	Z
LV	LV	HV
LV	HV	LV
HV	LV	LV
HV	HV	LV

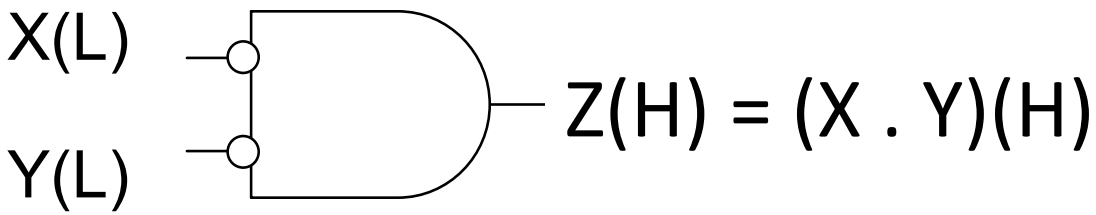
NOR gate realization of AND and OR (2)

X(H)	Y(H)	Z(L)
0	0	0
0	1	1
1	0	1
1	1	1

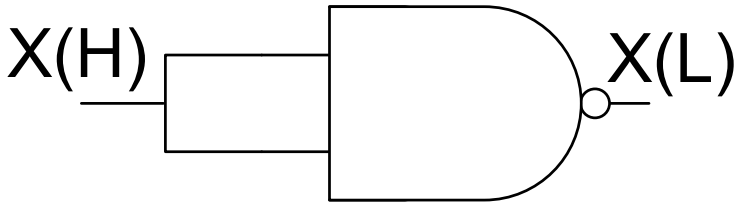
X	Y	Z
LV	LV	HV
LV	HV	LV
HV	LV	LV
HV	HV	LV

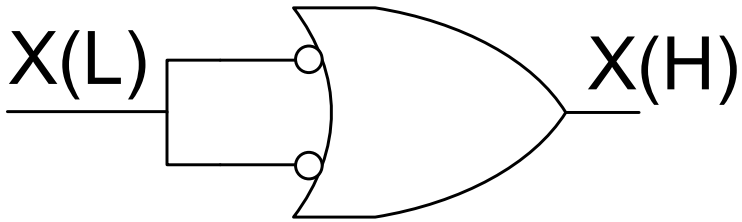
X(L)	Y(L)	Z(H)
1	1	1
1	0	0
0	1	0
0	0	0

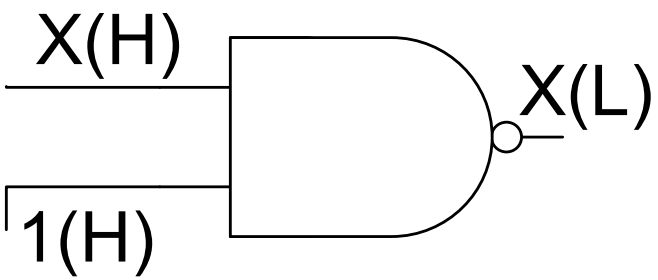


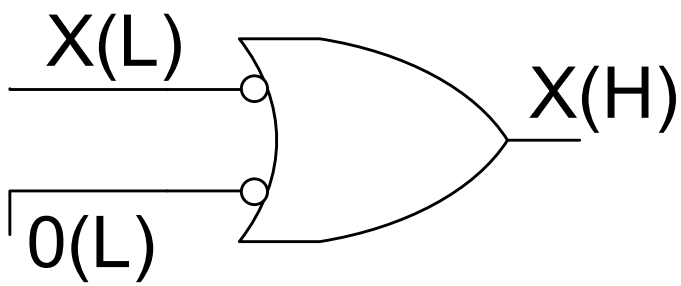


NAND and NOR Logic Level Conversion

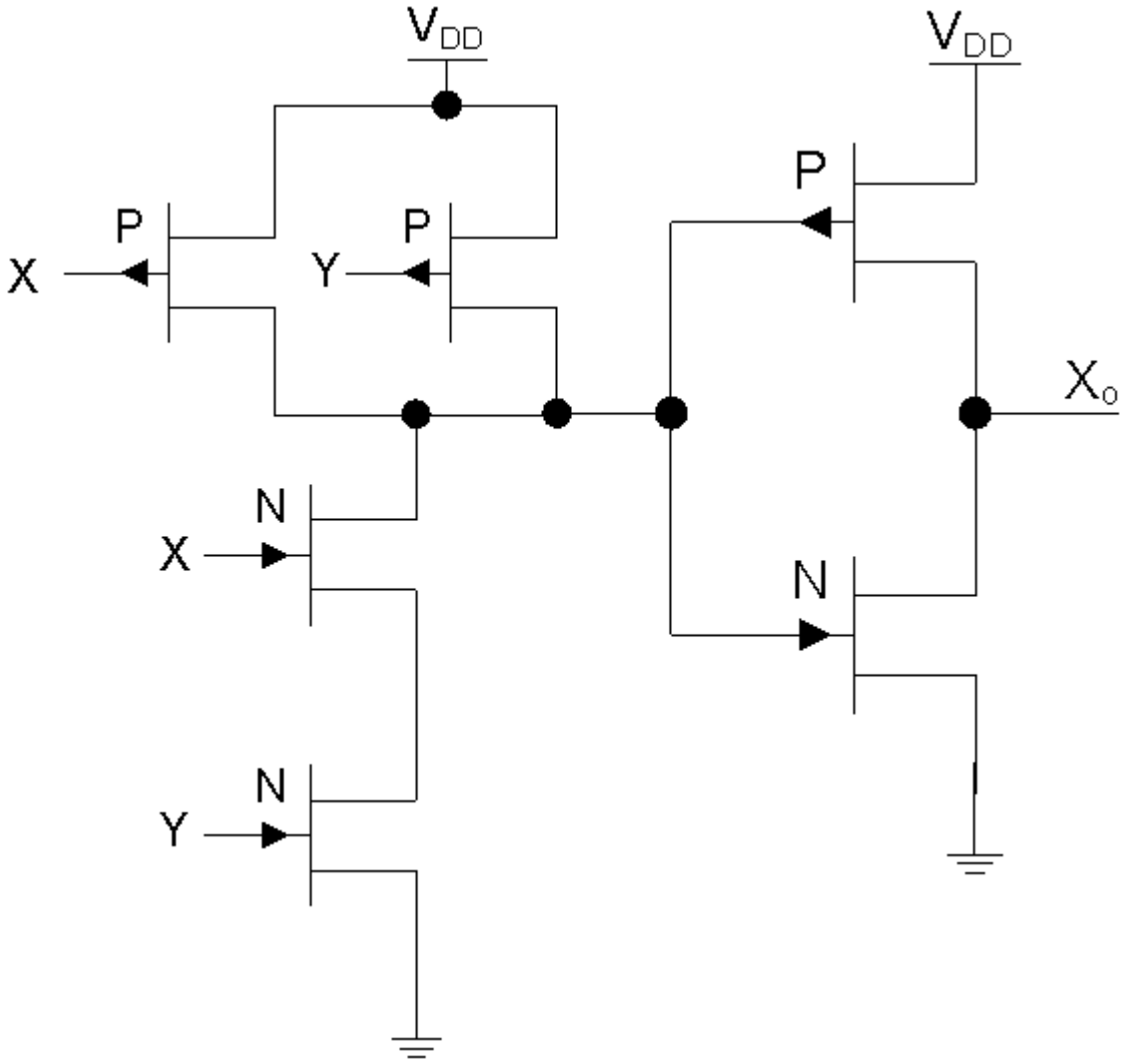








AND gate realization of AND and OR (1)



X	Y	Z
0	0	0
0	5	0
5	0	0
5	5	5

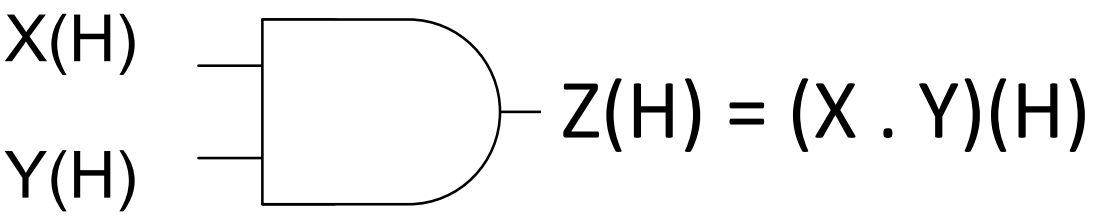
X	Y	Z
LV	LV	LV
LV	HV	LV
HV	LV	LV
HV	HV	HV

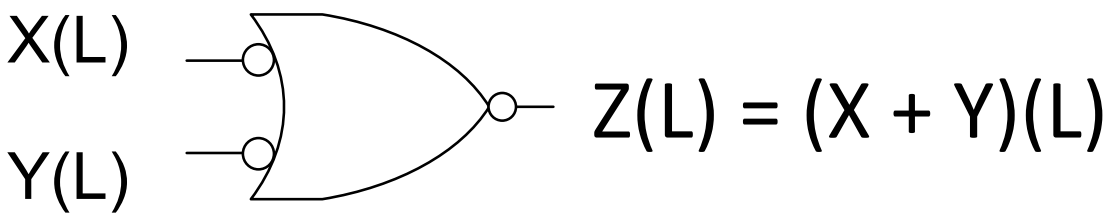
AND gate realization of AND and OR (2)

X(H)	Y(H)	Z(H)
0	0	0
0	1	0
1	0	0
1	1	1

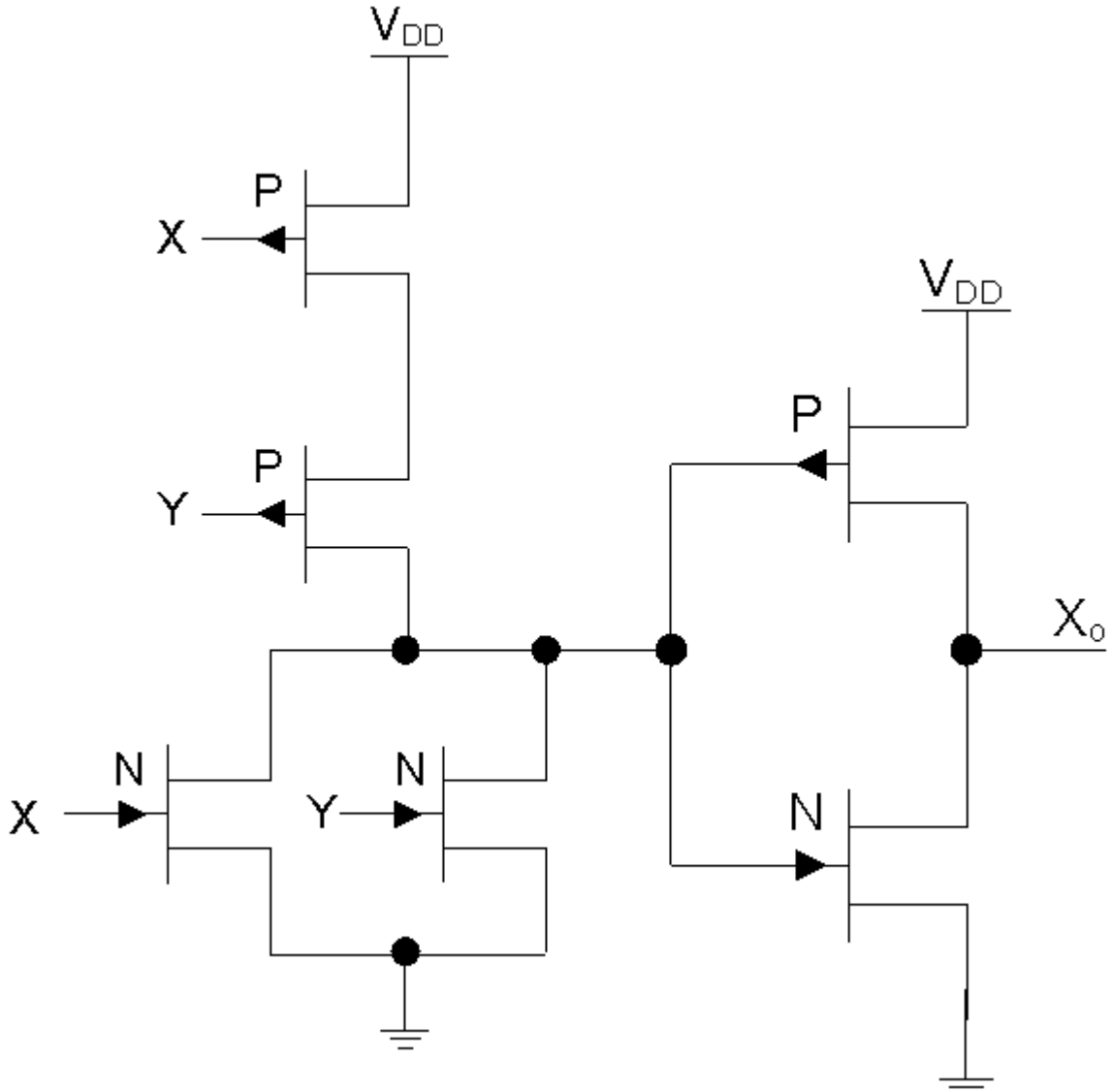
X	Y	Z
LV	LV	LV
LV	HV	LV
HV	LV	LV
HV	HV	HV

X(L)	Y(L)	Z(L)
1	1	1
1	0	1
0	1	1
0	0	0





OR gate realization of AND and OR (1)



X	Y	Z
0	0	0
0	5	5
5	0	5
5	5	5

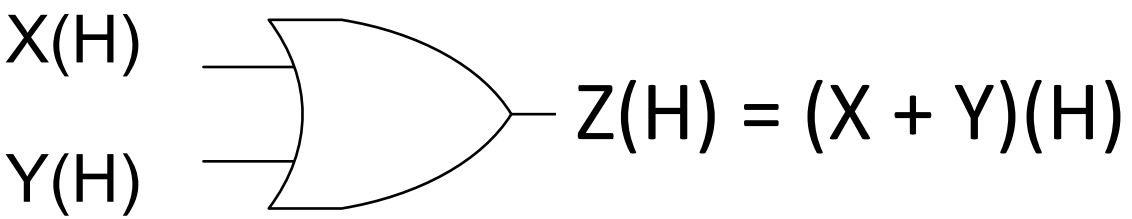
X	Y	Z
LV	LV	LV
LV	HV	HV
HV	LV	HV
HV	HV	HV

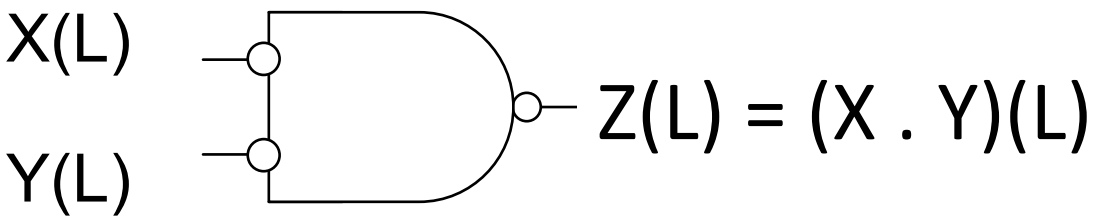
OR gate realization of AND and OR (2)

X(H)	Y(H)	Z(H)
0	0	0
0	1	1
1	0	1
1	1	1

X	Y	Z
LV	LV	LV
LV	HV	HV
HV	LV	HV
HV	HV	HV

X(L)	Y(L)	Z(L)
1	1	1
1	0	0
0	1	0
0	0	0

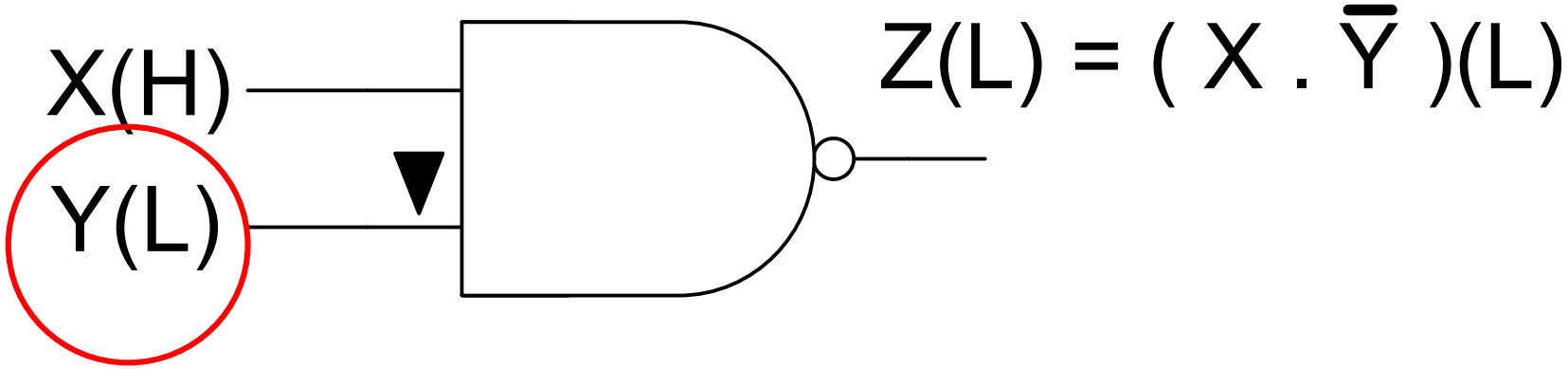




Logic Level Incompatibility

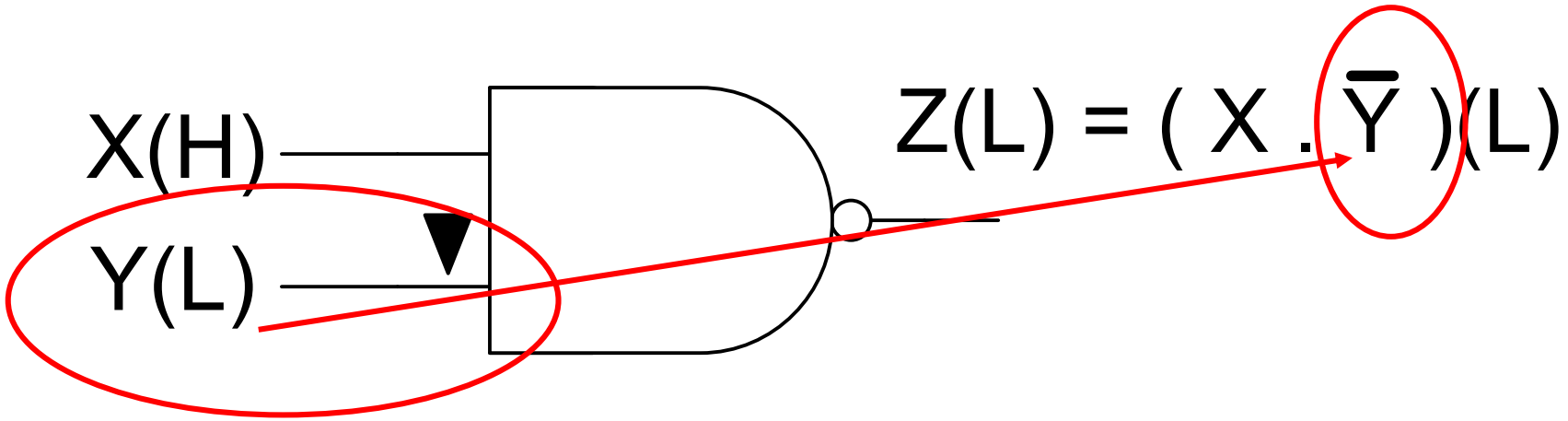
The input logic level doesn't meet with line input gate logic level

Place the incompatibility "∇" flag on the line input gate to indicate incompatibility logic level



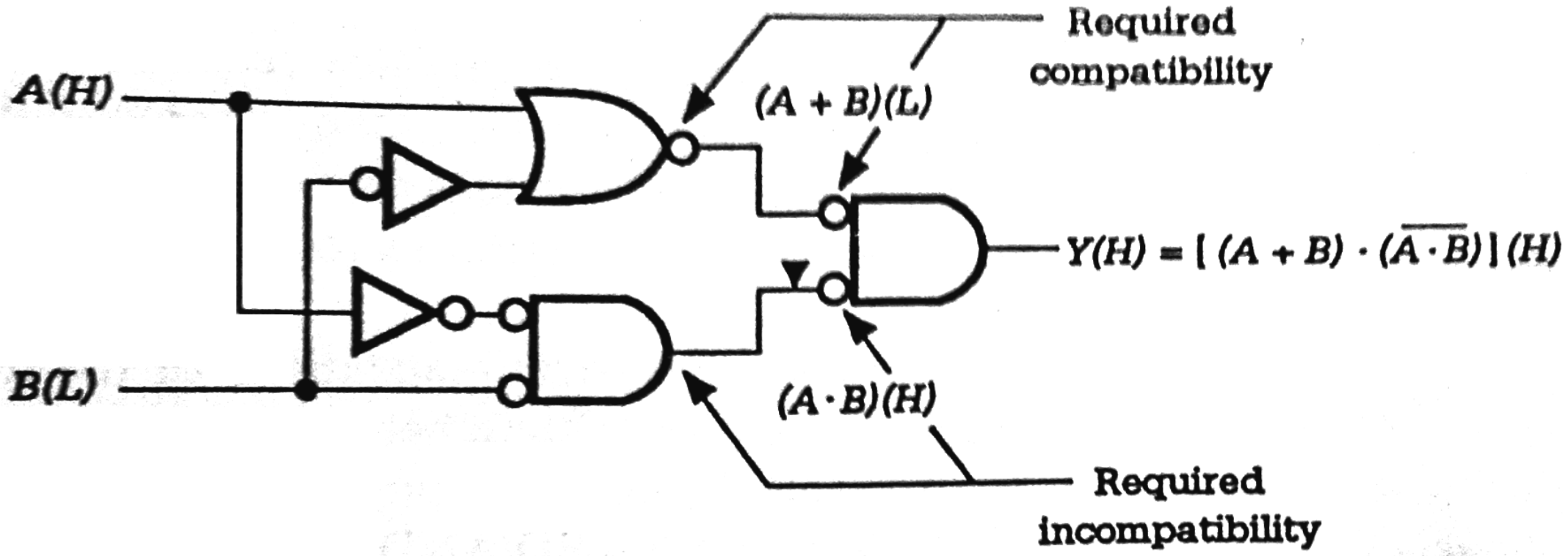
Complement

$$\alpha(L) = \bar{\alpha}(H) \qquad \bar{\alpha}(L) = \alpha(H)$$

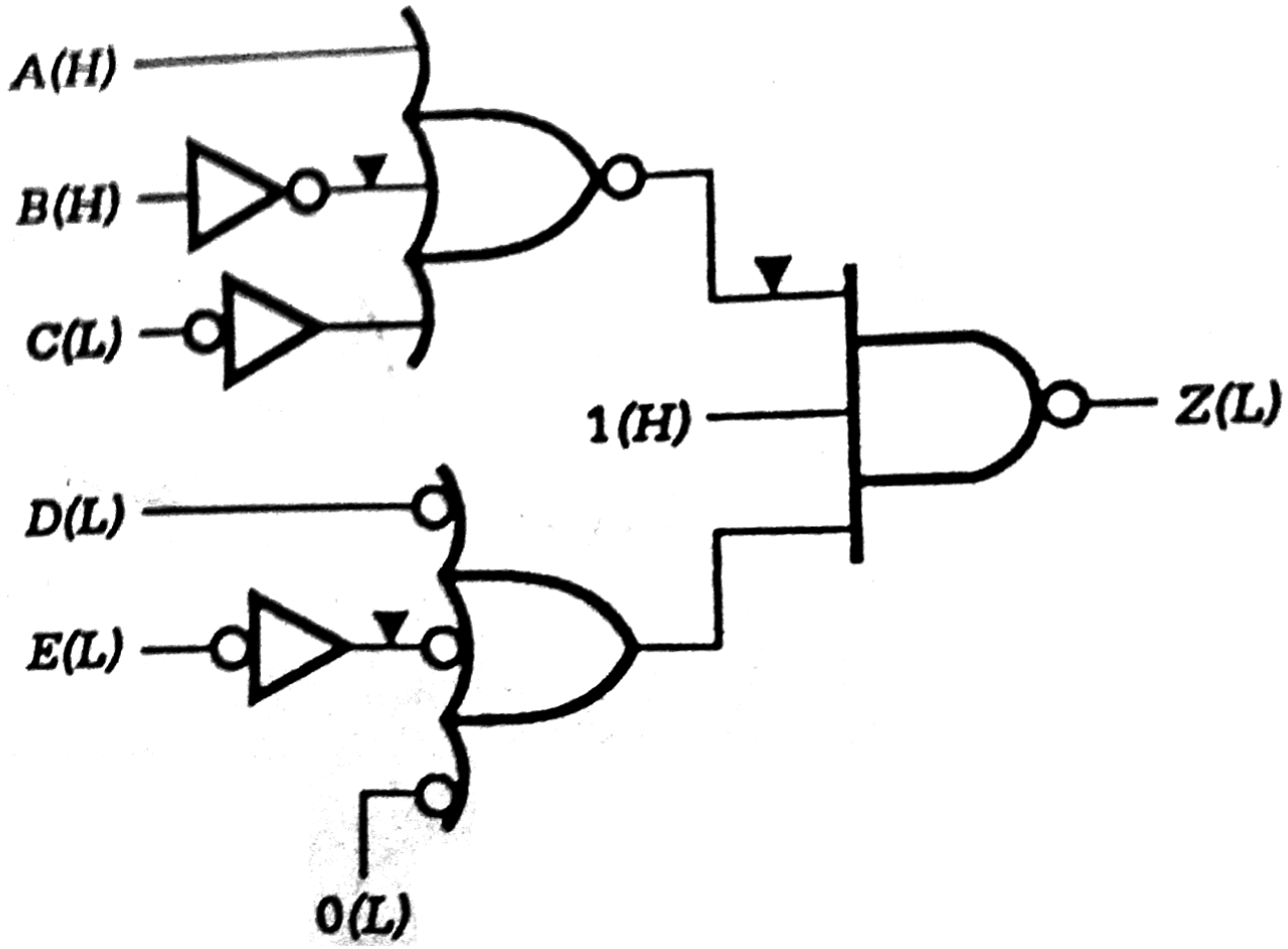


Reading of Logic circuit

" Input to Output State "



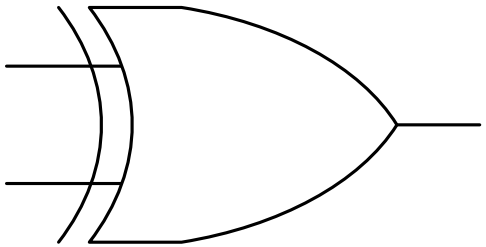
Construction of Logic circuit



" Output to Input State "

Function XOR and EQV

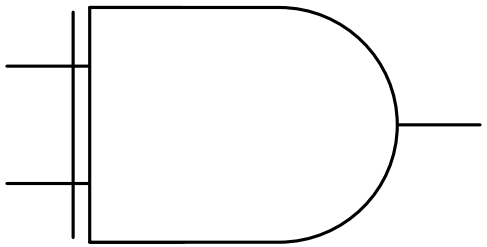
$\oplus \rightarrow XOR$



The output of a logic XOR circuit symbol is ACTIVE if one or the other of two inputs is ACTIVE but not both ACTIVE or INACTIVE

$$X = (\bar{A} \cdot B) + (A \cdot \bar{B}) = A \oplus B$$

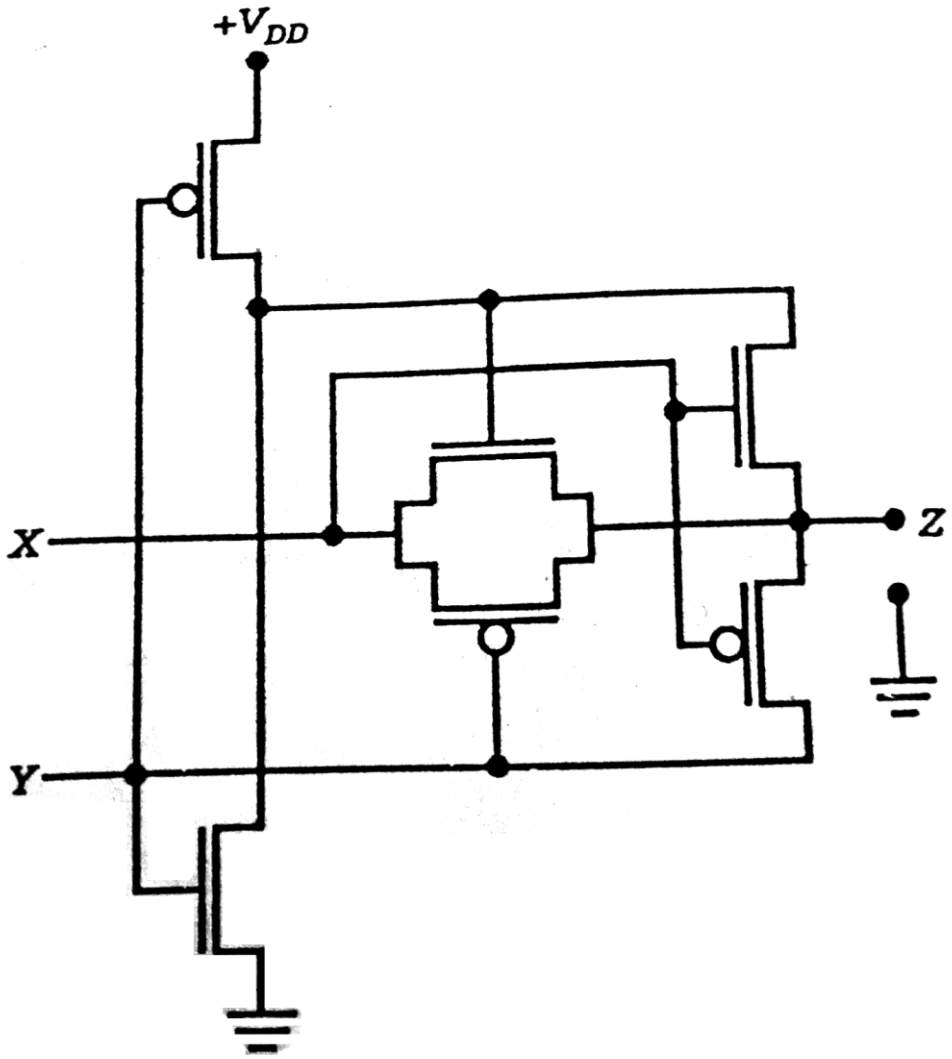
$\odot \rightarrow EQV$



The output of a logic EQV circuit symbol is ACTIVE if and only if both inputs are ACTIVE or if both inputs are INACTIVE

$$X = (A \cdot B) + (\bar{A} \cdot \bar{B}) = A \odot B$$

XOR gate realization of XOR and EQV function (1)



X	Y	Z
0	0	0
0	5	5
5	0	5
5	5	0

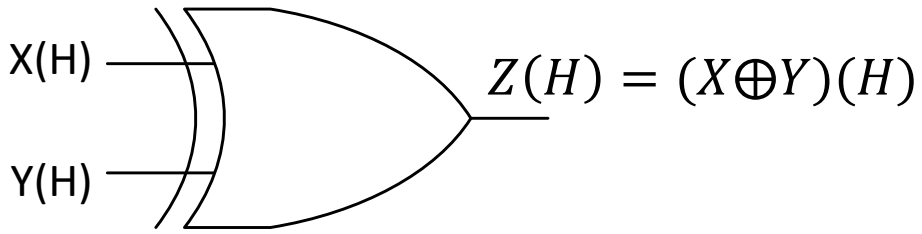
X	Y	Z
LV	LV	LV
LV	HV	HV
HV	LV	HV
HV	HV	LV

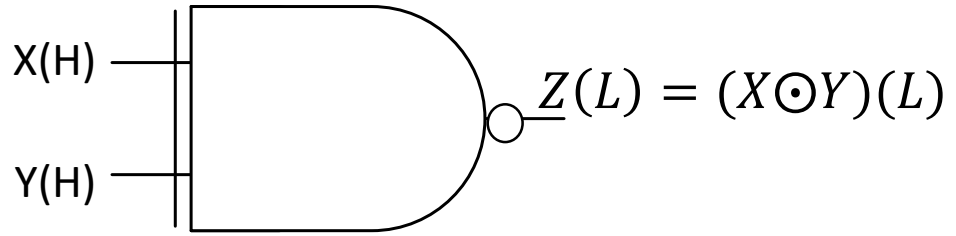
XOR gate realization of XOR and EQV function (2)

X(H)	Y(H)	Z(H)
0	0	0
0	1	1
1	0	1
1	1	0

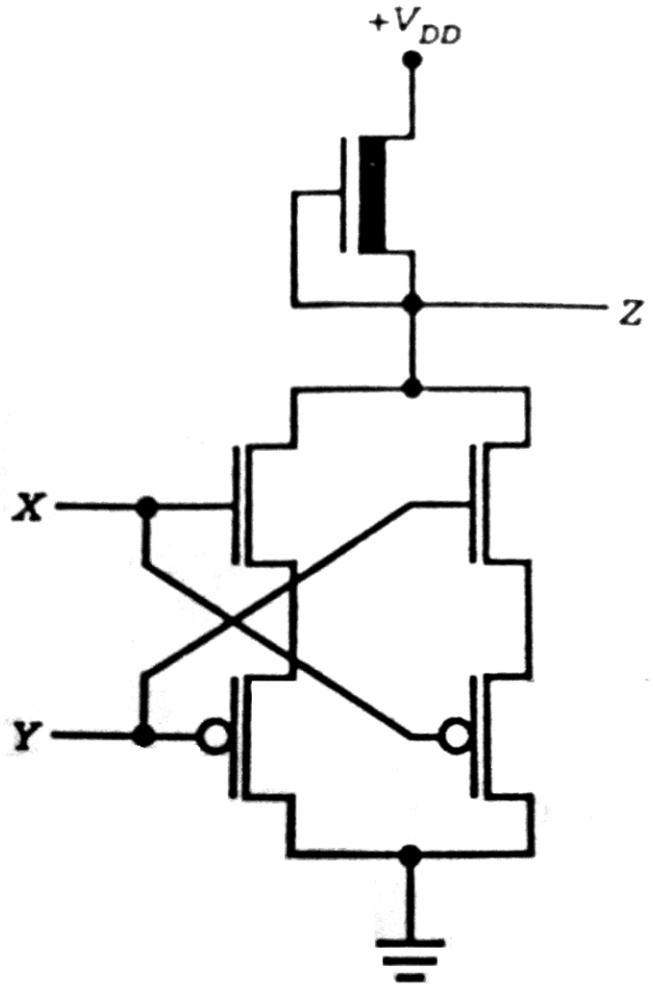
X	Y	Z
LV	LV	LV
LV	HV	HV
HV	LV	HV
HV	HV	LV

X(H)	Y(H)	Z(L)
0	0	1
0	1	0
1	0	0
1	1	1





EQV gate realization of XOR and EQV function (1)



X	Y	Z
0	0	5
0	5	0
5	0	0
5	5	5

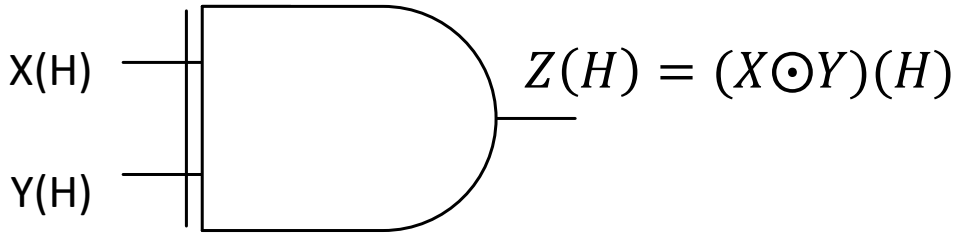
X	Y	Z
LV	LV	HV
LV	HV	LV
HV	LV	LV
HV	HV	HV

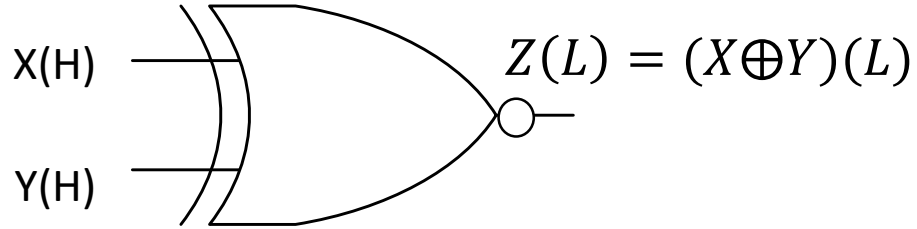
EQV gate realization of XOR and EQV function (2)

X(H)	Y(H)	Z(H)
0	0	1
0	1	0
1	0	0
1	1	1

X	Y	Z
LV	LV	HV
LV	HV	LV
HV	LV	LV
HV	HV	HV

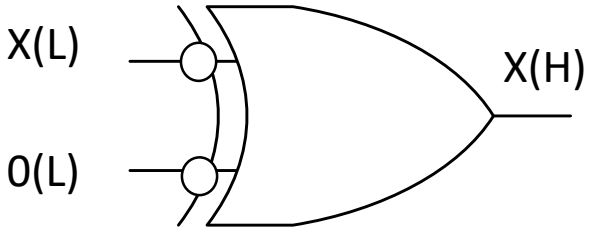
X(H)	Y(H)	Z(L)
0	0	0
0	1	1
1	0	1
1	1	0



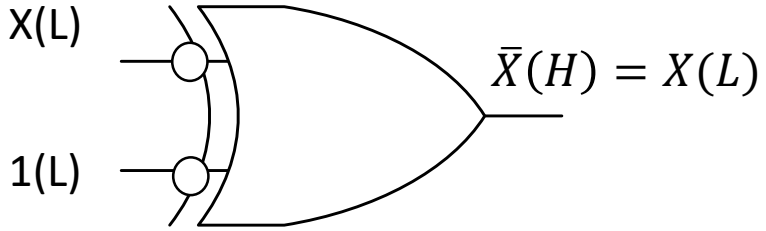


Controlled Logic Level Conversion

X(L)	Y(L)	Z(H)
1	1	0
1	0	1
0	1	1
0	0	0

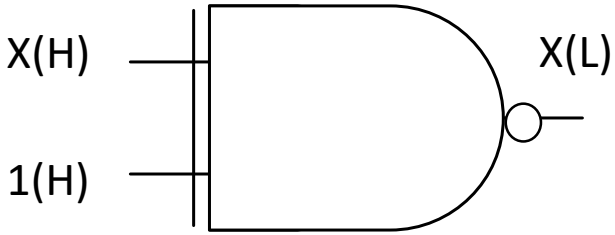


$X(L) \rightarrow X(H)$

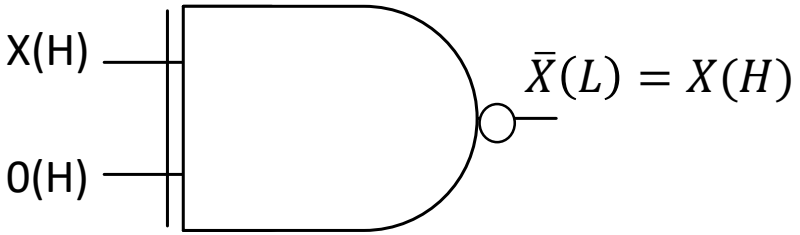


Transfer

X(H)	Y(H)	Z(L)
0	0	1
0	1	0
1	0	0
1	1	1



$X(H) \rightarrow X(L)$



Transfer