Combinational Logic Design

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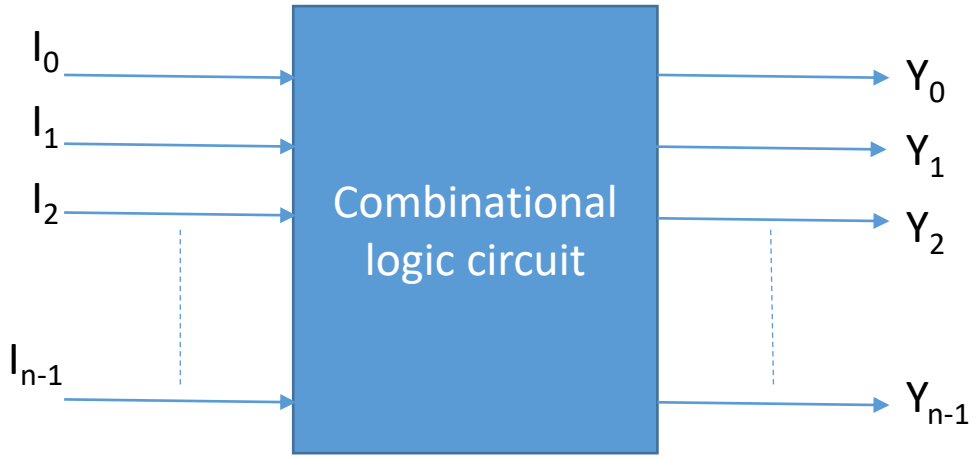
EC.184405 Rangkaian Digital dan Lab

Teknik Komputer

FTEIC - ITS

Combinational Circuit

Type of Digital circuit which the output is produced only depended on input combination at the certain time. This type of circuit isn't depended on output feedback or previous input. The time delay associated with the process will be neglected



Type of Combinational Digital Circuit

- Arithmetic-type circuit
  - ADDERs
  - SUBTRACTORs
  - MULTIPLIERs
  - DIVIDERS
  - COMPARATORS
  - PARITY GENERATORs and Error Detectors
- Multipurpose Circuit
  - DECODERs and ENCODERs
  - CODE CONVERTERs
  - MULTIPLEXERs and DEMULTIPLEXERs
  - Asynchronous SHIFTER
  - Arithmetic Logic Units (ALUs)
  - Read Only Memories (ROMs)
  - Programmable Logic Array (PLAa and PALs)

Design Procedures

Part 1. Understand the device ; Describe the function of the device; clearly indicate its (I/O) specification, and construct its block diagram

Part 2. State The Algorithms ; Indicate all algorithms binary manipulation necessary for the design

Part 3. Construct the Truth Table ; Construct a truth table that details the I/O relationship. The Truth Table usually in positive logic form

Part 4. Obtain the output Function ; Map and Minimize (or reduce) or read directly, the information in the truth table to obtain the logic expression for the output

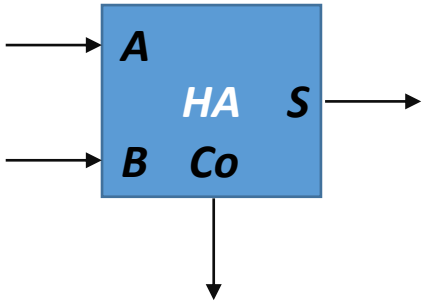
Part 5. Construct the logic Diagram ; Use either a gate or modular level approach (or both) to implement the logic expression. Implement from output to input and take into account any required MIXED LOGIC I/O condition.

Part 6. Check The Result ; Check the final logic circuit at the functional or logic level

Adder ; Half Adder (HA)

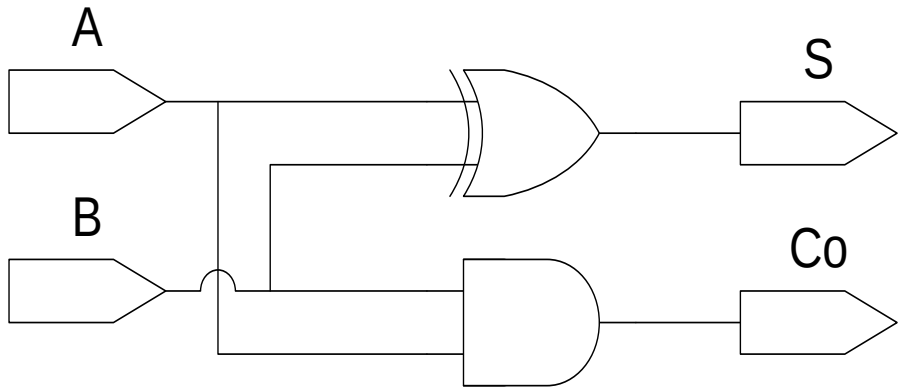
Single bit adder which perform an addition operation of two single bit input

Augend bit A; Addend bit B;
SUM (S) result and Carry out (Co)



A	0	0	1	1
+ B	+ 0	+ 1	+ 0	+ 1
Co S	0 0	0 1	0 1	1 0

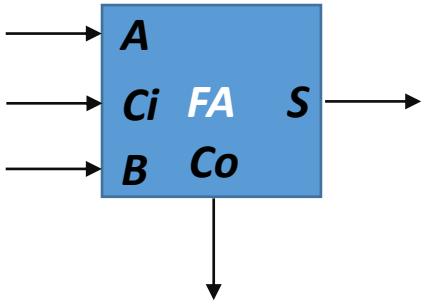
A	*B*	*S*	*Co*
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Adder ; Full Adder (FA)

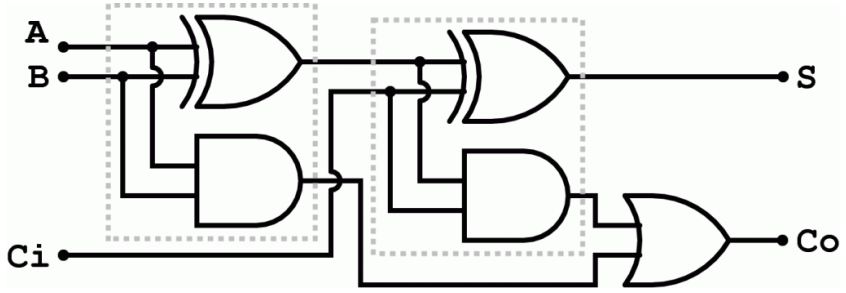
Single bit adder which perform an addition operation of three single bit input

Augend bit A; Addend bit B; Carry in (Ci)
SUM (S) result and Carry out (Co)



Ci	0	0	1	1
A	0	0	1	1
+ B	+ 0	+ 1	+ 0	+ 1
Co S	0 0	0 1	1 0	1 1

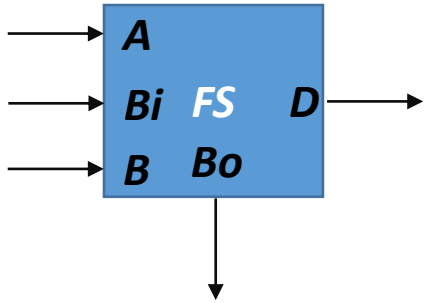
A	*B*	*Ci*	*S*	*Co*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Full Subtractor

Single bit Substractor which perform a substraction operation of three single bit input

Minuend bit A; Substrahend bit B; Borrow in (Bi)
Difference (D) result and Borrow out (Bo)



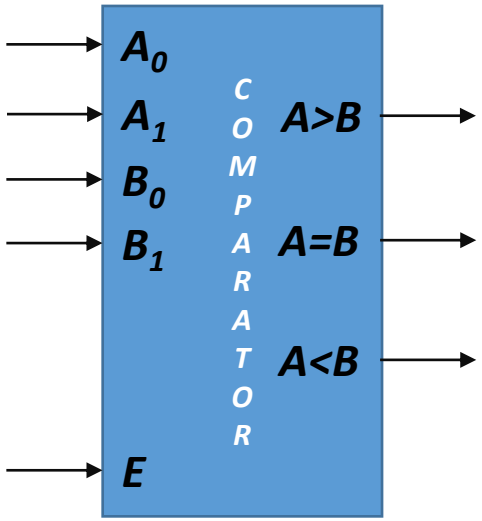
Bi	0	0	1	1
A	0	0	1	1
- B	- 0	- 1	- 0	- 1
Bo D	0 0	1 1	0 0	1 1

A	*B*	*Bi*	*D*	*Bo*
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Comparators

Comparing the value of two inputs

n inputs A ($A_{0..n-1}$) and B ($B_{0..n-1}$) ; output A>B, A<B and A=B ; Enable (E)

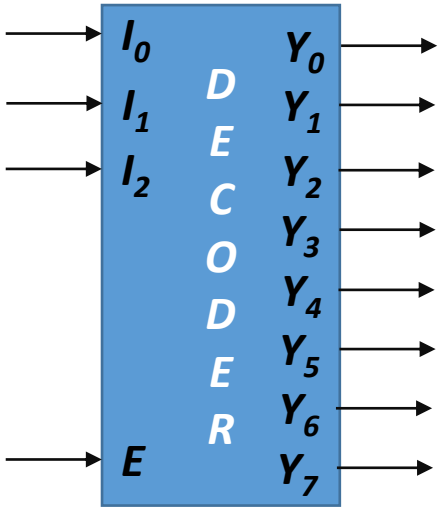


A_1	A_0	B_1	B_0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Decoder

Activating on of 2^n output every unique input pattern

n inputs ($I_{0..n-1}$); 2^n Outputs($Y_{0...2^n-1}$); Enable (E)



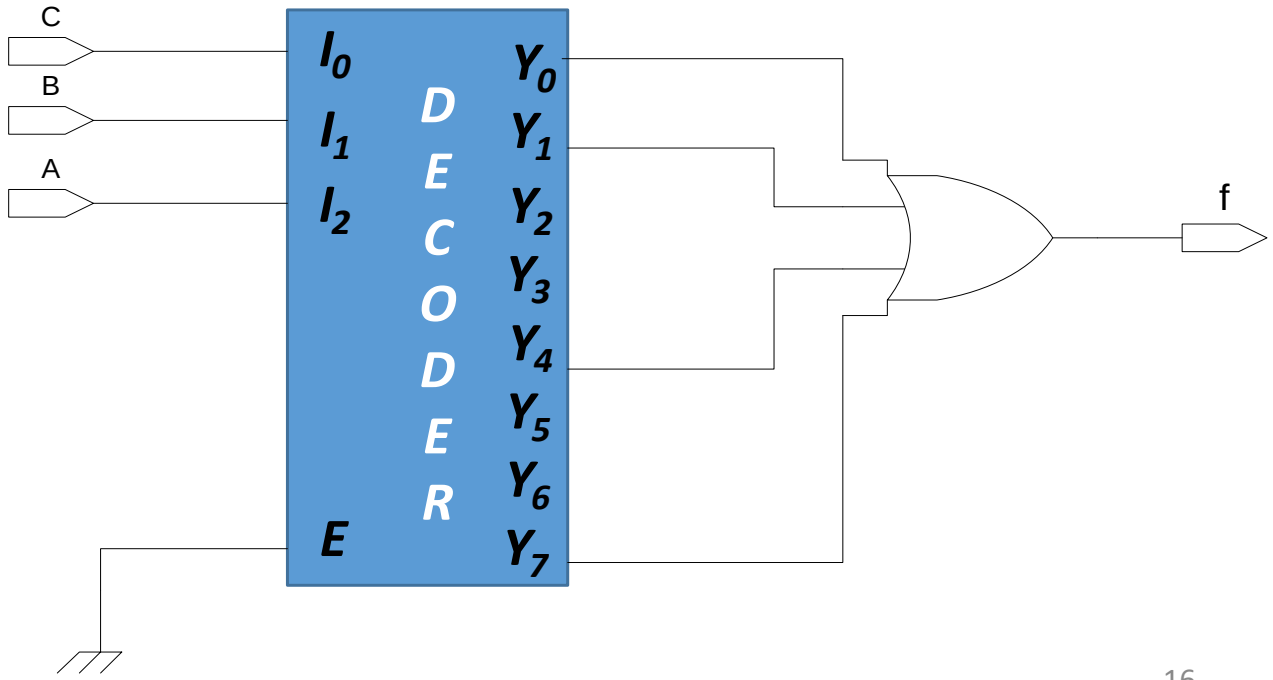
I_2	I_1	I_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Combinational Logic Design with Decoders

$$f(A,B,C) = \sum(0,1,4,7)$$

		I_1'		I_1	
		0	0	1	1
I_2'	0	1	1	0	0
I_2	1	1	0	1	0
		0	1	1	0
		I_0'	I_0		I_0'

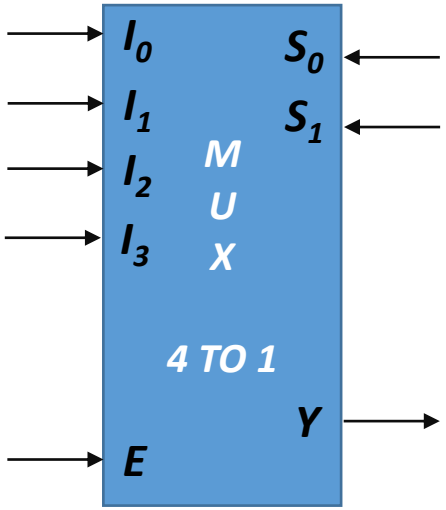
		B'		B	
		0	0	1	1
A'	0	1	1	0	0
A	1	1	0	1	0
		0	1	1	0
		C'	C		C'



Multiplexer

Selecting one of many data input lines for transmission to one or some destination

2^n inputs ($I_{0\ldots2^n-1}$); n selectors ($S_{0..n-1}$);
Enable (E), 1 output (Y);



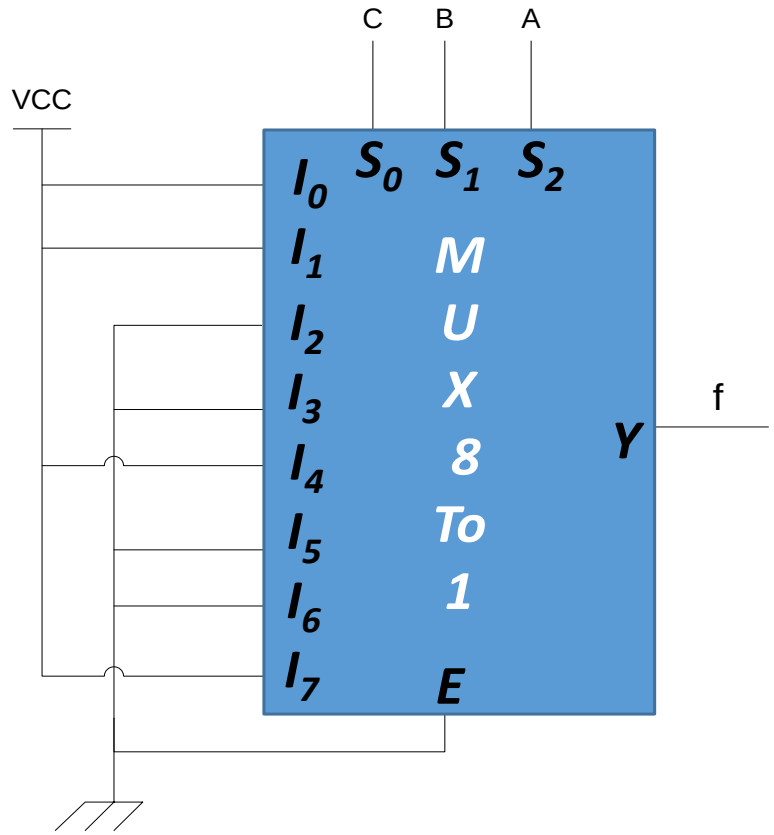
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Combinational Digital Design with Mux/Dmux

$$f(A,B,C) = \sum(0,1,4,7)$$

		S_1'		S_1	
		0	0	1	1
S_2'	0	I_0	I_1	I_3	I_2
S_2	1	I_4	I_5	I_7	I_6
		0	1	1	0
		S_0'	S_0		S_0'

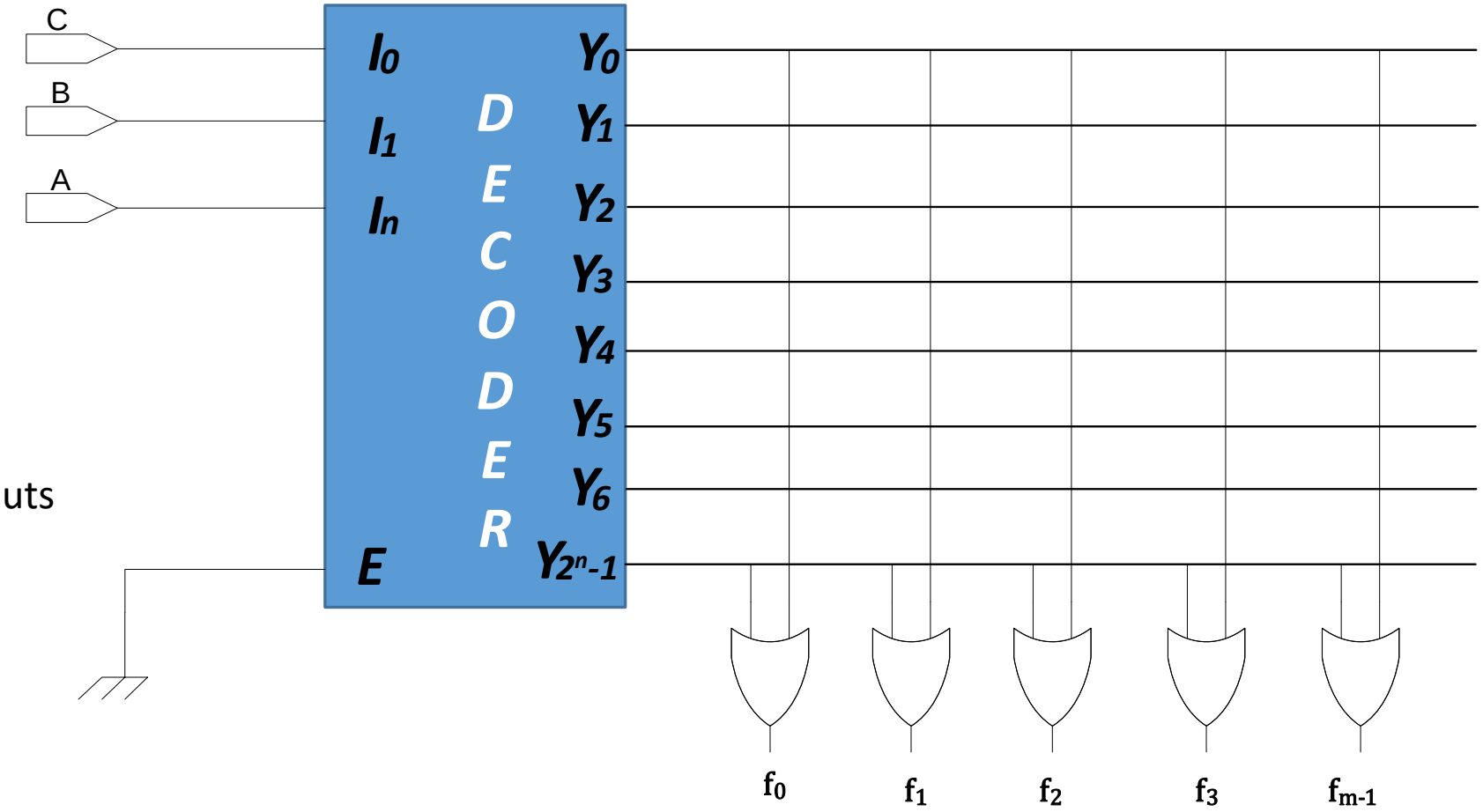
		B'		B	
		0	0	1	1
A'	0	1	1	0	0
A	1	1	0	1	0
		0	1	1	0
		C'	C		C'



Array Logic - ROMs

$2^n \times m = (2^n)(m)\ bits$

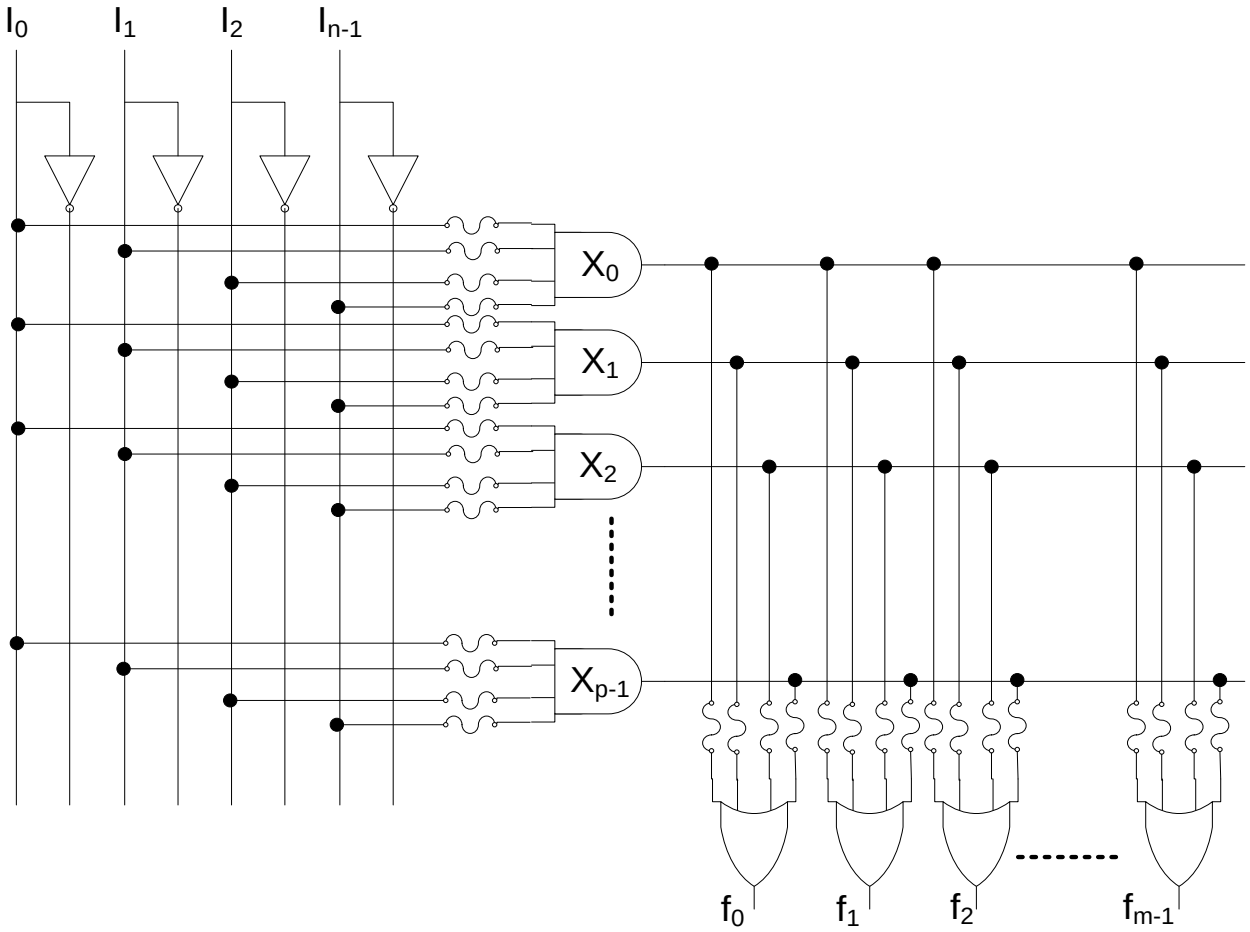
n = Number of Inputs
m = Number of Sum Terms / Outputs



PLA (Programmable Logic Array)

$$n \times p \times m$$

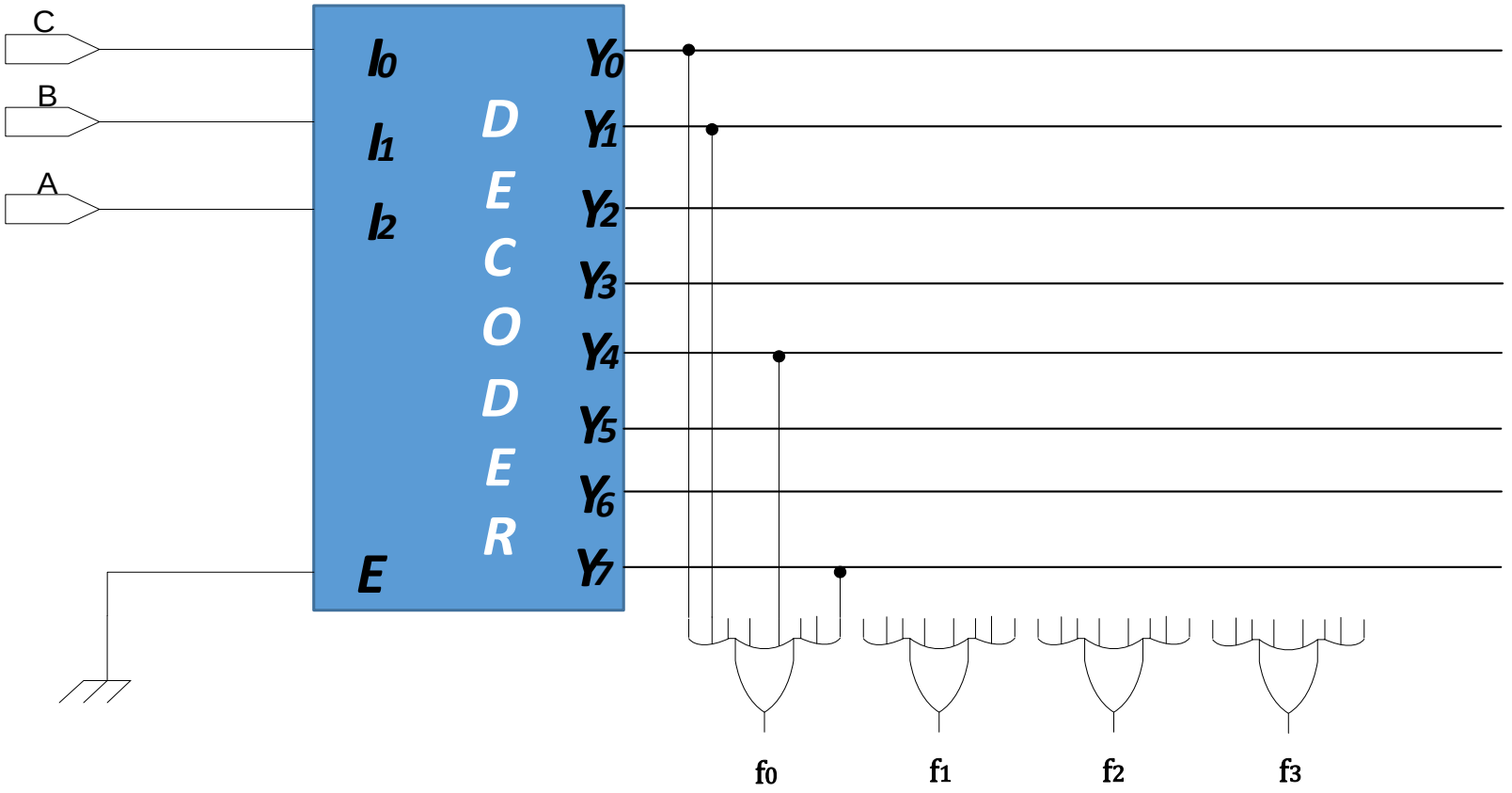
n = Number of Inputs
p = Number of Product Terms
m = Number of Sum Terms / Outputs



Combinational Digital Design with ROM

$$f(A,B,C) = \sum(0,1,4,7)$$

$$2^3 \times 4 = (2^3)(4)\ bits$$

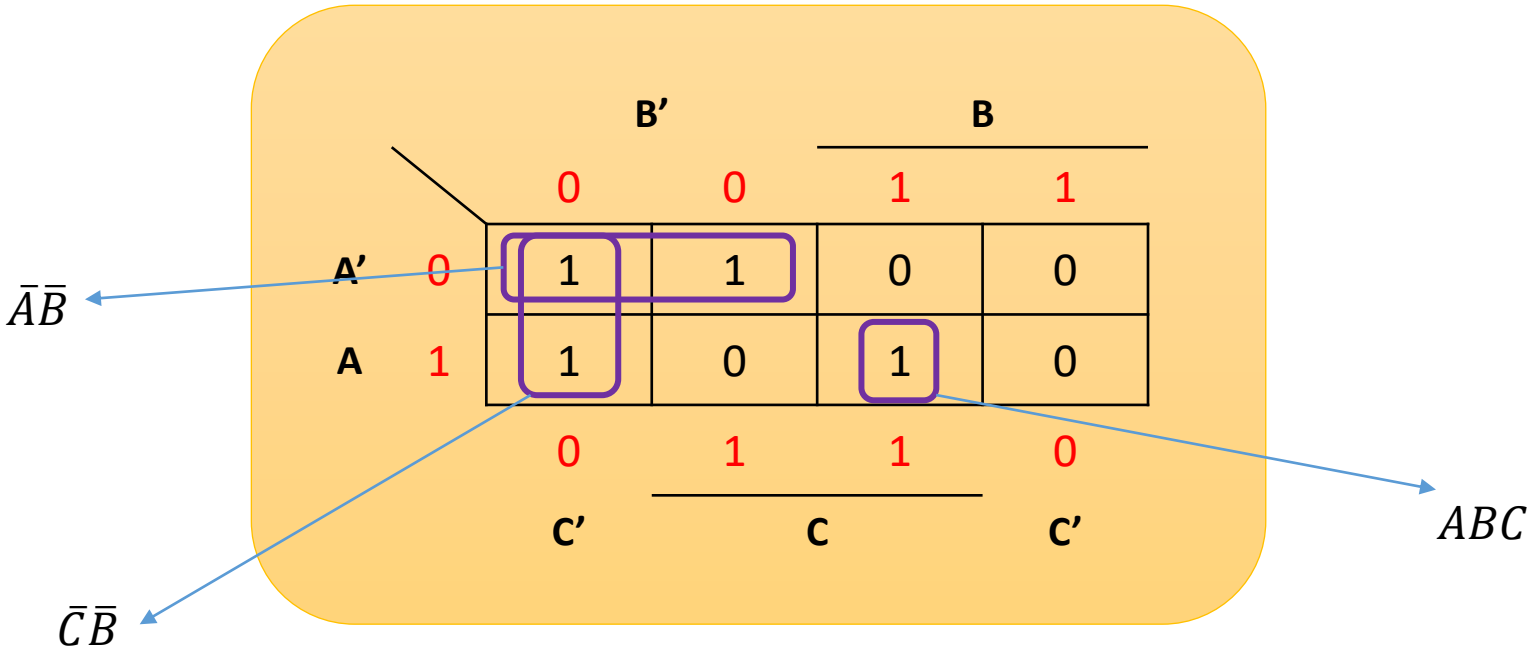


Combinational Digital Design with PLA

$$f(A,B,C) = \sum(0,1,4,7)$$

$n \times p \times m$

$3 \times 4 \times 4$



$$f(A,B,C) = ABC + \bar{A}\bar{B} + \bar{B}\bar{C}$$

X_0 X_1 X_2

Combinational Digital Design with PLA

$$f(A,B,C) = \sum(0,1,4,7)$$

$$3 \times 4 \times 4$$

$$f(A,B,C) = ABC + \bar{A}\bar{B} + \bar{B}\bar{C}$$

X_0 X_1 X_2