COMPUTER ORGANIZATION AND ARCHITECTURE DESIGNING FOR PERFORMANCE EIGHTH EDITION

William Stallings

CONTENTS

Web Site fo	or the Book iv					
About the	Author xi					
Preface xiii	i					
Chapter 0	Reader's Guide 1					
0.1	Outline of the Book 2					
0.2	A Roadmap for Readers and Instructors 2					
0.3	Why Study Computer Organization and Architecture 3					
0.4	Internet and Web Resources 4					
PART ON	E OVERVIEW 7					
Chapter 1	Introduction 8					
1.1	Organization and Architecture 9					
1.2	Structure and Function 10					
1.3	Key Terms and Review Questions 15					
Chapter 2	Computer Evolution and Performance 16					
2.1	A Brief History of Computers 17					
2.2	Designing for Performance 38					
2.3	The Evolution of the Intel x86 Architecture 44					
2.4	Embedded Systems and the ARM 46					
2.5	Performance Assessment 50					
2.6	Recommended Reading and Web Sites 57					
2.7	Key Terms, Review Questions, and Problems 59					
PART TW	O THE COMPUTER SYSTEM 63					
Chapter 3	A Top-Level View of Computer Function and Interconnection 65					
3.1	Computer Components 66					
3.2	Computer Function 68					
3.3	Interconnection Structures 83					
3.4	Bus Interconnection 85					
3.5 3.6	PCI 95 Programmended Programmend Web Sites 104					
3.7	Recommended Reading and Web Sites 104 Key Terms, Review Questions, and Problems 104					
3.7	Appendix 3A Timing Diagrams 108					
Chapter 4	Cache Memory 110					
4.1	Computer Memory System Overview 111					
4.2	Cache Memory Principles 118					
4.3	Elements of Cache Design 121					
4.4	Pentium 4 Cache Organization 140					
4.5	ARM Cache Organization 143					

vi CONTENTS

4.6 4.7	Recommended Reading 145 Key Terms, Review Questions, and Problems 146 Appendix 4A Performance Characteristics of Two-Level Memories 151					
Chapter 5	Internal Memory Technology 158					
5.1 5.2 5.3 5.4 5.5	Semiconductor Main Memory 159 Error Correction 169 Advanced DRAM Organization 173 Recommended Reading and Web Sites 179 Key Terms, Review Questions, and Problems 180					
Chapter 6	External Memory 184					
6.1 6.2 6.3 6.4 6.5 6.6	Magnetic Disk 185 RAID 194 Optical Memory 203 Magnetic Tape 210 Recommended Reading and Web Sites 212 Key Terms, Review Questions, and Problems 214					
Chapter 7	Input/Output 217					
7.1 7.2 7.3 7.4 7.5 7.6 7.7 7.8 7.9	External Devices 219 I/O Modules 222 Programmed I/O 224 Interrupt-Driven I/O 228 Direct Memory Access 236 I/O Channels and Processors 242 The External Interface: FireWire and Infiniband 244 Recommended Reading and Web Sites 253 Key Terms, Review Questions, and Problems 254					
Chapter 8	Operating System Support 259					
8.1 8.2 8.3 8.4 8.5 8.6 8.7	Operating System Overview 260 Scheduling 271 Memory Management 277 Pentium Memory Management 288 ARM Memory Management 293 Recommended Reading and Web Sites 298 Key Terms, Review Questions, and Problems 299					
PART THREE THE CENTRAL PROCESSING UNIT 303						
Chapter 9	Computer Arithmetic 305					

napter 9	Computer Arithmetic 305				
9.1	The Arithmetic and Logic Unit (ALU) 306				
9.2	Integer Representation 307				
9.3	Integer Arithmetic 312				
9.4	Floating-Point Representation 327				
9.5	Floating-Point Arithmetic 334				
9.6	Recommended Reading and Web Sites 342				
9.7	Key Terms, Review Questions, and Problems 344				

Chapter 10	Instruction Sets: Characteristics and Functions 348				
10.1	Machine Instruction Characteristics 349				
10.2	Types of Operands 356				
10.3	Intel x86 and ARM Data Types 358				
10.4	Types of Operations 362				
10.5	Intel x86 and ARM Operation Types 374				
10.6	Recommended Reading 384				
10.7	Key Terms, Review Questions, and Problems 385				
	Appendix 10A Stacks 390				
	Appendix 10B Little, Big, and Bi-Endian 396				
Chapter 11	Instruction Sets: Addressing Modes and Formats 400				
11.1	Addressing 401				
11.2	x86 and ARM Addressing Modes 408				
11.3	Instruction Formats 413				
11.4	x86 and ARM Instruction Formats 421				
11.5	Assembly Language 426				
11.6	Recommended Reading 428				
11.7	Key Terms, Review Questions, and Problems 428				
Chapter 12	Processor Structure and Function 432				
12.1	Processor Organization 433				
12.2	Register Organization 435				
12.3	The Instruction Cycle 440				
12.4	Instruction Pipelining 444				
12.5	The x86 Processor Family 461				
12.6	The ARM Processor 469				
12.7	Recommended Reading 475				
12.8	Key Terms, Review Questions, and Problems 476				
Chapter 13	Reduced Instruction Set Computers (RISCs) 480				
13.1	Instruction Execution Characteristics 482				
13.2	The Use of a Large Register File 487				
13.3	Compiler-Based Register Optimization 492				
13.4	Reduced Instruction Set Architecture 494				
13.5	RISC Pipelining 500				
13.6	MIPS R4000 504				
13.7	SPARC 511				
13.8	The RISC versus CISC Controversy 517				
13.9	Recommended Reading 518				
13.10	Key Terms, Review Questions, and Problems 518				
_	Instruction-Level Parallelism and Superscalar Processors 522				
14.1	Overview 524				
14.2	Design Issues 528				
14.3	Pentium 4 538				
14.4	ARM Cortex-A8 544				
14.5	Recommended Reading 552				
14 6	Key Terms Review Questions and Problems 554				

viii CONTENTS

PART FOUR THE CONTROL UNIT 559

Chapter 15 Control Unit Operation 56)6T
--------------------------------------	-----

- 15.1 Micro-operations 563
- 15.2 Control of the Processor 569
- 15.3 Hardwired Implementation 581
- 15.4 Recommended Reading 584
- 15.5 Key Terms, Review Questions, and Problems 584

Chapter 16 Microprogrammed Control 586

- 16.1 Basic Concepts 587
- 16.2 Microinstruction Sequencing 596
- 16.3 Microinstruction Execution 602
- 16.4 TI 8800 614
- 16.5 Recommended Reading 624
- 16.6 Key Terms, Review Questions, and Problems 625

PART FIVE PARALLEL ORGANIZATION 627

Chapter 17 Parallel Processing 628

- 17.1 The Use of Multiple Processors 630
- 17.2 Symmetric Multiprocessors 632
- 17.3 Cache Coherence and the MESI Protocol 640
- 17.4 Multithreading and Chip Multiprocessors 646
- 17.5 Clusters 653
- 17.6 Nonuniform Memory Access Computers 660
- 17.7 Vector Computation 664
- 17.8 Recommended Reading and Web Sites 676
- 17.9 Key Terms, Review Questions, and Problems 677

Chapter 18 Multicore Computers 684

- 18.1 HardwarePerformance Issues 685
- 18.2 Software Performance Issues 690
- 18.3 Multicore Organization 694
- 18.4 Intel x86 Multicore Organization 696
- 18.5 ARM11 MPCore 699
- 18.6 Recommended Reading and Web Sites 704
- 18.7 Key Terms, Review Questions, and Problems 705

Appendix A Projects for Teaching Computer Organization and Architecture 707

- A.1 Interactive Simulations 708
- A.2 Research Projects 708
- A.3 Simulation Projects 710
- A.4 Assembly Language Projects 711
- A.5 Reading/Report Assignments 711
- A.6 Writing Assignments 712
- A.7 Test Bank 712

Appendix B Assembly Language and Related Topics 713					
B.1	Assembly Language 714				
B.2	Assemblers 723				
B.3	Loading and Linking 728				
B.4	Recommended Reading and Web Sites 735				
B.5	Key Terms, Review Questions, and Problems 736				
ONLINE CHAPTERS					
WilliamStallings.com/COA/COA8e.ht					
Chapter 19	Number Systems 19-1				
19.1	The Decimal System 19-2				
19.2	The Binary System 19-2				
19.3	Converting between Binary and Decimal 19-3				
19.4	Hexadecimal Notation 19-5				
19.5	Key Terms, Review Questions, and Problems 19-8				
Chapter 20	Digital Logic 20-1				
20.1	Boolean Algebra 20-2				
20.2	Gates 20-4				
20.3	Combinational Circuits 20-7				
20.4	Sequential Circuits 20–24				
20.5	Programmable Logic Devices 20-33				
20.6	Recommended Reading and Web Site 20-38				
20.7	Key Terms and Problems 20-39				
Chapter 21 The IA-64 Architecture 21-1					
21.1	Motivation 21-3				
21.2	General Organization 21-4				
21.3	Predication, Speculation, and Software Pipelining 21-6				
21.4	IA-64 Instruction Set Architecture 21-23				
21.5	Itanium Organization 21-28				
21.6	Recommended Reading and Web Sites 21-31				
21.7	Key Terms, Review Questions, and Problems 21-32				
	ONLINE APPENDICES				
	WilliamStallings.com/COA/COA8e.html				
A 4: C	•				
Appendix C	C Hash Tables				
Appendix I	O Victim Cache Strategies				
D.1	Victim Cache				
D.2	Selective Victim Cache				
Appendix E	E Interleaved Memory				
Appendix F	International Reference Alphabet				
Appendix C	G Virtual Memory Page Replacement Algorithms				

the computers: processor, I/O, memory, peripheral devices. Part Two examines these components and looks in some detail at each component except the processor. This approach allows us to see the external functional requirements that drive the processor design, setting the stage for Part Three. In Part Three, we examine the processor in great detail. Because we have the context provided by Part Two, we are able, in Part Three, to see the design decisions that must be made so that the processor supports the overall function of the computer system. Next, in Part Four, we look at the control unit, which is at the heart of the processor. Again, the design of the control unit can best be explained in the context of the function it performs within the context of the processor. Finally, Part Five examines systems with multiple processors, including clusters, multiprocessor computers, and multicore computers.

0.3 WHY STUDY COMPUTER ORGANIZATION AND ARCHITECTURE?

The IEEE/ACM Computer Curricula 2001, prepared by the Joint Task Force on Computing Curricula of the IEEE (Institute of Electrical and Electronics Engineers) Computer Society and ACM (Association for Computing Machinery), lists computer architecture as one of the core subjects that should be in the curriculum of all students in computer science and computer engineering. The report says the following:

The computer lies at the heart of computing. Without it most of the computing disciplines today would be a branch of theoretical mathematics. To be a professional in any field of computing today, one should not regard the computer as just a black box that executes programs by magic. All students of computing should acquire some understanding and appreciation of a computer system's functional components, their characteristics, their performance, and their interactions. There are practical implications as well. Students need to understand computer architecture in order to structure a program so that it runs more efficiently on a real machine. In selecting a system to use, they should be able to understand the tradeoff among various components, such as CPU clock speed vs. memory size.

A more recent publication of the task force, Computer Engineering 2004 Curriculum Guidelines, emphasized the importance of Computer Architecture and Organization as follows:

Computer architecture is a key component of computer engineering and the practicing computer engineer should have a practical understanding of this topic. It is concerned with all aspects of the design and organization of the central processing unit and the integration of the CPU into the computer system itself. Architecture extends upward into computer software because a processor's architecture must cooperate with the operating system and system software. It is difficult to design an operating system well without knowledge of the underlying architecture. Moreover, the computer designer must have an understanding of software in order to implement the optimum architecture.

The computer architecture curriculum has to achieve multiple objectives. It must provide an overview of computer architecture and teach students the operation of a typical computing machine. It must cover basic principles, while acknowledging the complexity of existing commercial systems. Ideally, it should reinforce topics that are common to other areas of computer engineering; for example, teaching register indirect addressing reinforces the concept of pointers in C. Finally, students must understand how various peripheral devices interact with, and how they are interfaced to a CPU.

[CLEM00] gives the following examples as reasons for studying computer architecture:

- 1. Suppose a graduate enters the industry and is asked to select the most costeffective computer for use throughout a large organization. An understanding of the implications of spending more for various alternatives, such as a larger cache or a higher processor clock rate, is essential to making the decision.
- 2. Many processors are not used in PCs or servers but in embedded systems. A designer may program a processor in C that is embedded in some real-time or larger system, such as an intelligent automobile electronics controller. Debugging the system may require the use of a logic analyzer that displays the relationship between interrupt requests from engine sensors and machine-level code.
- 3. Concepts used in computer architecture find application in other courses. In particular, the way in which the computer provides architectural support for programming languages and operating system facilities reinforces concepts from those areas.

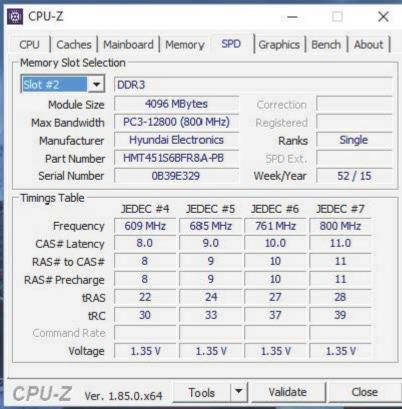
As can be seen by perusing the table of contents of this book, computer organization and architecture encompasses a broad range of design issues and concepts. A good overall understanding of these concepts will be useful both in other areas of study and in future work after graduation.

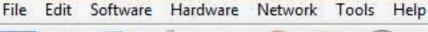
0.4 INTERNET AND WEB RESOURCES

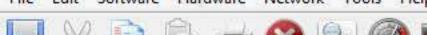
There are a number of resources available on the Internet and the Web that support this book and help readers keep up with developments in this field.

Web Sites for This Book

There is a Web page for this book at WilliamStallings.com/COA/COA8e.html. See the layout at the beginning of this book for a detailed description of that site.

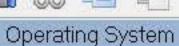




















Property























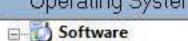




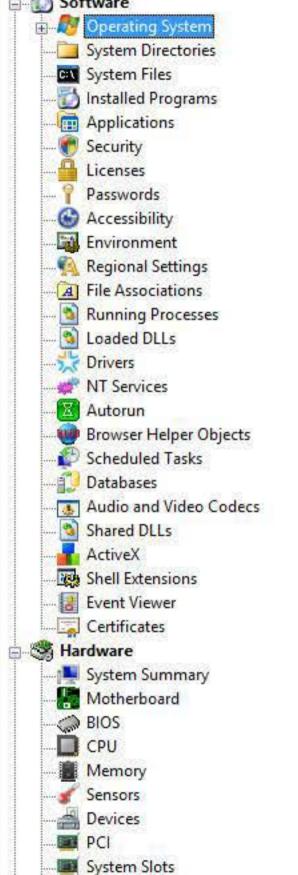








*



Metwork Adapters

Sound Devices

Video

 Operating System Windows 8.1 Pro Mame Features **Edition Type**

Edition ID Key Type

EULA SKU Language

Safe Mode Activation Status License Status

Genuine Remaining Grace Period

Checked Build **W** UAC Enabled

S Root Boot Device

System Device Kernel Version

Build Lab Build Lab Ex

Security Security MMC Version

Hardware DEP Available Automatic Updates Automatic Updates

Registration

Windows To Go Installation Time

Boot Time Up Time

· System Restore

Windows 8.1 (Update) Pro x64

Value

Terminal Services in Remote Admin Mode, 64 Bit Edition, Multiprocessor Free Professional

[Blue]X18-95588 Volume: GVLK Volume 48 [0x30]

English No Activated

Licensed [Windows(R) Operating System, VOLUME_KMSCLIENT channel] Yes

23 (169 Days, 23 Hours, 23 Minutes) No

Yes

C:\Windows\ \Device\HarddiskVolume1

\Device\HarddiskVolume2 6.3.9600.17056

9600.winblue_r3.140827-1500

9600.17328.amd64fre.winblue r3.140827-1500

3.0 Yes Enabled Enabled

256 bits

No

2014-12-08 01:31:33 2014-12-18 01:38:45

10 Hours 59 Minutes 8 seconds Enabled

■ Device Info	HW						•
GENERAL	soc	SYSTEM	SCREEN	MEMORY	CAMERA	BATTERY	SENSORS
Exynos 98	325	.					
CPU				Exynos 9825			
Vendor				Samsung			
Cores				8			
big.LITTLE				3 clusters			
Clusters				2 x 2.73 GHz 2 x 2.40 GHz 4 x 1.95 GHz			
Family				Mongoose-M4 Cortex-A75 Cortex-A55			
Mode				64-bit			
Machine				aarch64			
ABI				arm64-v8a			
Instructions				fp asimd evtstrm ae asimdrdm dcpop	s pmull sha1 sha2 c	rc32 atomics fphp as	simdhp cpuid
Process technology				7 nm			
Revision				r1p0 r2p1 r1p0			
Clock speed				442 - 2730 MHz			
Governor				schedutil			
Supported ABI				arm64-v8a armeabi-	-v7a armeabi		
GPU				Mali-G76			
Vendor				ARM			
OpenGL ES				3.2 v1.r32p1-01bet2	-mbs2v39_0.13180	le953429f661ecce1	d5e1d2b3ef
Vulkan				1.1			
Extensions				102 ■			
Clock speed				325 - 754 MHz			



GENERAL

SOC

SYSTEM

SCREEN



SENSORS









APPLICATIONS



CAMERA

BATTERY

MEMORY

Snapdragon 8 Gen 1	
CPU	sm8450
Vendor	Qualcomm
Cores	8
big.LITTLE	3 clusters
Clusters	1 x 3.00 GHz 3 x 2.50 GHz 4 x 1.78 GHz
Family	Cortex-X2 Cortex-A710 Cortex-A510
Mode	64-bit
Machine	aarch64
ABI	arm64-v8a
Instructions	fp asimd evtstrm aes pmull sha1 sha2 crc32 atomics fphp asimdhp cpuid asimdrdm jscvt fcma lrcpc dcpop sha3 sm3 sm4 asimddp sha512 sve asimdfhm dit uscat ilrcpc flagm ssbs sb paca pacg dcpodp flagm2 frint i8mm bf16 bti
Process technology	4 nm
Revision	r2p0 r0p2
Clock speed	307 - 2995 MHz
Governor	walt
Supported ABI	arm64-v8a armeabi-v7a armeabi
GPU	Adreno (TM) 730
Vendor	Qualcomm
OpenGL ES	3.2 V@0613.0 (GIT@fa3b9353c9, Ib62fda793a, 1647348410) (Date:03/15/22)
Vulkan	1.1
Extensions	104 ≡
Clock speed	124 - 818 MHz
Governor	msm-adreno-tz











THERMAL







