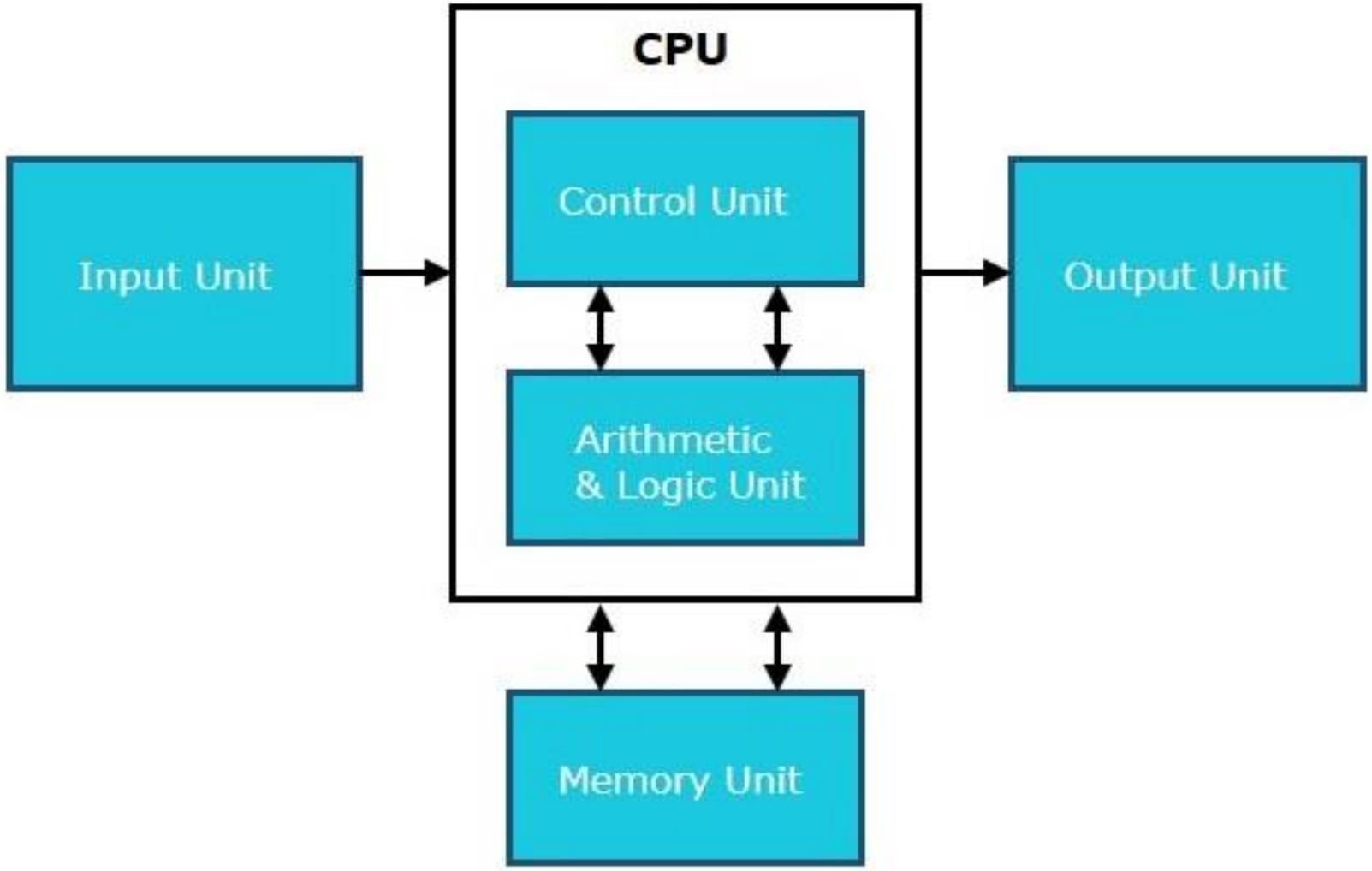
PENGALAMATAN MEMORI
AKSES OLEH CPU



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Kapasitas Memori

Kapasitas memori menunjukkan jumlah maksimum bit data yang dapat disimpan di dalam sebuah memori

- Dinyatakan dalam : Megabit, Gigabit, MegaByte (MB), KiloByte (KB)
- 1 Kbit = 2^{10} bit =1.024 bit
- 1 Mbit = 2^{20} bit, 1Gbit = 2^{30} bit
- 1 Byte = 8 bit
- 1 KiloByte = 1.024 x 8 bit
- Untuk menyatakan kapasitas memory jenis penyimpan permanen seperti hard disk, CD (Compact Disc), flash disk, SSD
- Dapat juga dinyatakan dalam : 2Kx8, 4Kx8, 32Kx16 dsb, lazim untuk memori jenis RAM (Random Access Memory) dan ROM (Read Only Memory)

Kapasitas Memori (2)

2K x 8

Menyatakan panjang bit dalam 1 set data yaitu 8 bit (D7 s.d. D0)

Menyatakan jumlah lokasi yang disediakan = 2x1024 = 2048 lokasi dengan 1 lokasi sel berisi 8 bit (1 byte) ➔ Memori 2KB

- Dari lokasi 0 s.d. lokasi 2047
- Dari 000 0000 0000 s.d. 111 1111 1111 = 000 s.d. 7FF
  - 11 bit jalur alamat (A10 s.d A0)

Contoh:

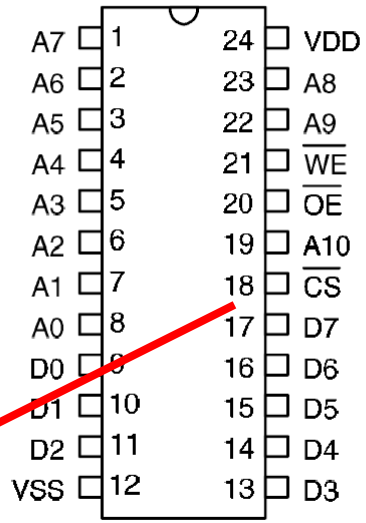
- HT6116-70
- CMOS 2Kx8-Bit SRAM

  The HT6116-70 is a 16384-bit static random access memory. It is organized with 2048 words of 8 bits in length

Chip Select (CS)	Read/Write (RW) (atau Write Enable/WE)	Operasi Memory (Hanya Ilustrasi/Contoh)
0	x	Tak ada operasi
1	0	Tulis data ke memory
1	1	Baca data dari memory

Kaki “Chip Select” (CS) lazimnya digunakan untuk “mengaktifkan” (memilih/*enable*) keping memori tsb

Pin Assignment



HT6116-70
– 24 DIP/SDIP/SOP

Decoder/Demultiplexer ("lawan" dari Multiplexer/Mux)

- Untuk memilih keping memori yang akan diakses oleh CPU
  - ➢Mengaktifkan Chip Select

➢Contoh: 74LS156P

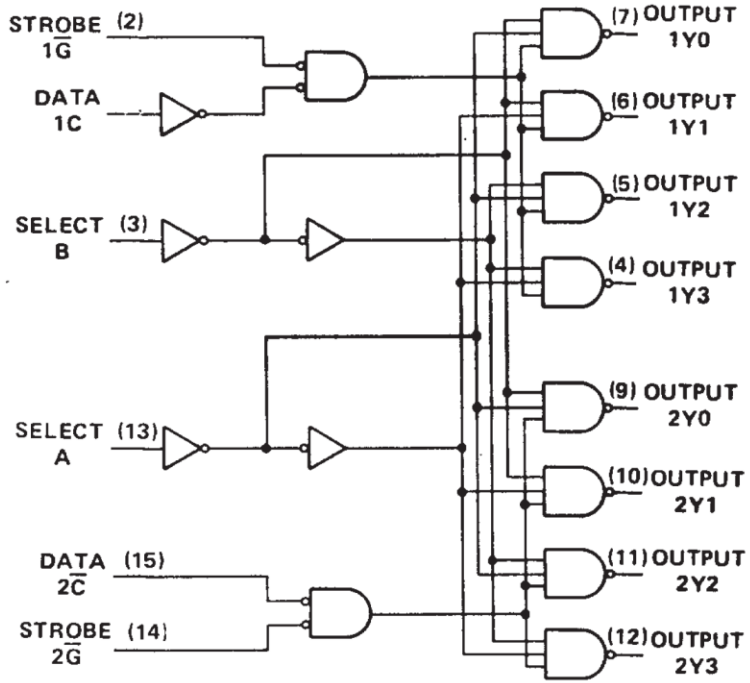
Tokopedia

Rp8.000 BEBAS ONGKIR

74LS156 Dual 2-Line To 4-Line Decoders / Demultiplexers

Datasheet

logic diagram (positive logic)

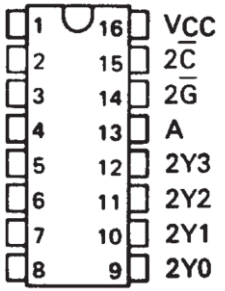


FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G̅	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

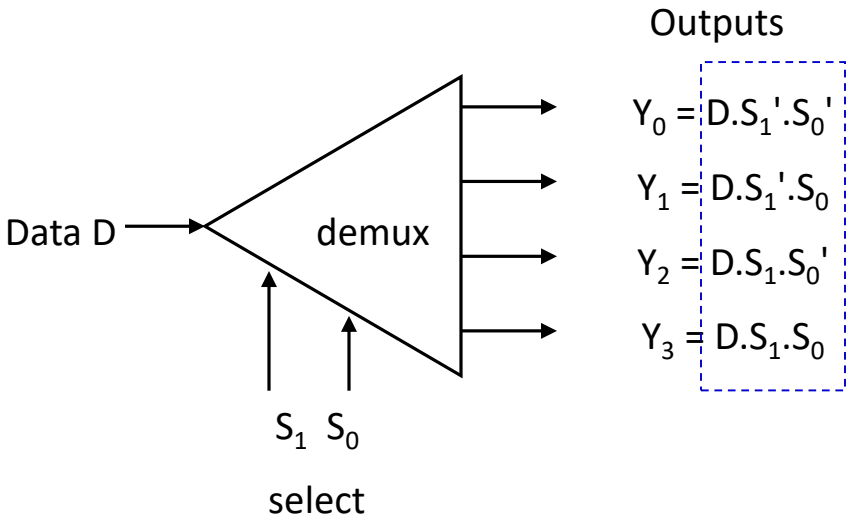
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G̅	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

SN54155, SN54156, SN54LS155A,
SN54LS156 . . . J OR W PACKAGE
SN74155, SN74156 . . . N PACKAGE
SN74LS155A, SN74LS156 . . . D OR N PACKAGE
(TOP VIEW)



Demultiplexer (1)

- Given an input line and a set of selection lines, the demultiplexer will direct data from input to a selected output line.
- An example of a 1-to-4 demultiplexer:



S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	D	0	0	0
0	1	0	D	0	0
1	0	0	0	D	0
1	1	0	0	0	D

Demultiplexer (2)

- Takes one input
- Out to one of 2^n possible outputs

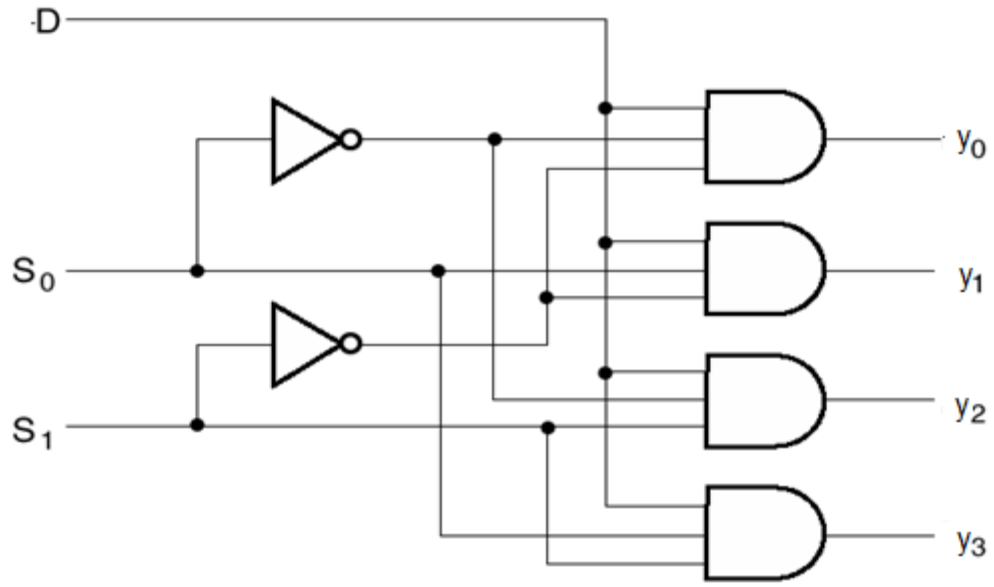
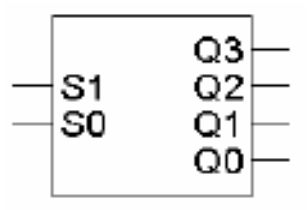


Fig. 3-24 1-to-4-Line Demultiplexer

Decoder (1)

What a decoder does

- A *n*-to-2^n decoder uses its *n*-bit input to determine which of 2^n outputs will be uniquely activated.



S1	S0	Q0	Q1	Q2	Q3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

- Here is a block diagram and truth table for a 2-to-4 decoder.
  - The two-bit input is called S1S0, and the four outputs are Q0-Q3.
  - If the input is the binary number i, then output Qi alone will be true.
- This circuit "decodes" a binary number into a "one-of-four" code.

Building a decoder

- We can use the truth table to derive minimal sum of products equations for each of the four outputs (Q0-Q3), based on the two inputs (S0-S1).

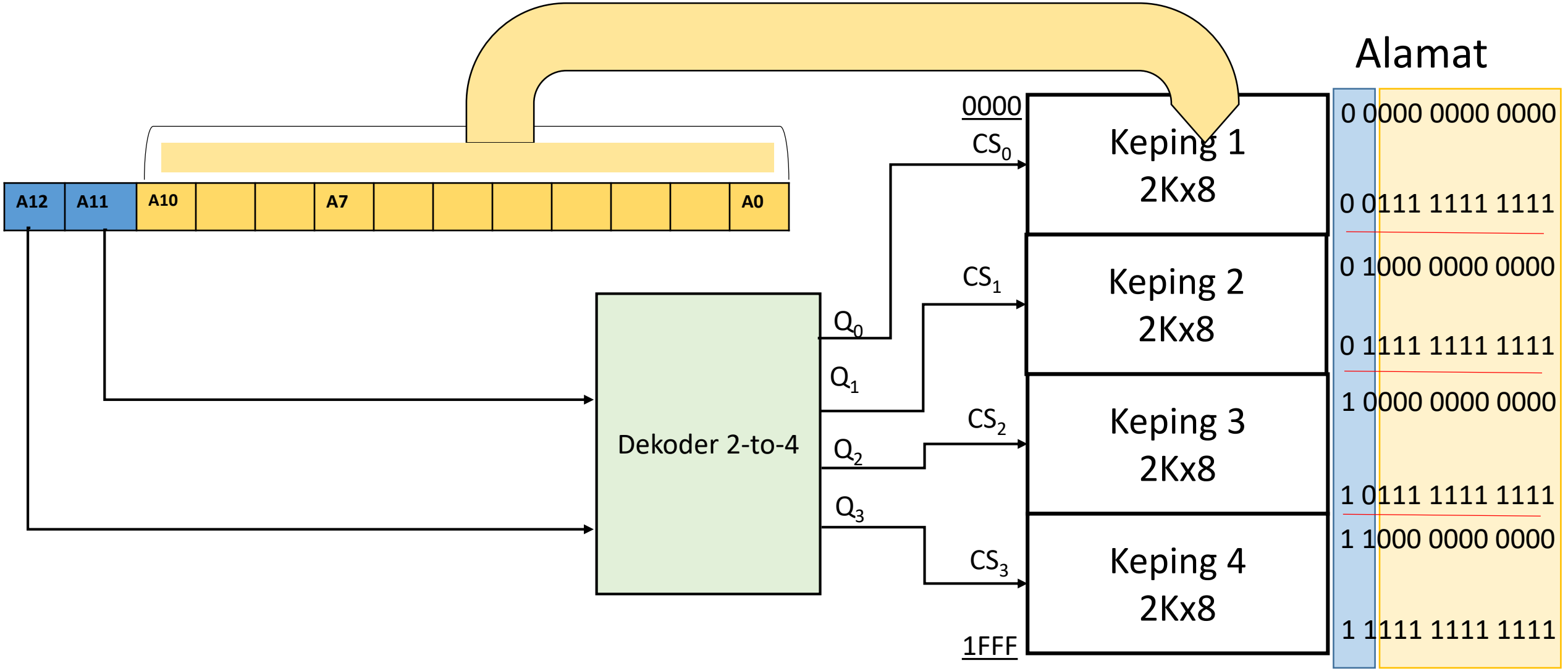
S1	S0	Q0	Q1	Q2	Q3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

- In this case there's not much to be simplified. Here are the equations:

Q0 = S1'S0'
Q1 = S1'S0
Q2 = S1 S0'
Q3 = S1 S0

CPU dengan akses RAM 8Kb

Device yang diperlukan
- RAM 2Kx8 (2 Kb) sebanyak 4 keping
  - 4 * 2Kb = 8 Kb (8192 byte)
- Dekoder 2-to-4



Semoga Memahami dan Mengerti

- Kembangkan imajinasi untuk
  - pengalamatan memori yang lebih besar
  - melibatkan lebih banyak keping memori