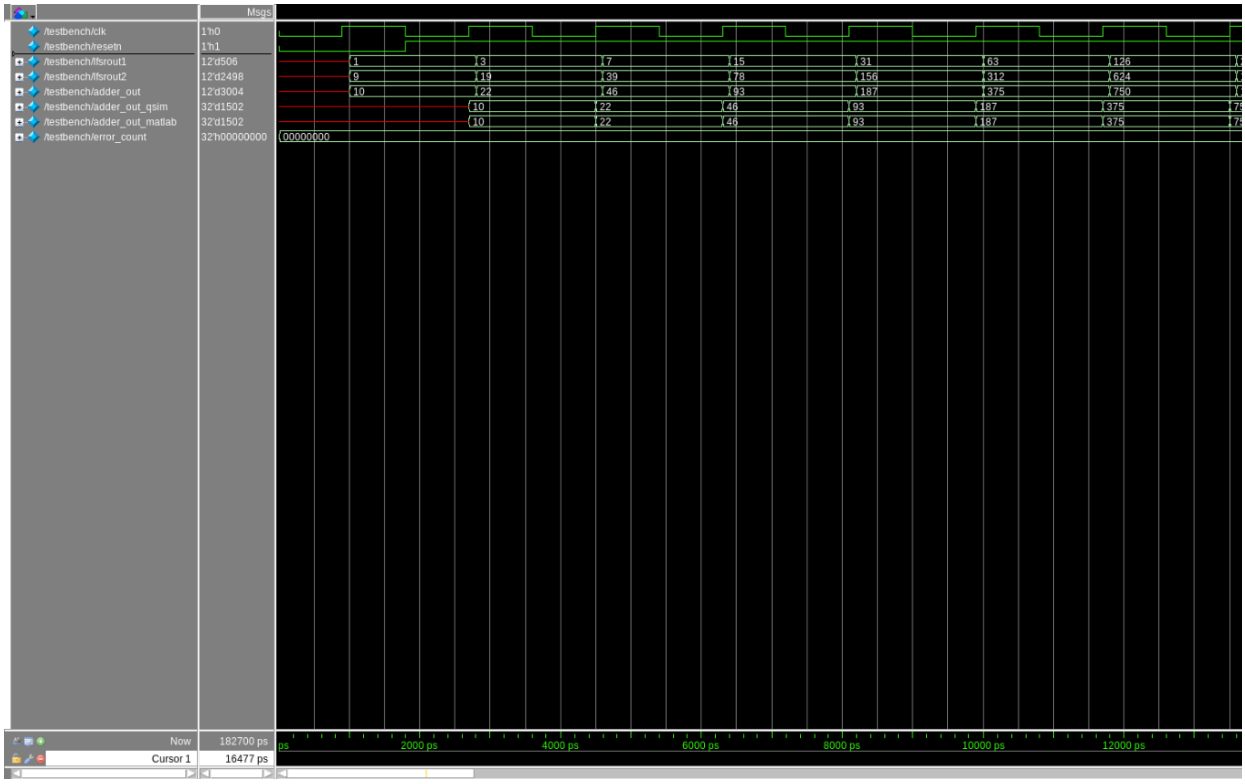
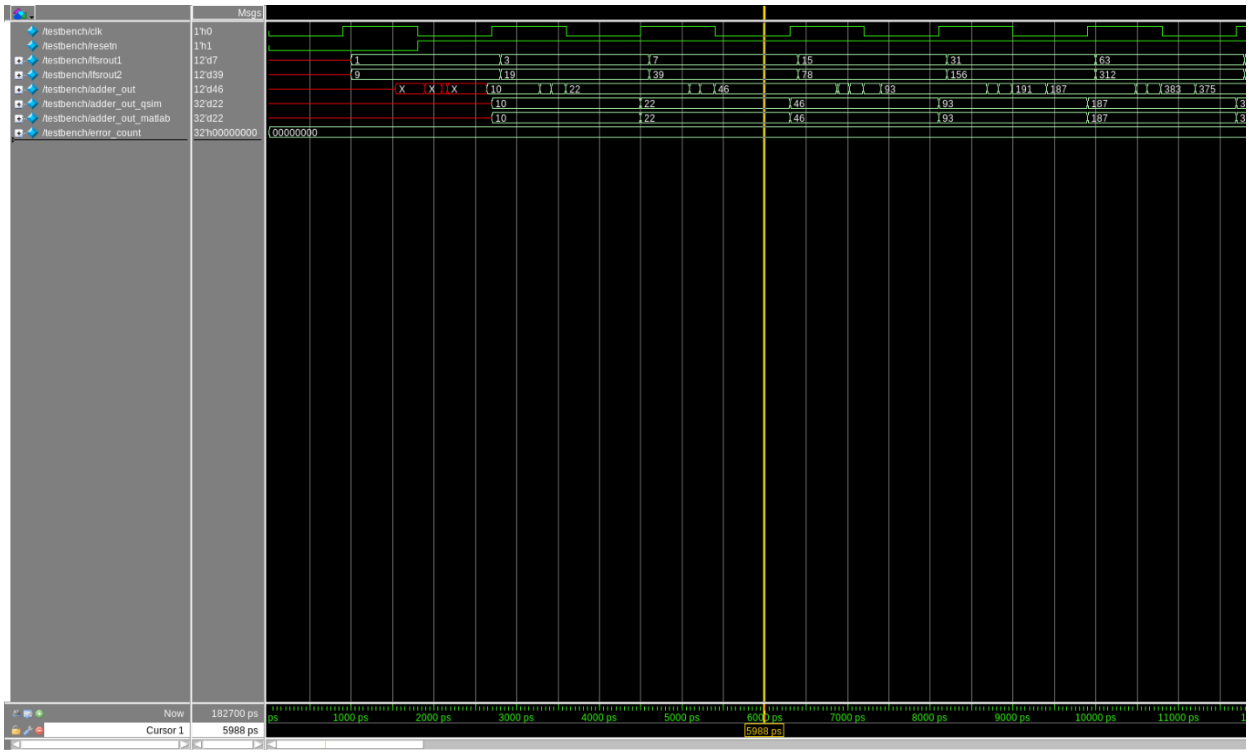
1. Dc simulation

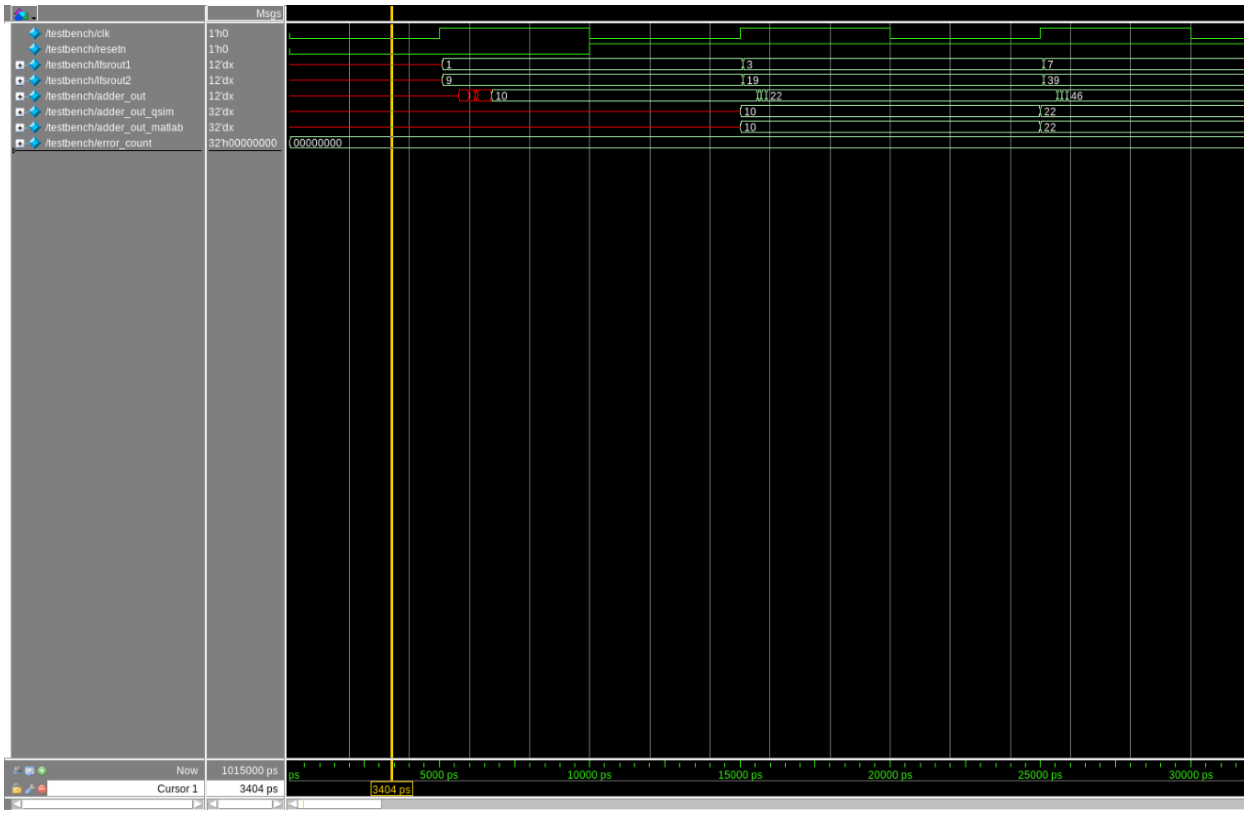
Wave in lab 2 (without sdf):



Wave with sdf file and clk period is 1.8:



Wave with sdf file and clk period is 10:



With the sdf file, we can simulate the gate circuit, and it's more accurate. There are delays between lfsr output and adder output (every bits need time to transit, the output can't be stable fast). When the clk period is too short, the delay can have an effect on the result (ep. 2 mistakes in 100 results)

2. Time

Critical path:

```
Startpoint: a[0] (input port clocked by clk)
Endpoint: sum[11] (output port clocked by clk)
Path Group: clk
Path Type: max

Point                                   Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                   0.0000     0.0000
clock network delay (ideal)             0.0000     0.0000
input external delay                    0.0500     0.0500 f
a[0] (in)                               0.0295     0.0795 f
U12/CO (CMPR32X2TS)                     0.6497     0.7292 f
U11/CO (CMPR32X2TS)                     0.4732     1.2024 f
U10/CO (CMPR32X2TS)                     0.4732     1.6756 f
U9/CO (CMPR32X2TS)                      0.4732     2.1488 f
U8/CO (CMPR32X2TS)                      0.4732     2.6220 f
U7/CO (CMPR32X2TS)                      0.4732     3.0952 f
U6/CO (CMPR32X2TS)                      0.4732     3.5684 f
U5/CO (CMPR32X2TS)                      0.4732     4.0417 f
U4/CO (CMPR32X2TS)                      0.4732     4.5149 f
U3/CO (CMPR32X2TS)                      0.4732     4.9881 f
U2/CO (CMPR32X2TS)                      0.4732     5.4613 f
U1/S (CMPR32X2TS)                       0.5538     6.0151 f
sum[11] (out)                           0.0000     6.0151 f
data arrival time                                  6.0151

clock clk (rise edge)                  10.0000    10.0000
clock network delay (ideal)             0.0000    10.0000
clock reconvergence pessimism           0.0000    10.0000
output external delay                  -0.0500     9.9500
data required time                                 9.9500
-----------------------------------------------------------
data required time                                 9.9500
data arrival time                                 -6.0151
-----------------------------------------------------------
slack (MET)                                        3.9349
```

Shortest path:

```
Startpoint: b[0] (input port clocked by clk)
Endpoint: sum[0] (output port clocked by clk)
Path Group: clk
Path Type: min

Point                                   Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                 0.0000     0.0000
clock network delay (ideal)           0.0000     0.0000
input external delay                  0.0500     0.0500 r
b[0] (in)                             0.0448     0.0948 r
U12/S (CMPR32X2TS)                    0.2732     0.3680 r
sum[0] (out)                          0.0000     0.3680 r
data arrival time                                0.3680

clock clk (rise edge)                 0.0000     0.0000
clock network delay (ideal)           0.0000     0.0000
clock reconvergence pessimism         0.0000     0.0000
output external delay                -0.0500    -0.0500
data required time                               -0.0500
-----------------------------------------------------------
data required time                               -0.0500
data arrival time                                -0.3680
-----------------------------------------------------------
slack (MET)                                       0.4180
```

3. Power

Adder doesn’t have clock, so it only has combinational power.

```
****************************************
Report : Time Based Power
Design : adder
Version: P-2019.03-SP2
Date   : Sun Oct 22 14:24:24 2023
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network              0.0000    0.0000    0.0000    0.0000 ( 0.00%)  i
register                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
combinational           2.079e-05 7.225e-06 7.449e-10 2.802e-05 (100.00%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 7.225e-06   (25.79%)
  Cell Internal Power  = 2.079e-05   (74.21%)
  Cell Leakage Power   = 7.449e-10   ( 0.00%)
                         ---------
Total Power            = 2.802e-05  (100.00%)

X Transition Power     =    0.0000
Glitching Power        =    0.0000

Peak Power             = 5.750e-04
Peak Time              =   225.100
```

```
****************************************
Report : Time Based Power
        -hierarchy
Design : adder
Version: P-2019.03-SP2
Date   : Sun Oct 22 14:24:24 2023
****************************************



                                    Int      Switch   Leak      Total
Hierarchy                           Power    Power    Power     Power    %
--------------------------------------------------------------------------------
adder                               2.08e-05 7.23e-06 7.45e-10  2.80e-05 100.0


                                    Peak     Peak            Glitch   X-tran
Hierarchy                           Power    Time            Power    Power
--------------------------------------------------------------------------------
adder                               5.75e-04 225.100-225.101    0.000    0.000
```

4. Timing.tcl

The adder doesn't have clock port, so only set virtual clock.

```
# Setting variables
set clk_period 10
set clk_uncertainty 0
set clk_transition 0.010
set typical_input_delay 0.05
set typical_output_delay 0.05
set typical_wire_load 0.005

# Create virtual clock, no port
set clk_name "clk"
create_clock -name $clk_name -period $clk_period

#Set clock uncertainty
set_clock_uncertainty $clk_uncertainty [get_clocks $clk_name]
#Propagated clock used for gated clocks only
set_clock_transition $clk_transition [get_clocks $clk_name]

# Set input and output delays
set_driving_cell -lib_cell INVX1TS [all_inputs]
set_input_delay $typical_input_delay [all_inputs] -clock $clk_name
#remove_input_delay -clock $clk_name
set_output_delay $typical_output_delay [all_outputs] -clock $clk_name

# Set loading of outputs
set_load 0.01 [all_outputs]
```