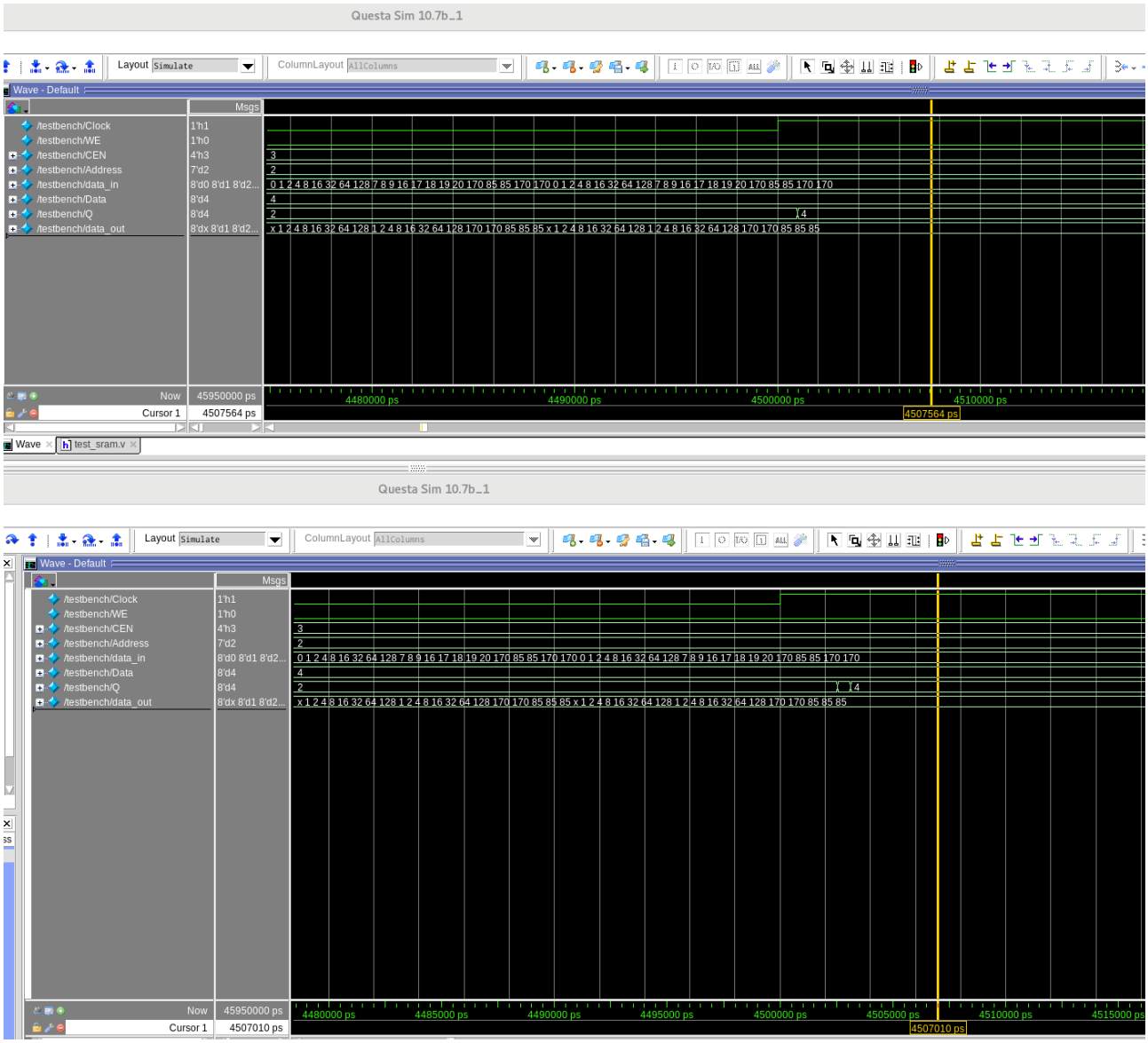
Simulation between rtl & dc:
Delay appeared



Power & time:
Got more accurate results

```
--------------------------------------------------------------------------------
                                  Switch   Int      Leak     Total
Hierarchy                         Power    Power    Power    Power    %
--------------------------------------------------------------------------------
sram                              2.72e-03    0.307 4.37e+05    0.311 100.0
1
```

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```
                                  Int      Switch   Leak     Total
Hierarchy                         Power    Power    Power    Power    %
--------------------------------------------------------------------------------
sram                              1.90e-07 8.83e-08 1.30e-09  2.80e-07 100.0

                                  Peak     Peak            Glitch   X-tran
Hierarchy                         Power    Time            Power    Power
--------------------------------------------------------------------------------
sram                              1.19e-02 20501.624-20501.625
                                                             0.000 5.43e-09
1
```

Open sram.dc.rpt ~/e4823/sram/result Save

```
  Startpoint: M5 (rising edge-triggered flip-flop clocked by clk)
  Endpoint: q_reg_0_ (positive level-sensitive latch clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                   Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   0.00       0.00
  clock network delay (ideal)             0.00       0.00
  M5/CLK (memory)                         0.00       0.00 r
  M5/Q[0] (memory)                        1.62       1.62 f
  U292/Y (AOI22X1TS)                      0.20       1.83 r
  U293/Y (NAND4X1TS)                      0.20       2.02 f
  U294/Y (AO22X1TS)                       0.49       2.51 f
  q_reg_0_/D (TLATXLTS)                   0.00       2.51 f
  data arrival time                                  2.51

  clock clk (rise edge)                   0.00       0.00
  clock network delay (ideal)             0.00       0.00
  q_reg_0_/G (TLATXLTS)                   0.00       0.00 r
  time borrowed from endpoint             2.51       2.51
  data required time                                 2.51
  -----------------------------------------------------------
  data required time                                 2.51
  data arrival time                                 -2.51
  -----------------------------------------------------------
  slack (MET)                                        0.00

  Time Borrowing Information
  -------------------------------------------------
  clk nominal pulse width                 50.00
  library setup time                      -0.38
  -------------------------------------------------
  max time borrow                         49.62
  actual time borrow                       2.51
  -------------------------------------------------


1
```

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Open | sram_pt.rpt | ~/e4823/sram/result | Save

```
Path Type: max

Point                                   Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                 0.0000     0.0000
clock network delay (ideal)           0.0000     0.0000
input external delay                  0.0500     0.0500 r
cen_c[1] (in)                         0.0424     0.0924 r
U150/Y (INVX2TS)                      0.0792     0.1716 f
U125/Y (CLKBUFX2TS)                   0.2110     0.3826 f
U128/Y (NOR3XLTS)                     0.6104     0.9930 r
U176/Y (INVX2TS)                      0.3716     1.3645 f
U144/Y (INVX2TS)                      0.1560     1.5205 r
U319/Y (AOI22X1TS)                    0.1133     1.6338 f
U323/Y (NAND4X1TS)                    0.1239     1.7577 r
U324/Y (AO22X1TS)                     0.2867     2.0444 r
q_reg_3_/D (TLATXLTS)                 0.0000     2.0444 r
data arrival time                                2.0444

clock clk (rise edge)                 0.0000     0.0000
clock network delay (ideal)           0.0000     0.0000
clock reconvergence pessimism         0.0000     0.0000
q_reg_3_/G (TLATXLTS)                            0.0000 r
time borrowed from endpoint           2.0444     2.0444
data required time                               2.0444
-----------------------------------------------------------
data required time                               2.0444
data arrival time                               -2.0444
-----------------------------------------------------------
slack (MET)                                      0.0000

Time Borrowing Information
-------------------------------------------------
clk nominal pulse width              50.0000
library setup time                   -0.0154
-------------------------------------------------
max time borrow                      49.9846
actual time borrow                    2.0444
-------------------------------------------------
```

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