Report 5 : 94%
Prelab 5 : 100%
Prelab 6 : 89%

Constructor University Bremen
Natural Science Laboratory
Electronics
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Lab Experiment 5- Metal Oxide Field Effect Transistor

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Place of execution: Teaching Lab EE
Bench 3
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INTRODUCTION

Objective

The aim of the experiment was to thoroughly understand the properties and practical applications of Field Effect Transistors (MOSFETs). This included analyzing their current-voltage (I-V) behavior and examining their functionality as amplifiers and switches.

Theory

Prelab

In this pre-lab we will assess the functioning of MOSFETs when operating in saturation mode, and we will also explore their use as switches.

Problem 1 : Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

1. **Differences Between Enhancement and Depletion MOSFETs**

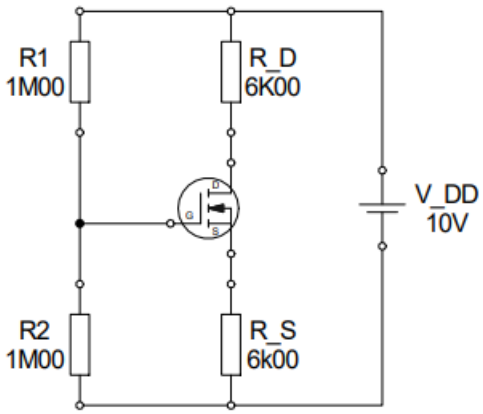
- In an enhancement MOSFET, the gate voltage creates a conductive channel between the drain and source, whereas, in a depletion MOSFET, the channel is inherently present without needing gate voltage.
- Enhancement MOSFETs require the gate voltage to exceed the threshold voltage to conduct, while depletion MOSFETs can conduct even at 0V gate voltage, as their channel is pre-established.

2. **Differences Between NMOS and PMOS Transistors**

- NMOS transistors have n-doped drain and source regions within a p-type substrate, while PMOS transistors feature p-doped drain and source regions within an n-type substrate.
- In NMOS transistors, current is transported by electrons, whereas in PMOS transistors, current is carried by holes.
- Enhancement-type NMOS transistors conduct when a positive gate voltage exceeds the threshold voltage.
- Enhancement-type PMOS transistors conduct when a negative gate voltage exceeds the threshold voltage in magnitude, indicating a negative threshold.

Problem 2 : MOSFET as Amplifier

Below is a picture showing the Common amplifier circuit.



$$I_{DS} = \mu_n C_G \frac{W}{2L}(V_{GS} - V_{th})^2 = k * (V_{GS} - V_{th})^2$$

The prefactor k is given by k = 0.5 mA/V2 . Vth = 1 V

Determining the gate-source and drain-source voltage and the drain current for the MOSFET amplifier:

$I_{DS} = k(V_{GS} - V_{TH})^2$

$R_{TH} = R1||R2$
$R_{TH} = \frac{1M * 1M}{2M}$
$R_{TH} = 0.5M\ \Omega$

$V_{THEV} = V_G$
$V_{THEV} = \frac{R1}{R1 + R2} * VDD$
$V_{THEV} = \frac{1 * 10^6}{1 * 10^6 + 1 * 10^6} * 10$
$V_{THEV} = 5V$

$V_{GS} = V_G - V_S$
$V_{GS} = 5 - I_s R_s$
$I_D = I_{DS} = I_s$
$I_{DS} = k(V_G - I_{DS}R_s - V_{TH})^2$
$I_{DS} = 0.0005(5 - I_{DS}(6000) - 1)^2$
$I_{DS} = 0.0005\big(4 - I_{DS}(6000)\big)^2$

$I_{DS} = 0.0005(16 - I_{DS}(48000) + 3.6 * 10^7 I_{DS}^2)^2$
$I_{DS} = (0.008 - 24I_{DS} + 18000I_{DS}^2)^2$
$0 = (0.008 - 24I_{DS} + 18000I_{DS}^2)^2$
$I_{DS} = I_D = 0.0005A\ or\ 0.0009A$
However, since 0.0009A will give a negative value, we will use 0.0005A

$V_{DD} = V_{RD} + V_{DS} + V_S$
$10 = 0.0005(6000) + V_{DS} + 0.0005(6000)$
$V_{DS} = 4V$
$V_{GS} = V_G - V_S$
$V_{GS} = 5 - 0.0005(6000)$
$V_{GS} = 2V$

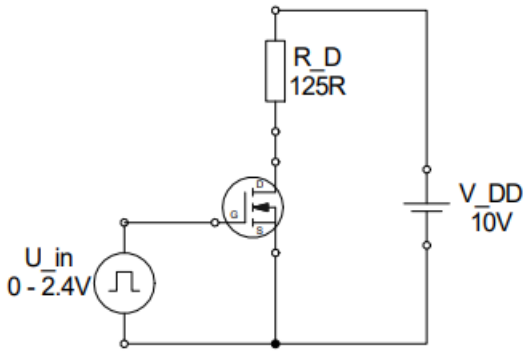
Showing that the MOSFET indeed operates in the saturation region:

In the saturation region
$V_{DS} > V_{GS} - V_{TH}$

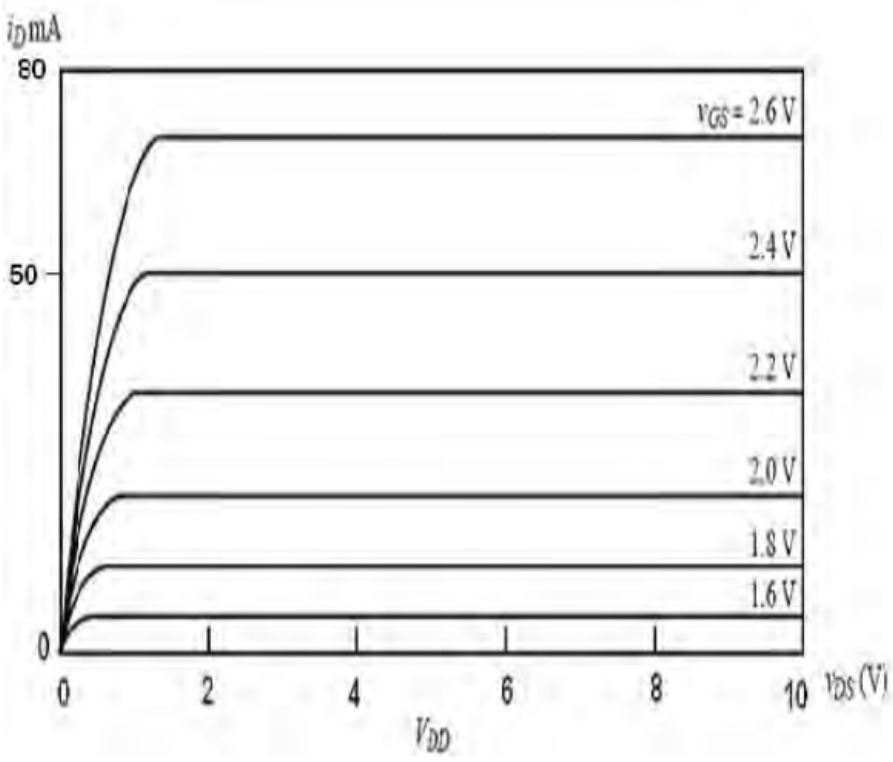
$V_{DS} > V_{GS} - V_{TH}$
$V_{DS} > V_{GS} - V_{TH}$
$4 > 2 - 1$

Therefore:
$V_{DS} > V_{GS} - V_{TH}$,
Is in the saturation region.

Problem 3 : MOSFET as Switch
Below is a picture showing MOSFET circuit as switch:



Below is a picture of the output characteristics graph:



For :
$V_G = 0V$
$I_{DS} = 0$
$V_{GS} = 0V$

Using KVL on the outer loop:
$V_{DD} = I_D R_D$
$I_D = \frac{V_{DD}}{R_D}$
$I_D = \frac{10}{125}$
$I_D = 0.08A$

$V_{DS} = V_{DD} - VR_D - V_S$
$V_{DS} = 10 - 10 - 0$
$V_{DS} = 0$

For :
$V_G = 2.4V$
$\mathrm{V_{GS}} = 2.4\mathrm{V}$

Using the graph:
$I_D = 50\ mA$
$V_{DD} = I_D R_D + V_{DS} + V_S$
$V_{DS} = V_{DD} - I_D R_D - V_S$
$V_{DS} = 10 - 0.05(125) - 0$
$V_{DS} = 3.75\ V$

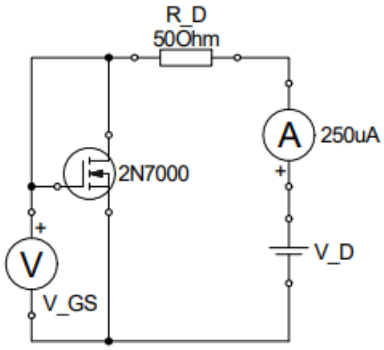
EXECUTION

Experiment Setup and results.

Preparation 1 : I/V Characteristic of a MOSFET

This part of the experiment focused on analyzing the current-voltage characteristics of an NMOS Field Effect Transistor. The circuit shown below was assembled on a breadboard to determine the threshold voltage Vth.

Below is a picture showing the output to determine V_{th} :



Execution 1.1

1. When $I_D = 250\mu A$, $V_{th} = V_{GS} = V_{DS}$.V_D is varied such that the ammeter A reads 250µA,V_{th} and I_D are measured and recorded with the results being shown below.

Results

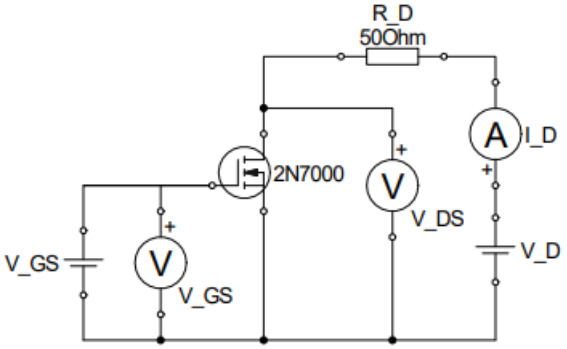
Below is a Table showing measured values:

Parameter	Value
VD (V)	2.2
ID (µA)	249.33
Vth (V)	2.094

Execution 1.2

The following circuit to measure the transfer characteristic:

Below is a picture of the circuit used for the transfer characteristic:



The gate source voltage was scanned from 0V to 3V. The drain source voltage V_{DS} was kept constant at 5V while changing V_{GS} and the results are shown in the Table below.

Results

Below is a Table showing measures values of the current and the gate and drain source voltage:

V_{GS} (V)	V_{DS} (V)	I_D (mA)
0	5.05	0
1.5	5.05	0
1.7	5.048	0
1.9	5.053	0.029
2	5.046	0.153
2.1	5.058	0.703
2.3	5.006	3.055
2.5	5.041	37.776
2.7	5.056	42.26
2.9	5.018	47.37
3	5.019	50.71

To measure the output characteristic for the gate source voltages 2V, 2.2V, 2.4V and 2.6V, the circuit above was used. The drain source voltage is scanned from
0V to 4V

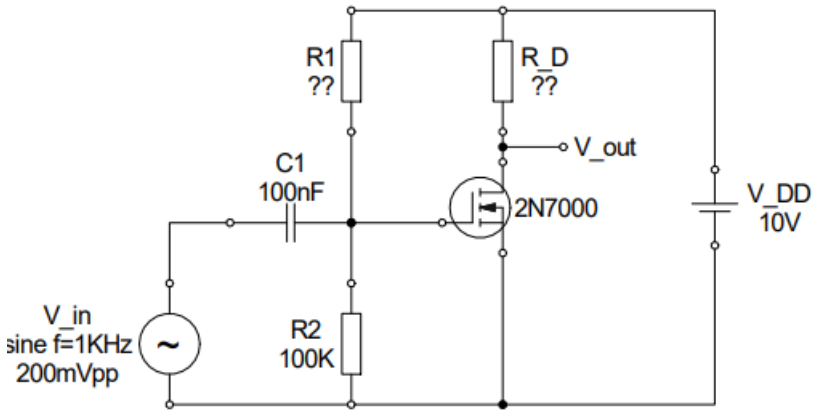
Below is Table showing measured values of the current and the gate and drain source voltage for different gate voltages:

V_{GS} (V)	2		2.2		2.4		2.6	
	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)
	0.035	0.018	0.258	0.014	0.389	0.006	0.015	0.002
	0.089	0.144	0.978	0.114	3.875	0.107	9.734	0.105
	0.094	0.273	1.144	0.304	4.836	0.201	14.149	0.202
	0.097	0.386	1.182	0.502	4.836	0.3	16.13	0.299
	0.097	0.435	1.2	0.701	5.557	0.507	15.159	0.402
	0.099	0.558	1.212	0.903	6.121	0.706	14.276	0.519
	0.099	0.627	1.22	1.009	6.919	0.91	13.9	0.602
	0.099	0.74	1.242	1.515	7.346	1	13.39	0.818
	0.099	0.853	1.26	1.999	9.922	1.498	13.712	1.018
	0.101	0.926	1.277	2.505	13.648	2.096	15.97	1.511
	0.1	1.08	1.295	3.013	16.339	2.505	19.065	2.012
	0.101	1.507	1.311	3.502	19.7	3.002	22.405	2.505
	0.104	2.008	1.327	4	23.281	3.5	25.856	3.001
	0.104	2.517			27.035	4.012	29.511	3.513
	0.105	3.008					33.314	4.009
	0.105	3.514						
	0.109	4.007						

Preparation 2 : MOSFET as Amplifier

This part of the experiment involved designing and implementing an amplifier circuit using a MOSFET. The circuit shown below was constructed on a breadboard.

Below is a picture showing an amplifier circuit using a MOSFET:



V_{GS} = 2.7 V, V_{DS} = 5 V, k = 72.2 mA/V2 , V_{th} = use measured value!

The values for R_1 and R_D were calculated to be:

$$V_{GS} = \frac{R_2}{R_1 + R_2} * V_{DD}$$

$$R_1 = \frac{V_{DD} R_2}{V_{GS}} - R_2$$

$$R_1 = \frac{10 * 100k}{2.7} - 100k$$

$$R_1 = 270.3\ k\Omega$$

$$I_{DS} = k(V_{GS} - V_{TH})^2$$
$$I_{DS} = 0.0722(2.7 - 2.1)^2$$
$$I_{DS} = 0.02599$$
$$I_{DS} = 0.026\ A$$

$$R_D = \frac{V_{DS}}{I_{DS}}$$

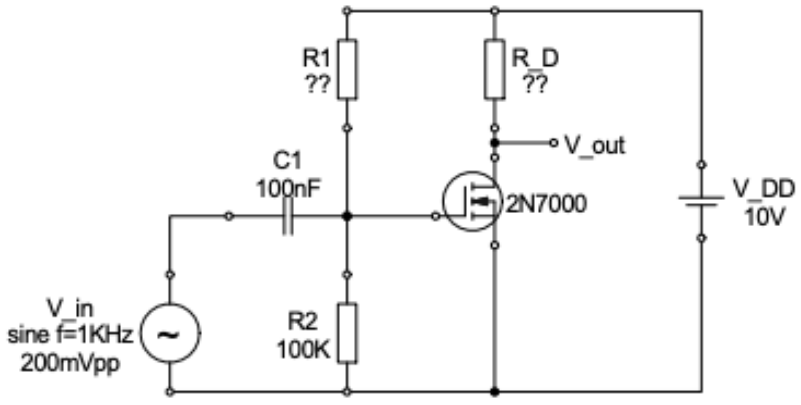
$$R_D = \frac{5}{0.026}$$
$$R_D = 192.3\Omega$$

R_D = 192. 3Ω *was not in the lab and the closest resistor was* 180. 00Ω which was used.

Execution 2

- The circuit is set up and a signal generator is linked, generating a sinusoidal input with an amplitude of 100mV and a frequency of 1kHz. The oscilloscope is attached across both the input and V_{out}.
- Hard copies showing the input and the output signals and the phase relation between them were taken.

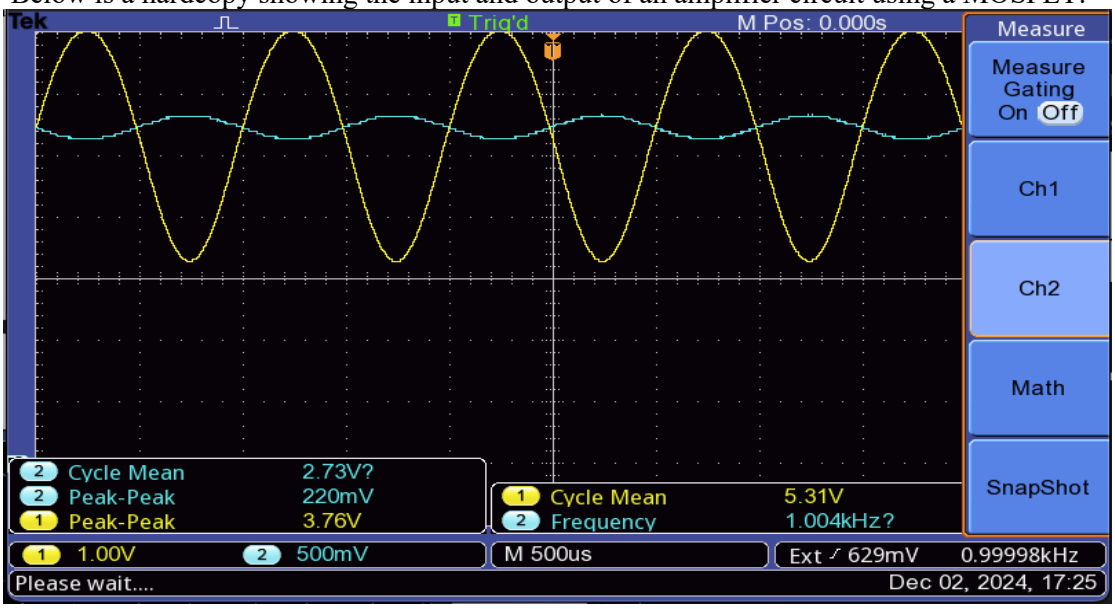
Below is a picture showing the circuit set up:



$V_{GS} = 2.7\,\mathrm{V}$, $V_{DS} = 5\,\mathrm{V}$, $k = 72.2\,\mathrm{mA/V^2}$, U_{th} = use measured value!

Results 2

Below is a hardcopy showing the input and output of an amplifier circuit using a MOSFET:



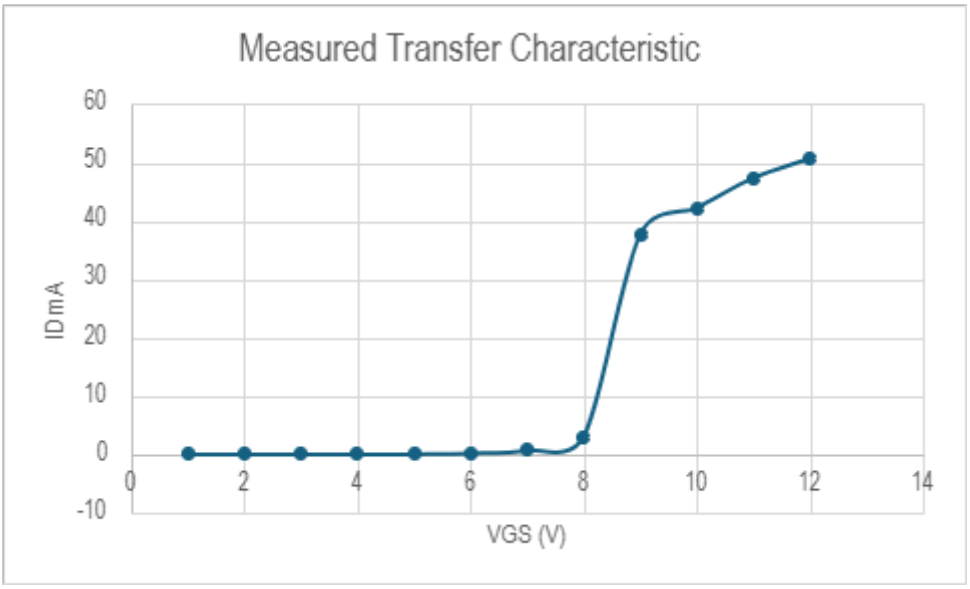
EVALUATION

Evaluation Experiment Part 1: : I/V Characteristic of a MOSFET

1. Plot the measured transfer characteristic.
2. Plot the measured output characteristic for the different gate source voltages.
3. Insert the $V_{DS} = V_{GS} - V_{th}$ line into the output characteristic.

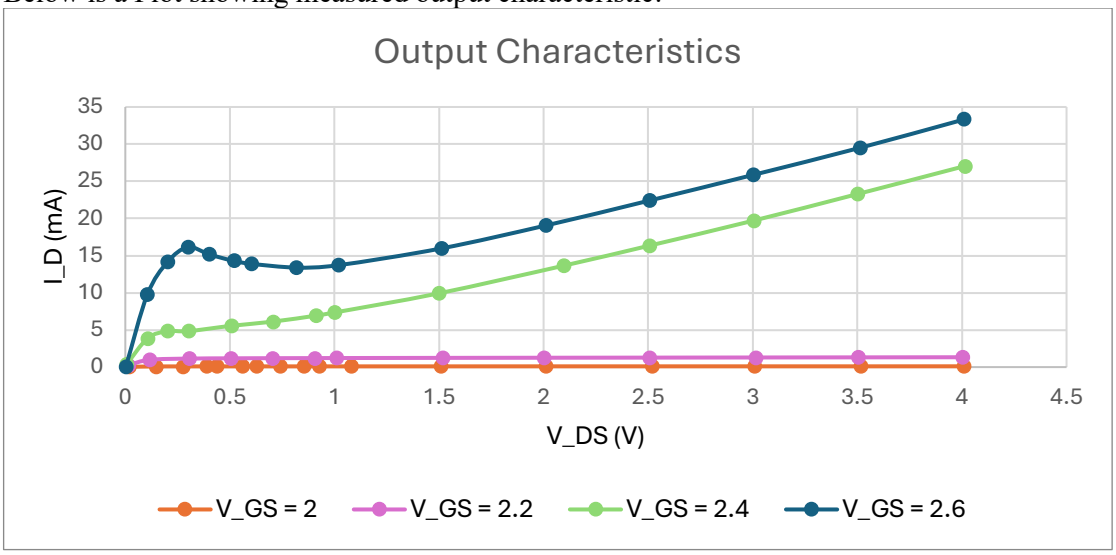
The measured transfer characteristic is plotted

Below is a Plot the measured transfer characteristic.



The measured output characteristic for the different gate source voltages is plotted:

Below is a Plot showing measured output characteristic:



To insert the $V_{DS} = V_{GS} - V_{th}$ line into the output characteristic:

$V_{DS} = V_{GS} - V_{TH}$

$I_{DS} = k(V_{GS} - V_{TH})^2$

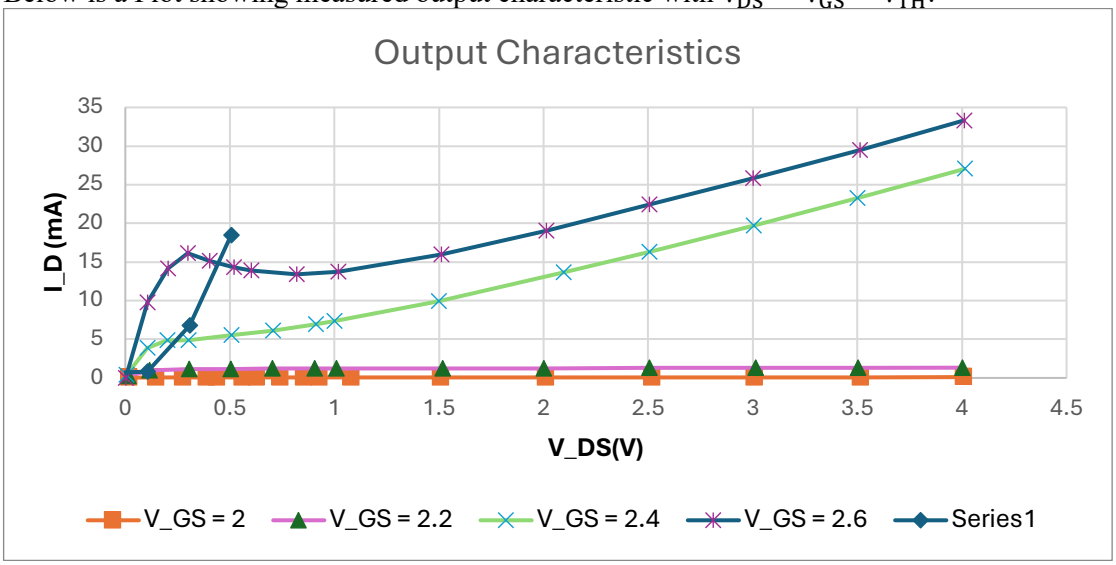
$I_{DS} = 72.2(2.00 - 2.094)^2$

$I_{DS} = 0.63796$

Below is a table showing calculated values of $V_{DS}=V_{GS}-V_{TH}$:

VGS(V)	$V_{DS} = V_{GS} - V_{TH}$	I_D mA
2.00	-0.094	0.6379592
2.20	0.106	0.8112392
2.40	0.306	6.7605192
2.60	0.506	18.4857992

Below is a Plot showing measured output characteristic with $V_{DS} = V_{GS} - V_{TH}$:



Problem 2 : MOSFET as Amplifier

1. In which mode (linear or saturation) does the transistor operate during amplification? Provide an explanation.
2. If the amplitude of the sinusoidal input voltage is too large clipping of the output voltage is observed. Determine the largest possible input voltage for which no clipping is observed.
3. Provide a mathematical expression for the voltage gain (theoretical voltage gain) of the circuit.
4. Determine the measured voltage gain and compare the measured voltage gain with the theoretical voltage gain.
5. Explain the phase relation between the input and the output.

The transistor operates in the saturation region because :

$V_{DS} > V_{GS} - V_{TH}$

$5 > 2.0 - 2.094$
$5 > 0.094$

This demonstrates that in the triode region, the voltage of a MOSFET is influenced by both the gate-source voltage VGS and the drain-source voltage VDS. However, in the saturation region, the output voltage depends solely on VGS. In the circuit analyzed during this experiment, the output voltage Vout is determined by the current flowing through the drain resistor RD, making it dependent only on VGS. Therefore, the MOSFET operates in the saturation region during amplification.

The maximum output that can be realised is:

$V_{out} = V_{DD}$
$V_{in} = \frac{V_{DD}}{G}$

$$V_{in} = \frac{10}{24} = 0.4\ V$$

This means that the maximum amplitude without clipping is 0.4V

Theoretical voltage gain:

$$V_{out} = V_{DD} - I_D R_D$$
$$V_{out} = V_{DD} - k(V_{GS} - V_{TH})^2 R_D$$

$$V_{out} = 10 - 0.0722(2.7 - 2.094)^2 * 192.367$$
$$V_{out} = 4.8994\ V$$

$$V_{in} = V_p = 0.2\ V$$
$$V_{out} = 4.8980\ V$$

$$A_V = \frac{V_{out}}{V_{in}}$$

$$A_V = \frac{4.8980}{0.2}$$

$$A_V = 24.49$$

The measured voltage gain:

$$A_V = \frac{V_{out}}{V_{in}}$$

$$A_V = \frac{3.28}{0.202}$$

$$A_V = 16.2376$$

The theoretical gain exceeds the experimental value due to variations in MOSFET parameters such as k and VGS. Moreover, while the calculated resistor value was 192.367 ohms, a 180-ohm resistor was used in the experiment, contributing to the observed discrepancies. Instrumental inaccuracies from the signal generator and oscilloscope further impacted the results. Additionally, the output voltage exhibits a 180-degree phase shift relative to the input voltage. This occurs because as the input voltage increases, the gate-source voltage VGS also rises, leading to an increase in drain current. This, in turn, causes a significant voltage drop across RD.

CONCLUSION

In the first part of the experiment, the output and I-V characteristics of MOSFETs were analyzed. The experimental data was used to plot an I-V characteristic graph, revealing an exponential relationship between the gate-to-source voltage VGS and the drain current ID. A threshold voltage of 2V was determined from the graph, closely aligning with the multimeter reading of 2.094V. An output characteristic graph was then plotted using fixed VGS values to examine the MOSFET's operating regions. The results matched theoretical predictions, showing a linear relationship between ID and the drain-to-source voltage VDS in the triode region, confirming the MOSFET's behavior as a resistor. In the saturation region, the drain current remained nearly constant, highlighting the MOSFET's capability as a current source.

In the second part of the experiment, the MOSFET's use as an amplifier was studied. When operating in the saturation region, the MOSFET functioned as an amplifier. The experimental data showed a gain of 24.49, compared to the theoretical gain of 16.23. The discrepancies between theoretical and experimental values could be attributed to variations in the MOSFET constant kk, the selected VGS, and the use of a different resistor value for RD. Instrumental inaccuracies from the signal generator and oscilloscope likely contributed to these differences as well.

REFERENCE

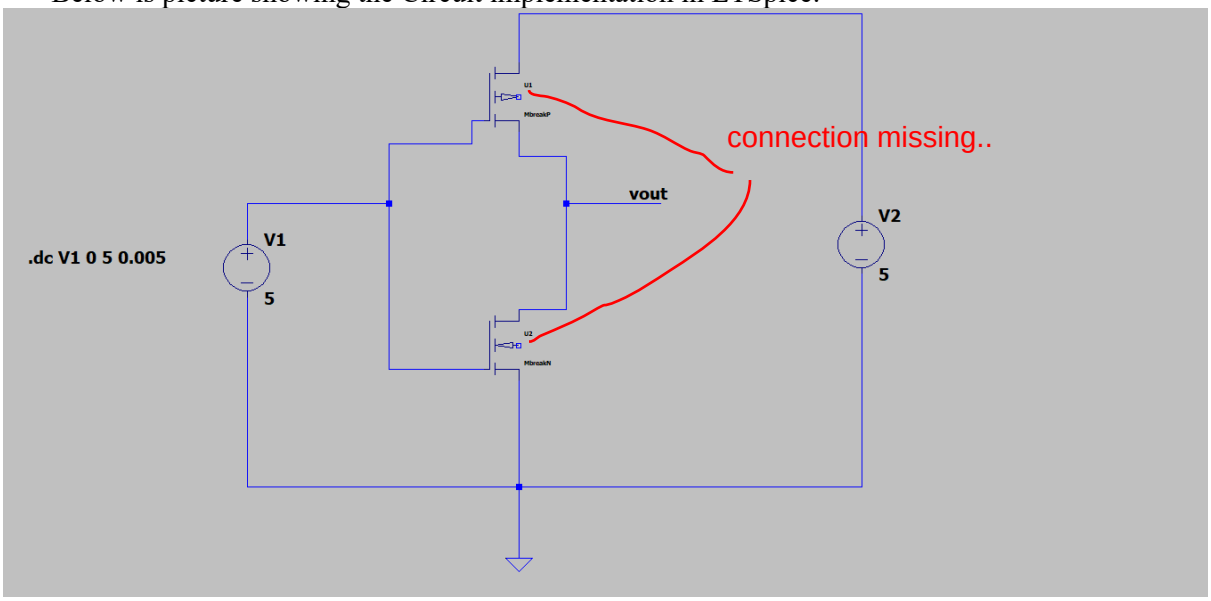
1. Uwe Pagel & Prof. Dr. Ing. Mojtaba Joodaki, Constructor University Bremen
2. CO-526-B Electronics Lab Manual

Prelab : CMOS Inverter and Logic Gates

Problem 1 : Voltage Transfer Characteristic of a CMOS inverter

1. Use 5V for the power supply VDD. Simulate the voltage transfer curve (VTC) of the CMOS inverter and extract the values of V_{OH}, V_{OL}, V_{IH}, V_{IL}, N_{ML}, N_{MH}, and V_{th}. Hint: Use the d() function of LTSpice to determine VIH, VIL!!
2. Simulate the current flowing through the inverter as a function of the input voltage.
3. For what input level the current reaches its maximum. Provide an explanation.

Below is picture showing the Circuit implementation in LTSpice:



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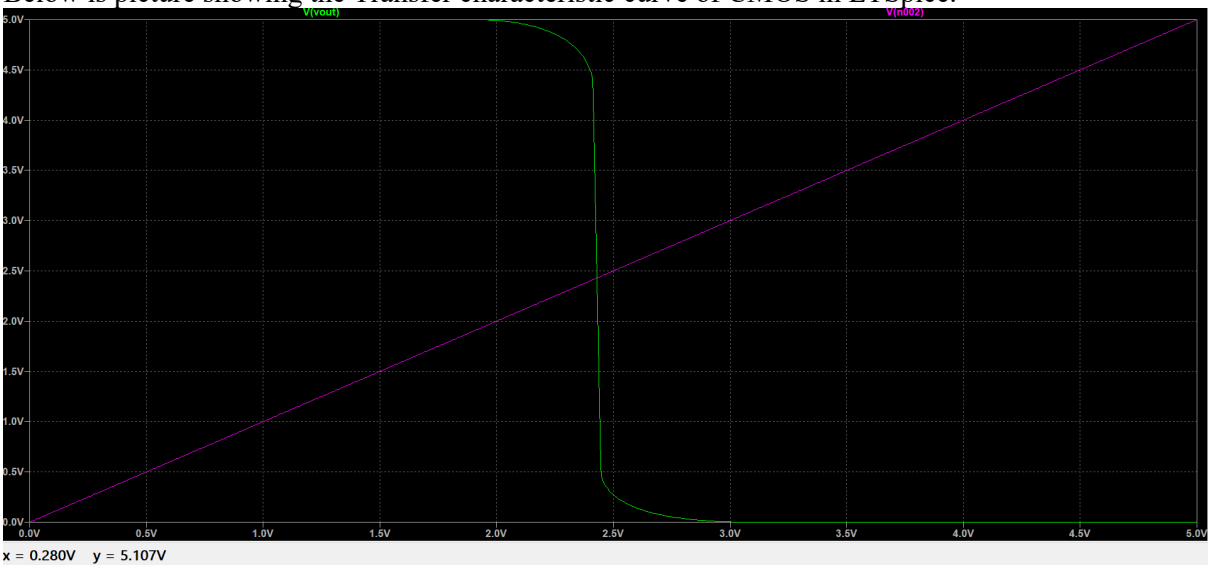
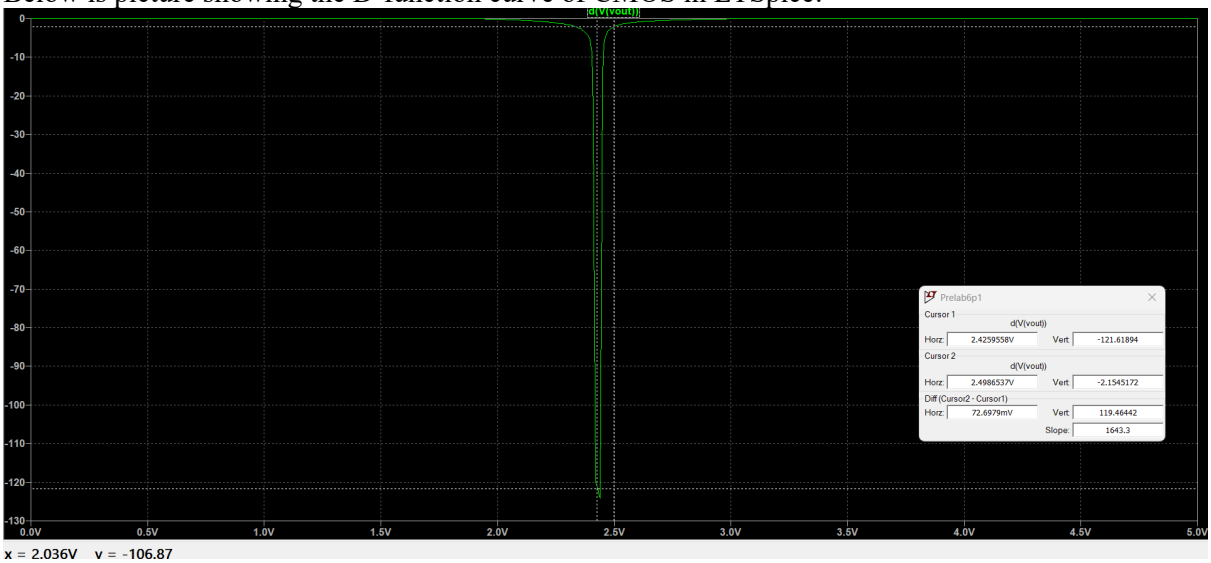
Below is picture showing the Transfer characteristic curve of CMOS in LTSpice:

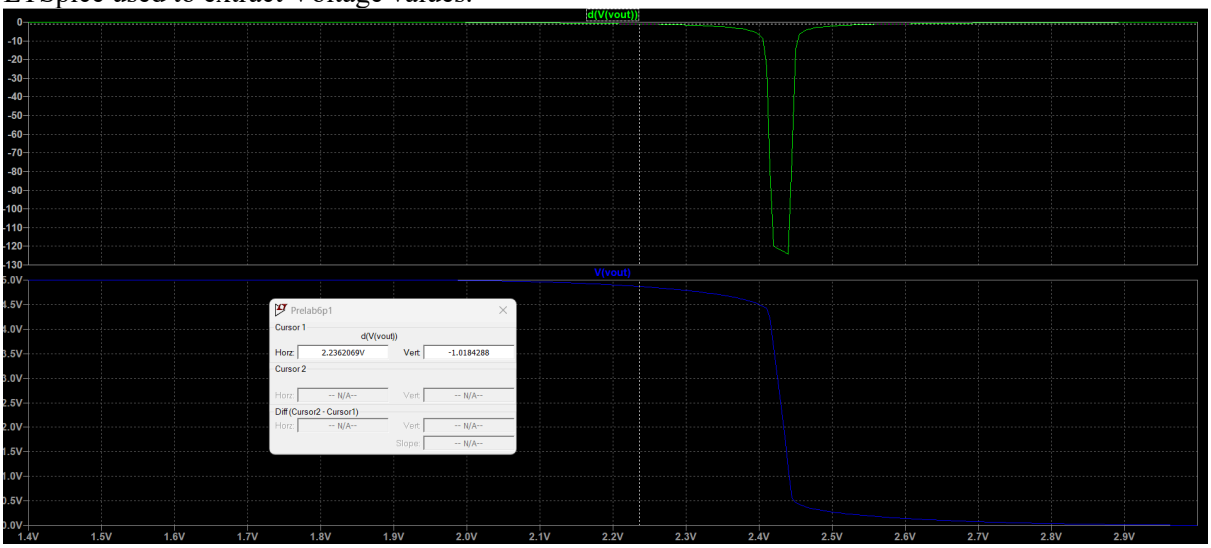


Below is picture showing the D-function curve of CMOS in LTSpice:

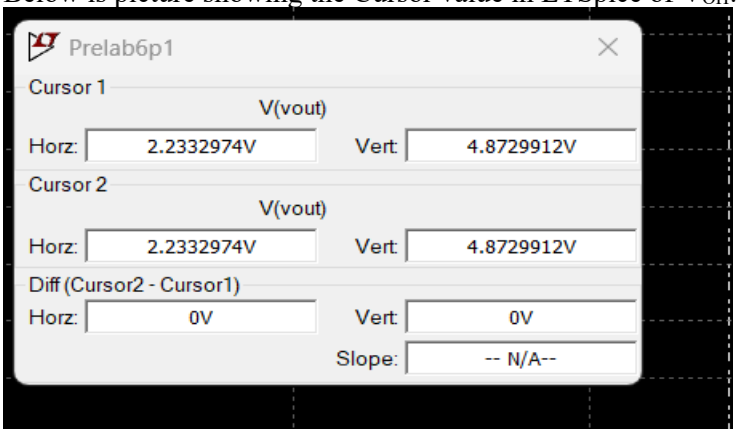


The cursors were used with the graphs to extract the values of V_{OH}, V_{OL}, V_{IH}, V_{IL}, N_{ML}, N_{MH}, and V_{th}.

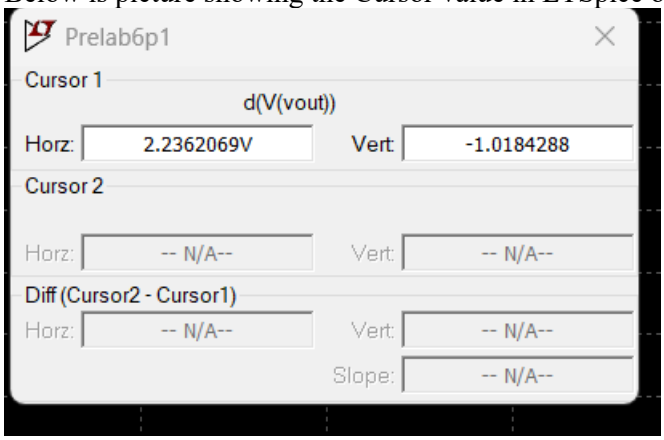
Below is picture showing the Transfer characteristics and D-function curve of CMOS in LTSpice used to extract Voltage values:



Below is picture showing the Cursor value in LTSpice of V_{OH}:



Below is picture showing the Cursor value in LTSpice of V_{IL}:

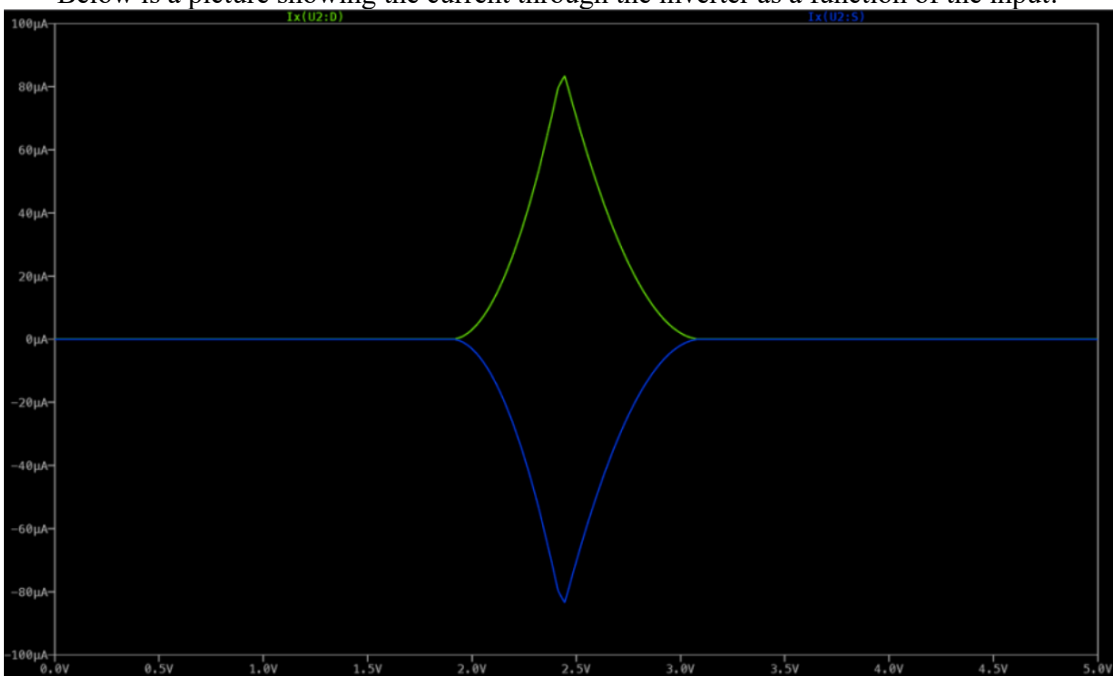


Below is a Table showing voltage values:

Name	Value (V)
V_{OH}	4.87
V_{OL}	0.162
V_{IH}	2.58
V_{IL}	2.23
N_{ML}	0.255
N_{MH}	0.042
V_{th}	2.43

Finding the current through the inverter as a function of the input:

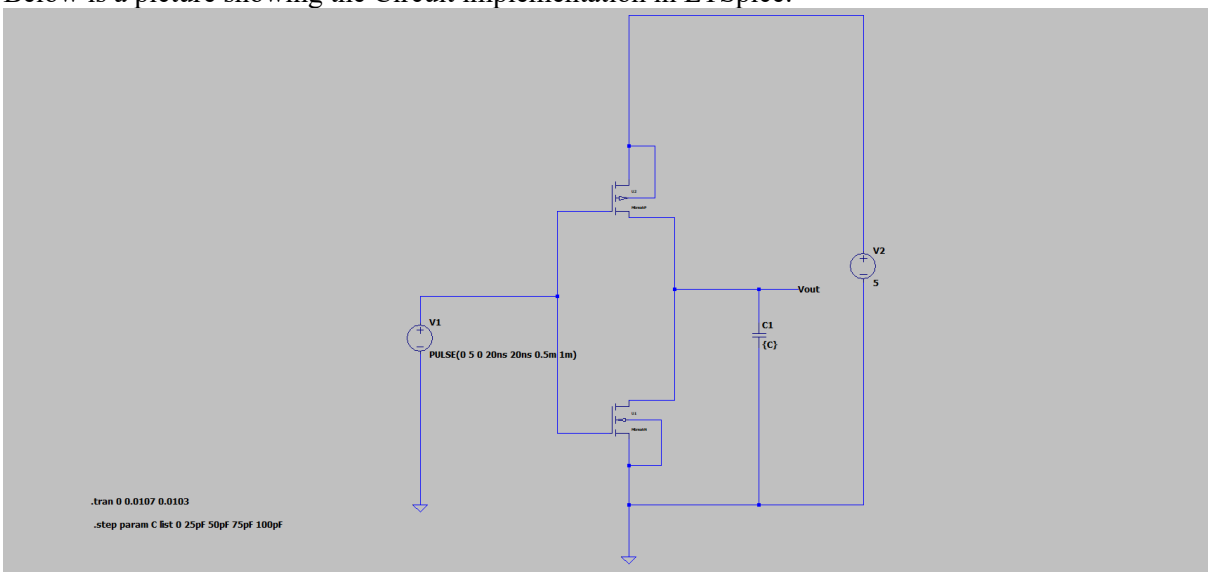
Below is a picture showing the current through the inverter as a function of the input:



The value of the minimum input and maximum output value. The current reaches its peak at an input of 2.4419V. This occurs when both transistors are in the ON state, resulting in the maximum current flow.

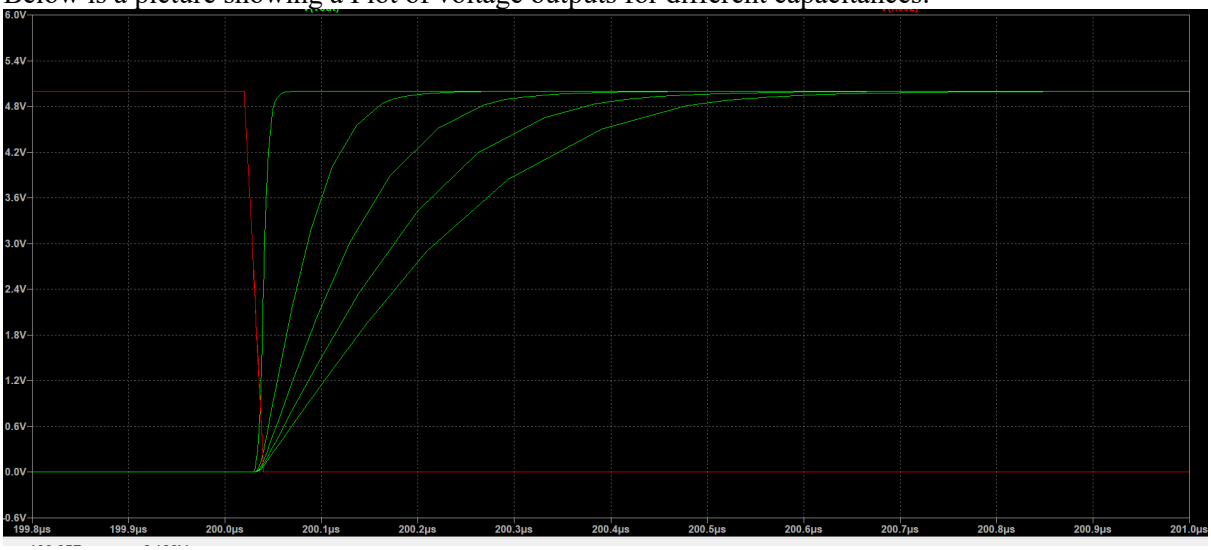
Problem 2 : CMOS Inverter with Capacitive Load

Below is a picture showing the Circuit implementation in LTSpice:

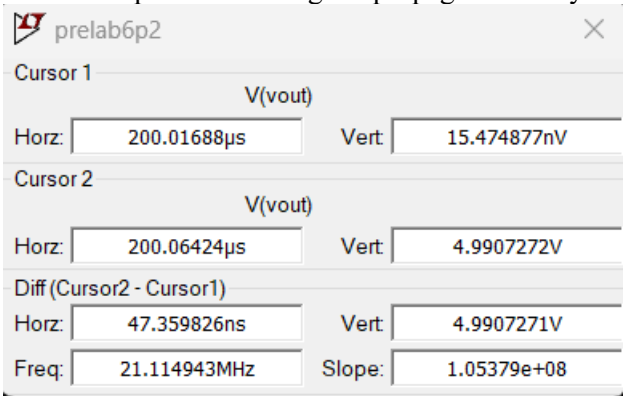


The graph generated of the propagation delay (tPLH = tPHL) is shown below:

Below is a picture showing a Plot of voltage outputs for different capacitances:



Below is a picture showing the propagation delay using the cursors is approximately 47.36ns.:



delay times?

The dynamic power dissipation for the CMOS inverter for different capacitors is obtained and shown below:

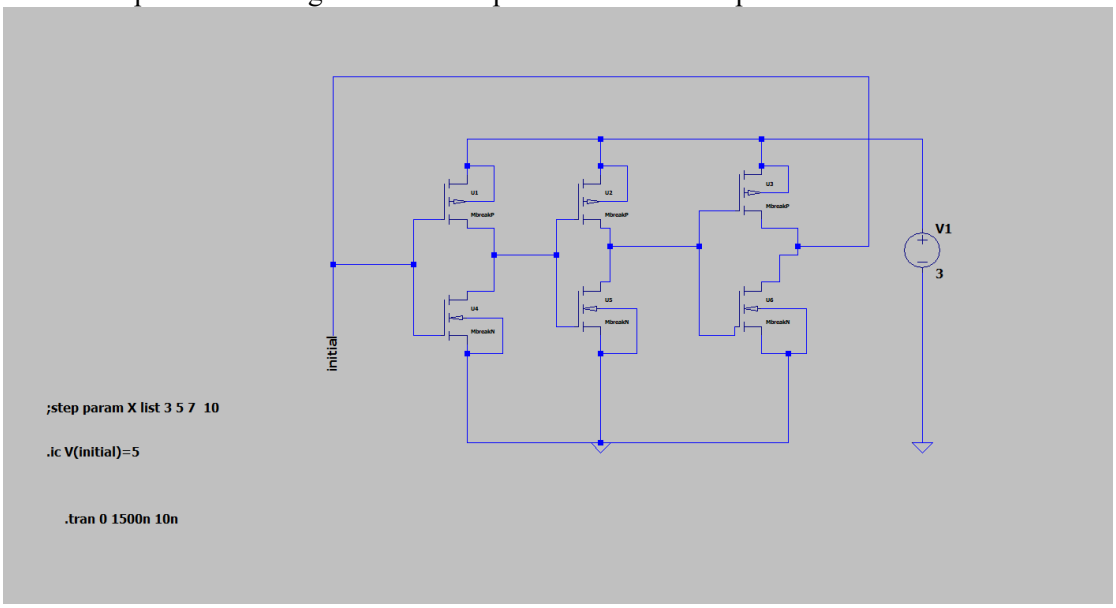
Dynamic power dissipated:

$P_D = fCV^2$
$P_D = 1000 * c * 10^{-12} * 5^2$
$P_D = 1000 * 25 * 10^{-12} * 5^2$
$P_D = 6.25 * 10^{-7}$

Below is a Table showing calculated values:

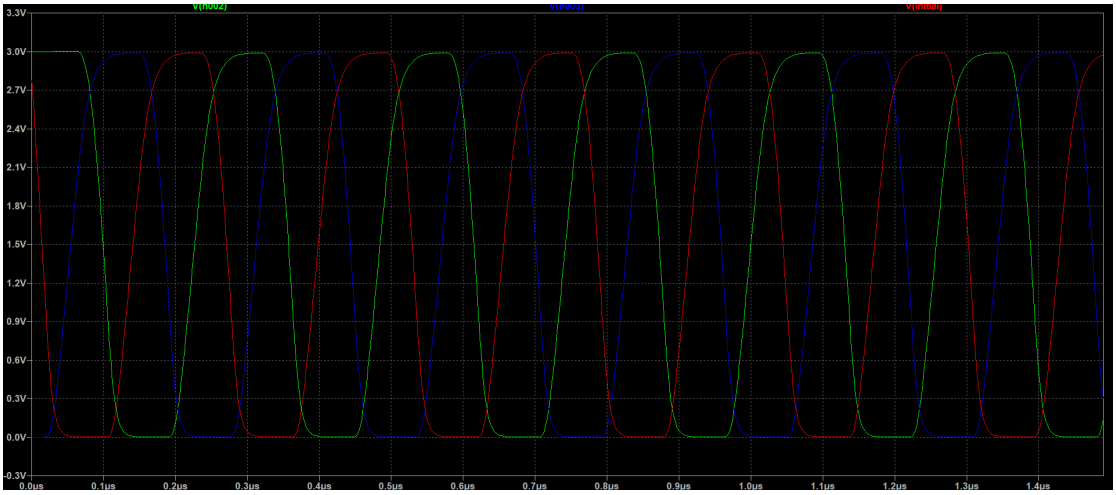
Capacitance (F)	Power dissipated(w)
25 pF	$6.25 * 10^{-7}$
50 pF	$1.25 * 10^{-6}$
75 pF	$1.875 * 10^{-6}$
100 pF	$2.5 * 10^{-6}$

Problem 3 : Propagation Delay of an Inverter Stage
Below is a picture showing the Circuit implementation in LTSpice:

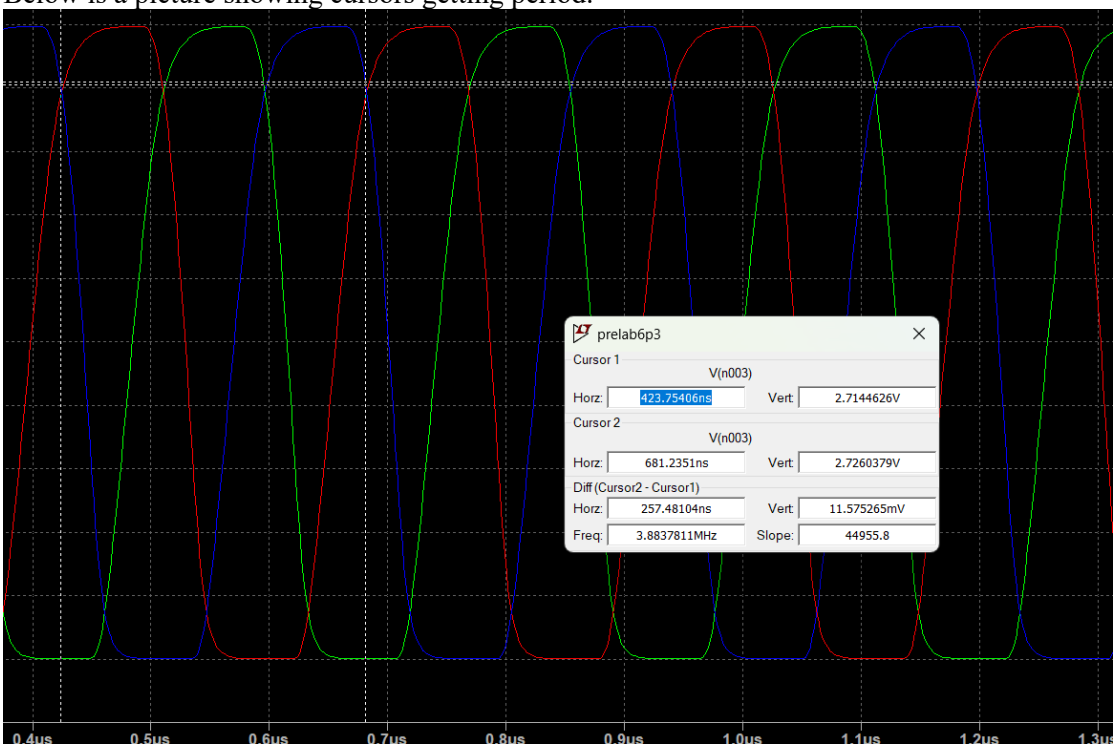


Determining the oscillation frequency of the ring oscillator and the propagation delay per inverter stage for supply voltages of 3 V, 5 V, 7 V and 10 V, respectively:

Below is a picture showing Voltage after first and second oscillator:



Below is a picture showing cursors getting period:



1. Determining the oscillation frequency of the ring oscillator and the propagation delay per inverter stage for supply voltages of 3 V, 5 V, 7 V and 10 V, respectively:

The other propagation delay was found using the following formula:

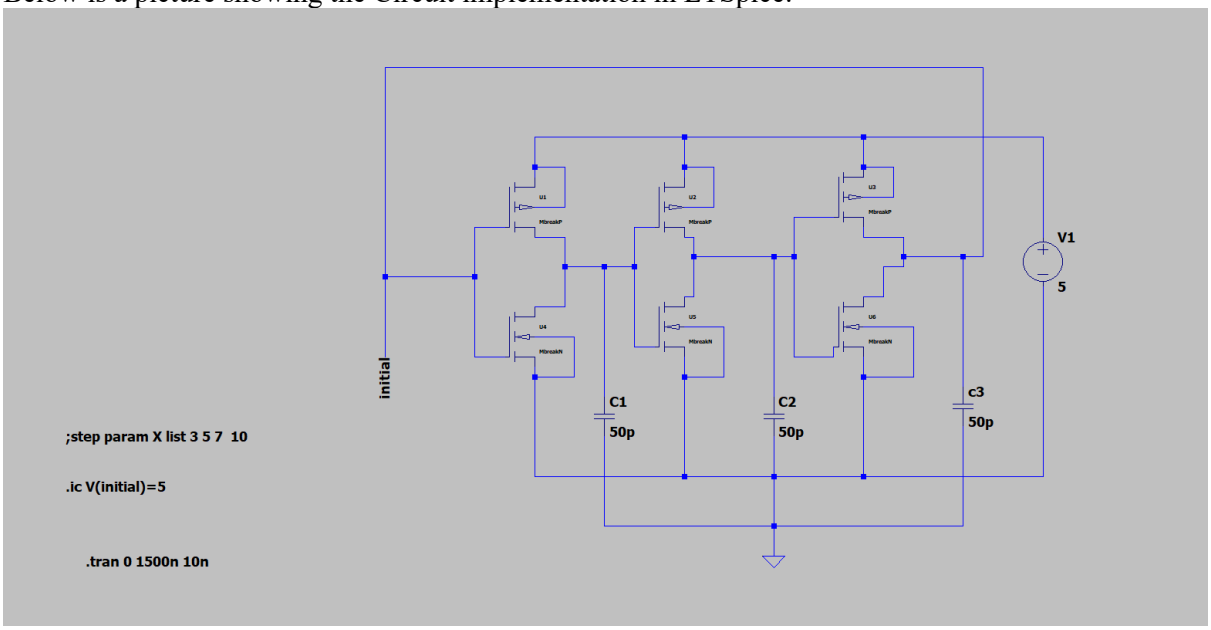
$$t_d = \frac{1}{2Nf}$$

where N is the number of rings in an oscillator.

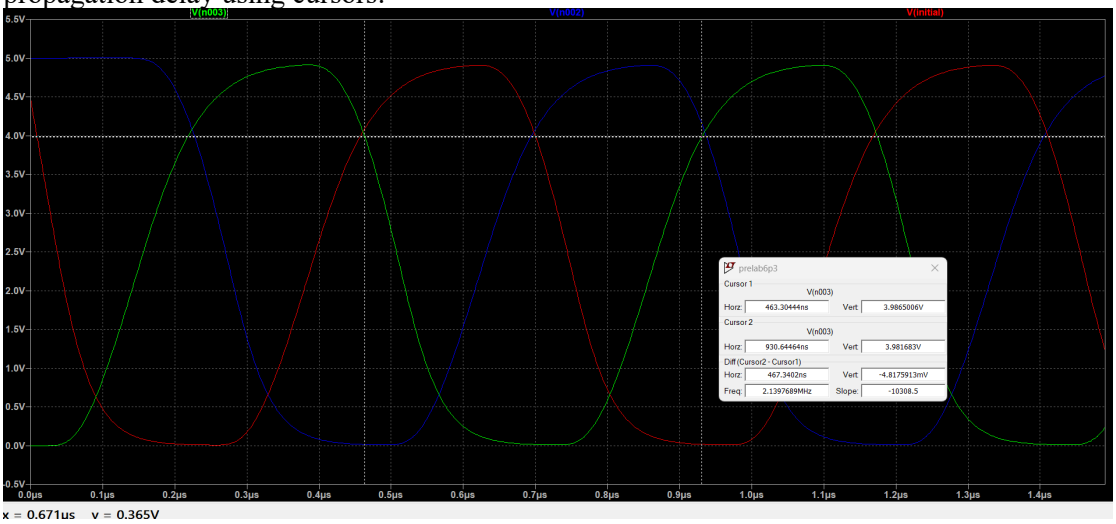
Below is a Table showing calculated values:

Voltage Supply(V)	Frequency (MHz)	Time delay (ns)
3	3.871	430.55
5	23.49	42.57
7	54.71	1.3055
10	121.28	4.12269

Below is a picture showing the Circuit implementation in LTSpice:



Below is a picture showing The measured oscillation frequency and the determined propagation delay using cursors:



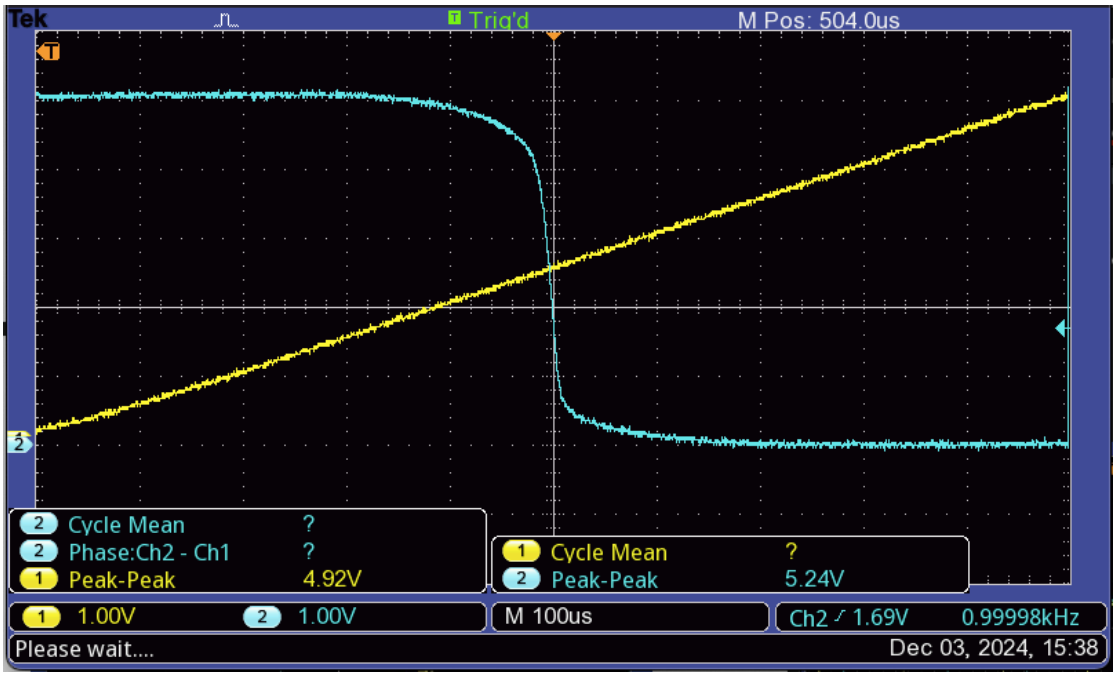
The frequency registers at 2.13MHz, with a propagation delay of 467.34ns. Introducing the capacitor load results in a decrease in frequency and an increase in time delay. Higher capacitance and power supply lead to increased power dissipation, while the opposite holds true.

why?

Execution CMOS Inverter and Logic Gates

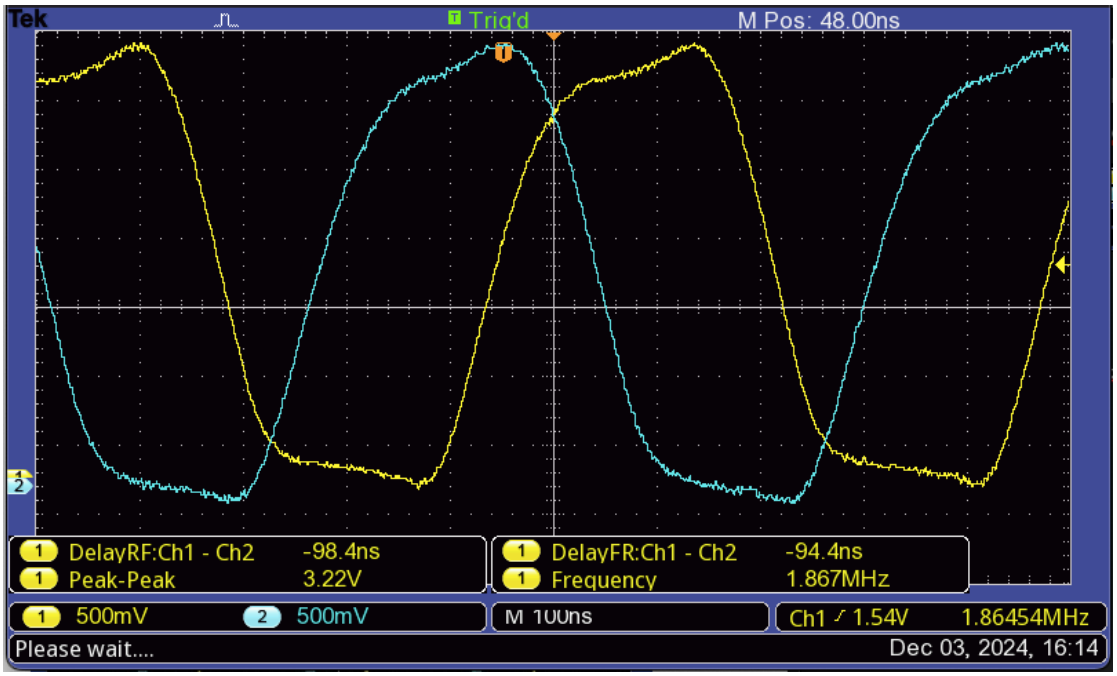
Problem 1 : Voltage transfer characteristic of an Inverter

Below is a hardcopy showing Vin ramp together with Vout on the screen :

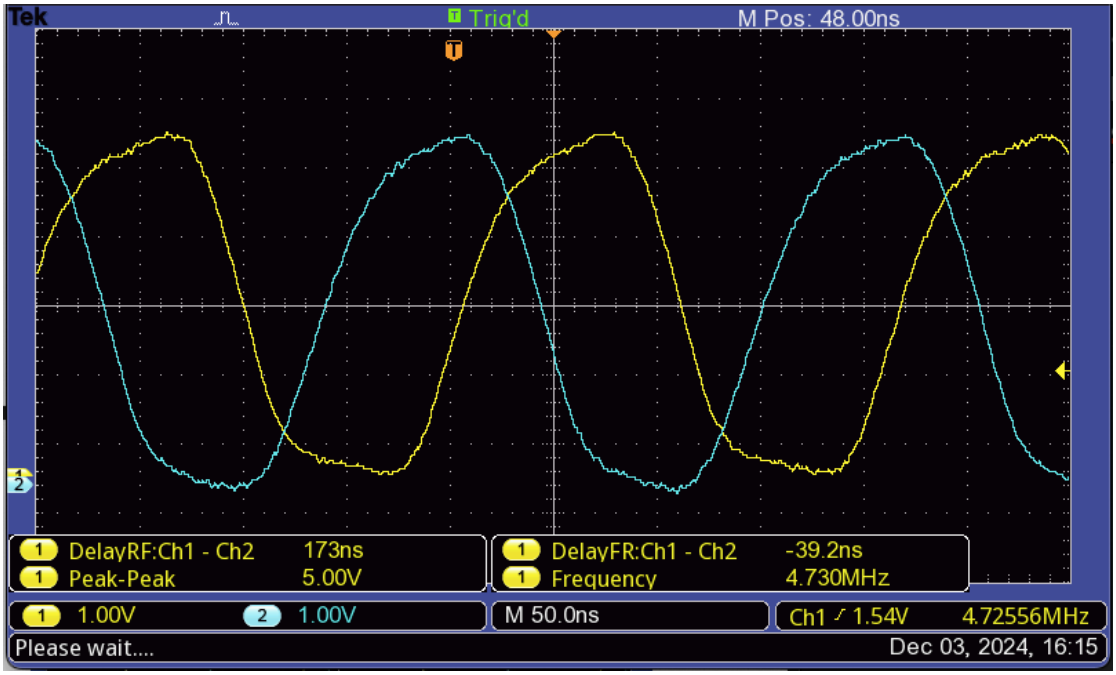


Problem 2 : Propagation Delay of an Inverter

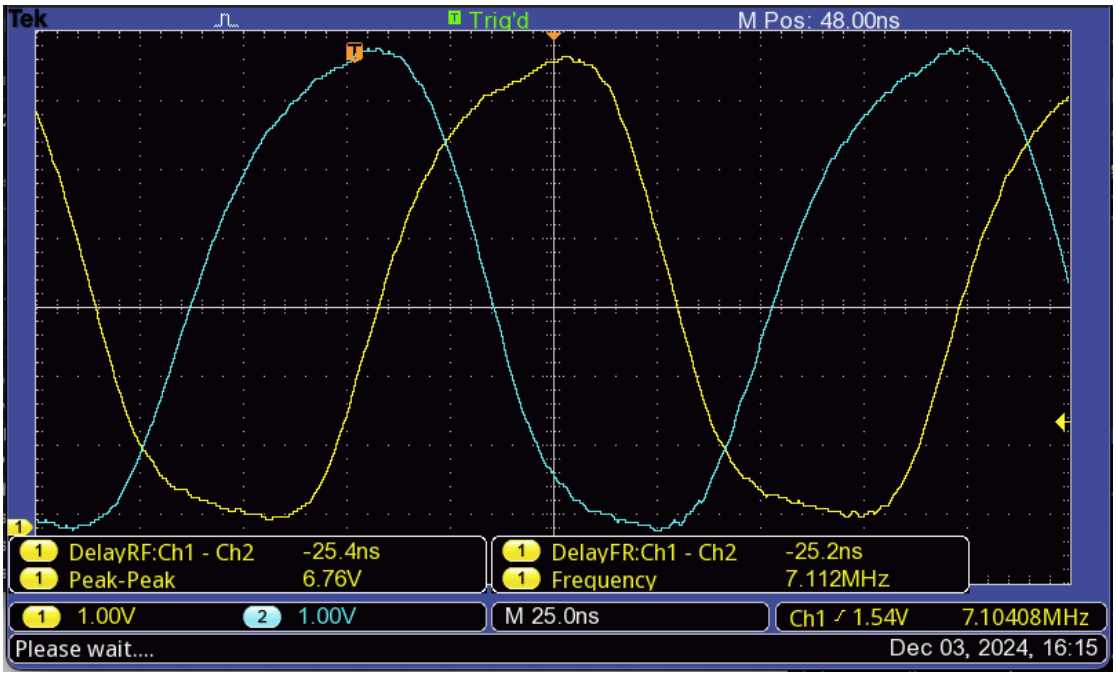
Below is a hardcopyt showing PLH and tPHL of first inverter at 3V:



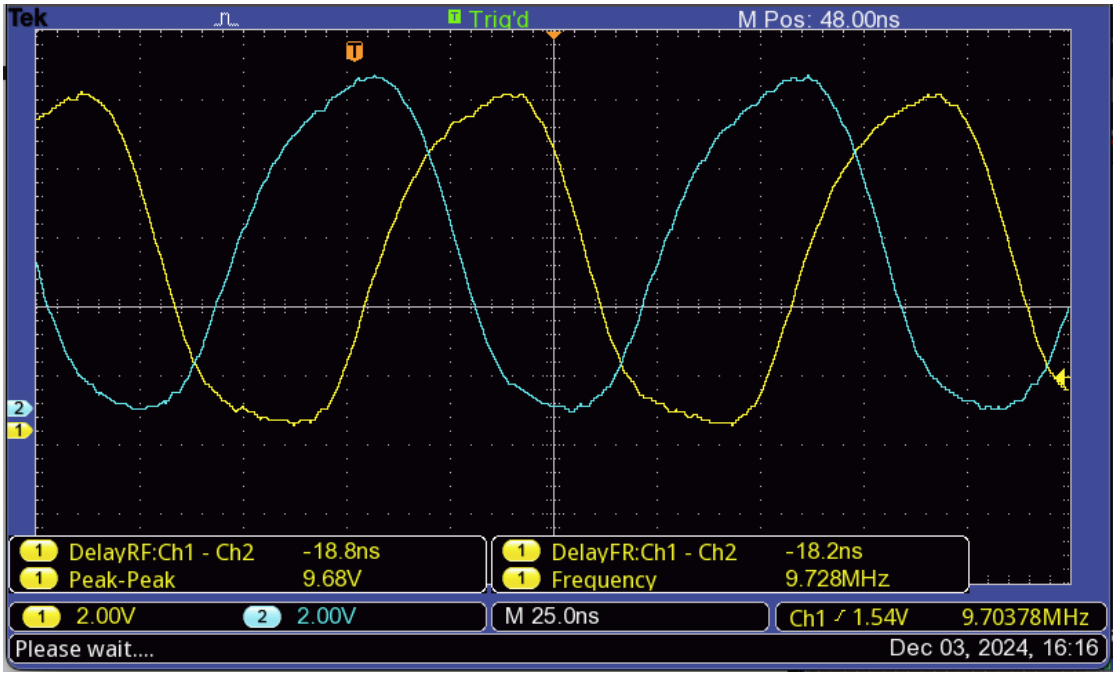
Below is a hardcopyt showing tPLH and tPHL of first inverter at 5V:



Below is a hardcopyt showing tPLH and tPHL of first inverter at 7V:



Below is a hardcopy showing tPLH and tPHL of first inverter at 10V:



Below is a hardcopyt showing tPLH and tPHL of first inverter at V_{DD}=5V: