Computer Organization and Architecture

Me lol

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Notes

- PYQs of BEX/BEI/BCT's CT603 are combined.

- BEX's and BCT's are kept with normal font.

- BEI's are kept with `this styling to differentiate`.

- Regular exam's questions are kept as **bold** while back exam are kept as normal font.

- Months are marked as:

  - Ba: Baisakh
  - Jth: Jestha
  - Asa: Ashar
  - Shr: Shrawan
  - Bh: Bhadra
  - Ash: Ashwin
  - Ka: Kartik
  - Mng: Mangsir
  - Po: Poush
  - Ma: Magh
  - Ch: Chaitra

Contents

1 Introduction

<div align="center">(3 Hours/6 Marks)</div>

1.1 Computer organization and architecture

1. Define computer architecture. [2] (**75 Ch**) [1.5] (81 Bh) [1] (**72 Ch**)
2. Define computer organization. [1.5] (**81 Bh**) [1] (**72 Ch**)
3. Differentiate between computer organization and architecture. [2] (**71 Ch**, 78 Ka) [3] (72 Ka)
4. Explain the design goals and performance metrics for a computer system regarding its organization and architecture. [5] (76 Ash)

1.2 Structure and function

1. Define structure and function of a computer system. [4] (80 Ba)
   $|\rightarrow$Explain about the structural and functional viewpoint of a computer. [4] (**79 Bh**)
2. Explain the functional view and four types of operations used in computer. [6] (68 Ch)

1.3 Designing for performance

1. What are the driving factors behind the need to design for performance? [4] (71 Shr)
2. How can we maintain a performance balance between processor and memory? [2] (**72 Ch**)
   $|\rightarrow$What is performance balance and why it is required? [3] (70 Asa)

1.4 Interconnection structures

1. Explain the Interconnection structures of computer. [6] (82 Ba, 75 Ash)
   $|\rightarrow$Definition [2] (73 Shr)
   $|\rightarrow$Explain different types. [4] (73 Shr)
2. Explain the interconnection of CPU with Memory and I/O devices along with different operations over them. [3+3] (**70 Ch**)

1.5 Bus interconnection

1. What do you understand by Bus Interconnection. [2] (71 Shr)
2. What does the width of address bus represent in a system? [2] (**75 Ch,71 Ch**)
3. Explain different elements of bus design. [2] (**79 Bh**) [3] (70 Asa)
4. Discuss the limitations of using single bus system to connect different devices. [2] (**75 Ch,72 Ch**)
5. Compare and explain the bus structure of typical computer system. [4] (78 Ka)
6. Explain different types of bus arbitration and compare them. [6] (**78 Bh**)
7. Why is bus hierarchy required? [2] (**71 Ch**)
8. Discuss about the usage of a Multiple Hierarchical Bus Architecture over single bus system. [6] (**80 Bh**)

1.6 PCI

1. What is PCI? [1] (76 Ash)
   $|\rightarrow$Describe PCI bus configuration. [3] (81 Ba)

2 Central Processing Unit

(10 Hours/18 Marks)

2.1 CPU Structure and Function

1. Explain the component of CPU. [2] (**78 Ch**)

2. Draw the instruction cycle state diagram with example. [6] (**76 Ch**)
   |→Draw instruction cycle, state diagram with interrupt and explain it. [6] (**74 Ch**)
   |→Explain instruction cycle state diagram. [3] (81 Ba)
   |→Explain instruction cycle state diagram with interrupt handling. [2] (80 Ba) [3] (**81 Bh**)
   |→Explain the computer functions with different cycles. [3] (72 Ka)

3. Explain the general organization of register in CPU. [6] (**71 Ch**)

2.2 Arithmetic and Logic Unit

1. What are the stages of ALU design? [2] (70 Asa)

2. Design a 1-bit ALU which can perform addition, AND, OR, and X-OR operations. [4] (**80 Bh**)

3. Design a 2-bit ALU that can perform subtraction, AND, OR and XOR. [8] (**75 Ch**)
   |→2-bit ALU performing addition, subtraction, OR and XOR. [6] (70 Asa)

2.3 Instruction Formats

1. What do you mean by instruction format? [4] (**72 Ch**)

2. Explain the different types of instruction formats. [3] (**71 Ch**) [4] (**80 Bh**)

3. Explain Instruction Format with its types? [2] (71 Shr)

4. What are the most common fields in an instruction. [2] (**68 Ch**)

5. Explain the logical and bit manipulation instruction with example. [4] (82 Ba)

6. Write down the code to evaluate in three address, two address, one address and zero address instruction format.

    a. Y = (A-B/C)*[D+(E*G)] [8] (**81 Bh**,**76 Ch**)
    b. X = ((A+B)/C) + (D-E) [8] (**79 Bh**)
    c. Y = (A+B)/C + D/(E*F) [8] (**75 Ch**)
    d. X = (P+Q) x (R+S) [8] (**74 Ch**)
    e. X = (A-B*F)*C+D/E [8] (**72 Ch**)
    f. X = (A+B) x (C+D) [5] (**71 Ch**) [6] (**68 Ch**, 71 Shr)
    g. Y = A/B+(CxD) + F(H/G) [8] (**70 Ch**
    h. Y = A+(B*C)+D [8] (**68 Ba**)
    i. Y = AB + (F/G) + CD [8] (**67 Asa**)
    j. Y = ((A+B) * (C-D))/E [8] (82 Ba)
    k. N = ((P-QxR)/S)+(T/U)+VxW) [8] (81 Ba)
    l. $X = \dfrac{\text{A-B+Cx(DxE-F)}}{\text{G+HxK}}$ [8] (80 Ba)

m. Y = (A-B/C) x (D+ExG)/F   [8] (78 Ka)

n. Y = (W+X) * (Y-Z)   [8] (76 Ash)

o. (*In present sources, operation is not given. If found, please contact*)   [8] (75 Ash)

p. Y = A * (B+D/C)+(G*E)/F   [8] (73 Shr)

q. Y = (A+B)*(C+D)+G/E*F   [8] (72 Ka)

2.4 Data Transfer and Manipulation

1. Explain data transfer instruction with example.   [4] (**81 Bh**)

2. Explain different types of data manipulation instructions with example.   [8] (**78 Bh**)
   |→What are the three types of data manipulation instructions used in computer? Explain.
                                                                           [8] (**67 Asa**)

2.5 Addressing Modes

1. What is addressing mode?   [2] (**80 Bh**,**76 Ch**,**68 Ch**)

2. Differentiate between Immediate and direct addressing modes.   [4] (**81 Bh**)

3. Descsribe the displacement addressing mode with example.   [4] (82 Ba)

4. Write down the need for addressing modes.   [2] (**74 Ch**)

5. Comparision of different types of addressing modes.   [6] (**76 Ch**) [8] (76 Ash) [10] (72 Ka)
   |→with adv/disadv.   [10] (78 Ka)
   |→with algorithm as well as adv/disadv.   [8] (**68 Ba**)

6. Write down different types of addressing mode and:
   |→Explain with adv/disadv.   [8] (81 Ba, 80 Ba) [10] (**70 Ch**)
   |→Explain with suitable example.   [6] (**80 Bh, 79 Bh**,**74 Ch**) [8] (**68 Ch**, 70 Asa)

7. Following instructions are given: [10] (73 Shr)

   a. LDA 2000H
   b. MVI B, 32H
   c. STAX D
   d. MOV A, B

   Which addressing modes are used in the above instructions? Explain briefly about them.

8. Describe the operation of LD (load) instruction under various addressing modes with syntax.
                                                                          [4] (**71 Ch**)

2.6 RISC and CISC

1. Comparison between RISC and CISC architecture.   [4] (71 Shr) [6] (**78 Bh**,**72 Ch**, 75 Ash)

2.7 64 − Bit Processor

3 Control Unit

(6 Hours/10 Marks)

3.1 Control Memory

1. Explain the organization of a control memory. [4] (71 Shr)

2. Explain block diagram of micro-programmed control organization. [4] (76 Ash)

3.2 Addressing sequencing

1. What is address sequencing? [3] (**71 Ch**,**67 Asa**)

2. Explain address sequencing with the help of a block diagram. [5] (**80 Bh**, 72 Ka)
   |→Explain the selection of address for control memory with its block diagram.
   [7] (**72 Ch**,**71 Ch**,**68 Ch**)

3. How does a sequencing logic work in micro-programmed control unit to execute a micro-program?
   [6] (**70 Ch**)

4. Explain the address sequencing capabilities required in a control memory. [5] (**67 Asa**)

3.3 Computer configuration

3.4 Microinstruction Format

1. Explain the microinstruction format. [3] (**80 Bh**) [4] (81 Ba) [5] (72 Ka)
   |→with example. [5] (**81 Bh**) [6] (71 Shr)
   |→Explain various fields in micro-instruction format with neat and clean block diagram.
   [3] (**68 Ch**)

3.5 Symbolic Microinstructions

1. How address of micro instruction is generated by next address generator in control unit? Explain
   with suitable diagram. [8] (**76 Ch**)

3.6 Symbolic Microprogram

1. Write a microprogram for the fetch cycle and addition cycle. [5] (**81 Bh**)
2. Differentiate between symbolic and bianry micro instruction. [4] (81 Ba)
3. Explain the operation of microprogram sequencer used in microprogrammed control unit.
   [5] (**79 Bh**)
4. Explain with diagram the working of microprogram sequencer for control memory. [6] (78 Ka)
5. Write down the symbolic microprogram for fetch routine and addition execute routine.
   [4] (78 Ka)
6. Describe various fields in micro-instruction format with diagram showing different fields.
   [6] (76 Ash)
7. Write micro program for fetch cycle. [4] (73 Shr)

3.7   Control Unit Operation

1. What are the types of control signals?   [3] (**68 Ba**)
2. Explain the basic hardwired control unit components.   [4] (82 Ba)
3. Explain microprogrammed control unit with block diagram.   [5] (**79 Bh**, 80 Ba)
   |→(*diagram not asked explicitly, just operation*)   [7] (**68 Ba**)
4. Differentiate between hardwired and microprogrammed control unit.
                              [4] (**74 Ch**, 70 Asa) [5] (**75 Ch**,**70 Ch**, 80 Ba)
5. Explain the organization structure of a microprogram control unit and the generation of control signals using microprogram.   [10] (**78 Bh**)

3.8   Design of Control Unit

1. Explain the micro program sequencer used in microprogrammed control unit.   [6] (**74 Ch**)
   |→Draw & explain block diagram of micro-programmed sequencer for control memory.
                              [5] (**75 Ch**) [10] (75 Ash)
2. Explain microinstruction format used in microprogramming control unit.   [6] (73 Shr)
3. What factors cause micro-programmed control unit to be selected over hardwired control unit.
                              [3] (**72 Ch**)
4. Explain with steps involved when you are designing
   |→hardwired control unit.   [6] (82 Ba)
   |→micro-program control unit.   [6] (70 Asa)

4 Pipeline and Vector processing

(5 Hours/10 Marks)

4.1 Pipelining

1. What is Pipelining? [1] (**81 Bh**)
   $|\rightarrow$ Define pipeline. [1] (72 Ka)

2. Explain types of pipelining. [3] (72 Ka)

3. How can we prove that pipelining improves the performance of a computer? [4] (81 Ba)

4. Derive the expression showing speed up ratio equals number of segments in pipeline. [3] (**75 Ch**)

5. Discuss in detail about data dependency problem that arises in pipelining along with its solution. [5] (**75 Ch**)

4.2 Parallel Processing

1. Explain the Flynn's classification of computer system. [4] (**81 Bh**,**72 Ch**)

2. Discuss about parallel processing. [4] (71 Shr)

3. How parallel processing can be achieved in pipelining, explain it with time-space diagram for four segments pipeline having six tasks. [6] (71 Shr)

4.3 Arithmetic Pipeline

1. Explain the instruction pipeline with example. [4] (**79 Bh**) [5] (**71 Ch**,**70 Ch**)
   $|\rightarrow$ Explain in detail how the arithmetic pipeline increases the performance of a system.
   [7] (73 Shr)

2. Explain arithmetic pipeline for solving floating-point addition/subtraction. [5] (81 Ba)

4.4 Instruction Pipeline

1. Explain the instruction pipeline with example. [5] (**71 Ch**,**70 Ch**)

2. Describe four stage instruction pipeline. [4] (**81 Bh**) [5] (**76 Ch**, 78 Ka)
   $|\rightarrow$ Explain with example. [8] (70 Asa)
   $|\rightarrow$ Explain with diagram. [6] (82 Ba)

3. Explain six stage instruction pipeline with example. [10] (75 Ash)

4. How pipeline processing is done in an instruction pipeline? [3] (78 Ka)

5. Construct time-space diagram for four instructions with four-stage pipeline and show how pipelining reduces the execution time? [5] (81 Ba)
   $|\rightarrow$ Explain the operation of instruction pipeline for processing four segment instruction cycle with the help of space-time diagram. [6] (81 Ba)
   $|\rightarrow$ Draw a time-space diagram for four segments having six tasks. [6] (**76 Ch**)

6. Show that the speedup factor for a pipelined processor is equal to the number of stages in a pipeline. [4] (**80 Bh**)

7. Explain about the different types of conflicts that can be seen in a pipeline. [6] (**80 Bh**)
   |→Discuss pipeline conflicts with examples. [4] (82 Ba)

8. What is meant by hazard in pipelining? [2] (76 Ash) [4] (**78 Bh**)

9. Describe different types of pipeline hazards. [4] (76 Ash)
   |→with example. [6] (**79 Bh**, 72 Ka)

10. What is instruction hazard in pipeline? [2] (70 Asa)

11. Explain with example data and control hazards in pipeline conflict. [6] (**78 Bh**)

12. How can you overcome hazards? [2] (76 Ash)

13. Explain control pipeline hazard and its solutions. [6] (**72 Ch**)

4.5 RISC Pipeline

1. RISC has the ability to use efficient instruction pipeline. Justify. [3] (73 Shr)

4.6 Vector Processing

4.7 Array Processing

5 Computer Arithmetic

(8 Hours/14 Marks)

5.1 Addition Algorithm

1. Explain the floating-point addition and subtraction process
   |→with example. [3+3] (**81 Bh, 79 Bh, 78 Bh**) [7] (73 Shr)
   |→with flowchart and example. [6] (78 Ka) [10] (**74 Ch**)
2. Draw a flowchart of floating point subtraction. [4] (70 Asa)

5.2 Subtraction Algorithm

5.3 Multiplication Algorithm

1. Draw a flowchart for Booth's multiplication algorithm for signed multiplication.
   [4] (78 Ka) [5] (**81 Bh**)
2. Explain booth's algorithm. [3] (**70 Ch**) [4] (**80 Bh**,**68 Ch**,**67 Asa**, 72 Ka) [5] (**76 Ch**)
   |→with example and give hardware requirement diagram. [10] (75 Ash)
   |→Explain with hardware algorithm with diagram. [5] (**72 Ch**)
   |→Write the algorithm. [5] (76 Ash, 71 Shr)
3. Design a booth multiplication algorithm hardware. [4] (**71 Ch**)
4. Explain floating point multiplication process with example. [3] (82 Ba)
5. Multiply using Booth's multiplication algorithm.
   |→-6 x 7 [5] (**81 Bh**, 80 Ba)
   |→-7 x 3 [6] (**74 Ch**)
   |→-6 x 12 [6] (72 Ka)
   |→10 x (-7) [6] (81 Ba)
   |→10 x (-5) [5] (**76 Ch**)
   |→5 x -6 [4] (**72 Ch**)
   |→(9) x (-3) [5] (71 Shr)
   |→23 x -21 [4] (**68 Ch**)
   |→9 x 4 [6] (**80 Bh**)
   |→8 x 4 [5] (76 Ash)
   |→8 x 9 [3] (**70 Ch**)
   |→6 x 7 [4] (**67 Asa**)
   |→-7 x -10 [4] (78 Ka)
   |→-6 x -11 [6] (**75 Ch**)
   |→-5 x -9 [5] (**72 Ch**)

5.4 Division Algorithm

1. How division operation can be performed? Explain with its hardware implementation.
   [10] (70 Asa)
2. Draw the flowchart for Restoring Division. [4] (81 Ba, 72 Ka)
3. Draw the flowchart for Non-restoring Division. [4] (**79 Bh**)
   |→Explain signed binary division algorithm. [4] (73 Shr)
4. Explain non-restoring division algorithm. [3] (**75 Ch**) [5] (**78 Bh**)
   |→with flowchart. [5] (82 Ba, 80 Ba)

$|\rightarrow$ with flowchart and example. [8] (**70 Ch**)

5. Draw the flowchart for division of floating point numbers. [4] (**72 Ch**,**71 Ch**)

6. Explain floating point division algorithm. [6] (**68 Ch**)

  $|\rightarrow$ with example. [3] (82 Ba)

7. Compare restoring division algorithm with non restoring algorithm. [4] (71 Shr) [6] (**80 Bh**, 76 Ash, 75 Ash)

  $|\rightarrow$ with example. [6] (**76 Ch**) [8] (**68 Ba**)

8. Divide using restoring division.

  $|\rightarrow \dfrac{11}{5}$ [6] (81 Ba)

  $|\rightarrow 13/5$ [6] (**79 Bh**)

  $|\rightarrow 10/3$ [7] (**75 Ch**)

9. Divide using non-restoring algorithm.

  $|\rightarrow 12/5$ [5] (82 Ba, 80 Ba)

  $|\rightarrow 10/5$ [5] (**78 Bh**)

  $|\rightarrow 15/4$ [4] (73 Shr)

5.5   Logical Operation

6 Memory System

(5 Hours/8 Marks)

6.1 Microcomputer Memory

6.2 Characteristics of memory systems

1. Explain in briefly the characteristics of a memory system. [3] (81 Ba)
   |→Write characteristics of memory system. [3] (**73 Ch**) [4] (**75 Ch**, 75 Ash) [8] (**68 Ba**)

6.3 The Memory Hierarchy

1. What is memory hierarchy and why it is formed in computer system? [2] (71 Shr)
   |→Why memory hierarchy is required in computer system? [3] (82 Ba)

2. Draw the memory hierarchy. [2] (**72 Ch**, 72 Ka)

6.4 Internal and External memory

6.5 Cache memory principles

1. Describe the cache memory principles. [3] (**81 Bh**)

2. Describe cache operation briefly. [2] (76 Ash)

3. Describe cache organization. [4] (**71 Ch**)

6.6 Elements of Cache design

1. Explain the various types of elements of cache design. [4] (75 Ash)

6.6.1 Cache size

6.6.2 Mapping function

1. Define cache mapping techniques. [2] (**76 Ch**,**68 Ba**)

2. Why cache management is necessary in mapping process? [2] (**67 Asa**)

3. Explain various mapping methods used in cashe memory organization and compare each of them with example. [6] (**71 Ch**) [10] (78 Ka)
   |→only explain. [6] (75 Ash)

4. Differentiate between direct mapping and set associative mapping. [5] (**81 Bh**) [7] (81 Ba)

5. Differentiate between direct and associative mapping address structure. [6] (**67 Asa**)

6. Differentiate between associative and set associative mapping with example. [5] (**70 Ch**)

7. What are the major differences between different cache mapping techniques? [2] (70 Asa)
   |→DIfferentiate among direct, associative and set associative mapping. [8] (**68 Ba**)

8. Explain direct cache mapping technique with example. [7] (**80 Bh**)
   |→ with diagram. [4] (**76 Ch**)
   |→ with organization diagram and example. [6] (71 Shr)
   |→ with merits and demerits. [6] (**72 Ch**)

9. Suppose main memory has 64 blocks and cache memory has 8 blocks when 10 blocks of main memory are used, show how mapping is performed in direct mapping technique. [6] (**75 Ch**)
   |→ main memory is 32 blocks, rest is same. [6] (70 Asa)
   |→ main memory is 32 blocks, cache has 8 blocks when 12 blocks are used. [6] (**74 Ch**)

10. What is set associative mapping? [2] (81 Ba) [3] (**79 Bh**)

11. Explain how set associative mapping technique combines the feature of direct and associative mapping technique. [3] (81 Ba) [5] (73 Shr)

12. Explain about associative mapping technique. [6] (76 Ash)
    |→ with example. [6] (72 Ka)

6.6.3 Replacement algorithm

1. Explain different replacement algorithm technique used in cache memory. [3] (81 Ba) [5] (**79 Bh**)

2. Explain LRU replacement algorithm in case of hit and miss with suitable example. [8] (**78 Bh**)
   |→ Explain th LRU replacement algorithm with example. [5] (82 Ba)

3. Why replacement algorithm is necessary in associative mapping? [4] (**76 Ch**)
   |→ Why replacement algorithm is used when designing cache? Explain with example.
   [8] (**67 Asa**)

6.6.4 Write policy

1. Explain different write policy techniques in cache memory. [3] (**80 Bh**, 73 Shr)

6.6.5 Number of caches

7 Input-Output organization

(6 Hours/10 Marks)

7.1 Peripheral devices

7.2 I/O modules

1. What are the functions of IO Modules? [3] (71 Shr)

7.3 Input-Output interface

1. Elaborate the roles of IO interface in a computer system. [4] (**79 Bh**,**71 Ch**)

2. Explain three reasons behind the requirement of IO interfaces. [3] (**75 Ch**)

3. Explain IO interface. [2] (**74 Ch**)
   |→with example. [6] (**68 Ba**)

4. What are the four types of IO commands that an interface receive during the communication link between the processor and peripherals? [4] (**67 Asa**)

5. Explain the IO bus and interface modules. [4] (**67 Asa**)

7.4 Modes of transfer

1. Explain three IO techniques for input of a block of data. [6] (**80 Bh**)

2. Differentiate between isolated and memory mapped IO. [4] (**78 Bh**,**72 Ch**)

3. Why memory address spaces are reduced memory mapped IO? [2] (**75 Ch**)

7.4.1 Programmed I/O

1. Explain how data transfer is performed with programmed IO technique with necessary diagram. [6] (**79 Bh**)

7.4.2 Interrupt-driven I/O

1. Differentiate between programmed I/O and iterrupt driven I/O. [5] (**81 Bh**)

2. How does a computer know which device issued the interrupt; if multiple devices, how does the selection take place? [5] (73 Shr)

3. What are the different types of priority interrupt? [4] (72 Ka)

4. What is the purpose of priority interrupt; explain priority interrupt types with key characteristics. [7] (71 Shr)

7.4.3 Direct Memory access

1. With the help of a neat diagram, explain how DMA technique is used to transfer data in a computer system. [6] (**78 Bh**) [7] (81 Ba)
   |→Explain DMA controller with suitable block diagram.
   [5] (**75 Ch**, 81 Ba) [6] (**72 Ch**, 78 Ka) [8] (76 Ash)

2. How does DMA have request over the CPU when both request a memory transfer? [2] (76 Ash)

3. How DMA technique is different from programmed IO? [4] (78 Ka)

4. Compare among program IO, interrupt drive IO and DMA.
   [8] (**76 Ch,74 Ch,68 Ba**) [10] (70 Asa)

5. Mention three possible configurations of DMA and compare them. [8] (**67 Asa**)

6. Describe the drawbacks of programmed IO and interrupt driven IO and explain how DMA overcomes their drawbacks. [6] (**71 Ch**)
   |→How does DMA overcome the problems of programmed IO and interrupt driven IO techniques?
   [5] (**70 Ch**)

7.5 I/O Processors

1. Explain the CPU and IOP communication channel using diagram. [5] (**81 Bh**)

2. Compare and contrast between DMA and I/O processor. [5] (82 Ba)

3. Why IOP is used in IO organization? [3] (81 Ba, 75 Ash) [5] (**70 Ch**, 73 Shr)

4. Show the role of IO processor to assist the operation of the CPU. [4] (**80 Bh**)

5. Explain CPU-IOP Communication with diagram. [5] (82 Ba, 81 Ba) [6] (72 Ka) [7] (75 Ash)

7.6 Data Communication Processor

1. Why data communication processor is required in IO ogranization? [2] (**76 Ch**)

8 Multiprocessors

<div align="center">(2 Hours/4 Marks)</div>

8.1 Characteristics of multiprocessors

1. List out the characteristics of a multiprocessor. [4] (**80 Bh**,**70 Ch**)

2. Describe how the multiprocessor systems increase the performance level and reliability.
[4] (73 Shr)

3. Explain about multiprocessor and multiprocessing in brief. [4] (72 Ka)

4. How can multiprocessor be classified according to their memory organization? Explain.
[4] (**71 Ch**)

8.2 Interconnection Structures

1. Discuss about loosely-coupled and tightly-coupled architecture. [4] (81 Ba)
   |→Difference between them. [4] (78 Ka)

2. Discuss about tightly-coupled multiprocessor with block diagram. [4] (76 Ash)

3. Explain the crossbar switch interconnection structure with block diagram. [4] (81 Ba)

4. Differentiate Crossbar switch and Multistage switching network. [4] (71 Shr)
   |→Briefly discuss 8x8 omega switching networking with example. [4] (82 Ba)
   |→Explain hypercube interconnection network with example. [4] (**76 Ch**)

5. Compare and contrast the interconnection structures used in multiprocessing environment.
[4] (**79 Bh, 78 Bh**)

8.3 Interprocessor Communication and Synchronization

1. Briefly discuss on inter-process communication and synchronization. [5] (**81 Bh**)

2. Explain inter-process synchronization with example. [4] (**74 Ch**, 70 Asa)
   |→with suitable mechanism. [4] (**72 Ch**)

3. Explain various configurations of OS in multiprocessor system. [4] (**74 Ch**)