

# Computer Organization and Architecture

Me lol

June 11, 2025

# Contents

<b>1</b>	<b>Introduction</b>	<b>4</b>
1.1	Computer organization and architecture . . . . .	4
1.2	Structure and function . . . . .	4
1.3	Designing for performance . . . . .	4
1.4	Interconnection structures . . . . .	4
1.5	Bus interconnection . . . . .	4
1.6	PCI . . . . .	4
<b>2</b>	<b>Central Processing Unit</b>	<b>5</b>
2.1	CPU Structure and Function . . . . .	5
2.2	Arithmetic and Logic Unit . . . . .	5
2.3	Instruction Formats . . . . .	5
2.4	Data Transfer and Manipulation . . . . .	6
2.5	Addressing Modes . . . . .	6
2.6	RISC and CISC . . . . .	6
2.7	64 – Bit Processor . . . . .	6
<b>3</b>	<b>Control Unit</b>	<b>7</b>
3.1	Control Memory . . . . .	7
3.2	Addressing sequencing . . . . .	7
3.3	Computer configuration . . . . .	7
3.4	Microinstruction Format . . . . .	7
3.5	Symbolic Microinstructions . . . . .	7
3.6	Symbolic Microprogram . . . . .	7
3.7	Control Unit Operation . . . . .	7
3.8	Design of Control Unit . . . . .	7
<b>4</b>	<b>Pipeline and Vector processing</b>	<b>8</b>
4.1	Pipelining . . . . .	8
4.2	Parallel Processing . . . . .	8
4.3	Arithmetic Pipeline . . . . .	8
4.4	Instruction Pipeline . . . . .	8
4.5	RISC Pipeline . . . . .	8
4.6	Vector Processing . . . . .	8
4.7	Array Processing . . . . .	8
<b>5</b>	<b>Computer Arithmetic</b>	<b>9</b>
5.1	Addition Algorithm . . . . .	9
5.2	Subtraction Algorithm . . . . .	9
5.3	Multiplication Algorithm . . . . .	9
5.4	Division Algorithm . . . . .	9
5.5	Logical Operation . . . . .	9
<b>6</b>	<b>Memory System</b>	<b>10</b>
6.1	Microcomputer Memory . . . . .	10
6.2	Characteristics of memory systems . . . . .	10
6.3	The Memory Hierarchy . . . . .	10
6.4	Internal and External memory . . . . .	10

6.5	Cache memory principles . . . . .	10
6.6	Elements of Cache design . . . . .	10
6.6.1	Cache size . . . . .	10
6.6.2	Mapping function . . . . .	10
6.6.3	Replacement algorithm . . . . .	10
6.6.4	Write policy . . . . .	10
6.6.5	Number of caches . . . . .	10
<b>7</b>	<b>Input-Output organization</b>	<b>11</b>
7.1	Peripheral devices . . . . .	11
7.2	I/O modules . . . . .	11
7.3	Input-Output interface . . . . .	11
7.4	Modes of transfer . . . . .	11
7.4.1	Programmed I/O . . . . .	11
7.4.2	Interrupt-driven I/O . . . . .	11
7.4.3	Direct Memory access . . . . .	11
7.5	I/O Processors . . . . .	11
7.6	Data Communication Processor . . . . .	11
<b>8</b>	<b>Multiprocessors</b>	<b>12</b>
8.1	Characteristics of multiprocessors . . . . .	12
8.2	Interconnection Structures . . . . .	12
8.3	Interprocessor Communication and Synchronization . . . . .	12

# 1 Introduction

(3 Hours/6 Marks)

## 1.1 Computer organization and architecture

1. Define computer architecture. [2] (**75 Ch**) [1.5] (81 Bh) [1] (**72 Ch**)
2. Define computer organization. [1.5] (**81 Bh**) [1] (**72 Ch**)
3. Differentiate between computer organization and architecture. [2] (**71 Ch**, 78 Ka) [3] (72 Ka)
4. Explain the design goals and performance metrics for a computer system regarding its organization and architecture. [5] (76 Ash)

## 1.2 Structure and function

1. Define structure and function of a computer system. [4] (80 Ba)  
|→ Explain about the structural and functional viewpoint of a computer. [4] (**79 Bh**)
2. Explain the functional view and four types of operations used in computer. [6] (68 Ch)

## 1.3 Designing for performance

1. What are the driving factors behind the need to design for performance? [4] (71 Shr)
2. How can we maintain a performance balance between processor and memory? [2] (**72 Ch**)  
|→ What is performance balance and why it is required? [3] (70 Asa)

## 1.4 Interconnection structures

1. Explain the Interconnection structures of computer. [6] (75 Ash)  
|→ Definition [2] (73 Shr)  
|→ Explain different types. [4] (73 Shr)
2. Explain the interconnection of CPU with Memory and I/O devices along with different operations over them. [3+3] (**70 Ch**)

## 1.5 Bus interconnection

1. What do you understand by Bus Interconnection. [2] (71 Shr)
2. What does the width of address bus represent in a system? [2] (**75 Ch**, **71 Ch**)
3. Explain different elements of bus design. [2] (**79 Bh**) [3] (70 Asa)
4. Discuss the limitations of using single bus system to connect different devices. [2] (**75 Ch**, **72 Ch**)
5. Compare and explain the bus structure of typical computer system. [4] (78 Ka)
6. Explain different types of bus arbitration and compare them. [6] (**78 Bh**)
7. Why is bus hierarchy required? [2] (**71 Ch**)
8. Discuss about the usage of a Multiple Hierarchical Bus Architecture over single bus system. [6] (**80 Bh**)

## 1.6 PCI

1. What is PCI? [1] (76 Ash)  
|→ Describe PCI bus configuration. [3] (81 Ba)

## 2 Central Processing Unit

(10 Hours/18 Marks)

### 2.1 CPU Structure and Function

1. Explain the component of CPU. [2] **(78 Ch)**
2. Draw the instruction cycle state diagram with example. [6] **(76 Ch)**  
|→ Draw instruction cycle, state diagram with interrupt and explain it. [6] **(74 Ch)**  
|→ Explain instruction cycle state diagram. [3] (81 Ba)  
|→ Explain instruction cycle state diagram with interrupt handling. [2] (80 Ba) [3] **(81 Bh)**  
|→ Explain the computer functions with different cycles. [3] (72 Ka)
3. Explain the general organization of register in CPU. [6] **(71 Ch)**

### 2.2 Arithmetic and Logic Unit

1. Design a 1-bit ALU which can perform addition, AND, OR, and X-OR operations. Explain the different types of instruction formats. [4+4] **(80 Bh)**
2. Design a 2-bit ALU that can perform subtraction, AND, OR and XOR. [8] **(75 Ch)**
3. What are the stages of ALU design? Explain with the example of 2-bit ALU performing addition, subtraction, OR and XOR. [8] (70 Asa)

### 2.3 Instruction Formats

1. What do you mean by instruction format? [4] **(72 Ch)**
2. What are the different types of instructions? [3] **(71 Ch)**
3. Explain Instruction Format with its types? [2] (71 Shr)
4. What are the most common fields in an instruction. [2] **(68 Ch)**
5. Write down the code to evaluate in three address, two address, one address and zero address instruction format.
  - a.  $Y = (A-B/C) * [D + (E * G)]$  [8] **(81 Bh, 76 Ch)**
  - b.  $N = ((P-Q \times R)/S) + (T/U) + V \times W$  [8] (81 Ba)
  - c.  $X = \frac{A-B+C \times (D \times E-F)}{G+H \times K}$  [8] (80 Ba)
  - d.  $X = ((A+B)/C) + (D-E)$  [8] **(79 Bh)**
  - e.  $Y = (A-B/C) \times (D+E \times G)/F$  [8] (78 Ka)
  - f.  $Y = (W+X) * (Y-Z)$  [8] (76 Ash)
  - g.  $Y = (A+B)/C + D/(E * F)$  [8] **(75 Ch)**
  - h. *(In present sources, operation is not given. If found, please contact)* [8] (75 Ash)
  - i.  $X = (P+Q) \times (R+S)$  [8] **(74 Ch)**
  - j.  $Y = A * (B+D/C) + (G * E)/F$  [8] (73 Shr)
  - k.  $X = (A-B * F) * C + D/E$  [8] **(72 Ch)**
  - l.  $Y = (A+B) * (C+D) + G/E * F$  [8] (72 Ka)
  - m.  $X = (A+B) \times (C+D)$  [5] **(71 Ch)** [6] **(68 Ch, 71 Shr)**
  - n.  $Y = A/B + (C \times D) + F(H/G)$  [8] **(70 Ch)**
  - o.  $Y = A + (B * C) + D$  [8] **(68 Ba)**
  - p.  $Y = AB + (F/G) + CD$  [8] **(67 Asa)**

## 2.4 Data Transfer and Manipulation

1. Explain data transfer instruction with example. [4] (**81 Bh**)
2. Explain different types of data manipulation instructions with example. [8] (**78 Bh**)  
|→ What are the three types of data manipulation instructions used in computer? Explain. [8] (**67 Asa**)

## 2.5 Addressing Modes

1. What is addressing mode? [2] (**80 Bh,76 Ch,68 Ch**)
2. Differentiate between Immediate and direct addressing modes. [4] (**81 Bh**)
3. Write down the need for addressing modes. [2] (**74 Ch**)
4. Comparison of different types of addressing modes. [6] (**76 Ch**) [8] (76 Ash) [10] (72 Ka)  
|→ with adv/disadv. [10] (78 Ka)  
|→ with algorithm as well as adv/disadv. [8] (**68 Ba**)
5. Write down different types of addressing mode and:  
|→ Explain with adv/disadv. [8] (81 Ba, 80 Ba) [10] (**70 Ch**)  
|→ Explain with suitable example. [6] (**80 Bh, 79 Bh,74 Ch**) [8] (**68 Ch**, 70 Asa)  
[10] (73 Shr)
6. Following instructions are give:  
a. LDA 2000H  
b. MVI B, 32H  
c. STAX D  
d. MOV A, B  
Which addressing modes are used in the above instructions? Explain briefly about them.
7. Describe the operation of LD (load) instruction under various addressing modes with syntax. [4] (**71 Ch**)

## 2.6 RISC and CISC

1. Comparison between RISC and CISC architecture. [6] (**78 Bh,72 Ch**, 75 Ash)

## 2.7 64 – Bit Processor

## **3 Control Unit**

(6 Hours/10 Marks)

- 3.1 Control Memory**
- 3.2 Addressing sequencing**
- 3.3 Computer configuration**
- 3.4 Microinstruction Format**
- 3.5 Symbolic Microinstructions**
- 3.6 Symbolic Microprogram**
- 3.7 Control Unit Operation**
- 3.8 Design of Control Unit**

## 4 Pipeline and Vector processing

(5 Hours/10 Marks)

- 4.1 Pipelining
- 4.2 Parallel Processing
- 4.3 Arithmetic Pipeline
- 4.4 Instruction Pipeline
- 4.5 RISC Pipeline
- 4.6 Vector Processing
- 4.7 Array Processing



## 5 Computer Arithmetic

(8 Hours/14 Marks)

### 5.1 Addition Algorithm

1. Explain the floating-point addition and subtraction process  
|→ with example. [3+3] (**81 Bh, 79 Bh, 78 Bh**) [7] (73 Shr)  
|→ with flowchart and example. [6] (78 Ka) [10] (**74 Ch**)

### 5.2 Subtraction Algorithm

### 5.3 Multiplication Algorithm

1. Draw a flowchart for Booth's multiplication algorithm for signed multiplication. [4] (78 Ka) [5] (**81 Bh**)
2. Explain booth's algorithm. [4] (**80 Bh**) [5] (**76 Ch**)  
|→ with example and give hardware requirement diagram. [10] (75 Ash)  
|→ Write the algorithm. [5] (76 Ash)
3. Multiply using Booth's multiplication algorithm.  
|→ -6 x 7 [5] (**81 Bh, 80 Ba**)  
|→ -7 x 3 [6] (**74 Ch**)  
|→ 10 x (-7) [6] (81 Ba)  
|→ 10 x (-5) [5] (**76 Ch**)  
|→ 9 x 4 [6] (**80 Bh**)  
|→ 8 x 4 [5] (76 Ash)  
|→ -7 x -10 [4] (78 Ka)  
|→ -6 x -11 [6] (**75 Ch**)

### 5.4 Division Algorithm

1. Draw the flowchart for Restoring Division. [4] (81 Ba)
2. Draw the flowchart for Non-restoring Division. [4] (**79 Bh**)  
|→ Explain signed binary division algorithm. [4] (73 Shr)
3. Explain non-restoring division algorithm. [3] (**75 Ch**) [5] (**78 Bh**)  
|→ with flowchart. [5] (80 Ba)
4. Compare restoring division algorithm with non restoring algorithm. [6] (**80 Bh, 76 Ash, 75 Ash**)  
|→ with example. [6] (**76 Ch**)
5. Divide using restoring division.  
|→  $\frac{11}{5}$  [6] (81 Ba)  
|→ 13/5 [6] (**79 Bh**)  
|→ 10/3 [7] (**75 Ch**)
6. Divide using non-restoring algorithm.  
|→ 12/5 [5] (80 Ba)  
|→ 10/5 [5] (**78 Bh**)  
|→ 15/4 [4] (73 Shr)

### 5.5 Logical Operation

## 6 Memory System

(5 Hours/8 Marks)

- 6.1 Microcomputer Memory
- 6.2 Characteristics of memory systems
- 6.3 The Memory Hierarchy
- 6.4 Internal and External memory
- 6.5 Cache memory principles
- 6.6 Elements of Cache design
  - 6.6.1 Cache size
  - 6.6.2 Mapping function
  - 6.6.3 Replacement algorithm
  - 6.6.4 Write policy
  - 6.6.5 Number of caches

## **7 Input-Output organization**

(6 Hours/10 Marks)

**7.1 Peripheral devices**

**7.2 I/O modules**

**7.3 Input-Output interface**

**7.4 Modes of transfer**

**7.4.1 Programmed I/O**

**7.4.2 Interrupt-driven I/O**

**7.4.3 Direct Memory access**

**7.5 I/O Processors**

**7.6 Data Communication Processor**

## **8 Multiprocessors**

(2 Hours/4 Marks)

**8.1 Characteristics of multiprocessors**

**8.2 Interconnection Structures**

**8.3 Interprocessor Communication and Synchronization**