PWM电机调速控制

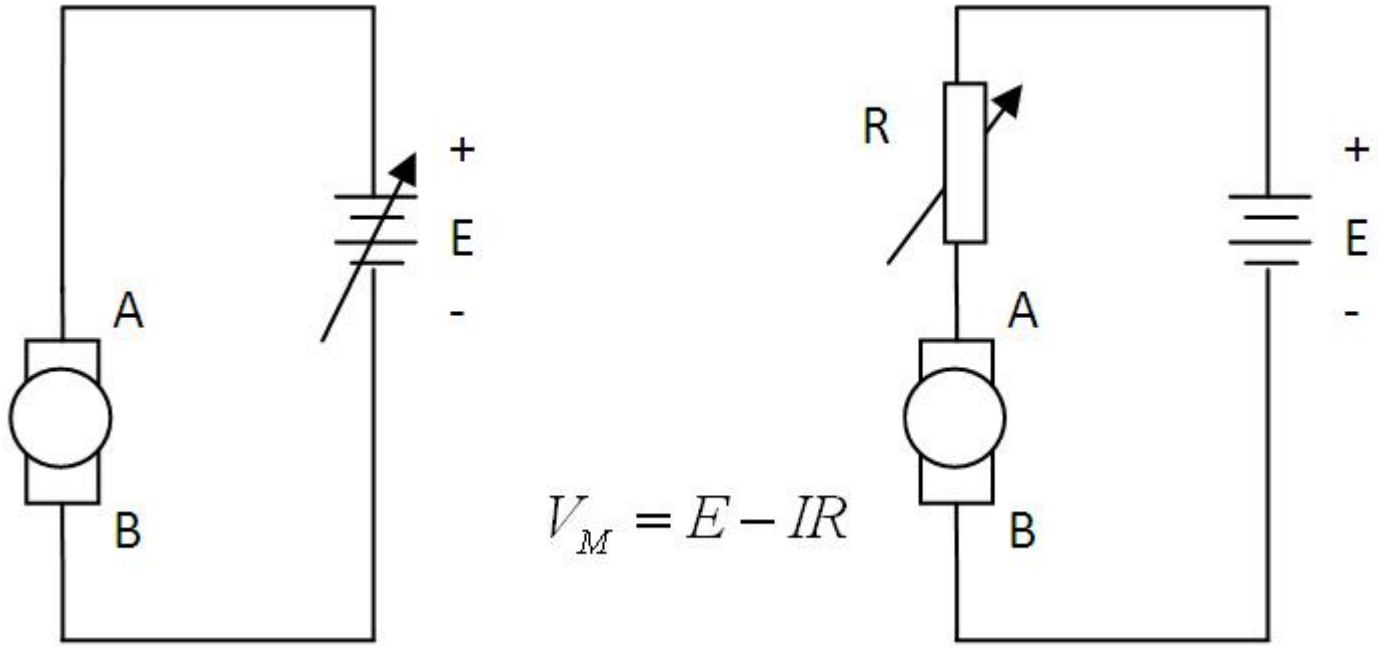
主讲　祁才君

电工电子基础教学中心

智能小车速度控制

- 何时需要控制小车速度
- 小车速度控制的常用方法
- 调速过程的控制策略

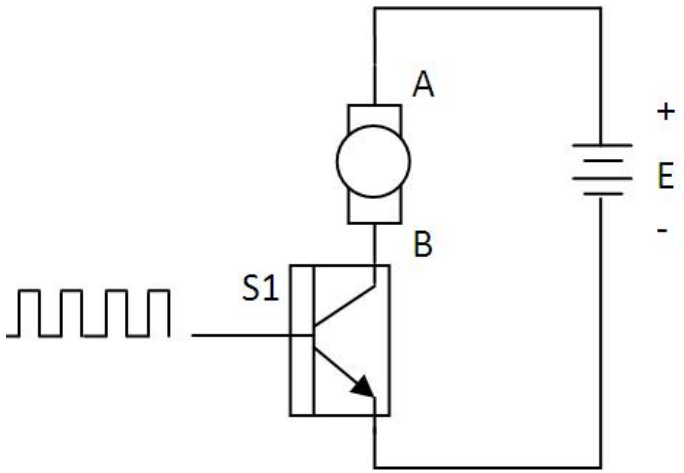
■直接调压调速法原理

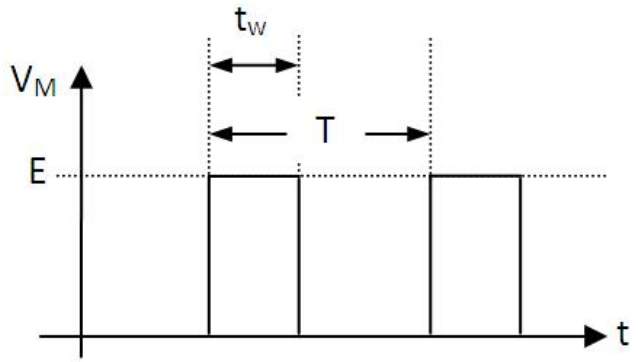


$$V_M = E - IR$$

- 电机两端电压低时，扭矩小，可能无法启动
- 调压电阻产生能耗，产生高热

■PWM调压调速法原理





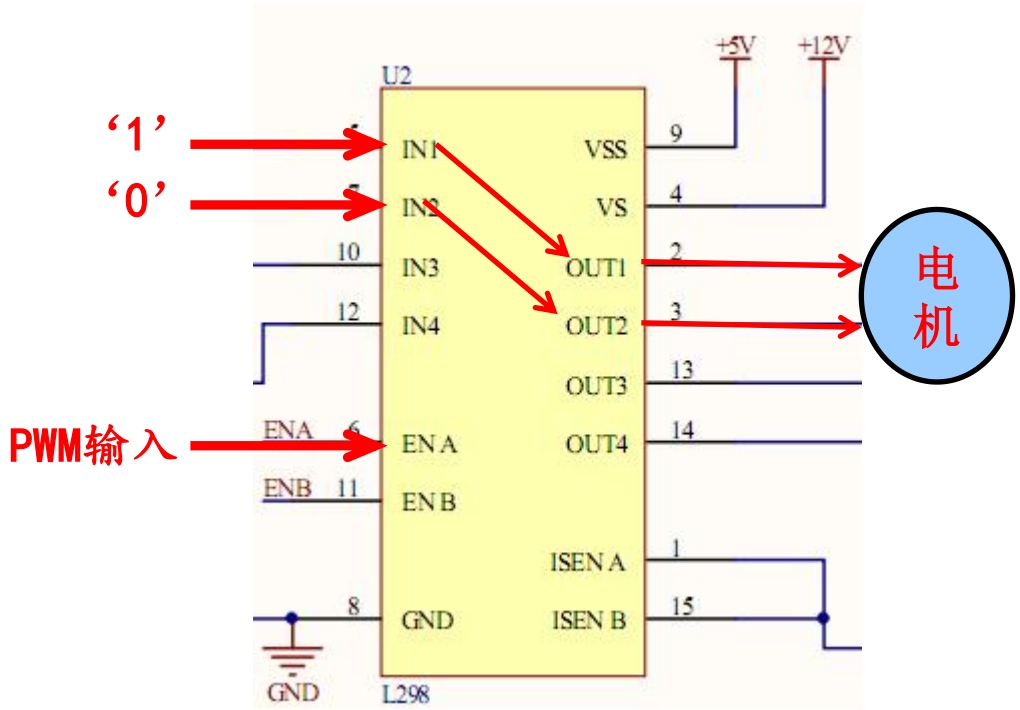
$$\bar{V}_M = \frac{tw}{T} \cdot E = \delta \cdot E$$

$$\delta \triangleq \frac{tw}{T}, \delta \in [0,1], \bar{V}_M = \delta \cdot E$$

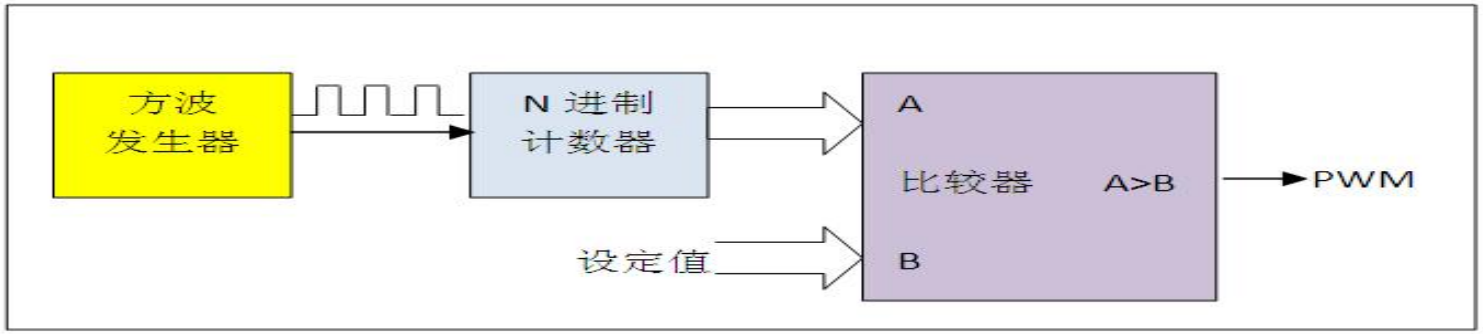
- 利用间歇导通和电机运动惯性调速
- 电机两端电压始终等于E，扭矩大
- S1导通时，V_{CE}=0，控制功耗小

■PWM调压调速法原理

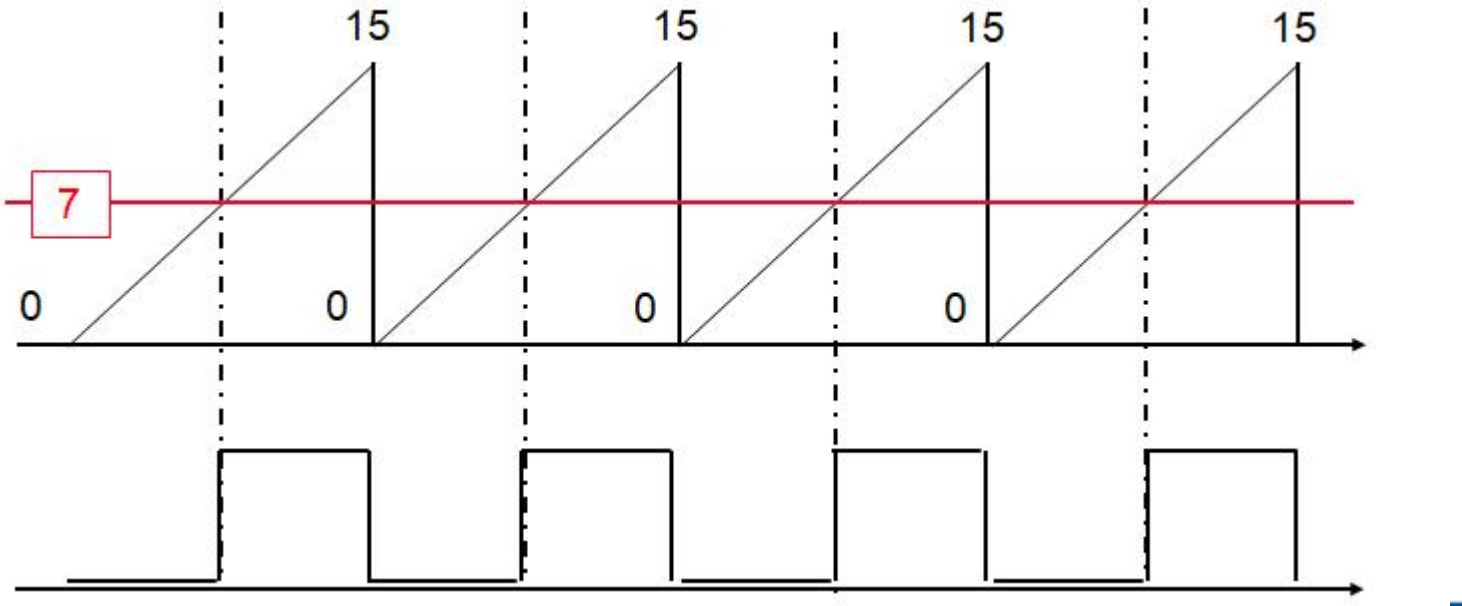
- H桥的PWM调速示意图



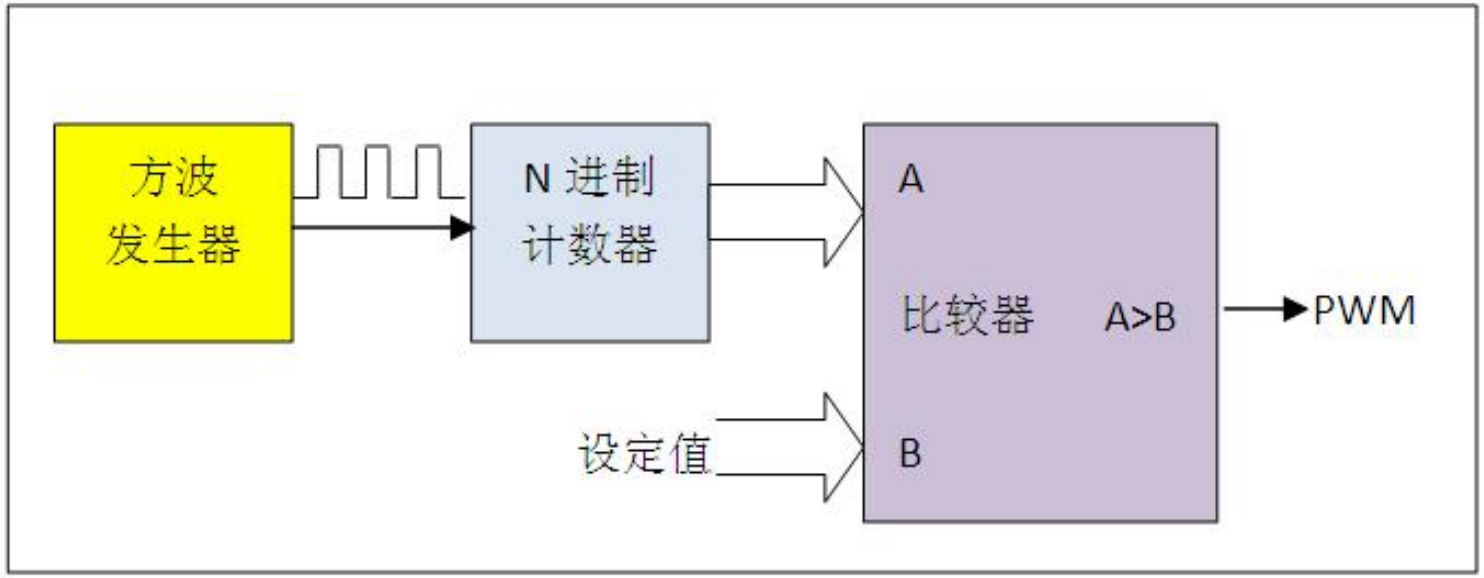
■数字式PWM电路



- 计数器输出产生锯齿波
- 比较器输出产生PWM波



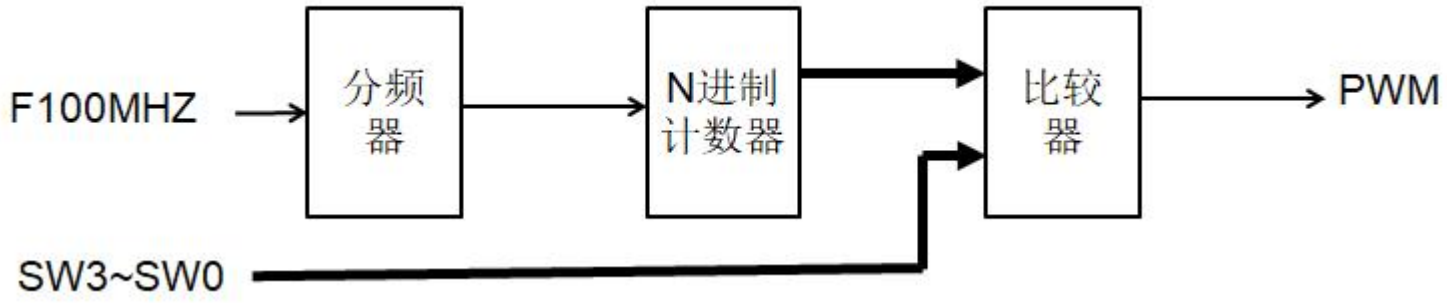
■数字式PWM电路的参数



- 若方波发生器的频率是f
- PWM波的频率等于f/N
- PWM波的占空比由比较设定值定，共N档

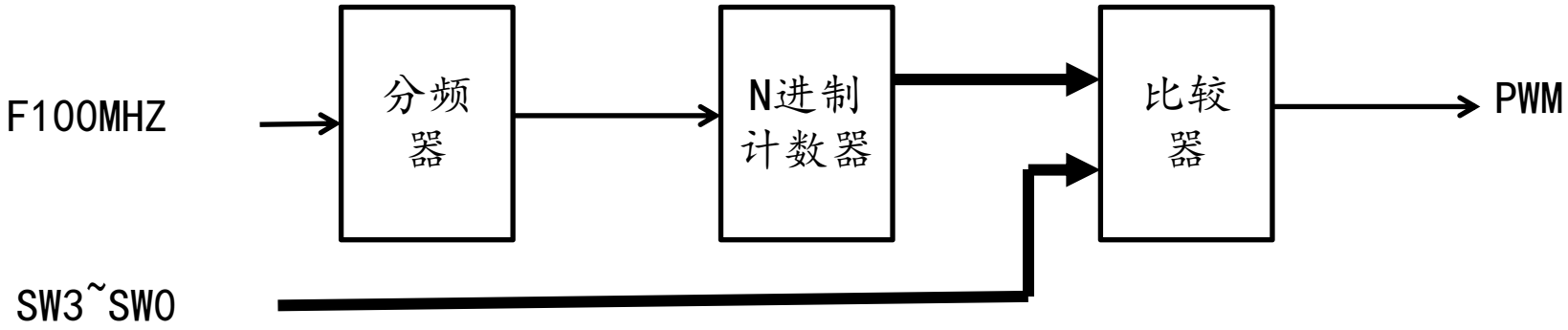
$$\delta = 0, \frac{1}{N} * 100\%, \frac{2}{N} * 100\% .....$$

■FPGA设计PWM的设计框图



- **分频器**：将系统50MHZ转换对应PWM要求的频率
- **N进制计数器**：产生锯齿波（建议16档既可，16进制计数器）
- **比较器**（若计数器是16进制，输出是4位二进制，比较器 2个4位二进制比较）

■PWM发生器需编写的VHDL源码



- 分频器VHDL源码
- N进制计数器源码
- 比较器源码
- 顶层源码

◆分频器参考源码

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity DIVX is
    port (
           Freq_in,Clr_n : in  std_logic;
           Div_num:in natural range 0 to 49999999;
           Freq_out: out  std_logic);
end DIVX ;

architecture BEHAV of DIVX  is

begin
process(Freq_in,Clr_n)
variable cnt_val :natural range 0 to 49999999;
begin
 if(Clr_n='0') then
    cnt_val:=0;
 elsif(Freq_in'event and Freq_in='1') then
  if(cnt_val=Div_num) then
   cnt_val:=0;
  elsif(cnt_val<Div_num/2) then
   cnt_val:=cnt_val+1;
   Freq_out<='0';
  else
   cnt_val:=cnt_val+1;
   Freq_out<='1';
  end if;
 end if;

end process;

end BEHAV;
```

◆16进制计数器参考源码

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity CNT16 is
    port (
           Clk,Clr_n : in  std_logic;
           Q: out  std_logic_vector(3 downto 0));
end CNT16 ;

architecture BEHAV of CNT16  is
signal Q_tmp: std_logic_vector(3 downto 0);
begin

process(Clk,Clr_n)

begin
 if(Clr_n='0') then
    Q_tmp<="0000";
 elsif(Clk'event and Clk='1') then
   Q_tmp<=Q_tmp+1;
 end if;

end process;

 Q<=Q_tmp;

end BEHAV;
```

◆二个四位二进制比较器参考源码

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity COMP4BIT is
    port (
            A,B: in  std_logic_vector(3 downto 0);
            AGB:out  std_logic);
end COMP4BIT ;

architecture BEHAV of COMP4BIT  is

begin

  process(A,B)
   begin
   if(A>B) then
      AGB<='1';
   else
      AGB<='0';
   end if;

  end process;

end BEHAV;
```

实验内容

（1）应用MODESIM软件设计、仿真PWM电路

①编写数字PWM产生电路的所有VHDL设计源码，并编译通过

②编写数字PWM电路中比较器的VHDL仿真源码，并给出仿真波形

③编写数字PWM电路中16进制计数器的VHDL仿真源码，并给出仿真波形

（2）基于FPGA开发板用QUARTUS软件综合、布线并产生并生成下载文件

（3）下载数字PWM产生电路，通过按键设定2种占空比，用示波器观察并记录PWM的输出波形，测量其周期、幅度和占空比。

（4）将PWM输出与电机驱动模块的总控输入ENA连接，IN1=1，IN2=0，观察不同占空比时电机的运动速度

□探究题

- PWM控制的优点主要是什么？在哪些应用中还有广泛应用？