[Please refer to appendix for how the problems were solved/my work for solutions.](#_Appendix)

1. Direct Mapping

  1) Divide the bits into tag, block and offset bits.

Offset: 5

Row: 6

Tag: 10

 2) What is the tag, line and offset for the address $123A63, in hexadecimal?

              tag:       0x247

              line:      0x13

              offset:   0x03

2. Fully Associative Mapping

  1) Divide the bits into tag and offset bits.

Offset: 5

Tag: 16

  2) What is the tag and offset for the address $123A63, in hexadecimal?

              tag:       0x91D3

              offset:   0x03

3. 4-way set associative mapping

Offset: 5

Row: 4

Tag: 12

2) What is the tag, set and offset for the address $123A63, in hexadecimal?

tag:       0x91D

set:       0x3

offset:   0x03

1. What is the hit ratio for the entire memory reference sequence (given in bold)?

5/14 = 35.7%

1. 2. What memory blocks will be in the cache after the last address has been assessed? Please fill in the Tag and Block first. Then, fill the actual address value for each offset location in the corresponding cell.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Tag (binary) | Block # | offset 0 | offset 1 | offset 2 | offset 3 |
| 0101 | 0 | 50 |  |  |  |
| 1010 | 1 | A4 |  |  |  |
| 1011 | 2 |  | B9 |  |  |
| 0100 | 3 |  |  |  | 4F |

1. Split the bits of virtual address and physical address.

**Virtual:**

Page:    3

Offset:   15

**Physical:**

Page:    2

Offset:   15

1. Split the bits in memory address based on the cache.

Offset: 8

Row: 3

Tag: 6

1. Suppose the processor has requested to access a memory in 0x32764 (which is virtual address)
2. Is it a page fault? Explain.

Yes, it is a page fault, I looked at the page table and did not see 7 but 6 there.

1. Show the changes of TLB, TLB LRU, page table and Mem LRU

|  |  |  |  |
| --- | --- | --- | --- |
| TLB | Virtual page # | Physical page # | Valid |
| 5 🡪 7 | 3 🡪 1 | 1 |
| 0 🡪0 | 2 🡪 2 | 1 |

**TLB LRU stack**

|  |
| --- |
| 0 🡪 0 |
| 5 🡪 7 |

**Page Table**

|  |  |  |
| --- | --- | --- |
| Virtual page # | Physical page # | Valid |
| 0 | 2 🡪 2 | 1 |
| 1 | 1 🡪 -- | 1 🡪 0 |
| 2 | -- | 0 |
| 3 | -- | 0 |
| 4 | 0 🡪 0 | 1 |
| 5 | 3 🡪 3 | 1 |
| 6 | -- | 0 |
| 7 | -- 🡪 1 | 0 🡪 1 |

**Mem LRU stack**

|  |
| --- |
| 0 🡪 7 |
| 5 🡪 0 |
| 4 🡪 5 |
| 1 🡪 4 |
|  |

3) Show the changes in Cache.

**Cache**

|  |  |  |
| --- | --- | --- |
| Line # | Tag | Data |
| 0 | 10 🡪 10 | \* |
| 1 | 0A 🡪0A | \* |
| 2 | C3 🡪 C3 | \* |
| 3 | 14 🡪 14 | \* |
| 4 | 28 🡪 28 | \* |
| 5 | 04 🡪 04 | \* |
| 6 | 37 🡪 37 | \* |
| 7 | 1D 🡪 14 | \* |

## **Appendix**











