Wareesha Ali

Software Engineer

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Experience

Micro Electronics Research Lab - MERL
Senior Research Intern Nov 2023 – Nov 2024

- Developed and deployed an AI-driven tool that converts user instructions into Verilog modules, cutting manual coding effort by 60%.
- Tuned prompt structures to increase Verilog code accuracy by 40%, ensuring compatibility with hardware simulation tools.
- Built and annotated over 3 domain-specific datasets tailored for Verilog generation, boosting LLM synthesis precision.
- Conducted 20+ simulation runs to validate AI-generated Verilog on FPGA, identifying and fixing 95% of synthesis errors.

Skills Summary

- **Languages:** Python, C#, Java,Scala, System Veilog, Chisle
- **Tools and Frameworks:** Git,GitHub,Pytourch,OpenAi playground, Docker,streamlit,Scikit-learn,TensorFlow
- **Areas of Interest:** Artificial Intelligence**,** LLMs, NLP,Software Documentation,Prompt Engineering
- **Soft Skills**: Communication, Team Collaboration, Conflict Resolution, Leadership, Project Prioritization

Key Projects

Enigma Chat: Apr 2024 - June 2025

- Built an FPGA-based chat platform using 256-bit post-quantum encryption (KyberQuanta), reducing key exchange latency by 40%.
- Implemented RISC-V and SystemVerilog logic blocks to accelerate cryptographic routines by 3× in simulation.
- **Tech Stack**: Python, System Verilog, Fpga, Git
- Github::EnigmaChat

GenieTalk: July 2024 - July 2024

- Developed a Streamlit-based chatbot using Gemini Pro LLM, handling over 500 daily queries with 95% response accuracy.
- Optimized Gemini Pro API calls to reduce latency by 70%, enabling near-instantaneous LLM responses.
- **Tech Stack**: Gemini Pro API, Streamlit, Python, Git
- Github: Genie Talk

Sentimeter: July 2024 - July 2024

- Developed a sentiment classifier using Python and Streamlit, achieving 92% accuracy across 3 sentiment categories on 1,000+ test entries.
- Designed and tuned an NLP pipeline across 5+ datasets, reducing preprocessing noise by 25% and boosting classification speed by 60%.
- **Tech Stack**: Streamlit, Python, Git, MATLAB
- Github:Sentimeter

Vulture LLM: Nov 2023-Nov 2024

- Developed a natural language to Verilog translation system that automated 80% of digital design prototyping tasks.
- Created and iteratively refined 100+ LLM prompts, improving Verilog module generation accuracy to 90%.
- Simulated and evaluated 150+ Verilog modules using Chisel and Scala testbenches, cutting simulation errors by 35%.
- **Tech Stack**: Chisel, Scala, Verilog, Python, Git

Education

- **Usaman Institute Of Technology Affiliated With NED University, Karachi - Pakistan**
  Bachelor of Science in Software Engineering - BSSE Nov 2021 - July 2025