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RT305X USB POWER APPLICATION NOTE

1 INTRODUCTION

This application note describes how the power-saving function starts, and the relationship between the new boot-loader and the Linux dwc_otg driver. The process and requirements for upgrading the SDK 3.2 with RT305x chipsets are also explained in this application note.

2 SCOPE

USB power and clock gating are disabled during boot-loader initialization in SDK3.2. They are then enabled after loading the Linux dwc_otg driver to save power.

3 DESCRIPTION

The RT305x chipset enables USB power and clock gating by default. To reduce power consumption and lower the working temperature, SDK3.2 and later versions disable the USB power and clock gating during the boot-loader initialization stage. The advantage is more power-saving.

However, an improper Linux dwc-otg driver may fail the USB initialization. Thus, it is important to upgrade the Linux dwc_otg driver correspondingly with uboot version SDK3.2 or later, if the USB feature is required. In this combination upgrade, the user benefits from lower power consumption.

3.1 SDK3.2 UBOOT

In SDK3.2 Uboot, the USB port is disabled in the file “rt2880_eth.c”, as shown below.

FILE: Uboot/drivers/rt2880_eth.c

```
void rt305x_esw_init(void)
{
……
   RT2882_REG(0xB01C0E00) = 0xF;       //disable USB module, optimize for power-saving
……
}
```

3.2 SDK3.2 DWG_OTG DRIVER

In SDK3.2 dwc_otg driver, we enable the USB port in module_init() and disable it in module_exit() in file dwc_otg_driver.c, as shown below.

FILE: source/linux-2.6.21.x/drivers/usb/dwc_otg/dwc_otg_driver.c

```
static int __init dwc_otg_driver_init(void)
{
        int retval = 0;
    struct lm_device *lmdev;
    *(unsigned long *)(KSEG1ADDR(RALINK_USB_OTG_BASE+0xE00)) = 0x0; //Enable USB Port
    lmdev = kzalloc(sizeof(struct lm_device), GFP_KERNEL);
    if (!lmdev)
    {
        printk("\n %s ,kzalloc(lm_device),fail   \n", __func__);
        return -ENOMEM;
    }
  ……..
};
```

```
static void __exit dwc_otg_driver_cleanup(void)
{
   printk(KERN_DEBUG "dwc_otg_driver_cleanup()\n");
   driver_remove_file(&dwc_otg_driver.drv, &driver_attr_debuglevel);
   driver_remove_file(&dwc_otg_driver.drv, &driver_attr_version);
   lm_driver_unregister(&dwc_otg_driver);
   *(unsigned long *)(KSEG1ADDR(RALINK_USB_OTG_BASE+0xE00)) = 0xF;   //Disable USB Port
   printk(KERN_INFO "%s module removed\n", dwc_driver_name);
}
```

4 CONCLUSION

SDK 3.2 turns off USB power by default, to lower power consumption, and the corresponding driver has been updated. Updating both SDK3.2 uBoot and the driver improves performance, and is strongly recommended.

5 APPENDIX - USB POWER AND CLOCK GATING REGISTER

5.3.6 Power and Clock Gating Register

5.3.6.1 Power and Clock Gating Control Register (PCGCCTL)

Offset: E00h

This register is available in Host and Device modes. The PwrClmp bit is available only if the OTG_EN_PWROPT parameter is set to 1 during core configuration. The application can use this register to control the core's power-down and clock gating features. For more information on how to use this register see "Partial Power-Down and Clock Gating Programming Model" on page 417.

Because the CSR module is turned off during power-down, this registers is implemented in the AHB Slave BIU module.

TABLE 5-68 Power and Clock Gating Control Register: PCGCCTL

Field	Description	Reset	Access
31:5	Reserved	27'h0	
4	PHY Suspended. (PhySuspended) Indicates that the PHY has been suspended. After the application sets the Stop Pclk bit (bit 0), this bit is updated once the PHY is suspended. Because the UTMI+ PHY suspend is controlled through a port, the UTMI+ PHY is suspended immediately after Stop Pclk is set. However, the ULPI PHY takes a few clocks to suspend, because the suspend information is conveyed through the ULPI protocol to the ULPI PHY.	1'b0	RO
3	Reset Power-Down Modules (RstPdwnModule) This bit is valid only in Partial Power-Down mode. The application sets this bit when the power is turned off. The application clears this bit after the power is turned on and the PHY clock is up.	1'b0	R_W
2	Power Clamp (PwrClmp) This bit is valid only in Partial Power-Down mode (OTG_EN_PWROPT = 1). The application sets this bit before the power is turned off to clamp the signals between the power-on modules and the power-off modules. The application clears the bit to disable the clamping before the power is turned on.	1'b0	R_W
1	Gate Hclk (GateHclk) The application sets this bit to gate hclk to modules other than the AHB Slave and Master and wakeup logic when the USB is suspended or the session is not valid. The application clears this bit when the USB is resumed or a new session starts.	1'b0	R_W
0	Stop Pclk (StopPclk) The application sets this bit to stop the PHY clock (phy_clk) when the USB is suspended, the session is not valid, or the device is disconnected. The application clears this bit when the USB is resumed or a new session starts.	1'b0	R_W