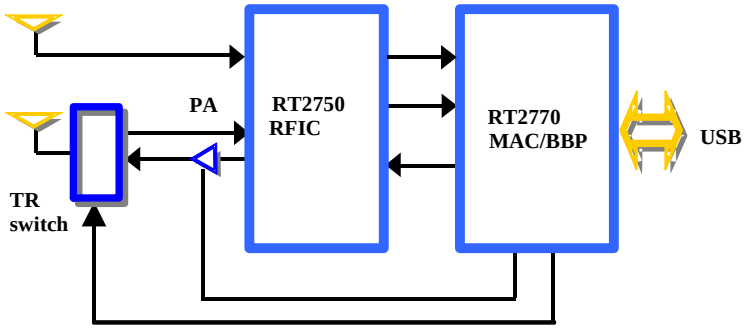
RT2770 802.11n MAC/BBP 1T2R Preliminary Data Sheet

Product Description

The RT2700 dual band MIMO 1T2R chipset for USB consists of two highly integrated ICs (RT2770 and RT2750) that fully comply with IEEE 802.11n draft 2.0 and IEEE 802.11 a/b/g standards and operate in 2.4GHz or 5GHz bands. The chipset delivers reliable, cost-effective, feature rich wireless connectivity at high throughput from an extended distance. Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators without overloading the host processor. The RT2700 is designed to support standard based features in the areas of security, quality of service and international regulation, giving end users the greatest performance anytime in any circumstance.



RT2770 MAC/BBP Features

RT2770 is the MAC/BBP IC for Ralink RT2700 chipset for USB. It supports 1T2R MIMO architecture with fully forward compatible with IEEE 802.11n standard. RT2700 is also backward compatible with the 802.11 a/b/g standard.

- 1x1/1x2 modes
- STBC Support for Extended Range
- 300Mbps RX PHY Rate, 150Mbps TX PHY Rate Support
- Legacy and High Throughput Modes
- 20MHz/40MHz bandwidth
- Reverse Direction Data Flow and Frame Aggregation
- WEP 64/128, WPA, WPA2 Support
- QoS – WMM, WMM-PS
- Multiple BSSID Support
- USB interface
- International Regulation - 802.11d + h
- Cisco CCX V1.0 V2.0 V3.0 Compliance
- Bluetooth Co-existence
- Low Power with Advanced Power Management
- Operating Systems - Windows XP, 2000, ME, 98SE, Vista, Linux, MAC
- 12mm x 12mm BGA-196 Package

Order Information

Part Number	Temp Range	Package
RT2770F	-10~85 ^{0}C	Lead free/ RoHS Compliant 196 BGA

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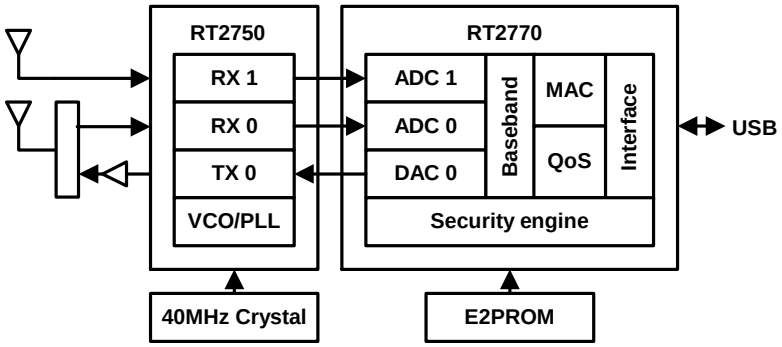
Block Diagram



RT2770 includes one-pair DACs and two-pair ADCs to support one transmit and two receive chains. After analog to digital conversion is the MIMO baseband processor that conducts effective space-timing OFDM processing up to two streams. MAC includes standard aggregation, and security modes defined in 802.11n draft spec. RT2770 supports USB 2.0 interface.

Ball Layout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PADM	PADP	CPU_A6	CPU_A9	EXT_PM_MODE	CPU_A11	CPU_A13	CPU_A14	CPU_A17	CPU_A20	CPU_D0	CPU_D3	CPU_D4	CPU_D7
B	CPU_A5	CPU_A4	CPU_A3	CPU_A8	CPU_PFL_CSN	CPU_A10	VCCIO_3	CPU_A16	CPU_A18	CPU_A19	CPU_D2	TEST4	CPU_D5	LNA_PE_A1
C	VDDL	CPU_A0	CPU_A1	CPU_A2	CPU_A7	PARA_FLASH	CPU_A12	VDD_3	CPU_A15	VCCIO_2	CPU_D1	VDD_2	PRST_N	LNA_PE_G1
D	VDDA	VDDA	RPU	VCCIO	VDD	GND	GND	GND	GND	CPU_A21	RST_N	CLK_PCI	CPU_D6	NC
E	VRES	CPU_A23	VDDD	GND	GND	GND	GND	GND	GND	GND	GND	VCCIO	LNA_PE_A0	LNA_PE_G0
F	SEL_INTCLK	CPU_A22	SUSPENDM	GND	GND	GND	GND	GND	GND	GND	GND	NC	PA_PE_A0	PA_PE_G0
G	LED_ACT_N	TEST5	VDD	GND	GND	GND	GND	GND	GND	GND	GND	SEL5G_N	PLLAHVDD	TR_SW0
H	LED_RDYG_N	LED_RDYA_N	VCCIO	GND	GND	GND	GND	GND	GND	GND	VREF	PLLDVDD	SEL5G_P	VDD33
J	GPIO3	GPIO2	GPIO4	TEST_EN	GND	GND	GND	GND	GND	GND	VCC12D	TR_SWN0	VDD	PLLCLK
K	GPIO1	GPIO0	VDD	VCCIO	GND	GND	GND	GND	GND	GND	VCC12D	VCC12D	RF_PE	VREF025N
L	EESK_SPISCK	EEDI_SPISI	RADIO_PE	EECS_SPICSN	GND	GND	GND	GND	GND	GND	VCC12A	VCC12A	TR_PE	VREF025P
M	EEDO_SPISO	RF_SDATA1	RF_SCS_N	TSSI	VCC12A	VCC12D	VCC12D	VCC12A	VCC12A	NC	VCC12A	VCC12A	IREF	VCC_RING
N	RF_SDATA0	RF_SCLK	NC	VCC_RING	VCC12A	VCC12D	VCC33A	VREFP	VREFN	NC	RFTXI_N0	RFTXQ_N0	RFRXQ_P0	RFRXQ_N0
P	NC	NC	NC	NC	RFRXI_P1	RFRXI_N1	RFRXQ_P1	RFRXQ_N1	NC	NC	RFTXI_P0	RFTXQ_P0	RFRXI_P0	RFRXI_N0

Ball Description

Ball	Name	I/O/P	Description
Analog controlled RF interface: 32 pins			
P1	NC		
P2	NC		
P3	NC		
P4	NC		
P5	RFRXI_P1	I	Positive signal of RX I differential input to ADC1
P6	RFRXI_N1	I	Negative signal of RX I differential input to ADC1
P7	RFRXQ_P1	I	Positive signal of RX Q differential input to ADC1
P8	RFRXQ_N1	I	Negative signal of RX Q differential input to ADC1
N8	VREFP	O	Reference voltage output point P for external bypass cap
N9	VREFN	O	Reference voltage output point N for external bypass cap
P9	NC		
P10	NC		
N10	NC		
M10	NC		
P11	RFTXI_P0	O	Positive signal of TX I differential output from 10bit DAC0
N11	RFTXI_N0	O	Negative signal of TX I differential output from DAC0
P12	RFTXQ_P0	O	Positive signal of TX Q differential output from DAC0
N12	RFTXQ_N0	O	Negative signal of TX Q differential output from DAC0
P13	RFRXI_P0	I	Positive signal of RX I differential input to ADC0
P14	RFRXI_N0	I	Negative signal of RX I differential input to ADC0
N13	RFRXQ_P0	I	Positive signal of RX Q differential input to ADC0
N14	RFRXQ_N0	I	Negative signal of RX Q differential input to ADC0
M13	IREF	I	Reference current input to ADC/DAC
H11	VREF	O	Reference voltage output for external bypass cap
L14	VREF025P	O	Reference voltage output point ¼ P for external bypass cap
K14	VREF025N	O	Reference voltage output point ¼ N for external bypass cap
M3	RF_SCS_N	O	RF channels RPI interface selection, active low
N1	RF_SDATA0	O	RF channel 0 RPI interface data.
N2	RF_SCLK	O	RF RPI interface clock for all RF channels
M2	RF_SDATA1	O	RF channel 1 RPI interface data.
N3	NC		
M4	TSSI	I	TSSI input to ADC
Analog power pins: 17 pins			
N7	VCC33A	P	3.3V analog power supply
N4,M14	VCC_RING	P	3.3V analog power supply
M5,N5,M8, M9,M11,M12 ,L11,L12	VCC12A	P	1.2V analog power supply
M6,N6,M7, K11,K12,J11	VCC12D	P	1.2V digital power supply
PLL interface: 4 pins			

Ball	Name	I/O/P	Description
J14	PLLCLK	I	40MHz clock for internal PLL.
H12	PLLDVDD	P	1.2V digital power supply to PLL
H14	VDD33	P	3.3V digital power supply to PLL
G13	PLLAHVDD	P	3.3V analog power supply to PLL
Digital controlled RF interface: 15 pins			
K13	RF_PE	O	RX and TX enable control for RF transceiver.
L13	TR_PE	O	RX and TX enable control for RF transceiver.
G14	TR_SW0	O	Positive signal of RX and TX switching control
J12	TR_SWN0	O	Negative signal of RX and TX switching control
H13	SEL5G_P	O	Positive signal of band select for 5GHz band
G12	SEL5G_N	O	Negative signal of band select for 5GHz band
F14	PA_PE_G0	O	LDO output for main path of 2.4GHz band RF power amplifier enable control
F13	PA_PE_A0	O	LDO output for main path of 5GHz band RF power amplifier enable control
E14	LNA_PE_G0	O	External LNA control for main path of 2.4GHz band.
E13	LNA_PE_A0	O	External LNA control for main path of 5GHz band.
F12	NC		
D14	NC		
C14	LNA_PE_G1	O	External LNA control for the other paths of 2.4GHz band.
B14	LNA_PE_A1	O	External LNA control for the other paths of 5GHz band.
L3	RADIO_PE	O	Radio power off
Parallel interface: 38 pins			
A14	CPU_D7	I/O	Parallel interface data. Pull up to VCCIO if not used.
D12	CLK_PCI	I	PCI clock Connect to GND.
D13	CPU_D6	I/O	Parallel interface data. Pull up to VCCIO if not used.
B13	CPU_D5	I/O	Parallel interface data. Pull up to VCCIO if not used.
C13	PRST_N	I	Power On reset
D11	RST_N	I	PCI reset. Connect to PRST_N
A13	CPU_D4	I/O	Parallel interface data. Pull up to VCCIO if not used.
A12	CPU_D3	I/O	Parallel interface data. Pull up to VCCIO if not used.
B11	CPU_D2	I/O	Parallel interface data. Pull up to VCCIO if not used.
C11	CPU_D1	I/O	Parallel interface data. Pull up to VCCIO if not used.
A11	CPU_D0	I/O	Parallel interface data. Pull up to VCCIO if not used.
E2	CPU_A23	O	Parallel interface address
F2	CPU_A22	O	Parallel interface address
D10	CPU_A21	O	Parallel interface address
A10	CPU_A20	O	Parallel interface address
B10	CPU_A19	O	Parallel interface address
B9	CPU_A18	O	Parallel interface address
A9	CPU_A17	O	Parallel interface address

Ball	Name	I/O/P	Description
B8	CPU_A16	O	Parallel interface address
C9	CPU_A15	O	Parallel interface address
A8	CPU_A14	O	Parallel interface address
A7	CPU_A13	O	Parallel interface address
C7	CPU_A12	O	Parallel interface address
A6	CPU_A11	O	Parallel interface address
B6	CPU_A10	O	Parallel interface address
C6	PARA_FLASH	I	Parallel flash mode. 0: no external parallel flash. 1: exist.
A5	EXT_PM_MODE	I	Firmware mode selection. 0: use internal ROM. 1: load firmware from external EEPROM.
B5	CPU_PFL_CSN	O	Parallel flash chip select
A4	CPU_A9	O	Parallel interface address
B4	CPU_A8	O	Parallel interface address
C5	CPU_A7	O	Parallel interface address
A3	CPU_A6	O	Parallel interface address
B1	CPU_A5	O	Parallel interface address
B2	CPU_A4	O	Parallel interface address
B3	CPU_A3	O	Parallel interface address
C4	CPU_A2	O	Parallel interface address
C3	CPU_A1	O	Parallel interface address
C2	CPU_A0	O	Parallel interface address
USB: 10 pins			
D2	VDDA	P	3.3V analog power
D3	RPU	I/O	Connect to an external 1.5K Ohm pull-up resistor
A2	PADP	I/O	USB data pin data+
A1	PADM	I/O	USB data pin data-
E3	VDDD	P	3.3V digital power
C1	VDDL	P	1.2V digital power
D1	VDDA	P	3.3V analog power
E1	VRES	I/O	Connect to an external 6.2K Ohm resistor for band-gap reference circuit
F3	SUSPENDM	O	USB suspend mode. 0: suspend 1: active
F1	SEL_INTCLK	I	Select internal clock. USB PHY clock source selection. 1: select internal clock 0: select external clock
LED: 3 pins			
G1	LED_ACT_N	O	LED flash in transmission
H2	LED_RDYA_N	O	LED active while operation in 5GHz mode.
H1	LED_RDYG_N	O	LED active while operation in 2.4GHz mode.
Test: 3 pin			
J4	TEST_EN	I	Enable test mode. Connect to GND for normal mode.
B12	TEST4	I	Test pin. Pull down to GND for normal mode,
G2	TEST5	I	Test pin. Pull down to GND for normal mode,
GPIO: 5 pins			
J3	GPIO4	I/O	GPIO. Default is input. Pull down to GND if not use.
J1	GPIO3	I/O	GPIO. Default is input. Pull down to GND if not

Ball	Name	I/O/P	Description
			use.
J2	GPIO2	I/O	GPIO. Default is input. Pull down to GND if not use.
K1	GPIO1	I/O	GPIO. Default is input. Pull down to GND if not use.
K2	GPIO0	I/O	GPIO. Default is input. Pull down to GND if not use.
EEPROM: 4 pins			
L4	EECS	O	serial EEPROM chip select
L1	EESK	O	serial EEPROM clock
L2	EEDI	O	serial output to EEPROM
M1	EEDO	I	serial input from EEPROM. Pull up to VCCIO.
Digital Power: 12 pins			
E12,C10,B7, D4,H3,K4	VCCIO	P	3.3V digital power supply
J13,C12,C8, D5,G3,K3	VDD	P	1.2V digital power supply
Ground: 53 pins			
D6,D7,D8, D9,E10,E11, E4,E5,E6,E7 ,E8,E9,F10, F11,F4,F5, F6,F7,F8,F9, G10,G11,G4 ,G5,G6,G7, G8,G9,H10, H4,H5,H6, H7,H8,H9, J10,J5,J6,J7, J8,J9,K10, K5,K6,K7,K8 ,K9,L10,L5, L6,L7,L8,L9	GND	P	Grounds
Total: 196 pins			

Absolute Maximum Ratings

Core Supply Voltage 1.32V
I/O Supply Voltage 3.6V
Input, Output or I/O Voltage.. GND –0.3V to Vcc+0.3V

Thermal Information

Thermal Resistance θ_{JA} (^{o}C/W) in free air for TFBGA (12mmx12mm) package... .. . . . . .36.6 ^{o}C/W
Maximum Junction Temperature . . . . . .125^{o}C
Maximum Storage Temperature . . . . -40^{o}C to 125^{o}C

Operating Conditions

Ambient Temperature Range . . . . . -10 to 85^{o}C
Core Supply Voltage . . . . . 1.2V +/- 10%
I/O Supply Voltage . . . . . 3.3V +/- 10%

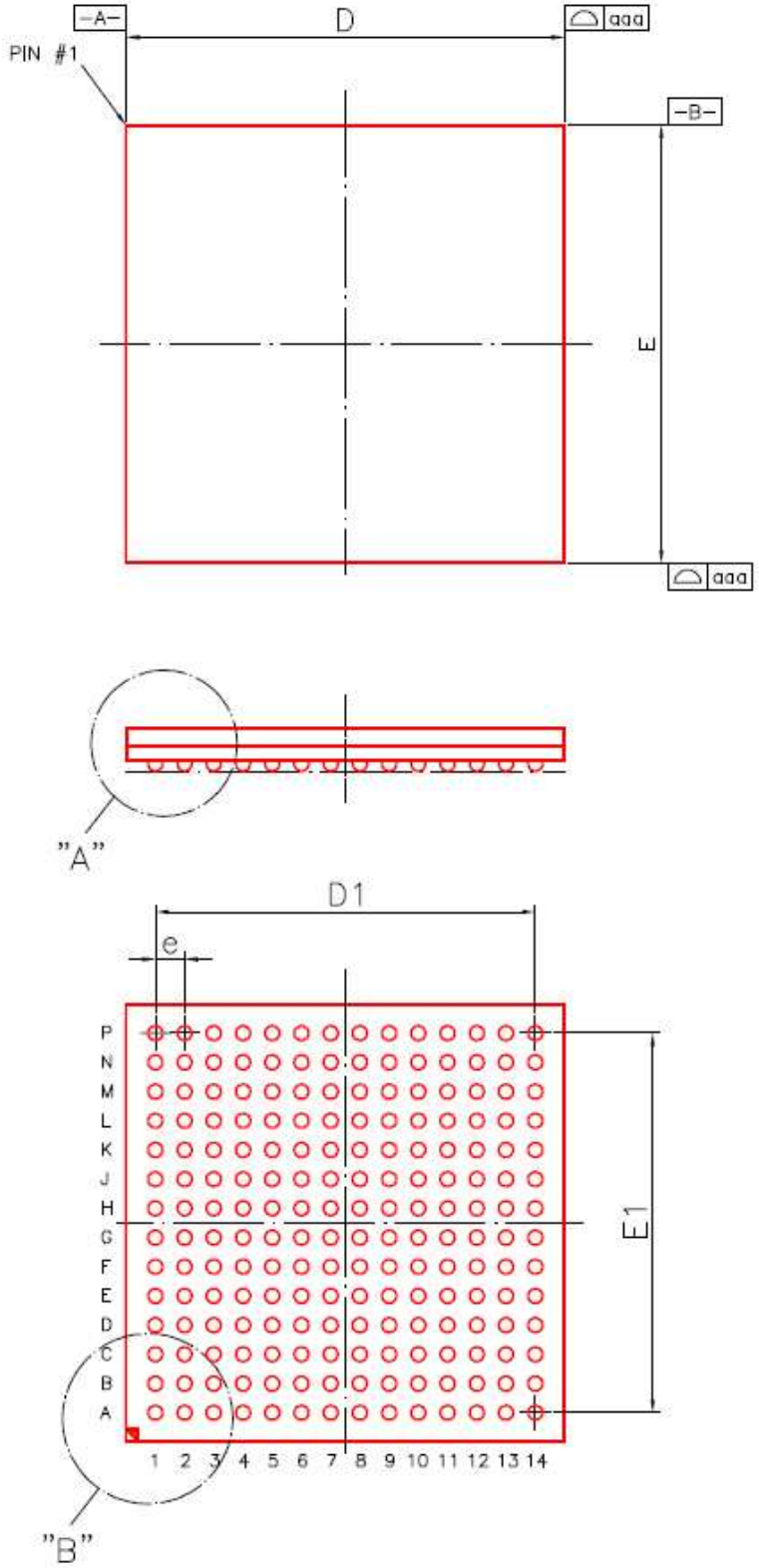
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

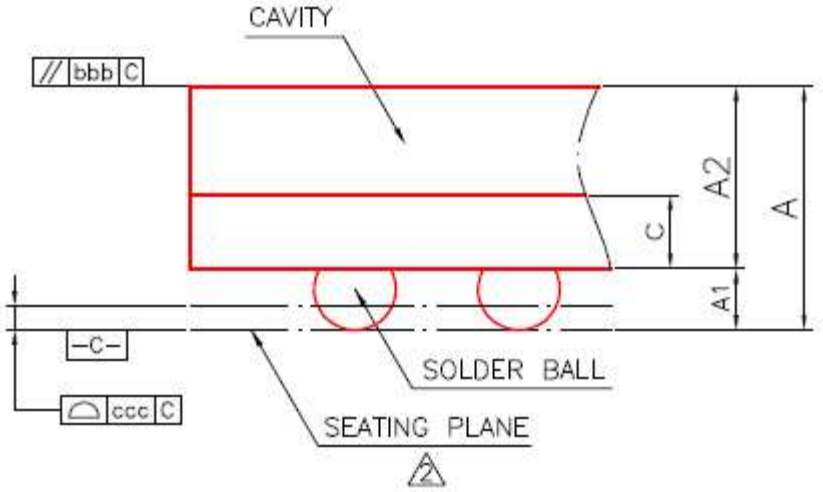
DC Electrical Characteristics

Parameters	Sym	Conditions	Min	Typ	Max	Unit
3.3V Supply Voltage	Vcc33		2.7	3.3	3.6	V
1.2V Supply Voltage	Vcc12			1.2		V
3.3V Current Consumption	Icc33			TBD		mA
1.2V Current Consumption	Icc12			350		mA

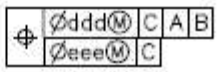
Package Information

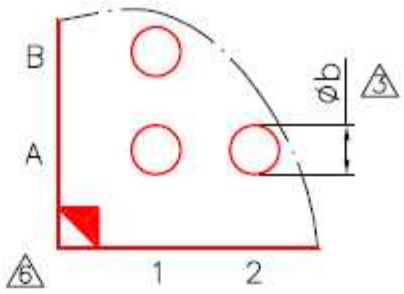
BGA (12x12x1.4mm)





DETAIL : "A"





DETAIL : "B"

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.80	0.89	0.98	0.031	0.035	0.039
c	0.32	0.36	0.40	0.013	0.014	0.016
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	---	10.40	---	---	0.409	---
E1	---	10.40	---	---	0.409	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.12			0.005		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	14/14			14/14		