雷 凌 科 技 股 份 有 限 公 司
新竹縣竹北市台元街３６號５樓 TEL:886-3-5600868 FAX:886-3-5600818
5F,No.36, Taiyuan St., Jhubei City, Hsinchu County 302, TAIWAN ,R.O.C.
www.ralinktech.com.tw

RT3052/RT3051/RT3050 EEPROM Format V1.3

Update history

Version	Date	Description	Modified by
1.0	2008/6/20	Initial version	Scott
		The RT3052 EEPROM format is modified based on RT2880 EEPROM format v1.3.1, add RT3052 definition	Scott
1.1	2008/10/23	Add RT3021 RFIC type	Daniel
1.2	2008/11/17	Add Maximum TX Power for 2.4Ghz band(4Eh) definition	Jun
1.3	2008/11/26	Modify the description of register @ 4Eh~4Fh. * Change register “Maximum TX Power for 2.4GHz band” to “EIRP TX Power for 2.4GHz band”	Daniel

Contents

1. General Description

This Document specify every field for RT305X (RT3052/RT3051/RT3050) EEPROM layout. RT305X EEPROM layout is based on RT2880's, generally speaking RT3052 and RT2880 wireless share the same EEPROM format, however,

There are two application usage for RT305X, one is use RT305X as a standalone router, the other is as an intelligent NIC(iNIC). The EEPROM definition will be different for these two applications.

2. RT3052 EEPROM Layout

2.1 EEPROM for iNIC application

Offset	Default (hex)	b15 ~b8	b7 ~ b0
00h	3052	Chip ID	
02h	0000	EEPROM Version	
04h		WLAN Mac Address [47:32]	
06h		WLAN Mac Address [31:16]	
08h		WLAN Mac Address [15:0]	
0Ah	FFFF	**Reserved**	
0Ch	FFFF	**Reserved**	
0Eh	FFFF	**Reserved**	
10h	FFFF	**Reserved**	
12h	FFFF	**Reserved**	
14h	FFFF	**Reserved**	
16h	FFFF	**Reserved**	**Reserved**
18h	FFFF	**Reserved**	
1Ah	FFFF	**Reserved**	
1Ch	FFFF	**Reserved**	
1Eh	FFFF	Reserved	
20h	FFFF	Reserved	
22h	FFFF	Reserved	
24h	FFFF	Low half word of Magic number (0x5244)	
26h	FFFF	High half word of Magic number (0x4D41)	
28h	FFFF	Low half word of SDRAM CFG0	
2Ah	FFFF	High half word of SDRAM CFG0	
2Ch	FFFF	Low half word of SDRAM CFG1	
2Eh	FFFF	High half word of SDRAM CFG1	
30h	FFFF	Source Address of in-band frame (0 for 00:0c:43:00:00:00) (FFFF for broadcast address)	
32h	FFFF	Protocol of in-band frame	

Offset	Default (hex)	b15 ~b8	b7 ~ b0
34h	FFFF	NIC Configuration 0	
36h	FFFF	NIC Configuration 1	
38h	FFFF	Country Region 2.4G band	**Reserved**
3Ah	FFFF	LED Mode	Frequency offset
3Ch	FFFF	Reserved	
3Eh	FFFF	LED ACT Configuration	
40h	FFFF	LED ACT Polarity	
42h	FFFF	NIC Configuration 2	
44h	FFFF	**Reserved**	External LNA gain for 2.4G Band
46h	0000	2.4G RSSI1 offset	2.4G RSSI0 offset
48h	0000	**Reserved**	Reserved
4Ah	0000	**Reserved**	**Reserved**
4Ch	0000	**Reserved**	**Reserved**
4Eh	FFFF	**Reserved**	Define the MAX TX power for 2.4G band
50h	FFFF	**Reserved**	20M/40M BW Power delta for 2.4G band
52h	FFFF	Channel 2 TX0 power	Channel 1 TX0 power
54h	FFFF	Channel 4 TX0 power	Channel 3 TX0 power
56h	FFFF	Channel 6 TX0 power	Channel 5 TX0 power
58h	FFFF	Channel 8 TX0 power	Channel 7 TX0 power
5Ah	FFFF	Channel 10 TX0 power	Channel 9 TX0 power
5Ch	FFFF	Channel 12 TX0 power	Channel 11 TX0 power
5Eh	FFFF	Channel 14 TX0 power	Channel 13 TX0 power
60h	FFFF	Channel 2 TX1power	Channel 1 TX1 power
62h	FFFF	Channel 4 TX1 power	Channel 3 TX1 power
64h	FFFF	Channel 6 TX1 power	Channel 5 TX1 power
66h	FFFF	Channel 8 TX1 power	Channel 7 TX1 power
68h	FFFF	Channel 10 TX1 power	Channel 9 TX1 power
6Ah	FFFF	Channel 12 TX1 power	Channel 11 TX1 power
6Ch	FFFF	Channel 14 TX1 power	Channel 13 TX1 power
6Eh	FFFF	2.4G TX power –3 TSSI boundary	2.4G TX power –4 TSSI boundary
70h	FFFF	2.4G TX power –1 TSSI boundary	2.4G TX power –2 TSSI boundary
72h	FFFF	2.4G TX power +1 TSSI boundary	2.4G TX power ±0 TSSI boundary
74h	FFFF	2.4G TX power +3 TSSI boundary	2.4G TX power +2 TSSI boundary
76h	FFFF	2.4G TX ALC step value	2.4G TX power +4 TSSI boundary
78h	FFFF	**Reserved**	**Reserved**
7Ah	FFFF	**Reserved**	**Reserved**

Offset	Default (hex)	b15 ~b8	b7 ~ b0
7Ch	FFFF	**Reserved**	**Reserved**
7Eh	FFFF	**Reserved**	**Reserved**
80h	FFFF	**Reserved**	**Reserved**
82h	FFFF	**Reserved**	**Reserved**
84h	FFFF	**Reserved**	**Reserved**
86h	FFFF	**Reserved**	**Reserved**
88h	FFFF	**Reserved**	**Reserved**
8Ah	FFFF	**Reserved**	**Reserved**
8Ch	FFFF	**Reserved**	**Reserved**
8Eh	FFFF	**Reserved**	**Reserved**
90h	FFFF	**Reserved**	**Reserved**
92h	FFFF	**Reserved**	**Reserved**
94h	FFFF	**Reserved**	**Reserved**
96h	FFFF	**Reserved**	**Reserved**
98h	FFFF	**Reserved**	**Reserved**
9Ah	FFFF	Reserved	**Reserved**
9Ch	FFFF	Reserved	Reserved
9Eh	FFFF	Reserved	Reserved
A0h	FFFF	Reserved	Reserved
A2h	FFFF	Reserved	Reserved
A4h	FFFF	Reserved	Reserved
A6h	FFFF	**Reserved**	**Reserved**
A8h	FFFF	**Reserved**	**Reserved**
AAh	FFFF	**Reserved**	**Reserved**
ACh	FFFF	**Reserved**	**Reserved**
AEh	FFFF	**Reserved**	**Reserved**
B0h	FFFF	**Reserved**	**Reserved**
B2h	FFFF	**Reserved**	**Reserved**
B4h	FFFF	**Reserved**	**Reserved**
B6h	FFFF	**Reserved**	**Reserved**
B8h	FFFF	**Reserved**	**Reserved**
BAh	FFFF	**Reserved**	**Reserved**
BCh	FFFF	**Reserved**	**Reserved**
BEh	FFFF	**Reserved**	**Reserved**
C0h	FFFF	**Reserved**	**Reserved**
C2h	FFFF	**Reserved**	**Reserved**

Offset	Default (hex)	b15 ~b8	b7 ~ b0
C4h	FFFF	**Reserved**	**Reserved**
C6h	FFFF	**Reserved**	**Reserved**
C8h	FFFF	Reserved	**Reserved**
CAh	FFFF	Reserved	Reserved
CCh	FFFF	Reserved	Reserved
CEh	FFFF	Reserved	Reserved
D0h	FFFF	Reserved	Reserved
D2h	FFFF	Reserved	Reserved
D4h	FFFF	**Reserved**	**Reserved**
D6h	FFFF	**Reserved**	**Reserved**
D8h	FFFF	**Reserved**	**Reserved**
DAh	FFFF	**Reserved**	**Reserved**
DCh	FFFF	**Reserved**	**Reserved**
DEh	6666	TX power for CCK 5.5M/11M	TX power for CCK 1M/2M
E0h	6666	TX power for OFDM 12M/18M	TX power for OFDM 6M/9M
E2h	6666	TX power for OFDM 48M/54M	TX power for OFDM 24M/36M
E4h	6666	TX power for HT MCS=2,3	TX power for HT MCS=0,1
E6h	6666	TX power for HT MCS=6,7	TX power for HT MCS=4,5
E8h	6666	TX power for HT MCS=10,11	TX power for HT MCS=8,9
EAh	6666	TX power for HT MCS=14,15	TX power for HT MCS=12,13
ECh	6666	TX power for STBC MCS=2,3	TX power for STBC MCS=0,1
EEh	6666	TX power for STBC MCS=6,7	TX power for STBC MCS=4,5
F0h	FFFF	Reserved	Reserved
F2h	FFFF	Reserved	Reserved
F4h	FFFF	Reserved	Reserved
F6h	FFFF	Reserved	Reserved
F8h	FFFF	Reserved	Reserved
FAh	FFFF	Reserved	Reserved
FCh	FFFF	Reserved	Reserved
FEh	FFFF	Reserved	Reserved
…	…	…	…

2.2 EEPROM for Standalone router application

Offset	Default (hex)	b15 ~b8	b7 ~ b0
00h	3052	Chip ID	
02h	0000	EEPROM Version	
04h		WLAN Mac Address [47:32]	
06h		WLAN Mac Address [31:16]	
08h		WLAN Mac Address [15:0]	
0Ah	FFFF	**Reserved**	
0Ch	FFFF	**Reserved**	
0Eh	FFFF	**Reserved**	
10h	FFFF	**Reserved**	
12h	FFFF	**Reserved**	
14h	FFFF	**Reserved**	
16h	FFFF	**Reserved**	**Reserved**
18h	FFFF	**Reserved**	
1Ah	FFFF	**Reserved**	
1Ch	FFFF	**Reserved**	
1Eh	FFFF	Reserved	
20h	FFFF	Reserved	
22h	FFFF	Reserved	
24h	FFFF	Reserved	
26h	FFFF	Reserved	
28h		MAC0 MAC address [47:32]	
2Ah		MAC0 MAC address [31:16]	
2Ch		MAC0 MAC address [15:0]	
2Eh		MAC1 MAC address [47:32]	
30h		MAC1 MAC address [31:16]	
32h		MAC1 MAC address [15:0]	
34h	FFFF	NIC Configuration 0	
36h	FFFF	NIC Configuration 1	
38h	FFFF	Country Region 2.4G band	**Reserved**
3Ah	FFFF	LED Mode	Frequency offset
3Ch	FFFF	Reserved	
3Eh	FFFF	LED ACT Configuration	
40h	FFFF	LED ACT Polarity	
42h	FFFF	NIC Configuration 2	
44h	FFFF	**Reserved**	External LNA gain for 2.4G Band

Offset	Default (hex)	b15 ~b8	b7 ~ b0
46h	0000	2.4G RSSI1 offset	2.4G RSSI0 offset
48h	0000	**Reserved**	2.4G RSSI2 offset
4Ah	0000	**Reserved**	**Reserved**
4Ch	0000	**Reserved**	**Reserved**
4Eh	FFFF	**Reserved**	Define the MAX TX power for 2.4G band
50h	FFFF	**Reserved**	20M/40M BW Power delta for 2.4G band
52h	FFFF	Channel 2 TX0 power	Channel 1 TX0 power
54h	FFFF	Channel 4 TX0 power	Channel 3 TX0 power
56h	FFFF	Channel 6 TX0 power	Channel 5 TX0 power
58h	FFFF	Channel 8 TX0 power	Channel 7 TX0 power
5Ah	FFFF	Channel 10 TX0 power	Channel 9 TX0 power
5Ch	FFFF	Channel 12 TX0 power	Channel 11 TX0 power
5Eh	FFFF	Channel 14 TX0 power	Channel 13 TX0 power
60h	FFFF	Channel 2 TX1power	Channel 1 TX1 power
62h	FFFF	Channel 4 TX1 power	Channel 3 TX1 power
64h	FFFF	Channel 6 TX1 power	Channel 5 TX1 power
66h	FFFF	Channel 8 TX1 power	Channel 7 TX1 power
68h	FFFF	Channel 10 TX1 power	Channel 9 TX1 power
6Ah	FFFF	Channel 12 TX1 power	Channel 11 TX1 power
6Ch	FFFF	Channel 14 TX1 power	Channel 13 TX1 power
6Eh	FFFF	2.4G TX power –3 TSSI boundary	2.4G TX power –4 TSSI boundary
70h	FFFF	2.4G TX power –1 TSSI boundary	2.4G TX power –2 TSSI boundary
72h	FFFF	2.4G TX power +1 TSSI boundary	2.4G TX power ±0 TSSI boundary
74h	FFFF	2.4G TX power +3 TSSI boundary	2.4G TX power +2 TSSI boundary
76h	FFFF	2.4G TX ALC step value	2.4G TX power +4 TSSI boundary
78h	FFFF	**Reserved**	**Reserved**
7Ah	FFFF	**Reserved**	**Reserved**
7Ch	FFFF	**Reserved**	**Reserved**
7Eh	FFFF	**Reserved**	**Reserved**
80h	FFFF	**Reserved**	**Reserved**
82h	FFFF	**Reserved**	**Reserved**
84h	FFFF	**Reserved**	**Reserved**
86h	FFFF	**Reserved**	**Reserved**
88h	FFFF	**Reserved**	**Reserved**
8Ah	FFFF	**Reserved**	**Reserved**
8Ch	FFFF	**Reserved**	**Reserved**

Offset	Default (hex)	b15 ~b8	b7 ~ b0
8Eh	FFFF	**Reserved**	**Reserved**
90h	FFFF	**Reserved**	**Reserved**
92h	FFFF	**Reserved**	**Reserved**
94h	FFFF	**Reserved**	**Reserved**
96h	FFFF	**Reserved**	**Reserved**
98h	FFFF	**Reserved**	**Reserved**
9Ah	FFFF	**Reserved**	**Reserved**
9Ch	FFFF	**Reserved**	**Reserved**
9Eh	FFFF	**Reserved**	**Reserved**
A0h	FFFF	**Reserved**	**Reserved**
A2h	FFFF	**Reserved**	**Reserved**
A4h	FFFF	**Reserved**	**Reserved**
A6h	FFFF	**Reserved**	**Reserved**
A8h	FFFF	**Reserved**	**Reserved**
AAh	FFFF	**Reserved**	**Reserved**
ACh	FFFF	**Reserved**	**Reserved**
AEh	FFFF	**Reserved**	**Reserved**
B0h	FFFF	**Reserved**	**Reserved**
B2h	FFFF	**Reserved**	**Reserved**
B4h	FFFF	**Reserved**	**Reserved**
B6h	FFFF	**Reserved**	**Reserved**
B8h	FFFF	**Reserved**	**Reserved**
BAh	FFFF	**Reserved**	**Reserved**
BCh	FFFF	**Reserved**	**Reserved**
BEh	FFFF	**Reserved**	**Reserved**
C0h	FFFF	**Reserved**	**Reserved**
C2h	FFFF	**Reserved**	**Reserved**
C4h	FFFF	**Reserved**	**Reserved**
C6h	FFFF	**Reserved**	**Reserved**
C8h	FFFF	**Reserved**	**Reserved**
CAh	FFFF	**Reserved**	**Reserved**
CCh	FFFF	**Reserved**	**Reserved**
CEh	FFFF	**Reserved**	**Reserved**
D0h	FFFF	**Reserved**	**Reserved**
D2h	FFFF	**Reserved**	**Reserved**
D4h	FFFF	**Reserved**	**Reserved**

Offset	Default (hex)	b15 ~b8	b7 ~ b0
D6h	FFFF	**Reserved**	**Reserved**
D8h	FFFF	**Reserved**	**Reserved**
DAh	FFFF	**Reserved**	**Reserved**
DCh	FFFF	**Reserved**	**Reserved**
DEh	6666	TX power for CCK 5.5M/11M	TX power for CCK 1M/2M
E0h	6666	TX power for OFDM 12M/18M	TX power for OFDM 6M/9M
E2h	6666	TX power for OFDM 48M/54M	TX power for OFDM 24M/36M
E4h	6666	TX power for HT MCS=2,3	TX power for HT MCS=0,1
E6h	6666	TX power for HT MCS=6,7	TX power for HT MCS=4,5
E8h	6666	TX power for HT MCS=10,11	TX power for HT MCS=8,9
EAh	6666	TX power for HT MCS=14,15	TX power for HT MCS=12,13
ECh	6666	TX power for STBC MCS=2,3	TX power for STBC MCS=0,1
EEh	6666	TX power for STBC MCS=6,7	TX power for STBC MCS=4,5
F0h	FFFF	Reserved	Reserved
F2h	FFFF	Reserved	Reserved
F4h	FFFF	Reserved	Reserved
F6h	FFFF	Reserved	Reserved
F8h	FFFF	Reserved	Reserved
FAh	FFFF	Reserved	Reserved
FCh	FFFF	Reserved	Reserved
FEh	FFFF	Reserved	Reserved
…	…	…	…

3. EEPROM Contents

3.1 E2PROM layout version # (02h)

Offset	Value	Description
02h	0	Version 0.
	1 ~ 255	Invalid version. Treat as version 0.

3.2 ASIC Boot-Rom Config(1Eh ~ 33h)

3.2.1 RT3052 reserved fields for RGMII device mode (iNIC)

Offset	Default (hex)	b15 ~b8	b7 ~ b0
1Eh	FFFF	Reserved	
20h	FFFF	Reserved	
22h	FFFF	Reserved	
24h	FFFF	Low half word of Magic number (0x5244)	
26h	FFFF	High half word of Magic number (0x4D41)	
28h	FFFF	Low half word of SDRAM CFG0	
2Ah	FFFF	High half word of SDRAM CFG0	
2Ch	FFFF	Low half word of SDRAM CFG1	
2Eh	FFFF	High half word of SDRAM CFG1	
30h	FFFF	Source Address of in-band frame (0 for 00:0c:43:00:00:00) (FFFF for broadcast address)	
32h	FFFF	Protocol of in-band frame	

fields 0x24 ~ 0x26 is the magic number for iNIC bootrom, if the magic number is correctly configured(written 0x5244 and 0x4d41), then

If the System configuration register bit 28(INIC_EE_SDRAM) is 1, then iNIC bootrom will read 0x28 ~ 0x2A, and use it's value for SDRAM_CFG0, and also read 0x2C ~ 0x2E, and use it's value for SDRAM_CFG1. If INIC_EE_SDRAM bit is 0, 0x28 ~ 0x2E is ignored.

If 0x30 is default value 0xFFFF, the bootrom will send bootstap frames using broadcast address as source address, if it's value is 0x0, it will use source address 00:0c:43:00:00:00

If 0x32 is default value 0xFFFF, then the Ethernet protocol filed for bootstrap frame will be 0xFFFF, and if it is other value, the Ethernet protocol will be that value.

3.2.2 RT3052 reserved fields for standalone router

Offset	Default (hex)	b15 ~b8	b7 ~ b0
1Eh	FFFF	reserved	
20h	FFFF	reserved	
22h	FFFF	reserved	
24h	FFFF	reserved	
26h	FFFF	reserved	
28h		MAC0 MAC address [15:0]	
2Ah		MAC0 MAC address [31:16]	
2Ch		MAC0 MAC address [47:32]	
2Eh		MAC1 MAC address [15:0]	
30h		MAC1 MAC address [31:16]	
32h		MAC1 MAC address [47:32]	

3.3 NIC Configuration 0 (0x34)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RFIC Type				TX Path setting				RX Path setting			
Reserved				1: RT2820 (2.4G 2T3R) 2: RT2850 (2.4G/5G 2T3R) 3: RT2720 (2.4G 1T2R) 4: RT2750 (2.4G/5G 1T2R) 5: RT3020 (2.4G, 1T1R inside RT3050) 6: RT2020 (2.4G) 7: RT3021 (2.4G 1T2R) 8: RT3022 (2.4G, 2T2R. inside RT3052)				1: 1TX 2: 2TX				1: 1RX 2: 2RX			

NIC Configuration 0 Register Bit Fields Description

Offset	Field	Description
34h	3:0	These fields are to provide the RX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 RX front-end in the system. 2 (0010): 2 RX front-end in the system. 3 ~ F (0100 ~ 1111): Reserved.
	7:4	These fields are to provide the TX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 TX front-end in the system. 2 (0010): 2 TX front-end in the system. 3 ~ F (0011 ~ 1111): Reserved.
35h	11:8	RFIC type. 0 (0000): Reserved 5 (0101): IC type is RT3020 (2.4GHz, 1T1R, inside RT3050) 6 (0110): IC type is RT3021 (2.4GHz, 1T2R, inside RT3051) 8 (1000): IC type is RT3022 (2.4GHz, 2T2R, inside RT3052) 9 ~ F (0101 ~ 1111): reserved
	15:12	Reserved.

3.4 NIC Configuration 1 (0x36)

Bit[7:0] = 0xFF will be treated as INVALID and used Default Value
Bit[15:8] = 0xFF will be treated as INVALID and used Default Value

7	6	5	4	3	2	1	0
WPS PBC	**Reserved**	2.4G side band for 40M BW	Proprietary Test bit	**Reserved**	EXT LNA 2.4G	TX ALC	**Reserved**
0: off (D) 1: on		0: off 1: on(D)	0: off(D) 1: on		0: off 1: on(D)	0: off(D) 1: on	

15 ~ 12	11	10	9	8
Reserved	Antenna Diversity	Broadband EXT LNA	**Reserved**	40M BW in 2.4G band
	0: off (D) 1: on	0: off 1: on		0: on (D) 1: off

NIC Configuration 1 Register Bit Fields Description

Offset	Field	Definition	Description	
36h	0	Reserved	Reserve.	
	1	TX ALC	The default value is 0. When the TX auto-level-calibration control is enabled (=1), the driver will automatic compensate TX power varied due to temperature variation.	
			0	Default value. Disable TX auto-level-calibration control.
			1	Enable TX auto-level-calibration control.
	2	External LNA for 11g (2.4 GHz) band	0	Board without external LNA must set this bit to 0.
			1	Default value. Board with external LNA.
	3	**Reserved**	**Reserved**	
	4	Proprietary TEST BIT#1	For debug purpose.	
	5	2.4G side band for 40M BW	For debug purpose.	
	6	**Reserved**	**Reserved**	
	7	WPS PBC	WPS Push Button Configuration control.	
			0	OFF: Disable WPS PBC function.
			1	ON: Enable WPS PBC function,
37h	8	40M BW in 2.4G band	0	Enable 11g 40M bandwidth.
			1	Disable 11g 40M bandwidth.

Offset	Field	Definition	Description	
	9	**Reserved**	**Reserved**	
	10	Broadband EXT LNA	0	Board without external LNA must set this bit to 0.
			1	Board with external LNA must set this bit to 1.
	11	Antenna Diversity	0	OFF: Disable antenna diversity function.
			1	ON: Enable antenna diversity function,
	15:12	Reserved	Reserved	

3.5 NIC Configuration 2 (0x42)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TX Stream				RX Stream			
								1: 1 Stream 2: 2 Stream				1: 1 Stream 2: 2 Stream			

NIC Configuration 0 Register Bit Fields Description

Offset	Field	Description
42h	3:0	These fields are to define the support RX stream number in the system. 0 (0000): Reserved. 1 (0001): 1 RX stream in the system. 2 (0010): 2 RX streams in the system. 3 ~ F (0011 ~ 1111): Reserved.
	7:4	These fields are to define the support TX stream number in the system. 0 (0000): Reserved. 1 (0001): 1 TX stream in the system. 2 (0010): 2 TX streams in the system. 3 ~ F (0011 ~ 1111): Reserved.
43h	15:8	Reserved.

Note:

1. Stream vs. data rate.

# Stream	Data rate
1 stream	MCS0~MCS7
2 stream	MCS0~MCS15.

2. Stream setting should be equal or less than front-end path setting (offset 0x34h).
3. Default=0xFF means that based on the front-end path setting (0x34h) for maximum capability.

3.6 Country Region Code for 2.4G band (0x39)

7	6	5	4	3	2	1	0
2.4GHz band country region code							

Default value = FFh, which means read from INF and registry, more flexible than reading from EEPROM, this is our current InstallShield CCS implementation. We do not recommend customers to read SKU from EEPROM. Value FFh is the default value.
CountryCode— Specify the domain code, can be FFh or one of the followings,

Index	Support Channels
0	CH1 – 11
1	CH1 – 13
2	CH10 – 11
3	CH10 – 13
4	CH14
5	CH1 – 14
6	CH3 – 9
7	CH5 – 13

Notes: If set to read SKU from EEPROM, only available if both 5GHz and 2.4GHz Country Region code registers are programmed.

3.7 Frequency offset (0x3A)

7	6	5	4	3	2	1	0
Frequency calibration							

For crystal frequency calibration purpose.

3.8 LED Mode Setting (0x3B)

7	6	5	4	3	2	1	0
GPIO Polarity	LED control modes						

Offset	Field	LED Mode		Description
3Bh	[6:0]	0	HW control	The default mode. Driver sets MAC register and MAC controls LED.
		1	FW default mode	The firmware controls how LED blinks.
		2	8sec scan	Same as LED mode 1 except that fast blink for 8sec when doing scanning.
		3-63	-	Reserved.
		64	Reserved	Reserved.
	7	GPIO Polarity		0: Negative polarity 1: Positive polarity

3.9 LED Configuration: (in EEPROM Byte 3Eh~3Fh)

7	6	5	4	3	2	1	0
Radio on and link down				Radio off			

15	14	13	12	11	10	9	8
Reserved				Radio on and link to G			

Offset	States	Field	RT3052 WLAN_LED behavior
3Eh	Radio off	[1:0]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		2	0: Solid on when no traffic 1: Slow blink when no traffic
		3	Reserved
	Radio on but link down	[5:4]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		6	0: Solid on when no traffic 1: Slow blink when no traffic
		7	Reserved
3Fh	Radio on and link to G	[9:8]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		10	0: Solid on when no traffic 1: Slow blink when no traffic
		11	Reserved
	Reserved	[15:12]	Reserved

3.10 LED Polarity: (in EEPROM Byte 40h~41h)

7	6	5	4	3	2	1	0
Reserved	LED ACT	Reserved	Reserved	Reserved	LED ACT	Reserved	Reserved
Radio on and link down				Radio off			

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	LED ACT	Reserved	Reserved
Reserved				Radio on and link to G			

Offset	States	Field	LED behavior	
40h	Radio off	0	Reserved	1: Positive polarity 0: Negative polarity
		1	Reserved	
		2	LED ACT	
		3	Reserved	Reserved and must be filled as 1.
	Radio on but link down	4	Reserved	1: Positive polarity 0: Negative polarity
		5	Reserved	
		6	LED ACT	
		7	Reserved	Reserved and must be filled as 1.
41h	Radio on and link to G	8	Reserved	1: Positive polarity 0: Negative polarity
		9	Reserved	
		10	LED ACT	
		11	Reserved	Reserved and must be filled as 1.
	Reserved	12	Reserved	Reserved and must be filled as 1.
		13	Reserved	
		14	Reserved	
		15	Reserved	

3.11 External LNA gain for 2.4GHz Band (44h)

External LNA gain for 2.4GHz Band Register Bit Fields Description

<table>
<tr><th>Offset</th><th>Field</th><th>Description</th></tr>
<tr><td>44h</td><td>7:0</td><td>External LNA gain for 2.4GHz Band.
1 step = 1 dB
Example:
<table>
<tr><td>Value</td><td>LNA gain (dB)</td></tr>
<tr><td>0000 0000</td><td>0</td></tr>
<tr><td>0000 0001</td><td>1</td></tr>
<tr><td>0000 1010</td><td>10</td></tr>
</table></td></tr>
</table>

3.12 EIRP TX Power for 2.4GHz band (4Eh)

The register is intend to limit the TX power for different countries in one SKU.

EIRP TX Power for 2.4GHz band Register Bit Fields Description

Offset	Field	Description
4Eh	7:0	2.4GHz maximum TX power. The register value is the board's EIRP value. The driver will compare the board's EIRP with each country allow TX power automatically if this function is enabled. FF (1111 1111): disable the maximum TX power comparison function. Ex: 08 (0000 1000): Board's EIRP is 8dBm 10 (0001 0000): Board's EIRP is 16dBm 12 (0001 0010): Board's EIRP is 18dBm
4Fh	15:8	Reserved

Example:

If antenna gain is 3dBi, board's maximum TX power is 17dBm. The Equivalent isotropically radiated power (EIRP) is 17+3=20dBm. The value of offset 4Eh is 14 (0001 0100).

Following table is based on the maximum TX power comparison function is enabled.

Country	Allowed TX power of the country (dBm)	Offset 4Eh = 14	Exact maximum EIRP (dBm)
A	20	20	20
B	16	20	16
C	18	20	18
D	23	20	20

Note:

If allowed country power is greater than the TX power setting of offset 4Eh, then the board maximum EIRP is the TX power setting of offset 4Eh.

If allowed country power is less than the TX power setting of offset 4Eh, then the board maximum EIRP is the country's allowed TX power.

3.13 20M/40M BW Power Delta for 2.4GHz band (50h)

This register is for driver compensates the TX power value of 40M BW with the configured delta value.

TX power delta configuration Register Bit Fields Description

Field	Description
5:0	40M BW TX power delta value (MAX=4). 000001: 1dBm 000010: 2dBm 000011: 3dBm 000100: 4dBm
6	1: increase 40M BW TX power with the delta value. 0: decrease 40M BW TX power with the delta value.
7	1: enableTX power compensation.

Example:

The default calibrated TX power is as followings with the TX power delta configuration is not enabled.

- 40M BW TX power= 14dBm and 20M BW TX power = 14dBm

If want keep 20M BW TX power in 14dBm while to reduce 40M BW TX power to 10dBm (delta=4dBm),

Apply following settings can meet the requirement.

- Set 50h = 84h (1000 0100)
- Set 51h = 84h (1000 0100)

3.14 2.4G band TX0 & TX1 Power (52h~6Dh)

Both the calibrated 2.4GHz TX0 & TX1 power values are saved in these registers.
To prevent reading from EMPTY E2PROM, driver treats these “Channel xx Tx Power” value 0 and any value > =0x20 as invalid. That is, only bit [0..4] in each byte contains valid data, [bit 5..7] MUST be 0.

Offset	b15 ~b8	b7 ~ b0
52h	Channel 2 TX0 power	Channel 1 TX0 power
54h	Channel 4 TX0 power	Channel 3 TX0 power
56h	Channel 6 TX0 power	Channel 5 TX0 power
58h	Channel 8 TX0 power	Channel 7 TX0 power
5Ah	Channel 10 TX0 power	Channel 9 TX0 power
5Ch	Channel 12 TX0 power	Channel 11 TX0 power
5Eh	Channel 14 TX0 power	Channel 13 TX0 power
60h	Channel 2 TX1power	Channel 1 TX1 power
62h	Channel 4 TX1 power	Channel 3 TX1 power
64h	Channel 6 TX1 power	Channel 5 TX1 power
66h	Channel 8 TX1 power	Channel 7 TX1 power
68h	Channel 10 TX1 power	Channel 9 TX1 power
6Ah	Channel 12 TX1 power	Channel 11 TX1 power
6Ch	Channel 14 TX1 power	Channel 13 TX1 power

3.15 Tx Power delta TSSI Boundary (6Eh ~ 76h)

Driver compares current TSSI value (from BBP R49) with this TSSI reference value as a base to decide if real-time TX power compensation is required. 0xFF will be treated as invalid value. This function is controlled by ‘TXALC’ bit in NIC configuration1 bit1.

3.16 Tx ALC step value for 2.4 band (77h)

Delta value for Tx Power step up/down(1 step=1dBm) auto-calibration.
Driver reads this value as delta value when doing real-time TX calibration. 0xFF will be treated as invalid value. This function controlled by ‘TXALC’ bit in NIC configuration1 bit1.

3.17 TX rate power configuration (DEh~EFh)

The default value=0x66, Bit [3:0] for TX0 power setting, Bit [7:4] for TX1 power setting.
The 1 step=1dBm.

Offset	Default Value	Description	Bit [7:4]	Bit [3:0]
DEh	66	TX power for CCK 1M/2M	TX1 power setting	TX0 power setting
DFh	66	TX power for CCK 5.5M/11M	TX1 power setting	TX0 power setting
E0h	66	TX power for OFDM 6M/9M	TX1 power setting	TX0 power setting
E1h	66	TX power for OFDM 12M/18M	TX1 power setting	TX0 power setting
E2h	66	TX power for OFDM 24M/36M	TX1 power setting	TX0 power setting
E3h	66	TX power for OFDM 48M/54M	TX1 power setting	TX0 power setting
E4h	66	TX power for HT MCS=0,1	TX1 power setting	TX0 power setting
E5h	666	TX power for HT MCS=2,3	TX1 power setting	TX0 power setting
E6h	66	TX power for HT MCS=4,5	TX1 power setting	TX0 power setting
E7h	66	TX power for HT MCS=6,7	TX1 power setting	TX0 power setting
E8h	66	TX power for HT MCS=8,9	TX1 power setting	TX0 power setting
E9h	66	TX power for HT MCS=10,11	TX1 power setting	TX0 power setting
EAh	66	TX power for HT MCS=12,13	TX1 power setting	TX0 power setting
EBh	66	TX power for HT MCS=14,15	TX1 power setting	TX0 power setting
ECh	66	TX power for STBC MCS=0,1	TX1 power setting	TX0 power setting
EDh	66	TX power for STBC MCS=2,3	TX1 power setting	TX0 power setting
EEh	66	TX power for STBC MCS=4,5	TX1 power setting	TX0 power setting
EFh	66	TX power for STBC MCS=6,7	TX1 power setting	TX0 power setting

Example:
If the calibrated TX0 & TX1 power =15dBm for MCS14&15=0x66 (offset=EBh).
Want to set both TX0 & TX1 power to 19dBm for MCS 0&1 (offset=E4h).
The power difference is 4dBm (19-15). It need to increase register value from 6 to A (4dBm= 4 step).
i.e. setting E4h=0xAAh can meet the power requirement.

3.18 Serial Number for Customer (110h ~ 117h)