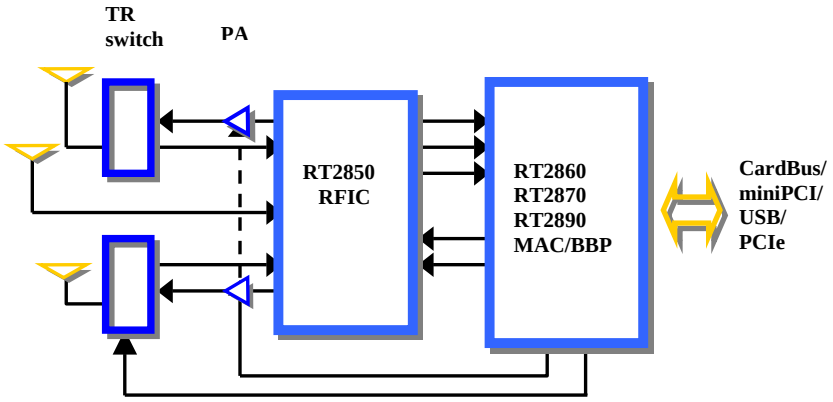
RT2860 802.11n MAC/BBP 2T3R Preliminary Data Sheet

Product Description

The RT2800 dual band MIMO 2T3R chipset for PCI consists of two highly integrated ICs (RT2860 and RT2850) that fully comply with IEEE 802.11n draft 2.0 and IEEE 802.11 a/b/g standards and operate in 2.4GHz or 5GHz bands. The chipset delivers reliable, cost-effective, feature rich wireless connectivity at high throughput from an extended distance. Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators without overloading the host processor. The RT2800 is designed to support standard based features in the areas of security, quality of service and international regulation, giving end users the greatest performance anytime in any circumstance.



RT2860 MAC/BBP Features

RT2860 is the MAC/BBP IC for Ralink RT2800 chipset for PCI. It supports 2T3R MIMO architecture with fully forward compatible with IEEE 802.11n standard. RT2800 is also backward compatible with the 802.11 a/b/g standard.

- 1x1/1x2/1x3/2x1/2x2/2x3 modes
- STBC Support for Extended Range
- 300MHz PHY Rate Support
- Legacy and High Throughput Modes
- 20MHz/40MHz bandwidth
- Reverse Direction Data Flow and Frame Aggregation
- WEP 64/128, WPA, WPA2 Support
- QoS – WMM, WMM-PS
- Wake on Wireless LAN
- Multiple BSSID Support
- CardBus / Mini PCI / PCI
- International Regulation - 802.11d + h
- Cisco CCX V1.0 V2.0 V3.0 Compliance
- Bluetooth Co-existence
- Low Power with Advanced Power Management
- Operating Systems - Windows XP, 2000, ME, 98SE, Vista, Linux, MAC
- 16mm x 16mm TQFP-144 Package 3.3V/1.2V, 3/5V PCI I/O

Order Information

Part Number	Temp Range	Package
RT2860T	-10~85 ^{0}C	Lead free/ RoHS Compliant 144 TQFP

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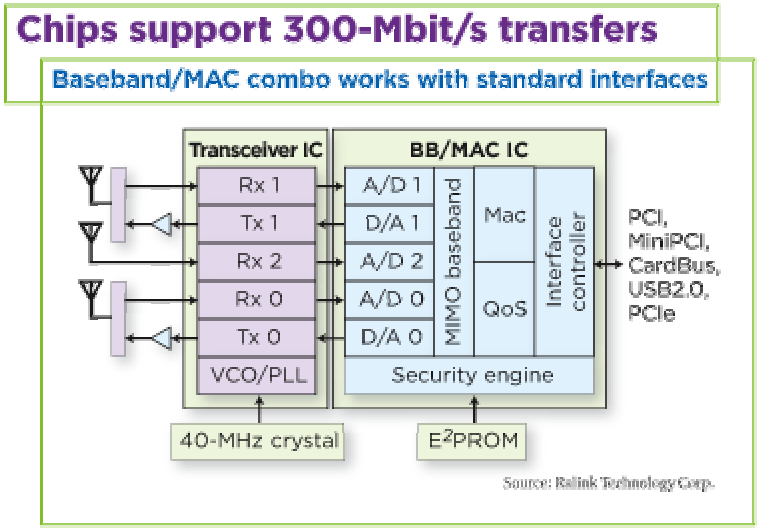
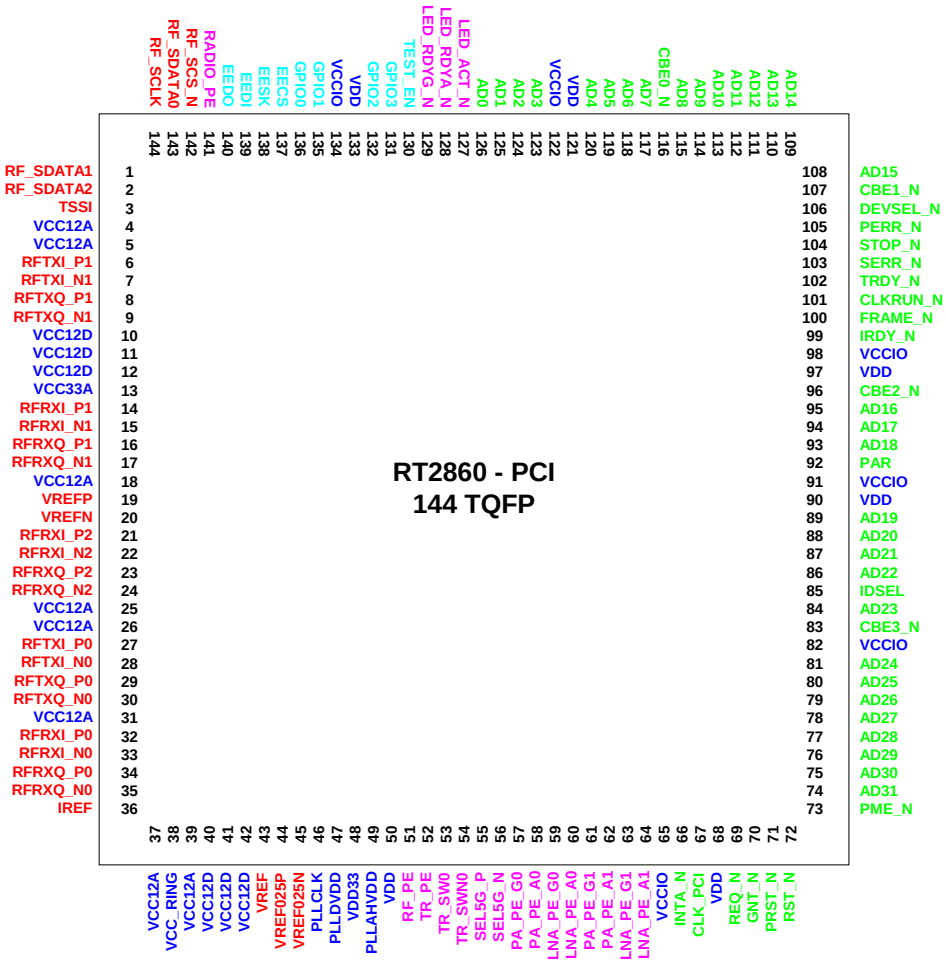
Block Diagram



RT2860 includes two DACs and three ADCs to support two transmit and three receive chains. After analog to digital conversion is the MIMO baseband processor that conducts effective space-timing OFDM processing up to two streams. MAC includes standard aggregation, and security modes defined in 802.11n draft spec. RT2860 supports PCI, miniPCI and Cardbus interfaces.

Pin Layout


RT2860 - PCI
144 TQFP
1 RF_SDATA1
2 RF_SDATA2
3 TSSI
4 VCC12A
5 VCC12A
6 RFTXI_P1
7 RFTXI_N1
8 RFTXQ_P1
9 RFTXQ_N1
10 VCC12D
11 VCC12D
12 VCC12D
13 VCC33A
14 RFRXI_P1
15 RFRXI_N1
16 RFRXQ_P1
17 RFRXQ_N1
18 VCC12A
19 VREFP
20 VREFN
21 RFRXI_P2
22 RFRXI_N2
23 RFRXQ_P2
24 RFRXQ_N2
25 VCC12A
26 VCC12A
27 RFTXI_P0
28 RFTXI_N0
29 RFTXQ_P0
30 RFTXQ_N0
31 VCC12A
32 RFRXI_P0
33 RFRXI_N0
34 RFRXQ_P0
35 RFRXQ_N0
36 IREF
37 VCC12A
38 VCC_RING
39 VCC12A
40 VCC12D
41 VCC12D
42 VCC12D
43 VREF
44 VREF025P
45 VREF025N
46 PLLCLK
47 PLLDVDD
48 VDD33
49 PLLAHVDD
50 VDD
51 RF_PE
52 TR_PE
53 TR_SW0
54 TR_SWN0
55 SEL5G_P
56 SEL5G_N
57 PA_PE_G0
58 PA_PE_A0
59 LNA_PE_G0
60 LNA_PE_A0
61 PA_PE_G1
62 PA_PE_A1
63 LNA_PE_G1
64 LNA_PE_A1
65 VCCIO
66 INTA_N
67 CLK_PCI
68 VDD
69 REQ_N
70 GNT_N
71 PRST_N
72 RST_N
73 PME_N
74 AD31
75 AD30
76 AD29
77 AD28
78 AD27
79 AD26
80 AD25
81 AD24
82 VCCIO
83 CBE3_N
84 AD23
85 IDSEL
86 AD22
87 AD21
88 AD20
89 AD19
90 VDD
91 VCCIO
92 PAR
93 AD18
94 AD17
95 AD16
96 CBE2_N
97 VDD
98 VCCIO
99 IRDY_N
100 FRAME_N
101 CLKRUN_N
102 TRDY_N
103 SERR_N
104 STOP_N
105 PERR_N
106 DEVSEL_N
107 CBE1_N
108 AD15
109 AD14
110 AD13
111 AD12
112 AD11
113 AD10
114 AD9
115 AD8
116 CBE0_N
117 AD7
118 AD6
119 AD5
120 AD4
121 VDD
122 VCCIO
123 AD3
124 AD2
125 AD1
126 AD0
127 LED_ACT_N
128 LED_RDYA_N
129 LED_RDYG_N
130 TEST_EN
131 GPIO3
132 GPIO2
133 VDD
134 VCCIO
135 GPIO1
136 GPIO0
137 EECS
138 EESK
139 EEDI
140 EEDO
141 RADIO_PE
142 RF_SCS_N
143 RF_SDATA0
144 RF_SCLK

Pin Description

Pin	Name	I/O/P	Description
Analog controlled RF interface: 32 pins			
6	RFTXI_P1	O	Positive signal of TX I differential output from DAC1
7	RFTXI_N1	O	Negative signal of TX I differential output from DAC1
8	RFTXQ_P1	O	Positive signal of TX Q differential output from DAC1
9	RFTXQ_N1	O	Negative signal of TX Q differential output from DAC1
14	RFRXI_P1	I	Positive signal of RX I differential input to ADC1
15	RFRXI_N1	I	Negative signal of RX I differential input to ADC1
16	RFRXQ_P1	I	Positive signal of RX Q differential input to ADC1
17	RFRXQ_N1	I	Negative signal of RX Q differential input to ADC1
19	VREFP	O	Reference voltage output point P for external bypass cap
20	VREFN	O	Reference voltage output point N for external bypass cap
21	RFRXI_P2	I	Positive signal of RX I differential input to ADC2
22	RFRXI_N2	I	Negative signal of RX I differential input to ADC2
23	RFRXQ_P2	I	Positive signal of RX Q differential input to ADC2
24	RFRXQ_N2	I	Negative signal of RX Q differential input to ADC2
27	RFTXI_P0	O	Positive signal of TX I differential output from 10bit DAC0
28	RFTXI_N0	O	Negative signal of TX I differential output from DAC0
29	RFTXQ_P0	O	Positive signal of TX Q differential output from DAC0
30	RFTXQ_N0	O	Negative signal of TX Q differential output from DAC0
32	RFRXI_P0	I	Positive signal of RX I differential input to ADC0
33	RFRXI_N0	I	Negative signal of RX I differential input to ADC0
34	RFRXQ_P0	I	Positive signal of RX Q differential input to ADC0
35	RFRXQ_N0	I	Negative signal of RX Q differential input to ADC0
36	IREF	I	Reference current input to ADC/DAC
43	VREF	O	Reference voltage output for external bypass cap
44	VREF025P	O	Reference voltage output point ¼ P for external bypass cap
45	VREF025N	O	Reference voltage output point ¼ N for external bypass cap
142	RF_SCS_N	O	RF channels RPI interface selection, active low
143	RF_SDATA0	O	RF channel 0 RPI interface data.
144	RF_SCLK	O	RF RPI interface clock for all RF channels
1	RF_SDATA1	O	RF channel 1 RPI interface data.
2	RF_SDATA2	O	RF channel 2 RPI interface data.
3	TSSI	I	TSSI input to ADC
Analog power pins: 16 pins			
13	VCC33A	P	3.3V analog power supply
38	VCC_RING	P	3.3V analog power supply
4,5,18,25,26, 31,37,39	VCC12A	P	1.2V analog power supply

Pin	Name	I/O/P	Description
10,11,12,40, 41,42	VCC12D	P	1.2V digital power supply
PLL interface: 4 pins			
46	PLLCLK	I	40MHz clock for internal PLL.
47	PLLDVDD	P	1.2V digital power supply to PLL
48	VDD33	P	3.3V digital power supply to PLL
49	PLLAHVDD	P	3.3V analog power supply to PLL
Digital controlled RF interface: 15 pins			
51	RF_PE	O	RX and TX enable control for RF transceiver.
52	TR_PE	O	RX and TX enable control for RF transceiver.
53	TR_SW0	O	Positive signal of RX and TX switching control
54	TR_SWN0	O	Negative signal of RX and TX switching control
55	SEL5G_P	O	Positive signal of band select for 5GHz band
56	SEL5G_N	O	Negative signal of band select for 5GHz band
57	PA_PE_G0	O	LDO output for main path of 2.4GHz band RF power amplifier enable control
58	PA_PE_A0	O	LDO output for main path of 5GHz band RF power amplifier enable control
59	LNA_PE_G0	O	External LNA control for main path of 2.4GHz band.
60	LNA_PE_A0	O	External LNA control for main path of 5GHz band.
61	PA_PE_G1	O	LDO output for the other paths of 2.4GHz band RF power amplifier enable control
62	PA_PE_A1	O	LDO output for the other paths of 5GHz band RF power amplifier enable control
63	LNA_PE_G1	O	External LNA control for the other paths of 2.4GHz band.
64	LNA_PE_A1	O	External LNA control for the other paths of 5GHz band.
141	RADIO_PE	O	Radio power off
PCI: 53 pins			
66	INTA_N	O	PCI interrupt
67	CLK_PCI	I	PCI clock
69	REQ_N	O	PCI bus request
70	GNT_N	I	PCI bus granted
71	PRST_N	I	Power On reset
72	RST_N	I	PCI reset
73	PME_N	O	Power management event
74	AD31	I/O	PCI address and data
75	AD30	I/O	PCI address and data
76	AD29	I/O	PCI address and data
77	AD28	I/O	PCI address and data
78	AD27	I/O	PCI address and data
79	AD26	I/O	PCI address and data
80	AD25	I/O	PCI address and data
81	AD24	I/O	PCI address and data
83	CBE3_N	I/O	PCI bus command and byte enable
84	AD23	I/O	PCI address and data
85	IDSEL	I	PCI initialization device select
86	AD22	I/O	PCI address and data
87	AD21	I/O	PCI address and data

Pin	Name	I/O/P	Description
88	AD20	I/O	PCI address and data
89	AD19	I/O	PCI address and data
92	PAR	I/O	PCI parity
93	AD18	I/O	PCI address and data
94	AD17	I/O	PCI address and data
95	AD16	I/O	PCI address and data
96	CBE2_N	I/O	PCI bus command and byte enable
99	IRDY_N	I/O	PCI initiator ready
100	FRAME_N	I/O	PCI cycle frame
101	CLKRUN_N	I/O	PCI clock running
102	TRDY_N	I/O	PCI target ready
103	SERR_N	O	PCI system error
104	STOP_N	I/O	PCI target stop
105	PERR_N	I/O	PCI parity error
106	DEVSEL_N	I/O	PCI device select
107	CBE1_N	I/O	PCI bus command and byte enable
108	AD15	I/O	PCI address and data
109	AD14	I/O	PCI address and data
110	AD13	I/O	PCI address and data
111	AD12	I/O	PCI address and data
112	AD11	I/O	PCI address and data
113	AD10	I/O	PCI address and data
114	AD9	I/O	PCI address and data
115	AD8	I/O	PCI address and data
116	CBE0_N	I/O	PCI bus command and byte enable
117	AD7	I/O	PCI address and data
118	AD6	I/O	PCI address and data
119	AD5	I/O	PCI address and data
120	AD4	I/O	PCI address and data
123	AD3	I/O	PCI address and data
124	AD2	I/O	PCI address and data
125	AD1	I/O	PCI address and data
126	AD0	I/O	PCI address and data
LED: 3 pins			
127	LED_ACT_N	O	LED flash in transmission
128	LED_RDYA_N	O	LED active while operation in 5GHz mode.
129	LED_RDYG_N	O	LED active while operation in 2.4GHz mode.
Test: 1 pin			
130	TEST_EN	I	Enable test mode. Connect to GND for normal mode.
GPIO: 4 pins			
131	GPIO3	I/O	GPIO. Default is input. Pull down to GND if not use.
132	GPIO2	I/O	GPIO. Default is input. Pull down to GND if not use.
135	GPIO1	I/O	GPIO. Default is input. Pull down to GND if not use.
136	GPIO0	I/O	GPIO. Default is input. Pull down to GND if not use.
EEPROM: 4 pins			
137	EECS	O	serial EEPROM chip select

Pin	Name	I/O/P	Description
138	EESK	O	serial EEPROM clock
139	EEDI	O	serial output to EEPROM
140	EEDO	I	serial input from EEPROM. Pull up to VCCIO.
Digital Power: 12 pins			
65,82,91,98, 122,134	VCCIO	P	3.3V digital power supply
50,68,90,97, 121,133	VDD	P	1.2V digital power supply
GND: exposed pad			
	GND	P	Ground pad
Total: 144 pins			

Absolute Maximum Ratings

Core Supply Voltage 1.32V
I/O Supply Voltage 3.6V
Input, Output or I/O Voltage.. GND –0.3V to Vcc+0.3V

Thermal Information

Thermal Resistance θ_{JA} (^{o}C/W) in free air for E-PAD TQFP (16mmx16mm) package... . . . . 19 ^{o}C/W
Maximum Junction Temperature . . . . . .125^{o}C
Maximum Storage Temperature . . . . -40^{o}C to 125^{o}C

Operating Conditions

Ambient Temperature Range . . . . . .-10 to 85^{o}C
Core Supply Voltage . . . . .1.2V +/- 10%
I/O Supply Voltage . . . . 3.3V +/- 10%

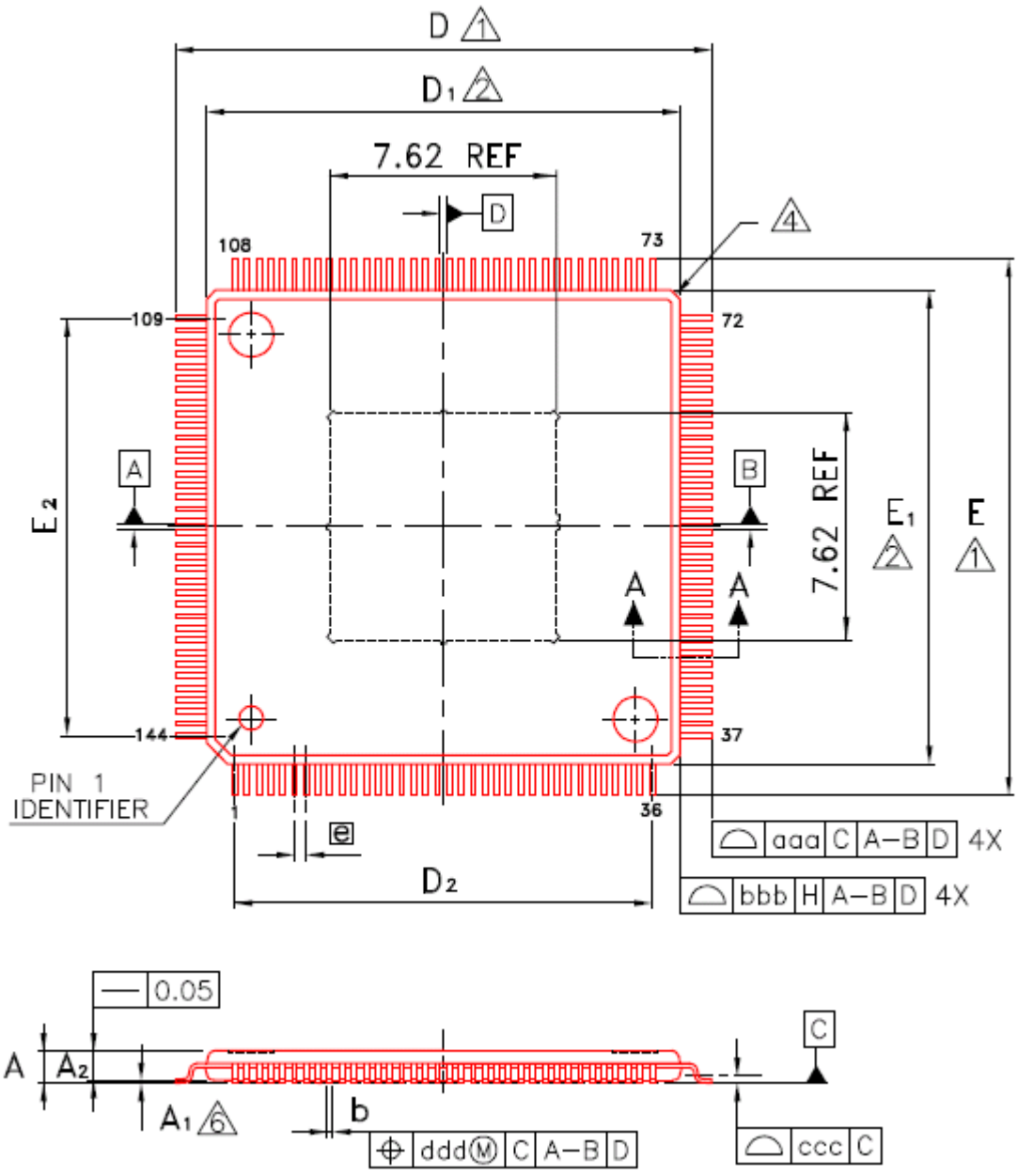
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

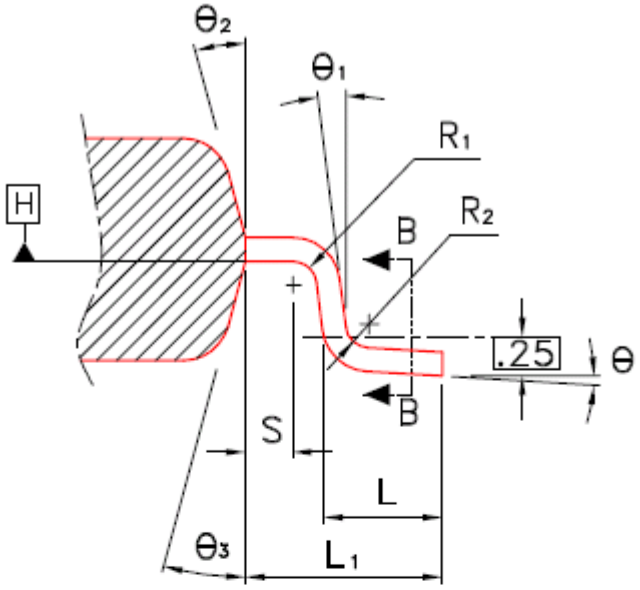
DC Electrical Characteristics

Parameters	Sym	Conditions	Min	Typ	Max	Unit
3.3V Supply Voltage	Vcc33		2.7	3.3	3.6	V
1.2V Supply Voltage	Vcc12			1.2		V
3.3V Current Consumption	Icc33			148		mA
1.2V Current Consumption	Icc12			350		mA

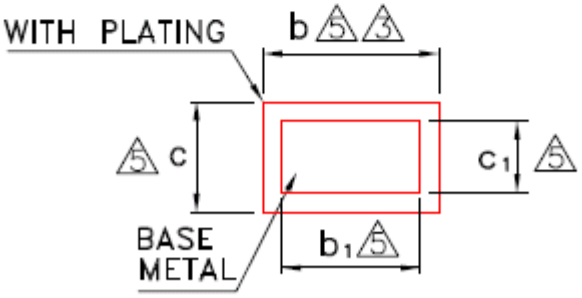
Package Information

TQFP 144 (16x16x1.0mm)





SECTION A–A



SECTION B–B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	1.00	1.10	1.20	0.039	0.043	0.047
A_1	0.05	0.10	0.15	0.002	0.004	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	18.00 BSC			0.709 BSC		
D_1	16.00 BSC			0.630 BSC		
D_2	14.00 BSC			0.551 BSC		
E	18.00 BSC			0.709 BSC		
E_1	16.00 BSC			0.630 BSC		
E_2	14.00 BSC			0.551 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		