

Application

- 802.11 b/g/n AP/Router
- Dual Band Concurrent Router

The RT3352 router-on-a-chip includes an 802.11n media access controller (MAC) and baseband, a 2.4GHz radio and FEM, a 400 MHz MIPS® 24K™ CPU core, a 5-port 10/100 switch and one RGMII. The RT3352 requires less and includes everything needed to build an AP router from a single chip. The embedded high performance CPU can process advanced applications effortlessly, such as routing, security and VoIP. The USB port can be configured to access external storage for Digital Home applications; the RT3352 also includes a wide selection of interfaces to enable many possible applications.

Features

- ◆ Embedded MIPS24KEc (400 MHz) with 32K I-Cache and 16K D-Cache
- ◆ 16/32-bit SDRAM DRAM up to 128 Mbytes
- ◆ 16/32-bit DDR2 up to 256Mbytes
- ◆ SPI Flash x2
- ◆ USB 2.0 host x2 or host/device
- ◆ 5 Ports 10/100 SW and RGMII
- ◆ I2C, I2S, SPI, PCM, UART, JTAG, MDC/MDIO/GPIO
- ◆ An optimized PMU: 3.3→1.8V SW, 1.8→1.2 LDO
- ◆ Green AP
 - Intelligent Clock Scaling (exclusive)
 - DDRII: ODT off, Self-refresh Mode
 - SDRAM: Pre-charge Power down

- NAS
- iNIC
- ◆ Hardware NAT & WAPI, SSCG, QoS, TCP/UDP/IP checksum off_loading
- ◆ 2T2R 2.4 GHz with 300Mbps PHY data rate
- ◆ Tx Power: 16dBm Rx Sensitivity: -76 dBm@54Mbps
- ◆ 20/40 MHz channel bandwidth
- ◆ Legacy 802.11b/g and High Throughput 802.11n modes
- ◆ Reverse Data Grant (RDG)
- ◆ Maximal Ratio Combining (MRC)
- ◆ 16 Multiple BSSID
- ◆ Security: WEP-64/WEP-128/TKIP/AES/WPA/WPA2/WAPI
- ◆ QoS: WMM/WMM-PS
- ◆ WPS (Wi-Fi Protected Setup) PBC, PIN
- ◆ Voice Enterprise : 802.11k+r
- ◆ Mesh Network: 802.11s
- ◆ AP Firmware: Linux 2.6.21 SDK, eCOS
- ◆ iNIC Driver: Linux 2.4/2.6

Order Information

Part Number	Temp Range	Package
RT3352F	-10~55°C	Green/ RoHS Compliant TFBGA 289 ball (14mmx14mm)

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Functional Block Diagram

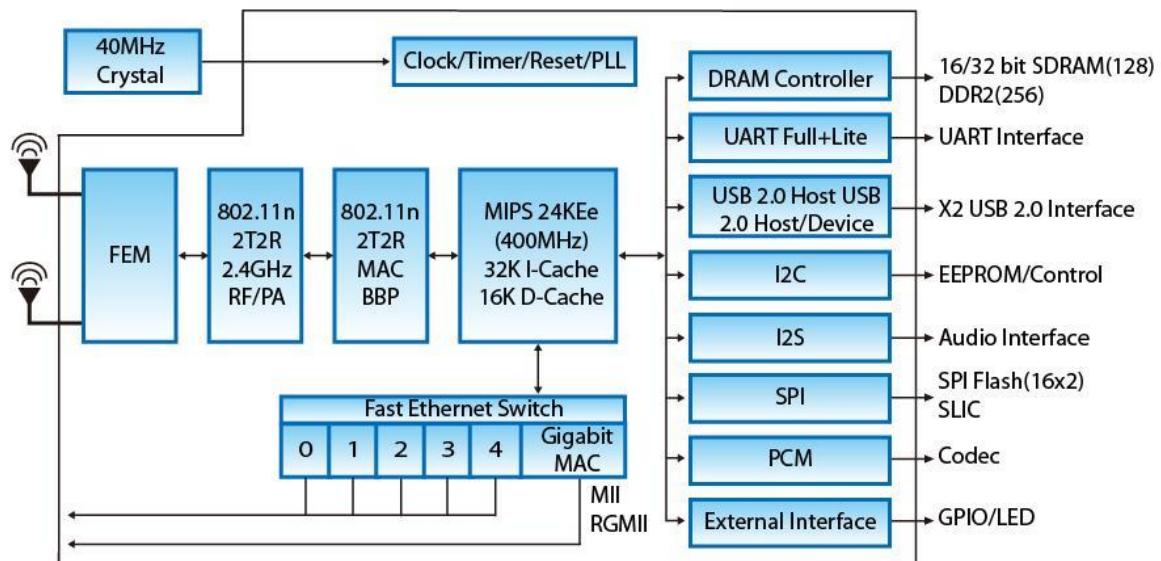


Fig. 1-1 RT3352 Functional Block Diagram

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1 Pin Description

1.1 289-Pins BGA Package Diagram

Top view (left portion)

	1	2	3	4	5	6	7	8	9
A	GND	RF0_PA_OUTN	RF0_PA_OUTP	RF0_2G_INN	RF0_2G_INP	PLL_VC_CAP	LDORF_OUT_V12	RF_BB2_V12A	ADC_V12
B	GND	RF0_PA_V33N	RF0_PA_V33P	RF0_PA1_V33A	GND	BG_V33A	LDORF_IN_VX	PLL_X2	PLL_X1
C	RF1_2G_INP	GND	RF0_V12A	RF0_IF_V12A	VCO_V12A	LDOPLL_OUT_V12	BG_RES_12K	BASE_TRX_IP	BASE_TRX_IN
D	RF1_2G_INN	RF1_PA_V33A	GND	GND	PLL_V12A	RF_BB1_V12A	RF_TSSI_IN	BASE_TRX_QP	BASE_TRX_QN
E	RF1_PA_OUTP	RF1_PA_V33P	RF1_IF_V12A	GND	GND	GND	GND	GND	GND
F	RF1_PA_OUTN	RF1_PA_V33N	RF1_V12A	GND	GND	GND	GND	GND	GND
G	GND	RF1_TX_V12A	GND	GND	GND	GND	GND	GND	GND
H	VIN_1P5	VFB_1P2	MDC	GE1_RXD0	GND	GND	GND	GND	GND
J	VOUT_1P2	FB	MDIO	GE1_RXDV	GND	GND	GND	GND	GND
K	EXT_LDO_1P8	COMP	GE1_RXD1	GE1_RXCLK	GND	GND	GND	GND	GND
L	DCDC_V33A	OUT_FB_1P8	GE1_RXD2	GE1_RXD3	SOC_CO_V12D	GND	GND	GND	GND
M	DCDC_V33D	EXT_LDO_1P5	GE1_TXD2	GE1_TXD3	SOC_CO_V12D	GND	GND	GND	GND
N	LGATE	UGATE	GE1_TXD1	GE1_TXCLK	SOC_IO_V33D	GND	GND	DDR_IO_V33D	DDR_IO_V33D
P	DIS_SW	GND	GE1_TXD0	GE1_TXEN	EPHY_V33A	EPHY_V33A	EPHY_V33A	MD31	MDQS3
R	EPHY_REF_RES	EPHY_TXP_P1	EPHY_TXN_P1	EPHY_RXN_P2	EPHY_RXP_P2	EPHY_RXP_P3	EPHY_RXN_P3	MD30	MD27
T	EPHY_RXN_P0	EPHY_TXN_P0	EPHY_RXN_P1	EPHY_TXN_P2	EPHY_TXN_P3	EPHY_RXN_P4	EPHY_TXN_P4	MD29	MDQM3
U	EPHY_RXP_P0	EPHY_TXP_P0	EPHY_RXP_P1	EPHY_TXP_P2	EPHY_TXP_P3	EPHY_RXP_P4	EPHY_TXP_P4	MD28	MD25

Top view (right portion)

	10	11	12	13	14	15	16	17
A	LNA_PE_G1	ANT_TRNB	EPHY_LED1_N	JTAG_TMS	SPI_MISO	SPI_CS0	TXD	RTS_N
B	LNA_PE_G0	ANT_TRN	EPHY_LED0_N	JTAG_TCLK	SPI莫斯	SPI_CLK	DTR_N	DCD_N
C	PA_PE_G1	EPHY_LED4_N	GPIO0	JTAG_TRST_N	SPI_CS1	DSR_N	CTS_N	UPHY1_PADP
D	PA_PE_G0	EPHY_LED3_N	JTAG_TDO	WLAN_LED_N	RIN	RXD	UPHY1_ID	UPHY1_PADM
E	PLL_AVDD_V12A	EPHY_LED2_N	JTAG_TDI	PORST_N	UPHY_VDDL_V12D	UPHY1_VBUS	UPHY1_VRES	UPHY0_PADP
F	PLL_DVDD_V12D	GND	GND	SOC_IO_V33D	UPHY_VDDA_V33A	UPHY0_VBUS	UPHY0_VRES	UPHY0_PADM
G	GND	GND	GND	SOC_IO_V33D	UPHY0_ID	RXD2	TXD2	I2C_SCLK
H	GND	GND	SOC_CO_V12D	SOC_CO_V12D	I2C_SD	MD0	MD1	MD2
J	GND	GND	DDR_IOC_V12D	DDR_IOC_V12D	MD3	MDQM0	MDQS0	MD6
K	GND	GND	DDR_IO_V33D	DDR_IO_V33D	MD8	MD7	MD5	MD4
L	GND	GND	DDR_IOL_V33D	DDR_IOL_V33D	MD13	MD10	MD11	MD9
M	GND	DDR_IO_V33D	DDR_IOR_V09D	MD15	MD12	MD14	MDQS1	MDQM1
N	DDR_IO_V33D	DDR_IO_V33D	DDR_IOR_V09D	MA0	MA3	MA8	MA10	MA13
P	MD22	MDQM2	MD16	MODT	MA6	MA4	MA5	MA12
R	MD23	MDQS2	MD17	MCKE	MCAS_N	MA2	MA7	MA11
T	MD24	MD20	MD18	MCK_N	MRAS_N	MBA0	MA1	MA9
U	MD26	MD21	MD19	MCK_P	MWE_N	MBA1	MBA2	MCS_N

1.2 Pin Description

Pin	Name	I/O/IPU/IPD	Driving	Description
JTAG				
C13	JTAG_TRST_N	I, IPU	4mA	JTAG TRST (active low)
B13	JTAG_TCLK	I, IPD	4mA	JTAG TCLK
A13	JTAG_TMS	I, IPD	4mA	JTAG TMS
E12	JTAG_TDI	I, IPD	4mA	JTAG TDI
D12	JTAG_TDO	O, IPD	4mA	JTAG TDO
UART Lite				
G15	RXD2	I, IPD	4mA	UART Lite RXD
G16	TXD2	O, IPD	4mA	UART Lite TXD
UART Full				
D15	RXD	I, IPD	4mA	UART RXD.
D14	RIN	I, IPD	4mA	UART RIN.
C16	CTS_N	I, IPD	4mA	UART CTS_N.
C15	DSR_N	I, IPD	4mA	UART DSR_N.
B17	DCD_N	I, IPD	4mA	UART DCD_N.
A16	TXD	O, IPD	4mA	UART TXD.
B16	DTR_N	O, IPD	4mA	UART DTR.
A17	RTS_N	O, IPD	4mA	UART RTS.
SPI/EEPROM				
A14	SPI_MISO	I, IPD	4mA	SPI master in slave out
B14	SPI莫斯	O, IPD	4mA	SPI master out slave in
B15	SPI_CLK	O, IPD	4mA	SPI clock
A15	SPI_CS0	O, IPD	4mA	SPI chip select0
C14	SPI_CS1	O, IPD	4mA	SPI chip select1
I2C				
G17	I2C_SCLK	I/O, IPU	4mA	I2C Clock
H14	I2C_SD	O, IPU	4mA	I2C Data
RGMII/MII (3.3v)				
K4	GE1_RXCLK	I/O, IPD	8mA	RGMII1 /GMII RX Clock
J4	GE1_RXDV	I, IPD	8mA	RGMII1 /GMII RX Data Valid
H4	GE1_RXD0	I, IPD	8mA	RGMII1 RX Data bit #0/GMII RX Data bit #0
K3	GE1_RXD1	I, IPD	8mA	RGMII1 RX Data bit #1/GMII RX Data bit #1
L3	GE1_RXD2	I, IPD	8mA	RGMII1 RX Data bit #2/GMII RX Data bit #2
L4	GE1_RXD3	I, IPD	8mA	RGMII1 RX Data bit #3/GMII RX Data bit #3
N4	GE1_TXCLK	I/O, IPD	12mA	RGMII1 /GMII TX Clock
P4	GE1_TXEN	O, IPD	12mA	RGMII1 /GMII TX Data Valid
P3	GE1_TXD0	O, IPD	12mA	RGMII1 TX Data bit #0/GMII TX Data bit #0
N3	GE1_TXD1	O, IPD	12mA	RGMII1 TX Data bit #1/GMII TX Data bit #1
M3	GE1_TXD2	O, IPD	12mA	RGMII1 TX Data bit #2/GMII TX Data bit #2
M4	GE1_TXD3	O, IPD	12mA	RGMII1 TX Data bit #3/GMII TX Data bit #3
PHY Management (2.5v or 3.3v)				
H3	MDC	O, IPD	8mA	PHY Management Clock. Shared with GPIO23
J3	MDIO	I/O, IPD	8mA	PHY Management Data. Shared with GPIO22
GPIO				
C12	GPIO0	I/O, IPD	8mA	GPIO0
5-Port PHY				
B12	EPHY_LED0_N	O, IPD	4mA	10/100 PHY Port #0 activity LED
A12	EPHY_LED1_N	O, IPD	4mA	10/100 PHY Port #1 activity LED

Pin	Name	I/O/IPU/IPD	Driving	Description
E11	EPHY_LED2_N	O, IPD	4mA	10/100 PHY Port #2 activity LED
D11	EPHY_LED3_N	O, IPD	4mA	10/100 PHY Port #3 activity LED
C11	EPHY_LED4_N	O, IPD	4mA	10/100 PHY Port #4 activity LED
R1	EPHY_REF_RES	A		Connect to an external resistor to provide accurate bias current
T1	EPHY_RXN_P0	I		10/100 PHY Port #0 RXN
U1	EPHY_RXP_P0	I		10/100 PHY Port #0 RXP
R2	EPHY_TXN_P0	O		10/100 PHY Port #0 TXN
T2	EPHY_TXP_P0	O		10/100 PHY Port #0 TXP
R3	EPHY_RXN_P1	I		10/100 PHY Port #1 RXN
T3	EPHY_RXP_P1	I		10/100 PHY Port #1 RXP
U3	EPHY_TXN_P1	O		10/100 PHY Port #1 TXN
U2	EPHY_TXP_P1	O		10/100 PHY Port #1 TXP
R4	EPHY_RXN_P2	I		10/100 PHY Port #2 RXN
R5	EPHY_RXP_P2	I		10/100 PHY Port #2 RXP
T4	EPHY_TXN_P2	O		10/100 PHY Port #2 TXN
U4	EPHY_TXP_P2	O		10/100 PHY Port #2 TXP
R7	EPHY_RXN_P3	I		10/100 PHY Port #3 RXN
R6	EPHY_RXP_P3	I		10/100 PHY Port #3 RXP
T5	EPHY_TXN_P3	O		10/100 PHY Port #3 TXN
R5	EPHY_TXP_P3	O		10/100 PHY Port #3 TXP
T6	EPHY_RXN_P4	I		10/100 PHY Port #4 RXN
U6	EPHY_RXP_P4	I		10/100 PHY Port #4 RXP
T7	EPHY_TXN_P4	O		10/100 PHY Port #4 TXN
U7	EPHY_TXP_P4	O		10/100 PHY Port #4 TXP
Misc				
E13	PORST_N	I, IPU	4mA	Power on reset
D13	WLAN_LED_N	O, IPD	4mA	WLAN Activity LED
B11	ANT_TRN	O, IPD	8mA	Positive signal for antenna T/R switch
A11	ANT_TRNB	O, IPD	8mA	Negative signal for antenna T/R switch
B10	LNA_PE_G0	O, IPD	16mA	External LNA0 3.3V power (50mA)
A10	LNA_PE_G1	O, IPD	16mA	External LNA1 3.3V power (50mA)
D10	PA_PE_G0	O, IPD	16mA	0~3.3V control for external PA0 (20mA)
C10	PA_PE_G1	O, IPD	16mA	0~3.3V control for external PA1 (20mA)
USB PHY (26 pads)				
F14	UPHY_VDDA_V33A	P		3.3v USB PHY analog power supply
E14	UPHY_VDDL_V12D	P		1.2v USB PHY digital power supply
F16	UPHY0_VRES	I/O		Connect to an external 8.2K Ohm resistor for band-gap reference circuit
F15	UPHY0_VBUS	I/O		USB VBUS pin; Connect to the VBUS pin of the USB connector
F17	UPHY0_PADM	I/O		USB data pin Data-
E17	UPHY0_PADP	I/O		USB data pin Data+
G14	UPHY0_ID	I/O		USB ID pin. Connect to ID pin on the Mini-type connect
E16	UPHY1_VRES	I/O		Connect to an external 8.2K Ohm resistor for band-gap reference circuit
E15	UPHY1_VBUS	I/O		USB VBUS pin; Connect to the VBUS pin of the USB connector
D17	UPHY1_PADM	I/O		USB data pin Data-
C17	UPHY1_PADP	I/O		USB data pin Data+

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Pin	Name	I/O/IPU/IPD	Driving	Description
D16	UPHY1_ID	I/O		USB ID pin. Connect to ID pin on the Mini-type connect
SDRAM/DDR2				
P8	MD31	I/O	8mA	SDRAM/DDR2 Data bit #31
R8	MD30	I/O	8mA	SDRAM/DDR2 Data bit #30
T8	MD29	I/O	8mA	SDRAM/DDR2 Data bit #29
U8	MD28	I/O	8mA	SDRAM/DDR2 Data bit #28
R9	MD27	I/O	8mA	SDRAM/DDR2 Data bit #27
U10	MD26	I/O	8mA	SDRAM/DDR2 Data bit #26
U9	MD25	I/O	8mA	SDRAM/DDR2 Data bit #25
T10	MD24	I/O	8mA	SDRAM/DDR2 Data bit #24
R10	MD23	I/O	8mA	SDRAM/DDR2 Data bit #23
P10	MD22	I/O	8mA	SDRAM/DDR2 Data bit #22
U11	MD21	I/O	8mA	SDRAM/DDR2 Data bit #21
T11	MD20	I/O	8mA	SDRAM/DDR2 Data bit #20
U12	MD19	I/O	8mA	SDRAM/DDR2 Data bit #19
T12	MD18	I/O	8mA	SDRAM/DDR2 Data bit #18
R12	MD17	I/O	8mA	SDRAM/DDR2 Data bit #17
P12	MD16	I/O	8mA	SDRAM/DDR2 Data bit #16
M13	MD15	I/O	8mA	SDRAM/DDR2 Data bit #15
M15	MD14	I/O	8mA	SDRAM/DDR2 Data bit #14
L14	MD13	I/O	8mA	SDRAM/DDR2 Data bit #13
M14	MD12	I/O	8mA	SDRAM/DDR2 Data bit #12
L16	MD11	I/O	8mA	SDRAM/DDR2 Data bit #11
L15	MD10	I/O	8mA	SDRAM/DDR2 Data bit #10
L17	MD9	I/O	8mA	SDRAM/DDR2 Data bit #9
K14	MD8	I/O	8mA	SDRAM/DDR2 Data bit #8
K15	MD7	I/O	8mA	SDRAM/DDR2 Data bit #7
J17	MD6	I/O	8mA	SDRAM/DDR2 Data bit #6
K16	MD5	I/O	8mA	SDRAM/DDR2 Data bit #5
K17	MD4	I/O	8mA	SDRAM/DDR2 Data bit #4
J14	MD3	I/O	8mA	SDRAM/DDR2 Data bit #3
H17	MD2	I/O	8mA	SDRAM/DDR2 Data bit #2
H16	MD1	I/O	8mA	SDRAM/DDR2 Data bit #1
H15	MD0	I/O	8mA	SDRAM/DDR2 Data bit #0
N17	MA13	O	8mA	DDR2 Address bit #13
P17	MA12	O	8mA	SDRAM/DDR2 Address bit #12
R17	MA11	O	8mA	SDRAM/DDR2 Address bit #11
N16	MA10	O	8mA	SDRAM/DDR2 Address bit #10
T17	MA9	O	8mA	SDRAM/DDR2 Address bit #9
N15	MA8	O	8mA	SDRAM/DDR2 Address bit #8
R16	MA7	O	8mA	SDRAM/DDR2 Address bit #7
P14	MA6	O	8mA	SDRAM/DDR2 Address bit #6
P16	MA5	O	8mA	SDRAM/DDR2 Address bit #5
P15	MA4	O	8mA	SDRAM/DDR2 Address bit #4
N14	MA3	O	8mA	SDRAM/DDR2 Address bit #3
R15	MA2	O	8mA	SDRAM/DDR2 Address bit #2
T16	MA1	O	8mA	SDRAM/DDR2 Address bit #1
N13	MA0	O	8mA	SDRAM/DDR2 Address bit #0
U16	MBA2	O	8mA	DDR2 MBA #2
U15	MBA1	O	8mA	SDRAM/DDR2 MBA #1

Pin	Name	I/O/IPU/IPD	Driving	Description
T15	MBA0	O	8mA	SDRAM/DDR2 MBA #0
T14	MRAS_N	O	8mA	SDRAM/DDR2 MRAS_N
R14	MCAS_N	O	8mA	SDRAM/DDR2 MCAS_N
U14	MWE_N	O	8mA	SDRAM/DDR2 MWE_N
U13	MCK_P	O	8mA	SDRAM MCK/DDR2 MCK_P
T13	MCK_N	O	8mA	DDR2 MCK_N
T9	MDQM3	O	8mA	SDRAM MDQM#3/DDR2 MDM#3
P11	MDQM2	O	8mA	SDRAM MDQM#2/DDR2 MDM#2
M17	MDQM1	O	8mA	SDRAM MDQM#1/DDR2 MDM#1
J15	MDQM0	O	8mA	SDRAM MDQM#0/DDR2 MDM#0
U17	MCS_N	O	8mA	SDRAM/DDR2 MCS_N
P9	MDQS3	I/O	8mA	DDR2 MDQS#3
R11	MDQS2	I/O	8mA	DDR2 MDQS#2
M16	MDQS1	I/O	8mA	DDR2 MDQS#1
J16	MDQS0	I/O	8mA	DDR2 MDQS#0
R13	MCKE	O, IPD	8mA	DDR2 MCKE
P13	ODT	O	8mA	DDR2 ODT
LDO				
P1	DIS_SW	I		SW or LDO select (default floating-->enable the SW regulator)
M1	DCDC_V33D	P		3.3v power supply only for gate driver of SW (Ipeak<200mA; Iavg<20mA)
N1	LGATE	A		Gate drive for external lower MOSFET
N2	UGATE	A		Gate drive for external upper MOSFET
J2	FB	A		SW regulator feedback voltage (0.75v) and feedback compensation network of the error amplifier.
K2	COMP	A		This pin is the error amplifier output and combination with the FB pin, to compensate the voltage-control
M2	EXT_LDO_1P5	P		Gate drive for external MOSFET or BJT
L1	DCDC_V33A	P		3.3v analog power
H2	VFB_1P2	P		1.2v regulation output feedback
K1	EXT_LDO_1P8	P		Gate drive for external BJT (Iavg<20mA)
L2	OUT_FB_1P8	P		Feedback voltage for 1.8v LDO
J1	VOUT_1P2	P		1.2v regulation output
H1	VIN_1P5	P		1.5v power input for internal MOS
PLL				
F10	PLL_DVDD_V12D	P		1.2V digital power supply to PLL
E10	PLL_AVDD_V12A	P		1..2V analog power supply to PLL
RF				
A5	RF0_2G_INP	I		2.4GHz RX0 input (positive)
A4	RF0_2G_INN	I		2.4GHz RX0 input (negative)
B4	RF0_PA1_V33A	P		3.3V Supply for RF channel 0
B3	RF0_PA_V33P	P		3.3V Supply for RF channel 0
A3	RF0_PA_OUTP	O		2.4GHz TX PA output (negative)
A2	RF0_PA_OUTN	O		2.4GHz TX0 output (negative)
B2	RF0_PA_V33N	P		3.3V Supply for RF channel 0
C4	RF0_IF_V12A	P		1.2V Supply for IF0
C4	RF0_LO_V12A	P		1.2V Supply for LO0
C3	RF0_V12A	P		1.2V Supply for RF0

Pin	Name	I/O/IPU/IPD	Driving	Description
G2	RF1_TX_V12A	P		1.2V Supply for RF TX
E3	RF1_IF_V12A	P		1.2V Supply for IF1
E3	RF1_LO_V12A	P		1.2V Supply for LO1
F3	RF1_V12A	P		1.2V Supply for RF1
C1	RF1_2G_INP	I		2.4GHz RX1 input (positive)
D1	RF1_2G_INN	I		2.4GHz RX1 input (negative)
D2	RF1_PA_V33A	P		3.3V Supply for RF channel 1
E2	RF1_PA_V33P	P		3.3V Supply for RF channel 1
E1	RF1_PA_OUTP	O		2.4GHz TX PA1 output (negative)
F1	RF1_PA_OUTN	O		2.4GHz TX1 output (negative)
F2	RF1_PA_V33N	P		3.3V Supply for RF channel 1
D7	RF_TSSI_IN	I		TX signal strength monitor input0 for 2.4G BAND (0 ~3.3V)
A9	ADC_V12	P		1.2V supply for ADC analog blocks
D9	BASE_TRX_QN	I/O		Baseband Q 20Mhz debug I/O (negative)
D8	BASE_TRX_QP	I/O		Baseband Q 20Mhz debug I/O (positive)
C9	BASE_TRX_IN	I/O		Baseband I 20Mhz debug I/O (negative)
C8	BASE_TRX_IP	I/O		Baseband I 20Mhz debug I/O (positive)
A8	RF_BB2_V12A	P		1.2V Supply for analog baseband
C7	BG_RES_12K	I/O		External reference resistor (12K ohm)
B6	BG_V33A	P		3.3V supply for band gap reference
A7	LDORF_OUT_V12	O		LDO 1.2V 200mA output for RF core
C6	LDOPLL_OUT_V12	O		LDO 1.2V 200mA output for PLL core
B7	LDORF_IN_VX	I		LDO 1.5~2V 300mA input for RF core and PLL
B9	PLL_X1	I		Crystal oscillator input
B8	PLL_X2	O		Crystal oscillator output
D5	PLL_V12A	P		1.2V Supply for PL
A6	PLL_VC_CAP	I/O		PLL external loop filter
C5	VCO_V12A	P		1.2V Supply for VCO output buffer
D6	RF_BB1_V12A	P		1.2V Supply for analog baseband
Power				
N5, G13, F13	SOC_IO_V33D	P		3.3v digital I/O power supply
L5, M5, H13, H12,	SOC_CO_V12D	P		1.2v digital core power supply
N12, M12	DDR_IOR_V09D	P		0.9v(GND) reference voltage power supply for DDR2(SDR)
L12, L13	DDR_IOL_V33D	P		1.8V(3.3V) level shifter power supply for DDR2(SDR)
N8, N9, N10, N11, M11, K12, K13	DDR_IO_V33D	P		1.8V(3.3V) I/O power supply for DDR2(SDR)
J12, J13	DDR_IOC_V12D	P		1.2v I/O core power supply for DDR2 and SDR
P5, P6, P7	EPHY_V33A	P		3.3V I/O power supply for EPHY
Ground				
A1,B1,G1,C2,P2, D3,G3,D4,E4,F4, G4,B5,E5,F5,G5, H5,J5,K5,E6,F6, G6,H6,J6,K6,L6,	GND	G		Ground pin

Pin	Name	I/O/IPU/IPD	Driving	Description
M6,N6,E7,F7,G7, H7,J7,K7,L7,M7, N7,E8,F8,G8,H8, J8,K8,L8,M8,E9, F9,G9,H9,J9,K9, L9,M9,G10,H10, J10,K10,L10,M10, F11,G11,H11,J11, K11,L11,F12,G12				
				Total:289pins

***Note:**

1. IPD means internal pull-down; IPU means internal pull-up; P means power.
2. While SPI_CS1 roles as WATCH DOG RESET, a pull-high resistance is necessary.

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1.3 Pins Sharing Scheme

Some pins are shared with GPIO to provide maximum flexibility for system designers. The RT3352 provides up to 45 GPIO pins. Users can configure SYSCFG and GPIOMODE registers in the System Control block to specify the pin function. Unless it specified explicitly, all the GPIO pins are in input mode after reset.

GPIO share scheme:

I/O Pad Group	Normal Mode	GPIO Mode
SPI_CS1	SPI_CS1	GPIO#45
SW_PHY_LED	EPHY_LED4_N	GPIO#44
	EPHY_LED3_N	GPIO#43
	EPHY_LED2_N	GPIO#42
	EPHY_LED1_N	GPIO#41
	EPHY_LED0_N	GPIO#40
PA	PA_PE_G1	GPIO#39
	PA_PE_G0	GPIO#38
LNA	LNA_PE_G1	GPIO#37
	LNA_PE_G0	GPIO#36
RGMII1	GE1_RXCLK	GPIO#35
	GE1_RXDV	GPIO#34
	GE1_RXD3	GPIO#33
	GE1_RXD2	GPIO#32
	GE1_RXD1	GPIO#31
	GE1_RXD0	GPIO#30
	GE1_TXCLK	GPIO#29
	GE1_TXEN	GPIO#28
	GE1_TXD3	GPIO#27
	GE1_TXD2	GPIO#26
	GE1_TXD1	GPIO#25
	GE1_TXD0	GPIO#24
	MDC	GPIO#23
	MDIO	GPIO#22
JTAG	JTAG_TRST_N	GPIO#21
	JTAG_TCLK	GPIO#20
	JTAG_TMS	GPIO#19
	JTAG_TDI	GPIO#18
	JTAG_TDO	GPIO#17
UARTL	RXD2	GPIO#16
	TXD2	GPIO#15
UARTF	RIN	GPIO#14
	DSR_N	GPIO#13
	DCD_N	GPIO#12
	DTR_N	GPIO#11
	RXD	GPIO#10
	CTS_N	GPIO#9
	TXD	GPIO#8
	RTS_N	GPIO#7
SPI	SPI_MISO	GPIO#6
	SPI_MOSI	GPIO#5
	SPI_CLK	GPIO#4
	SPI_CS0	GPIO#3
I2C	I2C_SCLK	GPIO#2
	I2C_SD	GPIO#1
GPIO	GPIO0	GPIO#0

UARTF pin share scheme:

Pin Name \	3'b000 UARTF	3'b001 PCM, UARTF	3'b010 PCM, I2S	3'b011 I2S UARTF	3'b100 PCM, GPIO	3'b101 GPIO, UARTF	3'b110 GPIO I2S	3'b111 GPIO
Pin Name								
RIN	RIN	PCMDTX	PCMDTX	RXD	PCMDTX	GPIO#14	GPIO#14	GPIO#14
DSR_N	DSR_N	PCMDRX	PCMDRX	CTS_N	PCMDRX	GPIO#13	GPIO#13	GPIO#13
DCD_N	DCD_N	PCMCLK	PCMCLK	TXD	PCMCLK	GPIO#12	GPIO#12	GPIO#12
DTR_N	DTR_N	PCMFS (out only)	PCMFS	RTS_N	PCMFS	GPIO#11	GPIO#11	GPIO#11
RXD	RXD	RXD	I2SSDI	I2SSDI	GPIO#10	RXD	I2SSDI	GPIO#10
CTS_N	CTS_N	CTS_N	I2SSDO	I2SSDO	GPIO#9	CTS_N	I2SSDO	GPIO#9
TXD	TXD	TXD	I2SWS	I2SWS	GPIO#8	TXD	I2SWS	GPIO#8
RTS_N	RTS_N	RTS_N	I2SCLK	I2SCLK	GPIO#7	RTS_N	I2SCLK	GPIO#7

PCM/I2S IO direction:

Pin Name \	I/O
Pin Name	
PCMDTX	O
PCMDRX	I
PCMCLK	I/O
PCMFS	I/O
I2SSDI	I
I2SSDO	O
I2SWS	I/O
I2SCLK	/O

RGMII pin share scheme:

Pin Name \	1'b0 RGMII1	1'b1 (default) GPIO
Pin Name		
GE1_RXCLK	GE1_RXCLK	GPIO#35
GE1_RXDV	GE1_RXDV	GPIO#34
GE1_RXD0~3	GE1_RXD0~3	GPIO#33~30
GE1_TXCLK	GE1_TXCLK	GPIO#29
GE1_TxDV	GE1_TxDV	GPIO#28
GE1_TxD0~3	GE1_TxD0~3	GPIO#27~24

SPI_CS1 share scheme: (SPI_CS1_MODE)

Pin Name \	2'b00	2'b01	2'b10(default)
Pin Name			
SPI_CS1	SPI_CS1	WDT_RST	GPIO#45

MDC share scheme: (REFCLK0_IS_PUT)

Pin Name \	1'b0(default)	1'b1
Pin Name		
MDC	MDC	REFCLK0_OUT

EPHY_LED pin share scheme: (EPHY_BT_GPIO_MODE)

Pin Name	2'b00 (default) EPHY_LED	2'b01 GPIO	2'b10 BT_MODE
EPHY_LED4_N	EPHY_LED4_N	GPIO#44	BT_ANT
EPHY_LED3_N	EPHY_LED3_N	GPIO#43	BT_WACT
EPHY_LED2_N	EPHY_LED2_N	GPIO#42	BT_FREQ
EPHY_LED1_N	EPHY_LED1_N	GPIO#41	BT_STAT
EPHY_LED0_N	EPHY_LED0_N	GPIO#40	BT_ACT

Notes :

1. All given GPIO are 4mA drive capable.
2. The default direction for GPIO pins are input(i.e. tri-state). Except these GPIO pins:
 - The GPIO17~21 shared with the JTAG interface. The default value for JTAG_GPIO_MODE is 0.

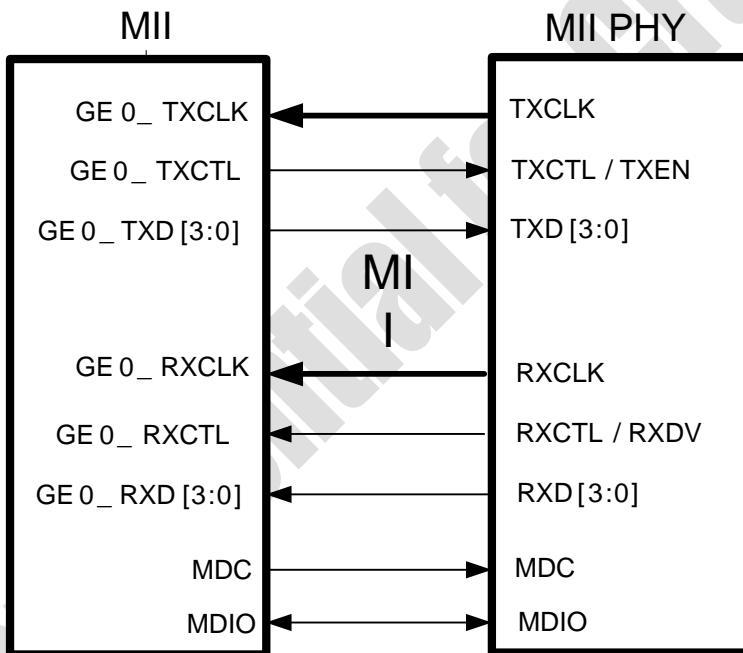


Fig. 1-3-1 MII → MII PHY

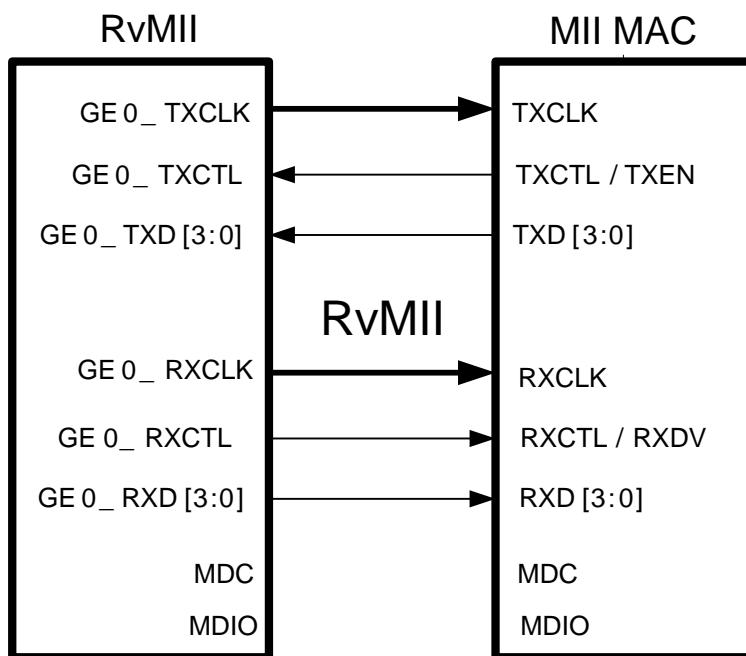


Fig. 1-3-2 RvMII → MII MAC

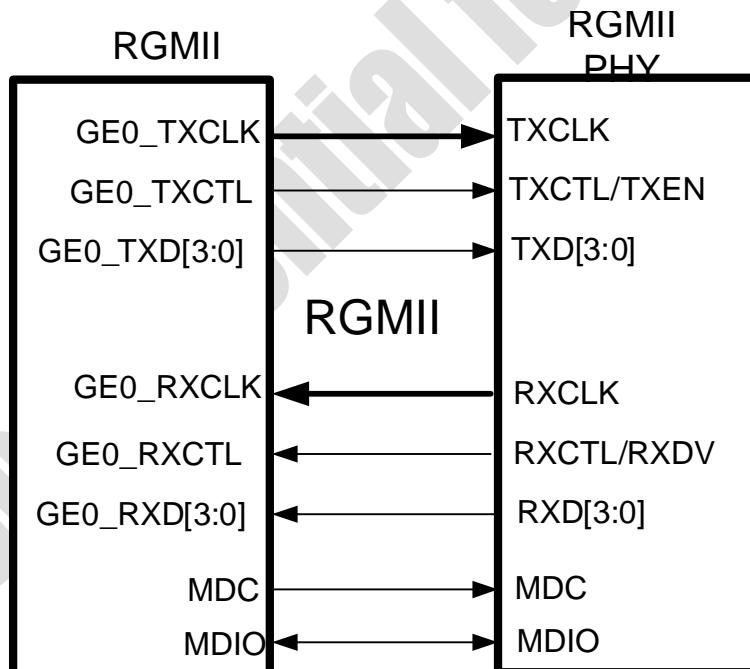


Fig. 1-3-3 RGMII → RGMII PHY

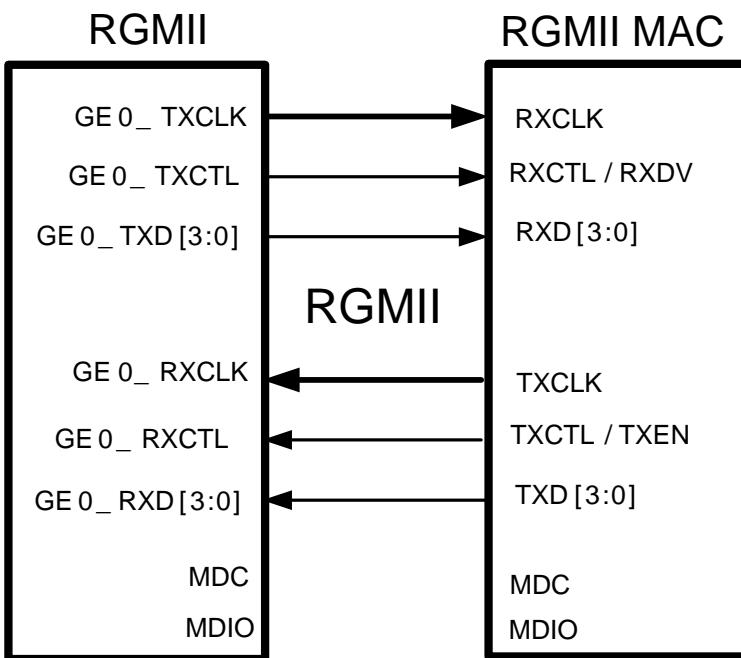


Fig. 1-3-4 RGMII → RGMII MAC

1.4 Boot strapping description

From signal pad:

Pin Name	Boot Strapping Signal Name	Description
SPI_CLK	XTAL_FREQ_HI	0: 20MHz 1: 40MHz
ANT_TRNB	BIGENDIAN	0: LITTLE ENDIAN 1: BIG ENDIAN
EPHY_LED4_N	DRAM_FROM_EE	0: DRAM configuration from boot strapping. 1: DRAM configuration(size/width) from EEPROM
MDC	DRAM_TYPE	0: SDRAM 1: DDR
WLAN_LED_N	DRAM_TOTAL_WIDTH	0: 16 1: 32
{ EPHY_LED3_N, EPHY_LDE2_N}	DRAM_SIZE (one dram cell)	INIC/AP(SDR)/AP(DDR2) 0: 2MB/8MB/32MB 1: 8MB/16MB/64MB 2: 16MB/32MB/128MB 3: 32MB/64MB/256MB
EPHY_LDE1_N	DRAM_WIDTH (one dram cell)	SDRAM(DDR2) 0: 16 (8) 1: 32 (16)
ANT_TRN	CPU_CLK_SEL	1 : 400 MHz (default) 0 : 384 MHz
{ SPI_MOSI , TXD2, TXD}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. In non-test/debug operation, 0: Normal mode (boot from SPI serial flash)(default) 1: iNIC-USB mode 2: iNIC-RGMII mode (GE1) 3: iNIC-MII mode (GE1) 4: iNIC-RVMII mode (GE1) 5: test mode 6: scan mode 7: debug mode

Note: 1. GE1 mode are defined in registers.

2. SDRAM or DDR2 memory cell used is defined in a register bit.

2 Maximum Ratings and Operating Conditions

2.1 Absolute Maximum Ratings

Supply Voltage	3.6V
Vcc to Vcc Decouple.....	-0.3 to +0.3V
Input, Output or I/O Voltage.....	GND –0.3V to Vcc+0.3V

2.2 Thermal Information

Maximum Junction Temperature (Plastic Package)	125°C
Maximum Lead Temperature (Soldering 10s).....	260°C

Thermal characteristics in still air condition

Thermal Resistance θJA (°C /W) for JEDEC 2L system PCB	59.5°C /W
Thermal Resistance θJA (°C /W) for JEDEC 4L system PCB	25.7 °C /W
Thermal Resistance θJC (°C /W) for JEDEC 2L system PCB	7.6 °C /W
Thermal Resistance θJC (°C /W) for JEDEC 4L system PCB	6.6 °C /W
Thermal Characterization parameter θJt (°C /W) for JEDEC 2L system PCB	2.2 °C /W
Thermal Characterization parameter θJt (°C /W) for JEDEC 4L system PCB	1.5 °C /W

Note: JEDEC 51-9 system FR4 PCB size: 101.5x114.5mm (4"x4.5")

2.3 Operating Conditions

Temperature Range	-10 to 55°C
Core Supply Voltage.....	1.2V +/- 5%
I/O Supply Voltage	3.3V +/- 10%

2.4 Storage Condition

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- a) Mounted within 168-hours of factory conditions < 30°C /60%RH
- b) Storage humidity needs to maintained at <10% RH
- c) Baking is necessary if customer expose the component to air over 168 hrs, baking condition: 125°C / 8hrs

2.5 External Xtal Specification

Frequency	20MHz/40MHz
Frequency offset	+/-20 ppm
VIH/VIL	Vcc-0.3V / 0.3V
Duty Cycle	45%~55%

2.6 DC Electrical Characteristics

Parameters	Sym	Conditions	Min	Typ	Max	Unit
3.3V Supply Voltage	Vcc33		3.0	3.3	3.6	V
1.2V Supply Voltage	Vcc12		1.14	1.2	1.26	V
3.3V Current Consumption	Icc33			217 mA		mA
1.5V Current Consumption	Icc15			656 mA		mA
2.0V Current Consumption	Icc20			514 mA		mA

2.7 AC Electrical Characteristics

2.7.1 SDRAM Interface

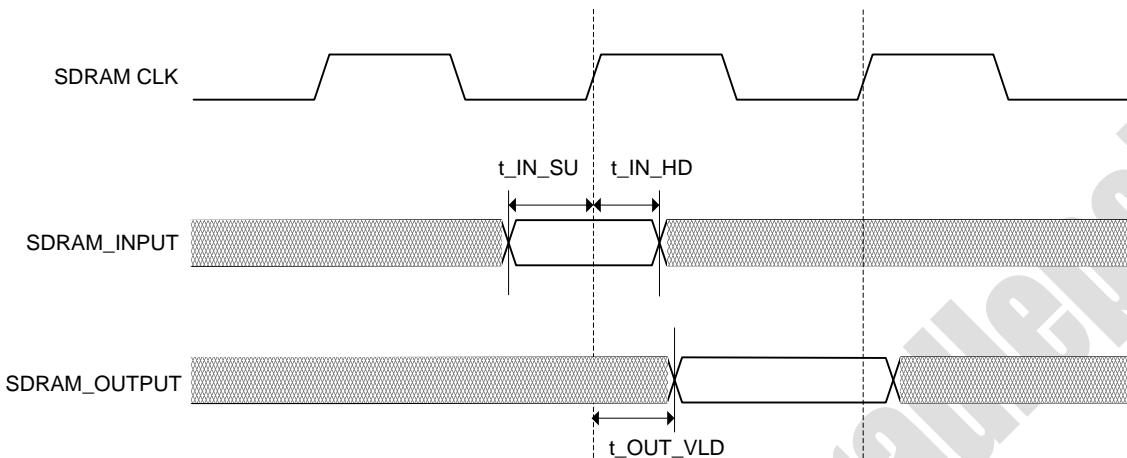


Fig. 2-7-1 SDRAM Interface

Symbol	Description	Min	Max	Unit	Remark
t_IN_SU	Setup time for Input signals (e.g. MD*)	1.5	-	ns	
t_IN_HD	Hold time for input signals	1.7	-	ns	
t_OUT_VLD	SDRAM_CLK to output signals (MA*, MD*, SDRAM_RAS_N,...) valid	0.8	5	ns	output load : 8pF

2.7.2 DDR2 SDRAM Interface

The DDR2 SDRAM interface complies with 133MHz timing requirements for standard DDR2 SDRAM. The interface drivers are SSTL_18 drivers matching the EIA/JEDEC standard JESD8-15A.

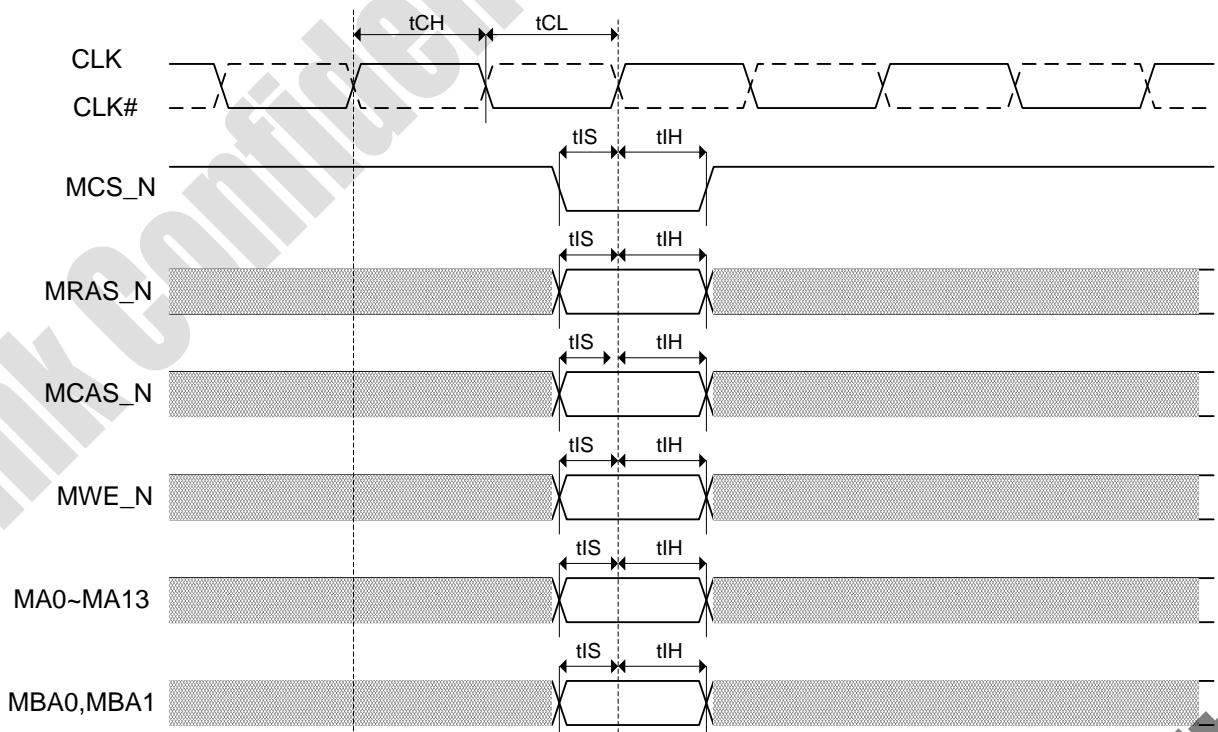


Fig. 2-7-2 DDR2 SDRAM Command

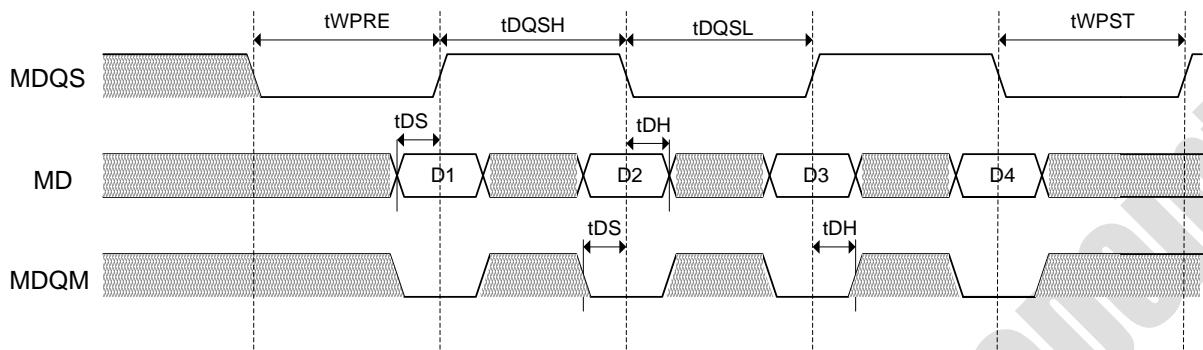


Fig. 2-7-3 DDR2 SDRAM Write data

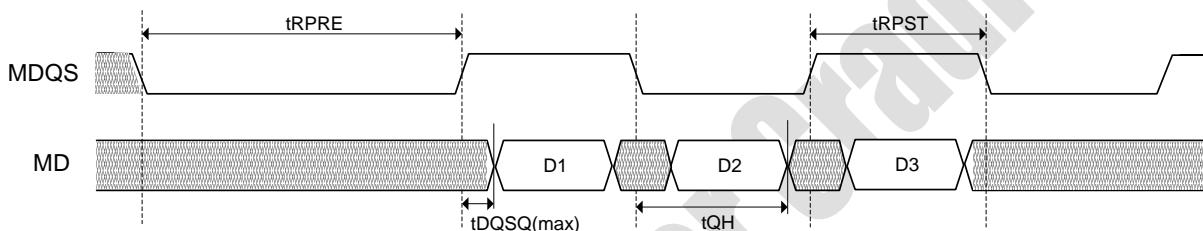


Fig. 2-7-4 DDR2 SDRAM Read data

Symbol	Description	Min	Max	Unit	Remark
tCK(avg)	Clock cycle time	7.5	-	ns	
tAC	DQ output access time from SDRAM CLK	-0.6	0.6	ns	
tDQSK	DQS output access time from SDRAM CLK	-0.6	0.6	ns	
tCH	SDRAM CLK high pulse width	0.46	0.54	tCK(avg)	
tCL	SDRAM CLK low pulse width	0.46	0.54	tCK(avg)	
tHP	SDRAM CLK half period	Min(tCH,tCL)	-	ns	
tIS	Address and control input setup time	2.0	-	ns	
tIH	Address and control input hold time	3.0	-	ns	
tDQSQ	Data skew of DQS and associated DQ	-	0.45	ns	
tQH	DQ/DQS output hold time from DQS	tHP-1.3	-	ns	
tRPRE	DQS read preamble	0.9	1.1	tCK	
tRPST	DQS read postamble	0.4	0.6	tCK	
tDQSS	DQS rising edge to CK rising edge	-0.25	0.25	tCK	
tDQSH	DQS input-high pulse width	0.35	-	tCK	
tDQL	DQS input-low pulse width	0.35	-	tCK	
tDSS	DQS falling edge to SDRAM CLK setup time	0.2	-	tCK	
tDSH	DQS falling edge hold time from SDRAM CLK	0.2	-	tCK	
tWPRE	DQS write preamble	0.35	-	tCK	
tWPST	DQS write postamble	0.4	0.6	tCK	
tDS	DQ and DQM input setup time	*0.55	-	ns	
tDH	DQ and DQM input hold time	*0.45	-	ns	

Note: 1. Depend on slew rate of DQS and DQ/DQM for single ended DQS.

2.7.3 RGMII Interface

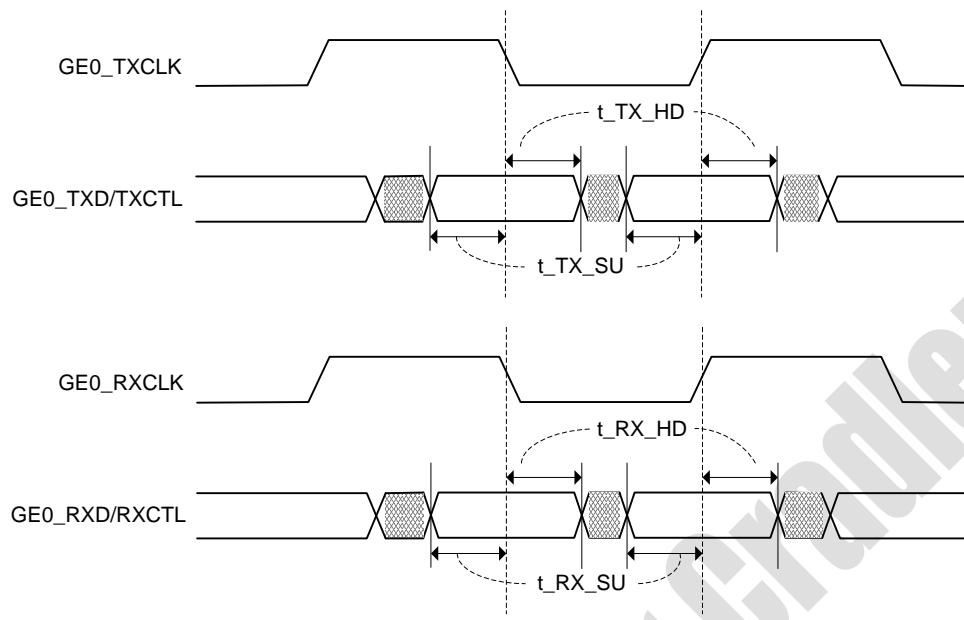
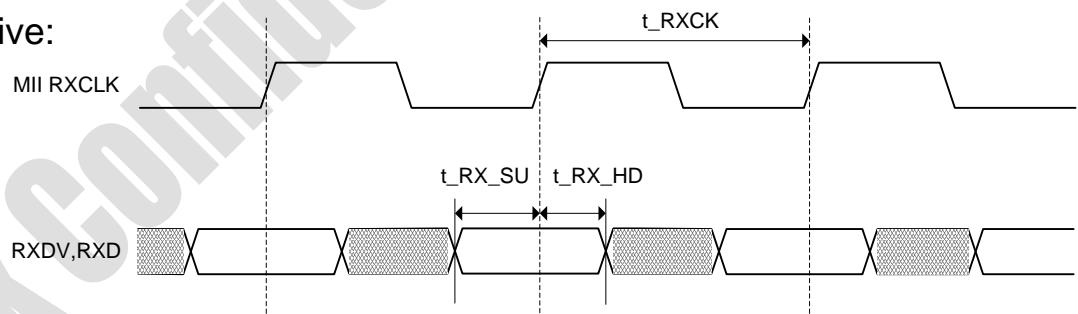


Fig. 2-7-5 RGMII Interface

Symbol	Description	Min	Max	Unit	Remark
t_TX_SU	Setup time for output signals (e.g. GE0_TXD*, GE0_TXEN)	1.2	-	ns	output load : 5pF
t_TX_HD	Hold time for output signals	1.2	-	ns	output load : 5pF
t_RX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	1.0	-	ns	
t_RX_HD	Hold time for input signals	1.0	-	ns	

2.7.4 MII Interface (25Mhz)

Receive:



Transmit:

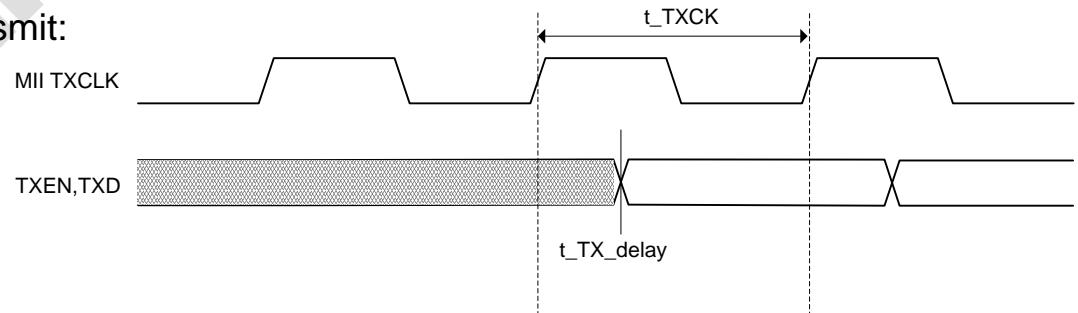


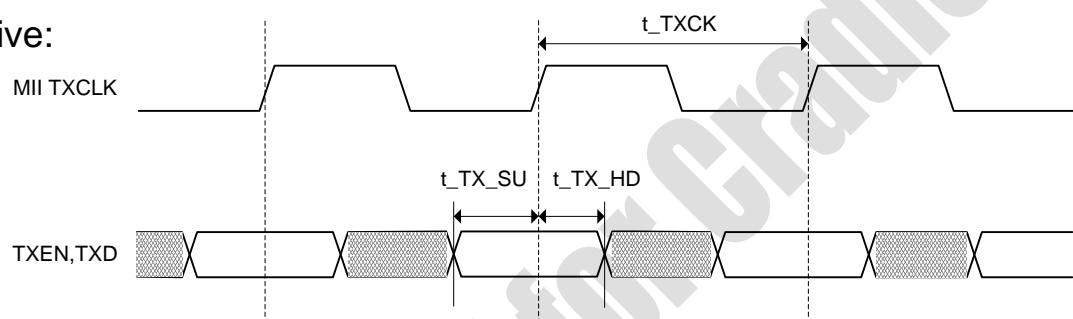
Fig. 2-7-6 MII Interface

(For 25Mhz TXCLK & RXCLK)

Symbol	Description	Min	Max	Unit	Remark
t_TX_delay	Delay to output signals (e.g. GEO_TXD*, GEO_TXEN)	6	22	ns	output load : 5pF
t_RX_SU	Setup time for input signals (e.g. GEO_RXD*, GEO_RXDV)	10	-	ns	
t_RX_HD	Hold time for input signals	5	-	ns	

2.7.5 RvMII Interface (PHY Mode MII Timing) (25Mhz)

Receive:



Transmit:

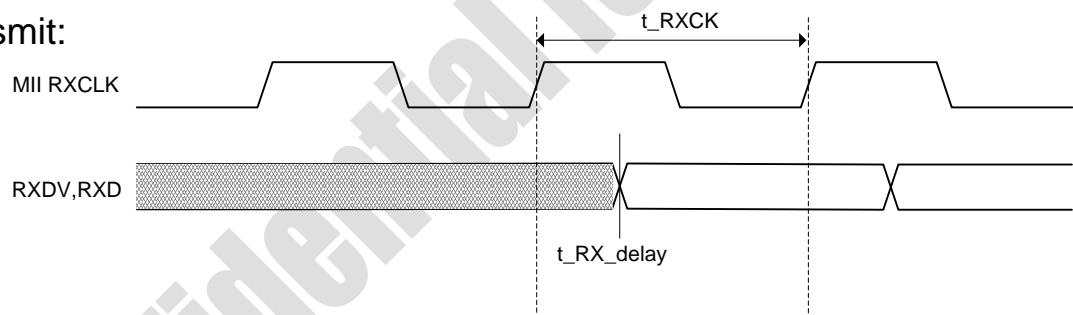
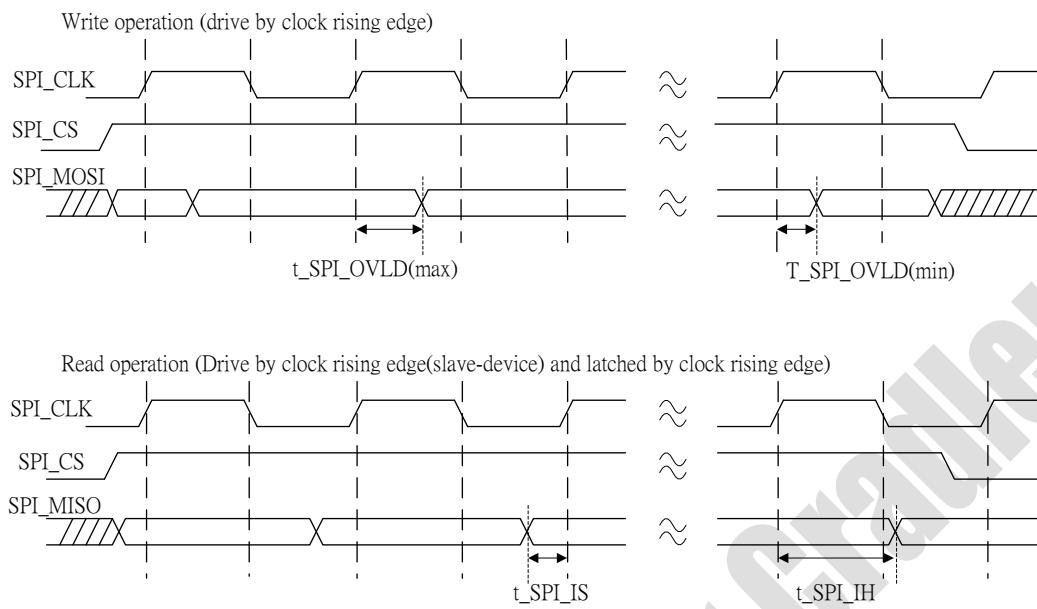


Fig. 2-7-7 RvMII Interface

(For 25Mhz TXCLK & RXCLK)

Symbol	Description	Min	Max	Unit	Remark
t_RX_delay	Delays to output signals (e.g. GEO_TXD*, GEO_TXEN)	5	25	ns	output load : 5pF
t_TX_SU	Setup time for input signals (e.g. GEO_RXD*, GEO_RXDV)	15	-	ns	
t_RX_HD	Hold time for input signals	6	-	ns	

2.7.6 SPI Interface



NOTICE: 1) SPI_CLK is gated clock.
 2) SPI_CS is controller by software

Fig. 2-7-8 SPI Interface

Symbol	Description	Min	Max	Unit	Remark
t_{SPI_IS}	Setup time for SPI input	6.0	-	ns	
t_{SPI_IH}	Hold time for SPI input	-1.0	-	ns	
t_{SPI_OVLD}	SPI_CLK to SPI output valid	-2.0	3.0	ns	output load: 5pF

2.7.7 I2S Interface

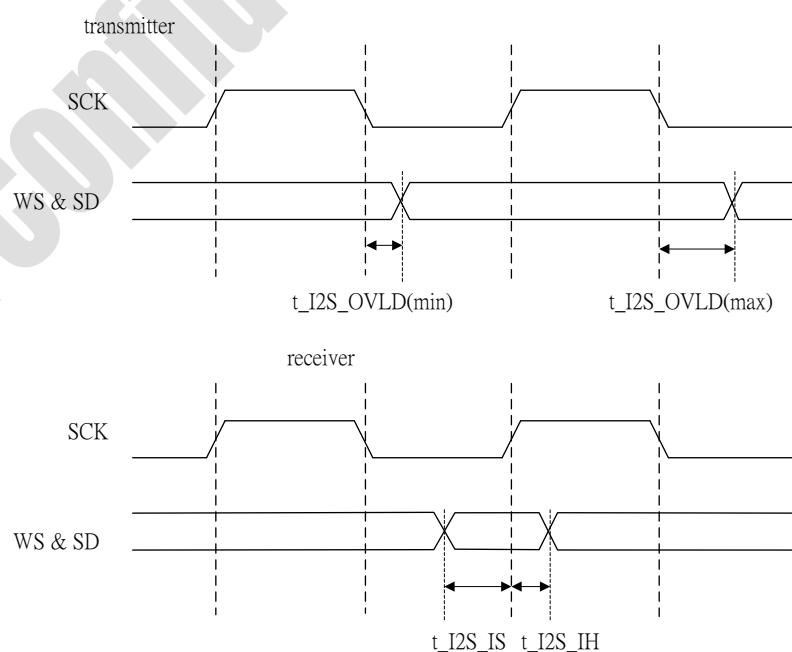


Fig. 2-7-9 I2S Interface

Symbol	Description	Min	Max	Unit	Remark
t_I2S_IS	Setup time for I2S input (data & ws)	3.5	-	ns	
t_I2S_IH	Hold time for I2S input (data & ws)	0.5	-	ns	
t_I2S_OVLD	I2S_CLK to I2S output (data & ws) valid	2.5	10.0	ns	output load: 5pF

2.7.8 PCM Interface

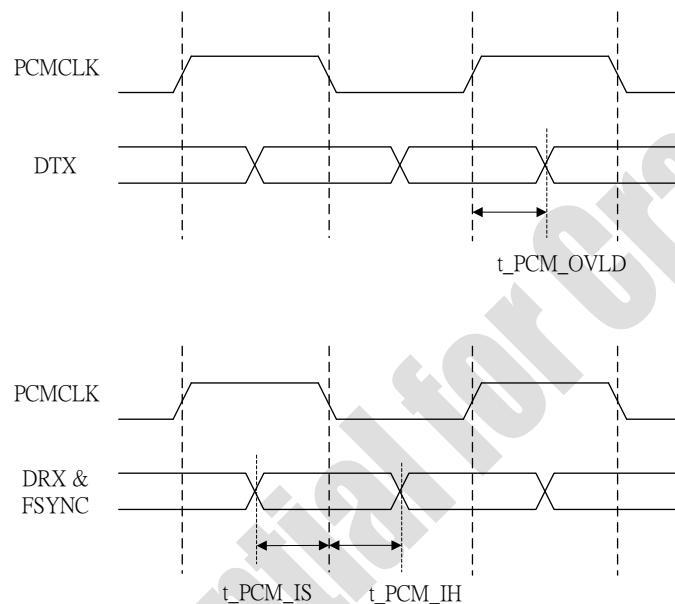


Fig. 2-7-10 PCM Interface

Symbol	Description	Min	Max	Unit	Remark
t_{PCM_IS}	Setup time for PCM input to PCM_CLK fall	3.0	-	ns	
t_{PCM_IH}	Hold time for PCM input to PCM_CLK fall	1.0	-	ns	
t_{PCM_OVLD}	PCM_CLK rise to PCM output valid	10.0	35.0	ns	output load: 5pF

2.7.9 Power On Sequence

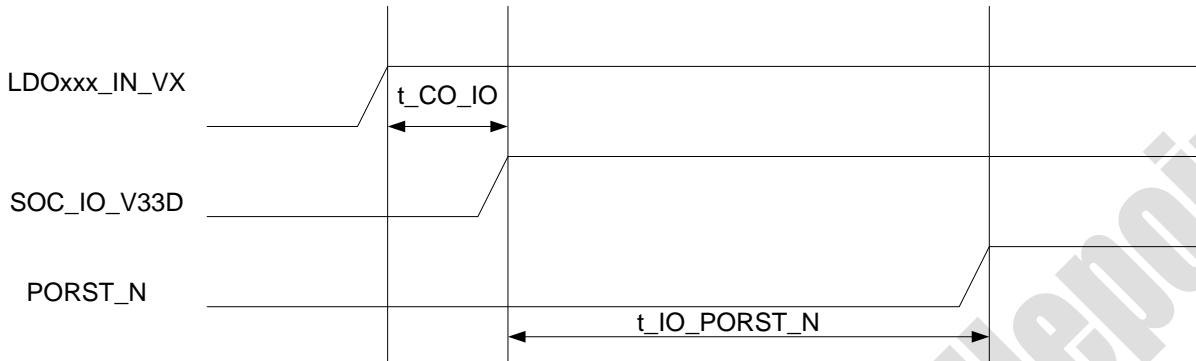


Fig. 2-7-11 Power ON Sequence

Symbol	Description	Min	Max	Unit	Remark
t_CO_IO	Time between core power on to I/O power on	0	-	ms	
t_IO_PORST_N	Time between I/O power on to PORST_N de-assertion	10	-	ms	

3 Function Description

3.1 Overview

The RT3352 SOC combines Ralink's 802.11n compliant 2T2R MAC/BBP/RF, a high performance 400/384MHz MIPS24KEc CPU core and USB host/device controller/PHY, , to enable a multitude of high performance, cost-effective 802.11n applications.

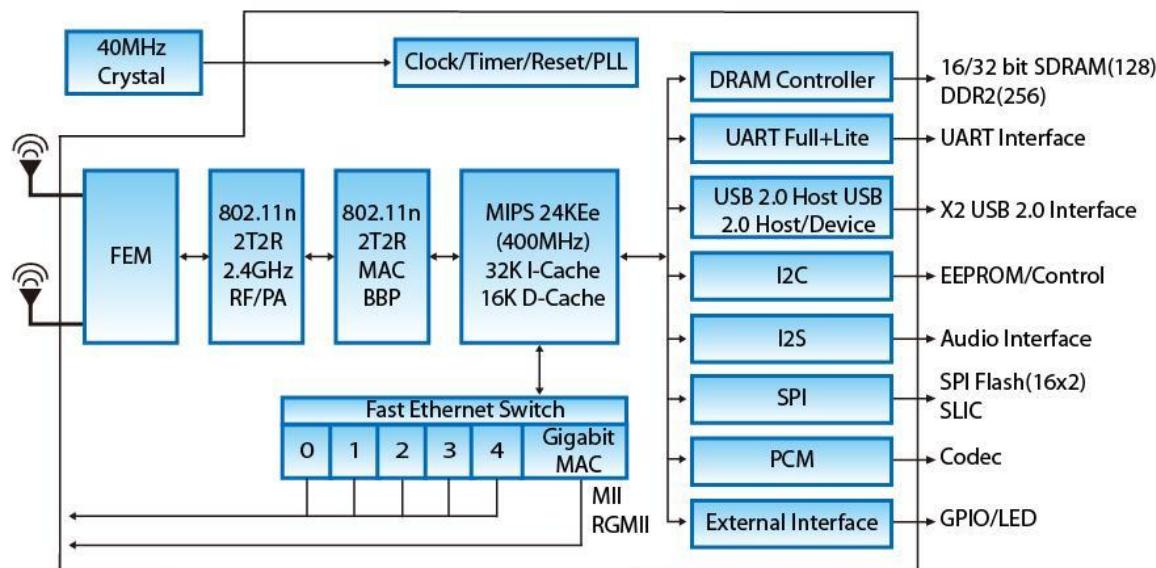


Fig. 3-1-1 RT3352 Block Diagram

There are several masters (MIPS 24K, USB , and 802.11n MAC/BBP/RF) in the RT3352 SoC on a high performance, low latency Rbus, (Ralink Bus). In addition, the RT3352 SoC supports lower speed peripherals such as UART, GPIO, and SPI via a low speed peripheral bus (Pbus).The SDRAM/DDR2 controller is the only bus slave on the Rbus. It includes an Advanced Memory Scheduler to arbitrate the requests from bus masters, enhancing the performance of memory access intensive tasks.

The RT3352 SoC embeds Ralink's market proven 802.11n 2T2R MAC/BBP/RF to provide a 300Mbps PHY rate on the wireless LAN interface. The MAC design employs a highly efficient DMA engine and hardware data processing accelerators, which free the CPU for user applications. The 802.11n 2T2R MAC/BBP/RF is designed to support standards based features in the area of security, quality of service and international regulation resulting in an enhanced end user experience.

3.2 Memory Map Summary

Start	End	Size	Description
0000.0000	-	0FFF.FFFF	256 M DDR2 256MB/SDRAM 128MB
1000.0000	-	1000.00FF	SYSCTL
1000.0100	-	1000.01FF	TIMER

1000.0200	-	1000.02FF	256	INTCTL
1000.0300	-	1000.03FF	256	MEM_CTRL (SDR/DDR)
1000.0400	-	1000.04FF	256	<<Reserved>>
1000.0500	-	1000.05FF	256	UART
1000.0600	-	1000.06FF	256	PIO
1000.0700	-	1000.07FF	256	Reserved>>
1000.0800	-	1000.08FF	256	Reserved>>
1000.0900	-	1000.09FF	256	I2C
1000.0A00	-	1000.0AFF	256	I2S
1000.0B00	-	1000.0BFF	256	SPI
1000.0C00	-	1000.0CFF	256	UARTLITE
1000.0D00	-	1000.0DFF	256	MIPS CNT
1000.2000	-	1000.27FF	2 K	PCM (up to 16 channel)
1000.2800	-	1000.2FFF	2 K	Generic DMA (up to 64 channel)
1000.3000	-	1000.37FF	2 K	Reserved>>
1000.3800	-	1000.3FFF	2 K	Reserved>>
1000.4000	-	100F.FFFF		<<Reserved>>
1010.0000	-	1010.FFFF	64 K	Frame Engine
1011.0000	-	1011.7FFF	32 K	Ethernet Swtich
1011.8000		1011.BFFF	16 K	ROM
1011.C000	-	1011.FFFF	16 K	<<Reserved>>
1012.0000	-	1012.7FFF	16 K	USB Device
1012.8000	-	1012.FFFF	16 K	<<Reserved>>
1013.0000	-	1013.7FFF	32 K	<<Reserved>>
1013.8000	-	1013.FFFF	32 K	<<Reserved>>
1014.0000	-	1017.FFFF	256 K	<<Reserved>>
1018.0000	-	101B.FFFF	256 K	802.11n MAC/BBP
101C.0000	-	101F.FFFF	256 K	USB Host
1020.0000	-	1023.FFFF	256 K	<<Reserved>>
1024.0000	-	1027.FFFF	256 K	<<Reserved>>
1028.0000	-	1BFF.FFFF		<<Reserved>>
1C00.0000	-	1C00.3FFF	16KB ROM	When system is power on, 16KB internal boot ROM is mapped.

3.3 MIPS 24K Processor

3.3.1 Features

- 8-stage pipeline
- 32-bit address paths
- 64-bit data paths to caches and external interface
- MIPS32-Compatible Instruction Set
- Multiply-Accumulate and Multiply-Subtract Instructions (MADD, MADDU, MSUB, MSUBU)
- Targeted Multiply Instruction (MUL)
- Zero/One Detect Instructions (CLZ, CLO)
- Wait Instruction (WAIT)
- Conditional Move Instructions (MOVZ, MOVN)
- Prefetch Instruction (PREF)
- MIPS32 Enhanced Architecture (Release 2) Features
- Vectored interrupts and support for external interrupt controller
- Programmable exception vector base
- Atomic interrupt enable/disable
- GPR shadow registers (optionally, one or three additional shadows can be added to minimize latency for interrupt handlers)
- Bit field manipulation instructions
- MIPS32 Privileged Resource Architecture
- MIPS DSP ASE
- Fractional data types (Q15, Q31)
- Saturating arithmetic
- SIMD instructions operate on 2x16b or 4x8b simultaneously
- 3 additional pairs of accumulator registers
- Programmable Memory Management Unit
- 32 dual-entry JTLB with variable page sizes
- 4-entry ITLB
- 8-entry DTLB
- Optional simple Fixed Mapping Translation (FMT) mechanism
- MIPS16e™ Code Compression
- 16 bit encodings of 32 bit instructions to improve code density
- Special PC-relative instructions for efficient loading of addresses and constants
- SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines
- Improved support for handling 8 and 16 bit datatypes
- Programmable L1 Cache Sizes
- Instruction cache size : 32KB
- Data cache size : 16KB
- 4-Way Set Associative
- Up to 8 outstanding load misses
- Write-back and write-through support
- 32-byte cache line size

3.3.2 Block Diagram

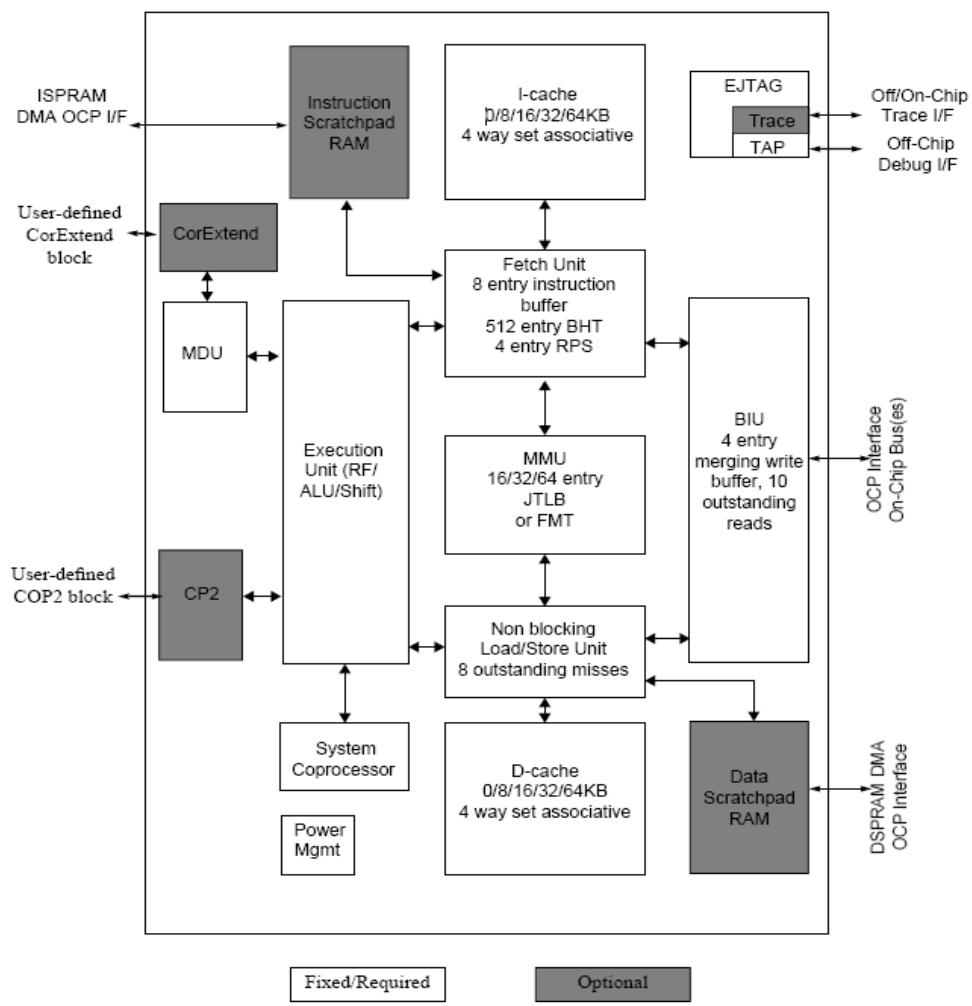


Fig. 3-3-1 MIPS 24KEc Processor Diagram

3.3.3 Clock Plan

CPU	CPU: BUS(period)	DDR2/SDR
266M < Freq ≤ 400M	1:3 / 1:4	133M
133M < Freq ≤ 266M	1:2 / 1:3 / 1:4	133M
Freq ≤ 133M	1:1 / 1:2 / 1:3 / 1:4	133M

Draft

3.4 System Control

3.4.1 Features

- Provide read-only chip revision registers
- Provide a window to access boot-strapping signals
- Support memory remapping configurations
- Support software reset to each platform building block
- Provide registers to determine GPIO and other peripheral pin muxing schemes
- Provide some power-on-reset only test registers for software programmers
- Combine miscellaneous registers (such as clock skew control, status register, memo registers,...etc)

3.4.2 Block Diagram

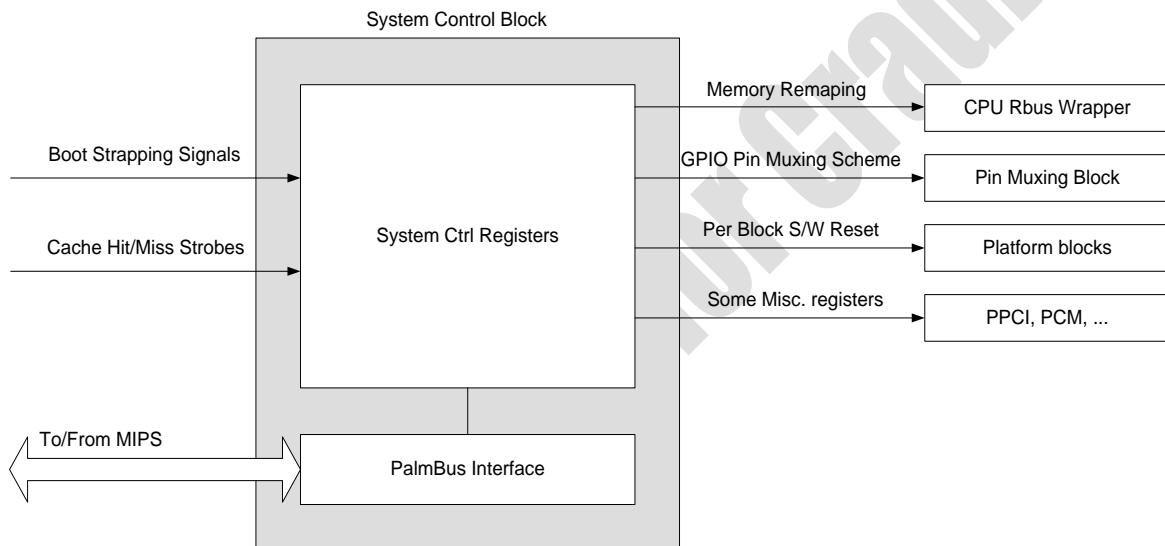


Fig. 3-4-1 System Control Block Diagram

3.4.3 Register Description (base: 0x1000.0000)

CHIPID0_3 : Chip ID ASCII Character 0-3 (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:24	RO	CHIP_ID3	ASCII CHIP Name Identification Character 3	8'h 33 ('3')
23:16	RO	CHIP_ID2	ASCII CHIP Name Identification Character 2	8'h 33 ('3')
15:8	RO	CHIP_ID1	ASCII CHIP Name Identification Character 1	8'h 54 ('T')
7:0	RO	CHIP_ID0	ASCII CHIP Name Identification Character 0	8'h 52 ('R')

CHIPID4_7 : Chip Name ASCII Character 4-7 (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:24	RO	CHIP_ID7	ASCII CHIP Name Identification Character 7	8'h 20 (' ')
23:16	RO	CHIP_ID6	ASCII CHIP Name Identification Character 6	8'h 20 (' ')
15:8	RO	CHIP_ID5	ASCII CHIP Name Identification Character 5	8'h 32 ('2')
7:0	RO	CHIP_ID4	ASCII CHIP Name Identification Character 4	8'h 35 ('5')

REVID : Chip Revision Identification (offset: 0x0C)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:8	RO	VER_ID	Chip Version Number	4'h1
7:4	-	-	Reserved	4'b0
3:0	RO	ECO_ID	Chip ECO Number	4'h1

SYSCFG0 : System Configuration Register1 (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:24	RW	TEST_CODE	Test code Note: Default value is from bootstrap and can be modified by software	Bootstrap
23:19	-	-	Reserved	
20	RO	XTAL_SEL	See section 1.4 for detail description	Bootstrap
19	RO	BIG_ENDIAN	See section 1.4 for detail description	Bootstrap
18	RO	DRAM_FROM_EE	See section 1.4 for detail description	Bootstrap
17	RO	DRAM_TYPE	See section 1.4 for detail description	Bootstrap
16	-	-	Reserved	0
15	RO	DRAM_TOTAL_WIDTH	See section 1.4 for detail description	Bootstrap
14:12	RO	DRAM_SIZE	0: 2MB 1: 8MB 2: 16MB 3: 32MB 4: 64MB 5: 128MB 6: 256MB	Bootstrap
11	-	-	Reserved	0
10	RO	DRAM_WIDTH	See section 1.4 for detail description	Bootstrap
9	-	-	Reserved	1'b0
8	RO	CPU_CLK_SEL	See section 1.4 for detail description	Bootstrap
7:3	-	-	Reserved	5'b0
2:0	RO	CHIP_MODE	See section 1.4 for detail description	Bootstrap

SYSCFG1 : System Configuration Register0 (offset: 0x14)

Bits	Type	Name	Description	Initial value
31:30	R/W	DDR_PAD_ODT_1	On die termination (Only apply to MA/MBA/MCS_N/MWE_N/MRAS_N/MCAS_N/MCKE pin). 2'b00: disable (SDR/DDR default) 2'b01: 75 ohm 2'b10: 150 ohm 2'b11: reserved Note: Default value is defined by bootstrap "DRAM_TYPE" and can be modified by software	Bootstrap
29:28	R/W	DDR_PAD_DRV_1	Pad driving apply to MA/MBA/MCS_N/MWE_N/MRAS_N/MCAS_N/MCKE pin. DDR: 2'b00: Full drive 2'b10: Half drive (default) SDR: 2'b10: High drive 2'b11: Low drive (default) Note: Default value is defined by bootstrap "DRAM_TYPE" and can be modified by software	Bootstrap
27	-	-	Reserved	
26	R/W	PULL_EN	PAD pull high/low enable 0: disable 1: enable	0
25	R/W	DDR_PAD_DS	selects input differential receiver under different supply voltage.	Bootstrap

			1'b0: DDR2 differential RX application (SDR/DDR default) 1'b1: reserved Note: Default value is defined by bootstrap "DRAM_TYPE" and can be modified by software	
24:23	R/W	DDR_PAD_ODT_0	On die termination (Only apply to DQ/DQS pin) 2'b00: disable (SDR default) 2'b01: 75 ohm 2'b10: 150 ohm(DDR default) 2'b11: reserved Note: Default value is defined by bootstrap "DRAM_TYPE" and can be modified by software	Bootstrap
22	R/W	DDR_PAD_LVCMOS	select Semi-differential for Rx 1'b0: differential Rx (DDR default) 1'b1: single-end Rx(SDR default) Note: Default value is defined by bootstrap "DRAM_TYPE" and can be modified by software	Bootstrap
21:20	R/W	DDR_PAD_DRV_0	Pad driving apply to DQ/DQS pin) DDR: 2'b00: Full drive 2'b10: Half drive (default) SDR: 2'b10: High drive 2'b11: Low drive (default) Note: Default value is defined by bootstrap "DRAM_TYPE" and can be modified by software	Bootstrap
19:14	-	-	Reserved	
13:12	R/W	GE1_MODE	Gigabit Port #1 Mode 2'b00 : RGMII Mode (10/100/1000 Mbps) 2'b01 : MII Mode (10/100M bps) 2'b10 : Reverse MII Mode (10/100M bps) 2'b11 : reserved	2'b00
11	-	-	Reserved	
10	R/W	USBO_HOST_MODE	0: Set USB#0 to Device Mode 1: Set USB#0 to Host Mode.	1'b0
9:0	-	-	Reserved	

TESTSTAT : Firmware Test Status Register (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:0	R/W	TSETSTAT[31:0]	Firmware Test Status Note : This register is reseted only by power on reset.	32'b0

TESTSTAT2 : Firmware Test Status Register 2 (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:0	R/W	TSETSTAT2[31:0]	Firmware Test Status 2 Note : This register is reseted only by power on reset.	32'b0

Reserved register (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	32'b0

Reserved register (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	32'b0

Reserved register (offset: 0x28)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	32'b0

CLKCFG0 : Clock Configuration Register 0 (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:30	R/W	SDRAM_CLK_SKEW	0 : zero delay 1: delay 200ps 2 : delay 400ps 3 : delay 600ps	2'b01
29:24	R/W	OSC_1US_DIV	1 usec count for reference clock and 32K clock generation Default value is for external XTAL 40MHz Need to change to 6'd19 when external XTAL is 20MHz(The XTAL_SEL is "0" in 0x1000_0010)	6'd39
23	-	-	Reserved	
22:18	R/W	INT_CLK_FDIV	The divisor number of reference clock frequency. Valid value is from 1~31 Fraction-N clock Frequency = (INT_CLK_FFRAC/INT_CLK_FDIV)*PLL_FREQ PLL_FREQ is either 400MHz or 384MHz in RT3352	5'd8
17	-	-	Reserved	
16:12	R/W	INT_CLK_FFRAC	The fraction number of reference clock frequency. Valid value is from 0~31 Fraction-N clock Frequency = (INT_CLK_FFRAC/INT_CLK_FDIV)*PLL_FREQ PLL_FREQ is either 400MHz or 384MHz in RT3352	5'd0
11:9	R/W	REFCLK0_RATE	0: 32K 1:12M 2:25M 3:40M 4:48M 5: Reserved 6: Internal Fraction-N_clk/2 7: Reserved	3'd0
8	R/W	REFCLK0_IS_OUT	To control the MDC as REFCLK0 output pin 0: MDC/GPIO (control by MDIO_GPIO_MODE in address 0x60) 1: Reference clock0 output	1'b0
7:0	-	Reserved		

CLKCFG1 : Clock Configuration Register 1 (offset: 0x30)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	
30	-	-	Reserved	
29	R/W	SYS_TCK_EN	System tick enable	1'b0
28:23	-	-	Reserved	
23	R/W	PDMA_CSR_CLK_GATE_BYP	PDMA csr clock gating bypass control (for USB/WLAN/FE) 0: disable bypass HW auto clock gating control for power saving 1: Bypass HW auto clock gating control	1'b1
22:21	-	-	Reserved	
20	R/W	UPHY1_CLK_EN	0 : USB PHY1 clock is gated 1 : USB PHY0 clock is enabled	1'b1
19	-	-	Reserved	
18	R/W	UPHY0_CLK_EN	0 : USB PHY0 clock is gated 1 : USB PHY0 clock is enabled	1'b1
17	-	-	Reserved	
16	R/W	GE1_CLK_EN	0 : GE1 clock is gated 1 : GE1 clock is enabled	1'b1

15:0	-	-	Reserved	1'b1
------	---	---	----------	------

RSTCTRL : Reset Control Register (offset: 0x34)

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	3'b0
28	RW	MIPS_CNT_RST	Write 1 to this bit will reset mips counter block Write 0 to de-assert reset.	1'b0
37:26	-	-	Reserved	3'b0
25	RW	UDEV_RST	Write 1 to this bit will reset USB Device block Write 0 to de-assert reset.	1'b0
24	RW	EPHY_RST	Write 1 to this bit will reset Ethernet PHY block Write 0 to de-assert reset.	1'b0
23	RW	ESW_RST	Write 1 to this bit will reset Ethernet Switch block Write 0 to de-assert reset.	1'b0
22	RW	UHST_RST	Write 1 to this bit will reset USB Host block Write 0 to de-assert reset.	1'b0
21	RW	FE_RST	Write 1 to this bit will reset Frame Engine block Write 0 to de-assert reset.	1'b0
20	RW	WLAN_RST	Write 1 to this bit will reset RT2863 block Write 0 to de-assert reset.	1'b0
19	RW	UARTL_RST	Write 1 to this bit will reset UART Lite block Write 0 to de-assert reset.	1'b0
18	RW	SPI	Write 1 to this bit will reset SPI block Write 0 to de-assert reset.	1'b0
17	RW	I2S	Write 1 to this bit will reset I2S block Write 0 to de-assert reset.	1'b0
16	RW	I2C	Write 1 to this bit will reset I2C block Write 0 to de-assert reset.	1'b0
15	-	-	Reserved	
14	RW	DMA	Write 1 to this bit will reset DMA block Write 0 to de-assert reset.	1'b0
13	RW	PIO	Write 1 to this bit will reset PIO block Write 0 to de-assert reset.	1'b0
12	RW	UART_RST	Write 1 to this bit will reset UART block Write 0 to de-assert reset.	1'b0
11	RW	PCM_RST	Write 1 to this bit will reset PCM block Write 0 to de-assert reset.	1'b0
10	RW	MC_RST	Write 1 to this bit will reset Memory Controller block Write 0 to de-assert reset.	1'b1
9	RW	INTC_RST	Write 1 to this bit will reset Interrupt Controller block Write 0 to de-assert reset.	1'b0
8	RW	TIMER_RST	Write 1 to this bit will reset Timer block Write 0 to de-assert reset.	1'b0
7:1	-	Reserved		7'b0
0	W1C	SYS_RST	Write 1 to this bit will reset Whole SoC	1'b0

RSTSTAT : Reset Status Register (offset: 0x38)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	28'b0
3	R/C	SWCPURST	Software CPU reset occurred This bit will be set if software reset the CPU by writing to the RSTCPU bit in RSTCTRL. Writing a '1' will clear this bit. Writing a '0' has not effect. Note : This register is reseted only by power on reset.	1'b0

2	R/C	SWSYSRST	Software system reset occurred This bit will be set if software reset the chip by writing to the RSTSYS bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has not effect. Note : This register is reseted only by power on reset.	1'b0
1	R/C	WDRST	Watchdog reset occurred This bit will be set if the watchdog timer reset the chip. Writing a '1' will clear this bit. Writing a '0' has not effect. Note : This register is reseted only by power on reset.	1'b0
0	-	-	Reserved	1'b0

CPU_SYS_CLKCFG : CPU and SYS clock control(offset: 0x3C)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	1'b0
30:24	R/W	OCP_FDIV	The divider number of OCP(bus) clock frequency It is refered when CPU_OCP_RATIO is set as "3'b100" OCP bus clock will be CPU_FREQ/OCP_FDIV	7'b0000011
23:19	-	-	Reserved	
18:16	R/W	CPU_OCP_RATIO	The ratio is system bus frequency compare with CPU frequency. 3'b000: 1 : 1 (CPU : SYS) 3'b001: 1 : 2 (CPU : SYS) 3'b010: 1 : 3 (CPU : SYS) 3'b011: 1 : 4 (CPU : SYS) 3'b100: 1: OCP_FDIV (Soft setting) Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL_FREQ * (CPU_FFRAC / CPU_FDIV) / (CPU_OCP_RATIO + 1) \geq 12\text{MHz}$	3'b010
15:13	-	-	Reserved	3'b000
12:8	R/W	CPU_FDIV	The divider number of CPU frequency The value must larger than or equal CPU_FFRAC. Valid value is from (1~31) CPU Frequency = $(CPU_FFRAC / CPU_FDIV) * PLL_FREQ$ Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL_FREQ * (CPU_FFRAC / CPU_FDIV) / (CPU_OCP_RATIO + 1) \geq 12\text{MHz}$	5'b00001
7:5	-	-	Reserved	3'b000
4:0	R/W	CPU_FFRAC	The fraction number of CPU frequency. Valid value is from 0~31 CPU Frequency = $(CPU_FFRAC / CPU_FDIV) * PLL_FREQ$ Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL_FREQ * (CPU_FFRAC / CPU_FDIV) / (CPU_OCP_RATIO + 1) \geq 12\text{MHz}$	5'b00001

CLK_LUT_CFG : CPU and SYS clock auto control(offset: 0x40)

Bits	Type	Name	Description	Initial value
31	R/W	CLK_LUT_EN	Clock Lookup table enable 0: Disable 1: Enable	1'b0

30:23	R/W	LUT_CNT	The counter is used to count the period of DRAM idle status. When the counter down count to zero, the cpu clock will be automatically change to specified frequency (400M*CPU_AUTO_FFRAC/CPU_AUTO_FDIV). The count period is ((AUTO_CNT+1)*16-1)us (Range is from 15us ~ 4095us)	8'd0
22:16	R/W	LUT_OCP_FDIV	The divider number of OCP(bus) clock frequency in auto mode. It is referred when CPU_AUTO_OCP_RATIO is set as "3'b100" OCP bus clock will be CPU_FREQ/AUTO_OCP_FDIV in auto enable mode	7'b00000011
15:13	R/W	CPU_LUT_OCP_RATIO	The ratio is system bus frequency compare with CPU frequency. 3'b000: 1 : 1 (Reserved) 3'b001: 1 : 2 (CPU : SYS) 3'b010: 1 : 3 (CPU : SYS) 3'b011: 1 : 4 (CPU : SYS) 3'b100: 1: AUTO_OCP_FDIV (Soft setting) Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL_FREQ * (CPU_FFRAC / CPU_FDIV) / (CPU_OCP_RATIO + 1) \geq 12\text{MHz}$	3'b010
12:8	R/W	CPU_LUT_FDIV	The divider number of CPU frequency The value must larger than or equal CPU_FFRAC. Valid value is from (1~31) CPU Frequency = $(CPU_FFRAC / CPU_FDIV) * PLL_FREQ$ Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL_FREQ * (CPU_FFRAC / CPU_FDIV) / (CPU_OCP_RATIO + 1) \geq 12\text{MHz}$	5'b00101
7:5	R/W	LUT_FREQ_SCAL	The lookup table of Clock frequency scaling 3'b100~3'b111: Reserved 3'b011: Sleep and RP will introduce the clock frequency scaling down 3'b010: Sleep will introduce the clock frequency scaling down 3'b001: RP will introduce the clock frequency scaling down 3'b000: None will introduce the clock frequency scaling down	3'b0
4:0	R/W	CPU_LUT_FFRAC	The fraction number of CPU frequency. Valid value is from 0~31 CPU Frequency = $(CPU_FFRAC / CPU_FDIV) * PLL_FREQ$ Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL_FREQ * (CPU_FFRAC / CPU_FDIV) / (CPU_OCP_RATIO + 1) \geq 12\text{MHz}$	5'b00001

CPU_CLK_AUTO_CFG: CPU clock auto dynamic control(offset: 0x44)

Bits	Type	Name	Description	Initial value
31	R/W	CPU_AUTO_CLK_EN	CPU auto clock enable 0: disable 1: enable <i>Note: After change this control from enable to disable,</i>	1'b0

			<i>software need to use CPU_SYS_CLKCFG(0x3C) register to reconfig the CPU back to 1:1 PLL frequency. Or the system will run at certain frequency which depend on system loading.</i>	
30:21	-	-	Reserved	10'b0
20:16	R/W	CLK_ADJ_STEP	The step of cpu clock adjustment. (2^31) The one step value is (PLL_CLK/CLK_ADJ_STEP)	5'd31
15:12	-	-	Reserved	4'b0
11:8	R/W	UTL_PERIOD	The unit is system tick. The calculation of CPU active utilization is during the period of (UTL_PERIOD+1)*system_tick_time. Ex. If the system tick is 4ms, the default CPU active utilization will be calculated during period of 8ms(2*4ms)	4'd1
7:6	-	-	Reserved	2'b0
5:4	R/W	UTL_HI_MARK	Set the high mark of CPU active utilization. When the CPU active utilization is higher than specified value, the CPU freq will be speeded up. 00: 50% 01: 62.5% 10: 75% 11: 87.5%	2'd1
3:2	-	-	Reserved	2'b0
1:0	R/W	UTL_LO_MARK	Set the low mark of CPU active utilization. When the CPU active utilization is lower than specified value, the CPU freq will be slowed down. 00: 12.5% 01: 25% 10: 37.5% 11: 50%	2'd2

SSC_CFG: Spreading spectrum clock control(offset: 0x54)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	
7:4	R/W	SSC_MODUMAG	modulation magnitude selection 0: +/-0.125% for center; -0.25% for down 1: +/-0.250% for center; -0.50% for down 2: +/-0.375% for center; -0.75% for down 3: +/-0.500% for center; -1.00% for down 4: +/-0.625% for center; -1.25% for down 5: +/-0.750% for center; -1.50% for down 6: +/-0.875% for center; -1.75% for down 7: +/-1.00% for center; -2.00% for down 8: +/-1.125% for center; -2.25% for down 9: +/-1.250% for center; -2.50% for down 10: +/-1.375% for center; -2.75% for down 11: +/-1.500% for center; -3.00% for down 12: +/-1.625% for center; -3.25% for down 13: +/-1.750% for center; -3.50% for down 14: +/-1.875% for center; -3.75% for down 15: +/-2.000% for center; -4.00% for down	4'b0011
3			Reserved	
2	R/W	SSC_MASHSEL	delta-sigma output select. 0: mash111; 1: mash11	1'b0
1	R/W	SSC_CDSPRD	0:Center spreading; 1: Down spreading	1'b0
0	R/W	SSC_EN	Spreading spectrum clock enable 0: Disable	1'b0

		1: Enable	
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GPIOMODE : GPIO Purpose Select (offset: 0x60)

Bits	Type	Name	Description	Initial value
31:23	-	-	Reserved	9'b0
22:21	R/W	SPI_CS1_MODE	SPI_CS1 as watch dog timeout 2'b00: SPI_CS1 2'b01: Watch dog reset output (active low for 3 system clocks) 2'b10: GPIO mode 2'b11: Reserved	2'b10
20	R/W	PA_G_GPIO_MODE	0: PA_G_mode 1: GPIO mode	1'b1
19	-	-	Reserved	
18	R/W	LNA_G_GPIO_MODE	0: LNA_G_mode 1: GPIO mode	1'b1
17:16	-	-	Reserved	
15:14	R/W	EPHY_BT_GPIO_MODE	00: Normal Mode 01: GPIO Mode 10: BT Mode	2'b00
13:10	-	-	Reserved	
9	R/W	GE1_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1
8	-	-	Reserved	1'b0
7	R/W	MDIO_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1
6	R/W	JTAG_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b0
5	R/W	UARTL_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1
4:2	R/W	UARTF_SHARE_MODE	UARF Full interface is shared with PCM, I2S, GPIO. The detailed UARF Mode Pin Sharing is shown in previous session.	3'b111
1	R/W	SPI_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1
0	R/W	I2C_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1

PMU : (offset: 0x88)

Bits	Type	Name	Description	Initial value
31:24	-	-		
23	R/W	a_sscperi	SSCG modulation period select (default :1)	1'b1
22	R/W	a_undisb	under voltage monitor function (default : 1)	1'b1
21:20	R/W	a_ssc	SSCG modulation frequency select (default :10)	2'b10
19:12	R/W	a_vtune	Programmable output voltage level (default: <10100100>)	8'b1010010 1
11				
10:8	R/W	a_dly	Output power MOSFET dead zone control (default : <011>).	3'b011
7:4	R/W	a_drven	Output power MOSFET driving control (default :<0100>).	4'b0100
3:1				
0	R/W	a_sscgen	Spread spectrum function enable (default : 0 (off))	1'b0

PMU1 : (offset: 0x8c)

Bits	Type	Name	Description	Initial value
31:16	-	-		
15:8	R/W	a_dig_Idolevel	ldo output level selection	8'b1001101 1
7:0	R/W	a_ddr_Idolevel	ldo output level selection	8'b1001110 0

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3.5 Timer

3.5.1 Features

- Independent clock pre-scale for each timer
- Independent interrupts for each timer
- Two General-purpose timers
- Periodic mode
- Free-running mode
- Time-out mode
- Second timer may be used as watchdog timer
- Watchdog timer resets system on time-out
- Timer Modes

Periodic:

In periodic mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. After reaching zero, the load value is reloaded into the timer and the timer counts down again. A load value of zero disables the timer.

Timeout:

In timeout mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. In this mode, the ENABLE bit is reset when the timer reaches zero, stopping the counter. After reaching zero, the load value is reloaded into the timer. A load value of zero disables the timer.

Free-running:

In free-running mode, the timer counts down to zero from FFFFh. An interrupt is generated when the count is zero. After reaching zero, FFFFh is reloaded into the timer. This mode is identical to the periodic mode with a load value of 65535. Though it is worth noting that if firmware writes to the load value register in this mode, the timer will still load that value even though that value will be ignored thereafter. Also note that when the timer is first enabled, it will begin counting down from its current value, not necessarily FFFFh.

Watchdog:

In watchdog mode, the timer counts down to zero from the load value. If the load value is not reloaded or the timer is not disabled before the count is zero, the chip will be reset. When this occurs, every register in the chip is reset except the watchdog reset status bit WDRST in the RSTSTAT register in the system control block; it remains set to alert firmware of the timeout event when it re-executes its bootstrap.

3.5.2 Block Diagram

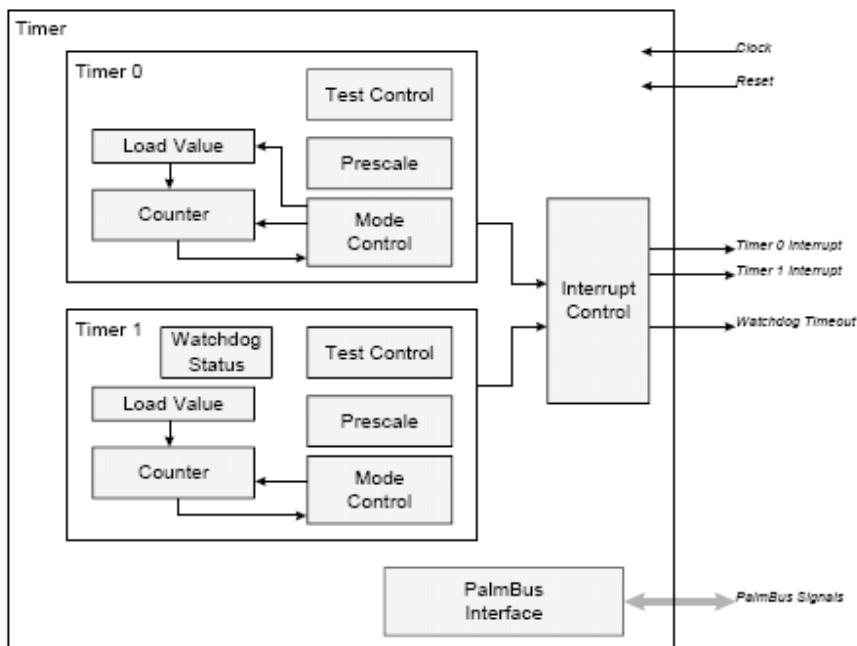


Fig. 3-5-1 Timer Block Diagram

3.5.3 Register Description (base: 0x1000.0100)

TMRSTAT: Timer Status Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:6	-	-	Reserved	26'b0
5	W	TMR1RST	Timer 1 Reset Writing a '1' to this bit will reset the Timer 1 to 0xFFFF if in free-running mode, or the value specified in the TMR1LOAD register in all other modes. Writing a '0' to this bit has no effect. Reading this bit will return a '0'.	1'b0
4	W	TMR0RST	Timer 0 Reset Writing a '1' to this bit will reset Timer 0 to 0xFFFF if in free-running mode, or the value specified in the TMR0LOAD register in all other modes. Writing a '0' to this bit has no effect. Reading this bit will return a '0'.	1'b0
3:2	-	-	Reserved	2'b0
1	W/C	TMR1INT	Timer 1 Interrupt Status This bit is set if Timer 1 has expired. The Timer 1 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit will clear the interrupt. Writing a '0' has no effect.	1'b0
0	W/C	TMROINT	Timer 0 Interrupt Status This bit is set if Timer 0 has expired. The Timer 0 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit will clear the interrupt. Writing a '0' has no effect.	1'b0

TMROLOAD: Timer 0 Load Value (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:16	R-	-	Reserved	16'b0

15:0	R/W	TMRLOAD[15:0]	Timer Load Value This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of 0 will disable the timer, except in free-running mode.	16'b0
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TMROVAL: Timer 0 Counter Value (offset: 0x14)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	RO	TMRVAL[15:0]	Timer Counter Value This register contains the current value of the timer. During functional operation, writes have no effect.	16'hffff

TMROCTL: Timer 0 Control (offset: 0x18)

Bits	Type	Name	Description	Initial value																
31:16	-	-	Reserved	16'b0																
15	R/W	TESTEN	Reserved for Test This bit should be written with a zero	1'b0																
14:8	-	-	Reserved	15'b0																
7	R/W	ENABLE	Timer Enable 0: Disable the timer. The timer will stop counting and will retain its current value. 1: Enable the timer. The timer will begin counting from its current value.	1'b0																
6	-	-	Reserved	1'b0																
5:4	R/W	MODE[1:0]	Timer Mode 0: Free-running 1: Periodic 2: Time-out 3: Time-out	1'b0																
3:0	R/W	PRESCALE[3:0]	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. <table border="1"> <tr> <th>Value</th> <th>Timer Clock Frequency</th> </tr> <tr> <td>0</td> <td>System clock</td> </tr> <tr> <td>1</td> <td>System clock / 4</td> </tr> <tr> <td>2</td> <td>System clock / 8</td> </tr> <tr> <td>3</td> <td>System clock / 16</td> </tr> <tr> <td>.</td> <td>.</td> </tr> <tr> <td>14</td> <td>System clock / 32768</td> </tr> <tr> <td>15</td> <td>System clock / 65536</td> </tr> </table>	Value	Timer Clock Frequency	0	System clock	1	System clock / 4	2	System clock / 8	3	System clock / 16	.	.	14	System clock / 32768	15	System clock / 65536	4'b0
Value	Timer Clock Frequency																			
0	System clock																			
1	System clock / 4																			
2	System clock / 8																			
3	System clock / 16																			
.	.																			
14	System clock / 32768																			
15	System clock / 65536																			
Note: The pre-scale value should not be changed unless the timer is disabled.																				

TMR1LOAD: Timer 1 Load Value (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	TMRLOAD[15:0]	Timer Load Value This register contains the load value for the timer. In all	16'b0

			modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of 0 will disable the timer, except in free-running mode.	
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TMR1VAL: Timer 1 Counter Value (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	RO	TMRVAL[15:0]	This register contains the current value of the timer. During functional operation, writes have no effect.	16'hffff

TMR1CTL: Timer 1 Control (offset: 0x28)

Bits	Type	Name	Description	Initial value																		
31:16	-	-	Reserved	16'b0																		
15	R/W	TESTEN	Reserved for Test This bit should be written with a zero	1'b0																		
14:8	-	-	Reserved	7'b0																		
7	R/W	ENABLE	Timer Enable 0: Disable the timer. The timer will stop counting and will retain its current value. 1: Enable the timer. The timer will begin counting from its current value.	1'b0																		
6	R/W	WD_TIMEOUT_SRC	Watchdog timeout alarm source 0: From Timer 1 1: From PMU watch dog timer	1'b0																		
5:4	R/W	MODE[1:0]	Timer Mode 0: Free-running 1: Periodic 2: Time-out 3: Watchdog	1'b0																		
2:0	R/W	PRESCALE[3:0]	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. <table border="1"> <thead> <tr> <th>Value</th> <th>Timer Clock Frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>System clock</td> </tr> <tr> <td>1</td> <td>System clock / 4</td> </tr> <tr> <td>2</td> <td>System clock / 8</td> </tr> <tr> <td>3</td> <td>System clock / 16</td> </tr> <tr> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> </tr> <tr> <td>14</td> <td>System clock / 32768</td> </tr> <tr> <td>15</td> <td>System clock / 65536</td> </tr> </tbody> </table> Note: The pre-scale value should not be changed unless the timer is disabled.	Value	Timer Clock Frequency	0	System clock	1	System clock / 4	2	System clock / 8	3	System clock / 16	14	System clock / 32768	15	System clock / 65536	3'b0
Value	Timer Clock Frequency																					
0	System clock																					
1	System clock / 4																					
2	System clock / 8																					
3	System clock / 16																					
.	.																					
.	.																					
14	System clock / 32768																					
15	System clock / 65536																					

3.6 Interrupt Controller

3.6.1 Features

- Support a central point for interrupt aggregation for platform related blocks
- Separated interrupt enable and disable registers
- Support global disable function
- 2-level Interrupt priority selection
- Each interrupt source can be directed to IRQ#0 or IRQ#1

Note : RT3352 supports MIPS 24K's vector interrupt mechanism.

There are 6 hardware interrupts supported by MIPS 24K. The interrupt allocation is shown below:

MIPS H/W interrupt pins	Connect to	Remark
HW_INT#5	Timer interrupt	Highest priority
HW_INT#4	802.11n NIC	
HW_INT#3	FE	
HW_INT#2	Reserved	
HW_INT#1	Other high priority interrupts (IRQ#1)	
HW_INT#0	Other low priority interrupts (IRQ#0)	Lowest priority

3.6.2 Block Diagram

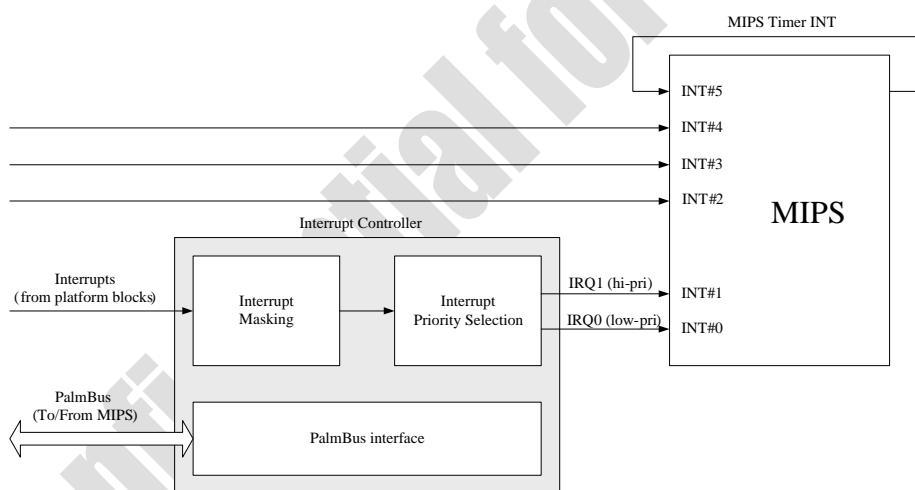


Fig. 3-6-1 Interrupt Controller Block Diagram

3.6.3 Register Description (base: 0x1000.0200)

IRQ0STAT: Interrupt Type 0 Status after Enable Mask (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	RO	UDEV	USB device interrupt status after mask	1'b0
18	RO	UHST	USB host interrupt status after mask	1'b0
17	RO	ESW	Ethernet Switch interrupt status after mask	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0

12	RO	UARTLITE	UARTLITE interrupt status after mask	1'b0
11	RO	-	Reserved	1'b0
10	RO	I2S	I2S interrupt status after mask	1'b0
9	RO	PC	MIPS performance counter interrupt status after mask	1'b0
8	RO	-	Reserved	1'b0
7	RO	DMA	DMA interrupt status after mask	1'b0
6	RO	PIO	PIO interrupt status after mask	1'b0
5	RO	UART	UART interrupt status after mask	1'b0
4	RO	PCM	PCM interrupt status after mask	1'b0
3	RO	ILL_ACC	Illegal access interrupt status after mask	1'b0
2	RO	WDTIMER	Watch dog timer interrupt status after mask	1'b0
1	RO	TIMERO	Timer 0 interrupt status after mask	1'b0
0	RO	SYSCTL	System control interrupt status after mask	1'b0

These bits are set if the corresponding interrupt is asserted from the source and with following two conditions

- The interrupt is not masked (bit not set in the INTDIS register)
- The interrupt type is set to INT0 (in the INTTYPE register).

Note that write to these bits are ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

IRQ1STAT: Interrupt Type 1 Status after Enable Mask (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	RO	UDEV	USB device interrupt status after mask	1'b0
18	RO	UHST	USB host interrupt status after mask	1'b0
17	RO	ESW	Ethernet Swtich interrupt status after mask	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0
12	RO	UARTLITE	UARTLITE interrupt status after mask	1'b0
11	-	-	Reserved	1'b0
10	RO	I2S	I2S interrupt status after mask	1'b0
9	RO	PC	MIPS performance counter interrupt status after mask	1'b0
8	-	-	Reserved	1'b0
7	RO	DMA	DMA interrupt status after mask	1'b0
6	RO	PIO	PIO interrupt status after mask	1'b0
5	RO	UART	UART interrupt status after mask	1'b0
4	RO	PCM	PCM interrupt status after mask	1'b0
3	RO	ILL_ACC	Illegal access interrupt status after mask	1'b0
2	RO	WDTIMER	Watch dog timer interrupt status after mask	1'b0
1	RO	TIMERO	Timer 0 interrupt status after mask	1'b0
0	RO	SYSCTL	System control interrupt status after mask	1'b0

These bits are set if the corresponding interrupt is asserted from the source and with following two conditions

- The interrupt is not masked (bit not set in the INTDIS register)
- The interrupt type is set to INT1 (in the INTTYPE register).

Note that writing to these bits is ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

INTTYPE: Interrupt Type (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	R/W	UDEV	USB device interrupt status type	1'b0
18	R/W	UHST	USB host interrupt status type	1'b0
17	R/W	ESW	Ethernet Swtich interrupt status type	1'b0
16	-	-	Reserved	1'b0

15:13	-	-	Reserved	3'b0
12	R/W	UARTLITE	UARTLITE interrupt status type	1'b0
11	-	-	Reserved	1'b0
10	R/W	I2S	I2S interrupt status type	1'b0
9	R/W	PC	MIPS performance counter interrupt status type	1'b0
8	-	-	Reserved	1'b0
7	R/W	DMA	DMA interrupt status after type	1'b0
6	R/W	PIO	PIO interrupt status after type	1'b0
5	R/W	UART	UART interrupt status type	1'b0
4	R/W	PCM	PCM interrupt status type	1'b0
3	R/W	ILL_ACC	Illegal access interrupt status type	1'b0
2	R/W	WDTIMER	Watch dog timer interrupt status type	1'b0
1	R/W	TIMERO	Timer 0 interrupt status type	1'b0
0	R/W	SYSCTL	System control interrupt status type	1'b0

These bits control whether an interrupt is IRQ0 or IRQ1. The interrupt type may be changed at any time; if the interrupt type is changed while the interrupt is active, the interrupt is immediately redirected.

INTRAW: Raw Interrupt Status before Enable Mask (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	RO	UDEV	USB device interrupt status before mask	1'b0
18	RO	UHST	USB host interrupt status before mask	1'b0
17	RO	ESW	Ethernet Swtich interrupt status before mask	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0
12	RO	UARTLITE	UARTLITE interrupt status before mask	1'b0
11	RO	-	Reserved	1'b0
10	RO	I2S	I2S interrupt status before r mask	1'b0
9	RO	PC	MIPS performance counter interrupt status before mask	1'b0
8	-	-	Reserved	1'b0
7	RO	DMA	DMA interrupt status before mask	1'b0
6	RO	PIO	PIO interrupt status before mask	1'b0
5	RO	UART	UART interrupt status before mask	
4	RO	PCM	PCM interrupt status before mask	1'b0
3	RO	ILL_ACC	Illegal access interrupt status before mask	1'b0
2	RO	WDTIMER	Watch dog timer interrupt status before mask	1'b0
1	RO	TIMERO	Timer 0 interrupt status before mask	1'b0
0	RO	SYSCTL	System control interrupt status before mask	1'b0

These bits are set if the corresponding interrupt is asserted from the source. The status bit is set if the interrupt is active, even if it is masked, and regardless of the interrupt type. This provides a single-access snapshot of all active interrupts for implementation of a polling system.

INTENA: Interrupt Enable (offset: 0x34)

Bits	Type	Name	Description	Initial value
31	R/W	GLOBAL	Global interrupt enable Writing a '1' to this bit allows interrupt masking to be performed based on each interrupt's individual enable mask. A read returns the global status ('1' if enabled).	1'b0
30:20	-	-	Reserved	12'b0
19	R/W	UDEV	USB device interrupt enable	1' b0
18	R/W	UHST	USB host interrupt enable	1'b0
17	R/W	ESW	Ethernet Swtich interrupt enable	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0

12	R/W	UARTLITE	UARTLITE interrupt enable	1'b0
11	-	-	Reserved	1'b0
10	R/W	I2S	I2S interrupt enable	1'b0
9	R/W	PC	MIPS performance counter interrupt enable	1'b0
8	-	-	Reserved	1'b0
7	RW	DMA	DMA interrupt enable	1'b0
6	RW	PIO	PIO interrupt enable	1'b0
5	RW	UART	UART interrupt enable	1'b0
4	RW	PCM	PCM interrupt enable	1'b0
3	RW	ILL_ACC	Illegal access interrupt enable	1'b0
2	RW	WDTIMER	Watch dog timer interrupt enable	1'b0
1	RW	TIMERO	Timer 0 interrupt enable	1'b0
0	RW	SYSCTL	System control interrupt enable	1'b0

Writing a '1' to these bits (except the GLOBAL bit) will enable the mask for the corresponding interrupt. The interrupt is asserted and the bit is set in the IRQ0STAT or IRQ1STAT registers if an interrupt is enabled. Writes of '0' are ignored. Reading either the INTENA or INTDIS register will return the current mask, where an interrupt is masked (disabled) if the bit is 'zero', and unmasked (enabled) if the bit is 'one'.

INTDIS: Interrupt Disable (offset: 0x38)

Bits	Type	Name	Description	Initial value
31	R/W	GLOBAL	Global interrupt disable Writing a '1' to this bit allows interrupt masking to be performed based on each interrupt's individual Disable mask. A read returns the global status ('1' if Disabled).	1'b0
30:20	-	-	Reserved	12'b0
19	RW	UDEV	USB device interrupt status disable	1'b0
18	RW	UHST	USB host interrupt status disable	1'b0
17	R/W	ESW	Ethernet Swtich interrupt disable	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0
12	R/W	UARTLITE	UARTLITE interrupt s disable	1'b0
11	-	-	Reserved	1'b0
10	R/W	I2S	I2S interrupt disable	1'b0
9	R/W	PC	MIPS performance counter interrupt disable	1'b0
8	RW	NAND	NAND flash controller interrupt disable	1'b0
7	RW	DMA	DMA interrupt disable	1'b0
6	RW	PIO	PIO interrupt disable	1'b0
5	RW	UART	UART interrupt disable	1'b0
4	RW	PCM	PCM interrupt disable	1'b0
3	RW	ILL_ACC	Illegal access interrupt disable	1'b0
2	RW	WDTIMER	Watch dog timer interrupt disable	1'b0
1	RW	TIMERO	Timer 0 interrupt disable	1'b0
0	RW	SYSCTL	System control interrupt disable	1'b0

Writing a '1' to these bits (except the GLOBAL bit) will disable the mask for the corresponding interrupt. The interrupt is asserted and the bit is set in the IRQ0STAT or IRQ1STAT registers if an interrupt is enabled. Writing '0' is ignored. Reading either the INTENA or INTDIS register will return the current mask, where an interrupt is masked (disabled) if the bit is 'zero', and unmasked (enabled) if the bit is 'one'.

3.7 System Tick Counter

3.7.1 Register Description (base: 0x1000.0D00)

STCK_CNT_CFG : MIPS Configuration Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	30'b0
1	R/W	EXT_STK_EN	External system tick enable 0: Use MIPS internal timer interrupt 1: Use extenal timer interrupt from external MIPS counter	1'b0
0	R/W	CNT_EN	Counter enable 0: Disable free run counter 1: Enable free run counter	1'b0

CMP_CNT : MIPS Compare Register (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	CMP_CNT	If the <i>Counter</i> ever equals Compare, then the timer circuit generates an interrupt. The interrupt remain active until Compare is written again	16'b0

CNT : MIPS Counter Register (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	CNT	This counter increase by 1 every 20us(50KHz). Count is writable/readable and will carry on counting from whatever value is loaded into it	16'b0

3.3 UART

3.3.1 Features

- 16550-compatible register set, except for Divisor Latch register
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- All standard baud rates up to 345600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loop-back control for communications link fault isolation

3.3.2 Block Diagram

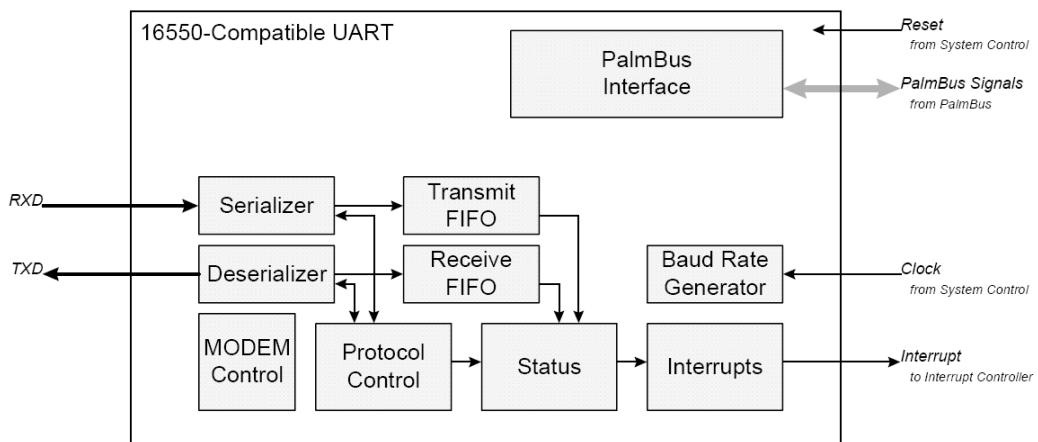


Fig. 3-8-1 UART block diagram

3.3.3 Register Description (base: 0x1000.0500)

RBR : Receive Buffer Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	RO	RXD[7:0]	Receive Buffer Data Receive data. Data is transferred to this register from the receive shift register after a full character is received. The OE bit in the LSR register is set, indication a receive buffer overrun, if the contents of this register has not been read before another character is received.	1'b0

TBR : Transmit Buffer Register (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	RO	TXD[7:0]	Transmit Buffer Data Transmit data. When a character is written to this register, it is stored in the transmitter holding register; if the transmitter register is empty, the character is moved to the transmitter register, starting transmission.	1'b0

IER : Interrupt Enable Register (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	28'b0
3	R/W	EDSSI	Enable Modem Interrupt 1: modem status (DCD, RI, DSR, CTS, DDCD, TERI, DDSR, and DCTS) intrupts. 0: Disable modem status (DCD, RI, DSR, CTS, DDCD, TERI, D and DCTS) interrupts.	1'b0
2	R/W	ELSI	Enable Receiver Line Status Interrupt 1: Enable line status (OE, PE, FE, and BI) interrupts. 0: Disable line status (OE, PE, FE, and BI) interrupts.	1'b0
1	R/W	ETBEI	Enable Transmitter Buffer Line Status Interrupt 1: Enable transmit buffer empty (THRE) interrupt. 0: Disable transmit buffer empty (THRE) interrupt.	1'b0
0	R/W	ERBFI	Enable Receiver Buffer Empty Interrupt 1: Enable data ready (DR) or character time-out interrupt. 0: Disable data ready (DR) or character time-out interrupt.	1'b0

IIR : Interrupt Identification Register (offset: 0x0C)

Bits	Type	Name	Description	Initial value																																				
31:8	-	-	Reserved	24'b0																																				
7:6	RO	FIFOENA[1:0]	FIFOs Enabled FIFOs Enabled. These bits reflect the FIFO enable bit setting in the FIFO Control Register. When the FIFO enable bit is set, both of these bits will be set high to a value of '11'. When the FIFO enable bit is cleared, both of these bits will be set low to a value of '00'.	1'b0																																				
5:4	-	-	Reserved	2'b0																																				
3:1	RO	INTID[2:0]	Interrupt Identifier Interrupt ID. These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. The interrupt encoding is given below. <table border="1"> <thead> <tr> <th>ID</th> <th>Priority</th> <th>Type</th> <th>Source</th> </tr> </thead> <tbody> <tr> <td>7</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>6</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>5</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>4</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>3</td> <td>1</td> <td>Receiver Line Status</td> <td>OE,PE,FE,BI</td> </tr> <tr> <td>2</td> <td>2</td> <td>Receiver Buffer Full</td> <td>DR</td> </tr> <tr> <td>1</td> <td>3</td> <td>Transmit buffer Empty</td> <td>THRE</td> </tr> <tr> <td>0</td> <td></td> <td>Undefined</td> <td></td> </tr> </tbody> </table> If more than one category of interrupt is asserted, only the highest priority ID will be given. The line and Modem status interrupts are cleared by reading the corresponding status register (LSR, MSR). The Receive Buffer Full interrupt will be cleared when all of the data is read from the receiver buffer. The Transmitter Buffer empty will be cleared when data is written to the TBR register. See also "Interrupt Priorities".	ID	Priority	Type	Source	7		Undefined		6		Undefined		5		Undefined		4		Undefined		3	1	Receiver Line Status	OE,PE,FE,BI	2	2	Receiver Buffer Full	DR	1	3	Transmit buffer Empty	THRE	0		Undefined		3'b0
ID	Priority	Type	Source																																					
7		Undefined																																						
6		Undefined																																						
5		Undefined																																						
4		Undefined																																						
3	1	Receiver Line Status	OE,PE,FE,BI																																					
2	2	Receiver Buffer Full	DR																																					
1	3	Transmit buffer Empty	THRE																																					
0		Undefined																																						
0	RO	INTPEND	Interrupt Pending 0: An interrupt bit is set and is not masked. 1: No interrupts are pending.	1'b1																																				

FCR : FIFO Control Register (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0

			Receiver Trigger Level The data ready interrupt (DR) will be asserted when the receive buffer depth is equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:											
7:6	R/W	RXTRIG[1:0]	<table border="1"> <thead> <tr> <th>RXTRIG</th><th>Trigger Level</th></tr> </thead> <tbody> <tr><td>0</td><td>1</td></tr> <tr><td>1</td><td>4</td></tr> <tr><td>2</td><td>8</td></tr> <tr><td>3</td><td>14</td></tr> </tbody> </table> <p>Note: This register is not used if the receive FIFO is disabled.</p>	RXTRIG	Trigger Level	0	1	1	4	2	8	3	14	2'b0
RXTRIG	Trigger Level													
0	1													
1	4													
2	8													
3	14													
5:4	R/W	TXTRIG[1:0]	<p>Transmitter Trigger Level The THRE interrupt will be asserted if the transmitter buffer depth is less than or equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:</p> <table border="1"> <thead> <tr> <th>TXTRIG</th><th>Trigger Level</th></tr> </thead> <tbody> <tr><td>0</td><td>1</td></tr> <tr><td>1</td><td>4</td></tr> <tr><td>2</td><td>8</td></tr> <tr><td>3</td><td>12</td></tr> </tbody> </table>	TXTRIG	Trigger Level	0	1	1	4	2	8	3	12	2'b0
TXTRIG	Trigger Level													
0	1													
1	4													
2	8													
3	12													
3	R/W	DMAMODE	Enable DMA transfers This bit is writeable and readable, but has no other hardware function.	1'b0										
2	W	TXRST	Transmitter Reset Writing a '1' to this bit will clear the transmit FIFO and reset the transmitter status. The shift register is not cleared.	1'b0										
1	W	RXRST	Receive Reset Writing a '1' to this bit will clear the receive FIFO and reset the receiver status. The shift register is not cleared.	1'b0										
0	R/W	FIFOENA	0: The Transmit and Receive FIFOs have the effective depth of one character. 1: The Transmit and Receive FIFOs are enabled. Note: The FIFO status and data are automatically cleared when this bit is changed.	1'b0										

LCR : Line Control Register (offset: 0x 14, 0x00000000, 0xfffff00, 00)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/W	DLAB	Divisor Latch Access Bit This bit has no functionality, and is retained for compatibility only	2'b0
6	R/W	SETBRK	Set Break Condition 0: Normal functionality. 1: Force TXD pin to '0'. Transmitter otherwise operates normally.	2'b0
5	R/W	FORCEPAR	Force Parity Bit 0: Normal functionality. 1: If even parity is selected, the (transmitted and checked) parity is forced to '0'; if odd parity is selected, the (transmitted and checked) parity is forced to '1'.	1'b0
4	R/W	EPS	Even Parity Select 0: Odd parity selected (checksum, including parity is '1'). 1: Even parity selected (checksum, including parity is '0').	1'b0

			Note: This bit is ignored if the PEN bit is '0'.	
3	R/W	PEN	Parity Enable 0: Parity is not transmitted or checked. 1: Parity is generated (transmit), and checked (receive).	1'b0
2	R/W	STB	Stop Bit Select 0: 1 stop bit is transmitted and received. 1: 1.5 stop bits are transmitted and received if WLS is '0'; 2 stop bits are transmitted and received if WLS is '1', '2', or '3'.	1'b0
1:0:	R/W	WLS[1:0]	Word Length Select 0: Each character is 5 bits in length 1: Each character is 6 bits in length 2: Each character is 7 bits in length 3: Each character is 8 bits in length	2'b0

MCR : Modem Control Register (offset: 0x18)

Bits	Type	Name	Description	Initial value												
31:5	-	-	Reserved	24'b0												
4	R/W	LOOP	Loop-back Mode Enable 0: Normal Operation. 1: The UART is put into loop-back mode, used for self-test: The TXD pin is driven high; the TXD signal connections are made internally <table border="1"> <tr> <td>Signal</td> <td>Wrapped back through...</td> </tr> <tr> <td>TXD</td> <td>RXD</td> </tr> <tr> <td>DTRN</td> <td>DSRN</td> </tr> <tr> <td>RTSN</td> <td>CTSN</td> </tr> <tr> <td>OUT1N</td> <td>RIN</td> </tr> <tr> <td>OUT2N</td> <td>DCDN</td> </tr> </table>	Signal	Wrapped back through...	TXD	RXD	DTRN	DSRN	RTSN	CTSN	OUT1N	RIN	OUT2N	DCDN	1'b0
Signal	Wrapped back through...															
TXD	RXD															
DTRN	DSRN															
RTSN	CTSN															
OUT1N	RIN															
OUT2N	DCDN															
3	R/W	OUT2	Out2 Value 0: OUT2N pin is driven to a high level. 1: OUT2N pin is driven to a low level. Note: This bit is only functional in loop-back mode.	0												
2	R/W	OUT1	Out1 Value 0: OUT1N pin is driven to a high level. 1: OUT1N pin is driven to a low level. Note: This bit is only functional in loop-back mode.	0												
1	R/W	RTS	Out1 Value 0: RTSN pin is driven to a high level. 1: RTSN pin is driven to a low level.	1'b0												
1	R/W	DTR	Reserved 0: DTRN pin is driven to a high level. 1: DTRN pin is driven to a low level.	1'b0												

LSR : Line Status Register (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/C	ERINFIFO	The FIFO contains data which had a parity or framing error This bit is set when the FIFO contains data that was received with a parity error, framing error or break condition.	1'b0
6	R/C	TEMPT	Transmitter Empty This bit is set when the transmitter shift register is empty, it will clear as soon as data is written to the TBR register.	1'b1
5	R/C	THRE	Transmitter Holding Register Empty This bit is set when the transmitter holding register is empty, it will clear as soon as data is written to the TBR register.	1'b1

4	R/C	BI	Break Interrupt This bit is set if a break is received, that is when the RXD signal is at a low state for more than one character transmission time (from start bit to stop bit). Under this condition, a single 'zero' is received.	1'b0
3	R/C	FE	Framing Error This bit is set if a valid stop bit is not detected. If a framing error occurs, the receiver will attempt to re-synchronize by sampling the Start Bit twice and then takes the data.	1'b0
2	R/C	PE	Parity Error This bit is set if the received parity is different from the expected value.	1'b0
1	R/C	OE	Overrun Error This bit is set when a receive overrun occurs. This will happen if a character is received before the previous character has been read by firmware.	1'b0
0	R/C	DR	Data Ready This bit is set when a character is received, and has been transferred in to the receiver buffer register. This bit will reset when all the characters are read from the receiver buffer register.	1'b0

MSR : Modem Status Register (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/C	DCD	Data Carrier Detect This bit is set when the DCDN (Data Carrier Detect) pin is at a low value.	1'b0
6	R/C	RI	Ring Indicator This bit is set when the RIN (Ring Indicator) pin is at a low value.	1'b1
5	R/C	DSR	Data Set Ready This bit is set when the DSRN (Data Set Ready) pin is at a low value.	1'b0
4	R/C	CTS	Clear to Send This bit is set when the CTSN (Clear to Send) pin is at a low value.	1'b0
3	R/C	DDCD	Delta Data Carrier Detect This bit is set when the DCDN (Data Carrier Detect) pin changes.	1'b0
2	R/C	TERI	Trailing Edge Ring Indicator This bit is set when the RIN (Ring Indicator) pin changes from a low to a high value.	1'b0
1	R/C	DDSR	Delta Data Set Ready This bit is set when the DSRN (Data Set Ready) pin changes.	1'b0
0	R/C	DCTS	Delta Clear to Send This bit is set when the CTSN (Clear to Send) pin changes.	1'b0

SCRATCH : Scratch Register (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	SCRATCH[7:0]	Scratch This register is defined as a scratch register in 16550 application. It has no hardware function, and is retained for compatibility only.	8'b0

DL : Clock Divider Divisor Latch (offset: 0x28)

Bits	Type	Name	Description	Initial value																								
31:16	-	-	Reserved	16'b0																								
15:0	R/W	DL[15:0]	<p>Divisor Latch This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as: baud rate = 40MHz / (CLKDIV * 16).</p> <p>Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only.</p> <p>NOTE: DL[15:0] should be >= 4</p> <table border="1"> <thead> <tr> <th>Src clock(MHz)</th> <th>Req Baud rate</th> <th>DL[15:0]</th> <th>Err Rate (%)</th> </tr> </thead> <tbody> <tr> <td>40000000</td> <td>57000</td> <td>44</td> <td>-0.32%</td> </tr> <tr> <td></td> <td>115200</td> <td>22</td> <td>-1.36%</td> </tr> <tr> <td></td> <td>230400</td> <td>11</td> <td>-1.36%</td> </tr> <tr> <td></td> <td>345600</td> <td>7</td> <td>3.34%</td> </tr> <tr> <td></td> <td>460800</td> <td>5</td> <td>8.51%</td> </tr> </tbody> </table>	Src clock(MHz)	Req Baud rate	DL[15:0]	Err Rate (%)	40000000	57000	44	-0.32%		115200	22	-1.36%		230400	11	-1.36%		345600	7	3.34%		460800	5	8.51%	16'h0001
Src clock(MHz)	Req Baud rate	DL[15:0]	Err Rate (%)																									
40000000	57000	44	-0.32%																									
	115200	22	-1.36%																									
	230400	11	-1.36%																									
	345600	7	3.34%																									
	460800	5	8.51%																									

DLLO : Clock Divider Divisor Latch Low (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLLO[7:0]	<p>This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility.</p> <p>Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.</p>	8'b1

DLHI : Clock Divider Divisor Latch High (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLHI[7:0]	<p>This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility.</p> <p>Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.</p>	8'b0

3.4 UART Lite

3.4.1 Features

- 2-pin UART
- 16550-compatible register set, except for Divisor Latch register
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- All standard baud rates up to 345600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loop-back control for communications link fault isolation

3.4.2 Block Diagram

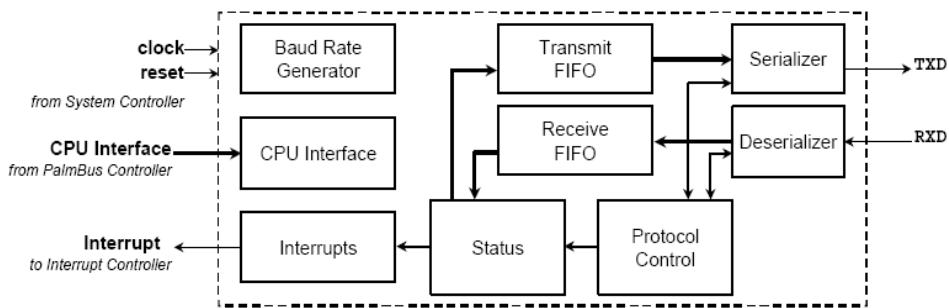


Fig. 3-9-1 UART Lite Block Diagram

3.4.3 Register Description (base: 0x1000.0C00)

RBR: Receive Buffer Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	RO	RXD[7:0]	Receive Buffer Data Receive data. Data is transferred to this register from the receive shift register after a full character is received. The OE bit in the LSR register is set, indication a receive buffer overrun, if the contents of this register has not been read before another character is received.	8'b0

TBR: Transmit Buffer Register (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	RO	TXD[7:0]	Transmit Buffer Data Transmit data. When a character is written to this register, it is stored in the transmitter holding register; if the transmitter register is empty, the character is moved to the transmitter register, starting transmission.	8'b0

IER : Interrupt Enable Register (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:3	-	-	Reserved	29'b0
2	R/W	ELSI	Enable Receiver Line Status Interrupt 1: Enable line status (OE, PE, FE, and BI) interrupts. 0: Disable line status (OE, PE, FE, and BI) interrupts.	1'b0
1	R/W	ETBEI	Enable Transmitter Buffer Line Status Interrupt 1: Enable transmit buffer empty (THRE) interrupt. 0: Disable transmit buffer empty (THRE) interrupt.	1'b0
0	R/W	ERBFI	Enable Receiver Buffer Empty Interrupt 1: Enable data ready (DR) or character time-out interrupt. 0: Disable data ready (DR) or character time-out interrupt.	1'b0

IIR: Interrupt Identification Register (offset: 0xC)

Bits	Type	Name	Description	Initial value																																								
31:8	-	-	Reserved	24'b0																																								
7:6	RO	FIFOENA [1:0]	FIFOs Enabled FIFOs Enabled. These bits reflect the FIFO enable bit setting in the FIFO Control Register. When the FIFO enable bit is set, both of these bits will be set high to a value of '11'. When the FIFO enable bit is cleared, both of these bits will be set low to a value of '00'.	1'b0																																								
5:4	-	-	Reserved	2'b0																																								
3:1	RO	INTID[2:0]	Interrupt Identifier Interrupt ID. These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. The interrupt encoding is given below.	3'b0																																								
			<table border="1"> <thead> <tr> <th>ID</th> <th>Priority</th> <th>Type</th> <th>Source</th> </tr> </thead> <tbody> <tr> <td>7</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>6</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>5</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>4</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>3</td> <td>1</td> <td>Receiver Line Status</td> <td>OE,PE,FE,BI</td> </tr> <tr> <td>2</td> <td>2</td> <td>Receiver Buffer Full</td> <td>DR</td> </tr> <tr> <td>1</td> <td>3</td> <td>Transmit buffer</td> <td>THRE</td> </tr> <tr> <td>0</td> <td>4</td> <td>Empty</td> <td>DCTD,DDSR, RI,</td> </tr> <tr> <td></td> <td></td> <td>Modem Status</td> <td>DCD</td> </tr> </tbody> </table> <p>If more than one category of interrupt is asserted, only the highest priority ID will be given. The line and Modem status interrupts are cleared by reading the corresponding status register (LSR, MSR). The Receive Buffer Full interrupt will be cleared when all of the data is read from the receiver buffer. The Transmitter Buffer empty will be cleared when data is written to the TBR register. See also "Interrupt Priorities".</p>	ID	Priority	Type	Source	7		Undefined		6		Undefined		5		Undefined		4		Undefined		3	1	Receiver Line Status	OE,PE,FE,BI	2	2	Receiver Buffer Full	DR	1	3	Transmit buffer	THRE	0	4	Empty	DCTD,DDSR, RI,			Modem Status	DCD	
ID	Priority	Type	Source																																									
7		Undefined																																										
6		Undefined																																										
5		Undefined																																										
4		Undefined																																										
3	1	Receiver Line Status	OE,PE,FE,BI																																									
2	2	Receiver Buffer Full	DR																																									
1	3	Transmit buffer	THRE																																									
0	4	Empty	DCTD,DDSR, RI,																																									
		Modem Status	DCD																																									
0	RO	INTPEND	Interrupt Pending 0: An interrupt bit is set and is not masked. 1: No interrupts are pending.	1'b0																																								

FCR: FIFO Control Register (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:6	R/W	RXTRIG [1:0]	Receiver Trigger Level The data ready interrupt (DR) will be asserted when the receiver buffer depth is equal to the number of characters programmed in the trigger register. The trigger level encoding	2'b0

			is as follows:											
			<table border="1"> <thead> <tr> <th>RXTRIG</th><th>Trigger Level</th></tr> </thead> <tbody> <tr> <td>0</td><td>1</td></tr> <tr> <td>1</td><td>4</td></tr> <tr> <td>2</td><td>8</td></tr> <tr> <td>3</td><td>14</td></tr> </tbody> </table>	RXTRIG	Trigger Level	0	1	1	4	2	8	3	14	
RXTRIG	Trigger Level													
0	1													
1	4													
2	8													
3	14													
			Note: This register is not used if the receive FIFO is disabled.											
5:4	R/W	TXTRIG[1:0]	<p>Transmitter Trigger Level The THRE interrupt will be asserted if the transmitter buffer depth is less than or equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:</p> <table border="1"> <thead> <tr> <th>TXTRIG</th><th>Trigger Level</th></tr> </thead> <tbody> <tr> <td>0</td><td>1</td></tr> <tr> <td>1</td><td>4</td></tr> <tr> <td>2</td><td>8</td></tr> <tr> <td>3</td><td>12</td></tr> </tbody> </table>	TXTRIG	Trigger Level	0	1	1	4	2	8	3	12	2'b0
TXTRIG	Trigger Level													
0	1													
1	4													
2	8													
3	12													
3	R/W	DMAMODE	Enable DMA transfers This bit is writeable and readable, but has no other hardware function.	1'b0										
2	W	TXRST	Transmitter Reset Writing a '1' to this bit will clear the transmit FIFO and reset the transmitter status. The shift register is not cleared.	1'b0										
1	W	RXRST	Receive Reset Writing a '1' to this bit will clear the receive FIFO and reset the receiver status. The shift register is not cleared.	1'b0										
0	R/W	FIFOENA	0: The Transmit and Receive FIFOs have the effective depth of one character. 1: The Transmit and Receive FIFOs are enabled. Note: The FIFO status and data are automatically cleared when this bit is changed.	1'b0										

LCR: Line Control Register (offset: 0x14)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/W	DLAB	Divisor Latch Access Bit This bit has no functionality, and is retained for compatibility only	2'b0
6	R/W	SETBRK	Set Break Condition 0: Normal functionality. 1: Force TXD pin to '0'. Transmitter otherwise operates normally.	2'b0
5	R/W	FORCEPAR	Force Parity Bit 0: Normal functionality. 1: If even parity is selected, the (transmitted and checked) parity is forced to '0'; if odd parity is selected, the (transmitted and checked) parity is forced to '1'.	1'b0
4	R/W	EPS	Even Parity Select 0: Odd parity selected (checksum, including parity is '1'). 1: Even parity selected (checksum, including parity is '0'). Note: This bit is ignored if the PEN bit is '0'.	1'b0
3	R/W	PEN	Parity Enable 0: Parity is not transmitted or checked. 1: Parity is generated (transmit), and checked (receive).	1'b0
2	R/W	STB	Stop Bit Select	1'b0

			0: 1 stop bit is transmitted and received. 1: 1.5 stop bits are transmitted and received if WLS is '0'; 2 stop bits are transmitted and received if WLS is '1', '2', or '3'.	
1:0:	R/W	WLS[1:0]	Word Length Select 0: Each character is 5 bits in length 1: Each character is 6 bits in length 2: Each character is 7 bits in length 3: Each character is 8 bits in length	2'b0

MCR: Modem Control Register (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	24'b0
4	R/W	LOOP	Loop-back Mode Enable 0: Normal Operation. 1: The UART is put into loop-back mode, used for self-test: The TXD pin is driven high; the TXD signal are connected to RXD internally.	1'b0
3:0	RO	-	Reserved	7'b0

LSR: Line Status Register (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/C	ERINFIFO	The FIFO contains data which had a parity or framing error This bit is set when the FIFO contains data that was received with a parity error, framing error or break condition.	2'b0
6	R/C	TEMPT	Transmitter Empty This bit is set when the transmitter shift register is empty, it will clear as soon as data is written to the TBR register.	1'b0
5	R/C	THRE	Transmitter Holding Register Empty This bit is set when the transmitter holding register is empty, it will clear as soon as data is written to the TBR register.	1'b0
4	R/C	BI	Break Interrupt This bit is set if a break is received, that is when the RXD signal is at a low state for more than one character transmission time (from start bit to stop bit). Under this condition, a single 'zero' is received.	1'b0
3	R/C	FE	Framing Error This bit is set if a valid stop bit is not detected. If a framing error occurs, the receiver will attempt to re-synchronize by sampling the Start Bit twice and then takes the data.	1'b0
2	R/C	PE	Parity Error This bit is set if the received parity is different from the expected value.	1'b0
1	R/C	OE	Overrun Error This bit is set when a receive overrun occurs. This will happen if a character is received before the previous character has been read by firmware.	1'b0
0	R/C	DR	Data Ready This bit is set when a character is received, and has been transferred in to the receiver buffer register. This bit will reset when all the characters are read from the receiver buffer register.	1'b0

DL: Clock Divider Divisor Latch (offset: 0x28)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0

			Divisor Latch This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as: Baud rate = system clock frequency / (CLKDIV * 16). Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only.	
15:0	R/W	DL[15:0]	NOTE: DL[15:0] should be >= 4	16'h0001

DLLO: Clock Divider Divisor Latch Low (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLLO[7:0]	This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility. Note: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	8'b1

DLHI : Clock Divider Divisor Latch High (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLHI[7:0]	This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility. Note: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	8'b0

IFCTL : Interface Control (offset: 0x34)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	31'b0
0	R/W	IFCTL	Open Collector Mode Control. This register controls if the UART Lite TXD output functions in open collector mode or is always driven. When set to '0', the output is always driven with the value of the transmit data signal. When set to a '1', the TXD output functions in open collector mode, where the TXD output is either driven low (when the transmit data output is active low) or tri-stated (when the transmit data output is active high).	1'b0

3.5 Programmable I/O

3.5.1 Features

- Support 45 programmable I/Os
- Parameterized numbers of independent inputs, outputs, and inputs
- Independent polarity controls for each pin
- Independently masked edge detect interrupt on any input transition
- Programmable I/O pins are shared pin with MDIO, JTAG, UART-Lite, UART, SPI, PCM, I2C, GE1, EPHY_LED

3.5.2 Block Diagram

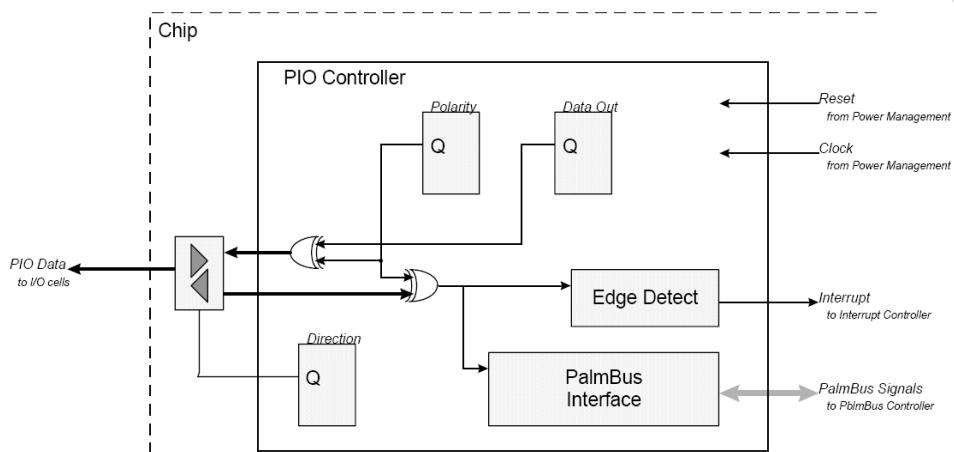


Fig. 3-10-1 Program I/O Block Diagram

3.5.3 Register Description (base: 0x1000.0600)

GPIO23_00_INT: Programmed I/O Interrupt Status (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOINT[23:0]	A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing "1" to either this register or the PIOEDGE register. Note: Changes to the PIO pins can only be detected when the clock is running.	24'b0

GPIO23_00_EDGE: Programmed I/O Edge Status (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOEDGE[23:0]	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit will be set), the PIOEDGE bit will be '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit will be set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are cleared by writing "1" to either this register or the PIOINT register. Note: Changes to the PIO pins can only be detected when the clock is running.	24'b0

GPIO23_00_RENA: Programmed I/O Rising Edge Interrupt Enable (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIORENA[23:0]	Rising edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set. Note: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	24'b0

GPIO23_00_FENA: Programmed I/O Falling Edge Interrupt Enable (offset: 0x0C)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIOFMASK [23:0]	Falling edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set. Note: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	24'b0

GPIO23_00_DATA: Programmed I/O Data (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIODATA[23:0]	Data Pin for Program I/O These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	24'b0

GPIO23_00_DIR: Programmed I/O Direction (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIODIR[23:0]	Program I/O Pin Direction These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers.	24'b0

GPIO23_00_POL: Programmed I/O Pin Polarity (offset: 0x28)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIOPOL[23:0]	Program I/O Pin Polarity These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at	24'b0

			any PIO pin, the corresponding bit should be set to '1'; a value of '0' will not modify the pin data. Note: The polarity controls affect both input and output modes.	
--	--	--	--	--

GPIO23_00_SET: Set PIO Data Bit (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOSET[23:0]	These bits are used for setting bits in the PIODATA output register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

GPIO23_00_RESET: Clear PIO Data bit (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIORESET[23:0]	These bits are used for clearing bits in the PIODATA output register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

GPIO23_00_TOG: Toggle PIO Data bit (offset: 0x34)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOTOG[23:0]	These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

GPIO39_24_INT : Program I/O Interrupt (offset: 0x38)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIOINT[15:0]	A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing "1" to either this register or the PIOEDGE register. Note: Changes to the PIO pins can only be detected when the clock is running.	16'b0

GPIO39_24_EDGE : Program I/O Edge Status (offset: 0x3c)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIOEDGE [15:0]	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit will be set), the PIOEDGE bit will be '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit will be set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are cleared by writing "1" to either this register or the PIOINT register. Note: Changes to the PIO pins can only be detected when the clock is running.	16'b0

GPIO39_24_RENA : Program I/O Rising Edge Interrupt Enable (offset: 0x40)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIORENA[15:0]	Rising edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set. Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.	16'b0

GPIO39_24_FENA : Program I/O Falling Edge Interrupt Enable (offset: 0x44)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIOFENA[15:0]	Falling edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set. Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.	16'b0

GPIO39_24_DATA : Program I/O Data (offset: 0x48)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIODATA[15:0]	Data Pin for Program I/O These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	16'b0

GPIO39_24_DIR : Program I/O Direction (offset: 0x4c)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIODATA[15:0]	Program I/O Pin Direction These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers.	16'b0

GPIO39_24_POL : Program I/O Pin Polarity (offset: 0x50)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIOPOL[15:0]	Program I/O Pin Polarity These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data	16'b0

			at any PIO pin, the corresponding bit should be set to '1'; a value of '0' will not modify the pin data. Note: The polarity controls affect both input and output modes.	
--	--	--	---	--

GPIO39_24_SET : Set PIO Data Bit (offset: 0x54)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIOSET[15:0]	These bits are used for setting bits in the PIODATA output register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	16'b0

GPIO39_24_RESET : Clear PIO Data bit [39:24](offset: 0x58)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIORESET[15:0]	These bits are used for clearing bits in the PIODATA output register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	16'b0

GPIO39_24_TOG : Toggle PIO Data bit (offset: 0x5c)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIOTOG[15:0]	These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	16'b0

GPIO45_40_INT : Program I/O Interrupt Status (offset: 0x60)

Bits	Type	Name	Description	Initial value
5:0	R/C	PIOINT[5:0]	A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing "1" to either this register or the PIOEDGE register. Note: Changes to the PIO pins can only be detected when the clock is running.	6'b0

GPIO45_40_EDGE : Program I/O Edge Status (offset: 0x64)

Bits	Type	Name	Description	Initial value
5:0	R/C	PIOEDGE[5:0]	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit will be set), the PIOEDGE bit will be '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit will be set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are cleared by writing "1" to either this register or the PIOINT register. Note: Changes to the PIO pins can only be detected when the clock is running.	6'b0

GPIO45_40_RENA : Program I/O Rising Edge Interrupt Enable (offset: 0x68)

Bits	Type	Name	Description	Initial value
5:0	R/W	PIORENA[5:0]	Rising edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set.	6'b0

			Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.	
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GPIO45_40_FENA : Program I/O Falling Edge Interrupt Enable (offset: 0x6C)

Bits	Type	Name	Description	Initial value
5:0	R/W	PIORENA[5:0]	Falling edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set. Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.	6'b0

GPIO45_40_DATA : Program I/O Data (offset: 0x70)

Bits	Type	Name	Description	Initial value
5:0	R/W	PIODATA[5:0]	Data Pin for Program I/O These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	6'b0

GPIO45_40_DIR : Program I/O Direction (offset: 0x74)

Bits	Type	Name	Description	Initial value
5:0	R/W	PIODIR [5:0]	Program I/O Pin Direction These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers.	6'b0

GPIO45_40_POL : Program I/O Pin Polarity(offset: 0x78)

Bits	Type	Name	Description	Initial value
5:0	R/W	PIOPOL [5:0]	Program I/O Pin Polarity These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at PIO pin, the corresponding bit should be set to '1'; a value of '0' will not modify the pin data. Note: The polarity controls affect both input and output modes.	6'b0

GPIO45_40_SET : Set PIO Data Bit (offset: 0x7C)

Bits	Type	Name	Description	Initial value
5:0	R/C	PIOSET [5:0]	These bits are used for setting bits in the PIODATA output register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	6'b0

GPIO45_40_RESET : Clear PIO Data bit (offset: 0x80)

Bits	Type	Name	Description	Initial value
5:0	R/C	PIORESET [5:0]	These bits are used for clearing bits in the PIODATA output	6'b0

			register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	
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GPIO45_40_TOG : Toggle PIO Data bit (offset: 0x84)

Bits	Type	Name	Description	Initial value
5:0	R/C	PIOTOG [5:0]	These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	6'b0

3.18 I2C Controller

3.5.4 Features

- Programmable I2C bus clock rate
- Supports the Synchronous Inter Integrated Circuits (I2C) serial protocol
- Bi-directional data transfer
- Programmable address width up to 8 bits
- Sequential byte read or write capability
- Device address and data address can be transmitted for device, page and address selection
- Supports Standard mode and Fast mode

3.5.5 Block Diagram

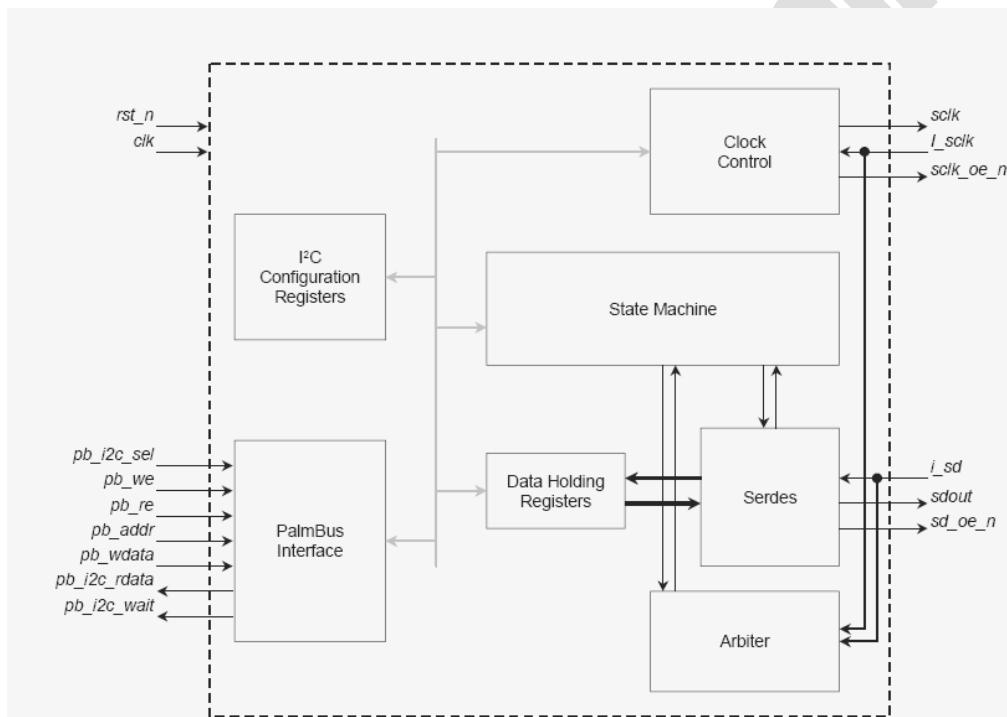


Fig. 3-11-1 I2C Controller Block Diagram

3.5.6 Register Description (base: 0x1000.0900)

CONFIG: I2C Configuration Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:5	R/W	ADDRLEN [2:0]	Address Length The value written to this register plus one will indicate the number of address bits to be transferred from the I2C ADDR register. Program '0' for a 1-bit address, '1' for a 2-bit address, etc.)	3'b0
4:2	R/W	DEVADLEN [2:0]	Device Address Length The value written to this register plus one indicates the number of device address bits to be transferred from the	3'b0

			DEVADDR register. This field should be programmed to '6' for compliance with I2C bus protocol.	
1	R/W	ADDRDIS	0: Normal transfers will occur with the address being Transmitted, followed by read or write data. 1: The controller will read or write serial data without transferring the address.	1'b0
0	R/W	DEVADDIS	0: The device address will be transmitted before the data address. 1: The controller will not transfer the device address. Note: if this bit is set, the ADDRDIS bit is ignored, and an address is always transmitted. Note: most I2C slave devices require a device address to be transmitted; this bit should typically be set to '0'.	1'b0

CLKDIV: I2C Clock Divisor Register (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	CLKDIV[15:0]	Clock Divisor The value written to this register is used to generate the I2C bus SCLK signal by applying the following equation: SCLK frequency = 40MHz / (2 x CLKDIV) Note: Only values of 8 and above are valid. Note: Due to synchronization between the I2C internal clock and the system clock, the exact equation is actually SCLK frequency = pb_clk frequency / ((2 x CLKDIV) + 5). For most systems, CLKDIV is usually programmed to very larger numbers since the system clock frequency should be orders of magnitude faster than the I2C bus clock. These results in the synchronization errors being insignificant and the exact equation approximating the simpler one given above.	16'b0

DEVADDR: I2C Device Address Register (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:7	-	-	Reserved	25'b0
6:0	R/W	DEVADDR[6:0]	I2C Device Address This value is transmitted as the device address, if DEVADDIS bit in the CONFIG register is not set to '1'.	7'b0

ADDR: I2C Address Register (offset: 0x0c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	ADDR[7:0]	I2C Address These bits store the 8-bits of address to be sent to the external I2C slave devices when the ADDRDIS bit is '0'.	8'b0

DATAOUT: I2C Data Out Register (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DATAOUT [7:0]	I2C Data Out These bits store the 8-bits of data to be written to the external I2C slave devices during a write transfer.	8'b0

DATAIN: I2C Data In Register (offset: 0x14)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0

7:0	RO	DATAIN[7:0]	I2C Data In These bits store the 8-bits of data received from the external I2C slave devices during a read transaction. The DATARDY bit in the STATUS register is set to '1' when data is valid in this register.	8'b0
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STATUS: I2C Status Register (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	27'b0
4	RO	STARTERR	Start Overflow Error This bit is set when the STARTXFR register is written and a transfer is in progress. When this occurs, the write to the STARTXFR register is ignored. This bit is automatically cleared if firmware writes to the STARTXFR register when the BUSY bit cleared.	1'b0
3	RO	ACKERR	I2C Acknowledge Error Detect This bit is set when the Host controller did not receive a proper acknowledge from the I2C slave device after the transmission of a device address, address, or data out. This bit is automatically cleared when firmware writes to the STARTXFR register.	1'b0
2	RO	DATARDY	I2C Data Ready for Read This bit indicates that the receive buffer contains valid data. It is set when data is received from an I2C slave device and is transferred from the interface shift register to the DATAIN register. This bit is automatically cleared when firmware reads the DATAIN register.	1'b0
1	RO	SDOEMPTY	I2C Serial Data Out Register Empty This bit indicates that the transmit data buffer is empty. It is cleared when the DATAOUT register is written to by software, and set to '1' when transmit data is transferred from the DATAOUT register to the interface shift register. Firmware may write to the DATAOUT register when this bit is '1'.	1'b1
0	RO	BUSY	I2C State Machine Busy This bit is '1' when the I2C interface is active, and '0' when it is idle. Firmware may initiate an I2C transfer when this bit is '0', and should not modify any I2C host controller registers while it is '1'.	1'b0

STARTXFR: I2C Transfer Start Register (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	30'b0
1	R/W	NODATA	Initiate transfer without transferring data When this register is written with this bit set, an address-only transaction is initiated. If DEVADDIS is '0', the device address, direction, address and stop condition are transmitted to the I2C slave device. If DEVADDIS is '1', the address and stop condition are transmitted to the I2C slave device. This bit should be written with a '0' for normal I2C bus accesses. Note: ADDRDIS is ignored if this bit is set for a transaction.	1'b0
0	R/W	RWDIR	Read/Write Direction When this register is written with this bit set, a read transaction is initiated; when written with this bit reset, a write transaction is initiated. Note: this bit is shifted out to the I2C slave device after the device address; if DEVADDIS is '1', this bit is not shifted out to the device.	1'b0

BYTCNT: I2C Byte Counter Register (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:6	-	-	Reserved	26'b0
5:0	R/W	BYTCNT[5:0]	Byte Count used for sequential reads/writes The value written to this register plus one indicates the number of data bytes to be written to or read from the external I2C slave device. If its value is non-zero, multiple sequential read or write cycles will be issued with a single address (and/or device address).	6'b0

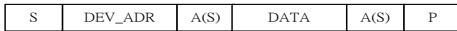
Programming Description.

Write Operation: (Single)

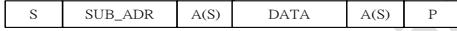


PS: the bit-width of DEV_ADR is defined in REG(CONFIG) bit[7:5]
the bit-width of SUB_ADR is defined in REG(CONFIG) bit[4:2]

PS: As REG(CONFIG) bit[1]=1'b1, the SUB_ADR field will be absent. (the waveform will be shown as below.)



PS: As REG(CONFIG) bit[0]=1'b1, the DEV_ADR field will be absent. (the waveform will be shown as below.)


Sequence Write Operation:


Action-1: SET REG(STARTXFR) bit[2]=1'b1, the "STOP" <P> field will absent.
Action-2: SET REG(STARTXFR) bit[2]=1'b0, the "STOP" <P> field will appear.


Initialization:

- 1) config the REG(CLKDIV) to decide the clock frequency of I2C
- 2) config the bit width of DEV_ADDR & SUB_ADDR by configure REG(CONFIG)

Read/Write Operation:

- 1) Write the DEV_ADDR and SUB_ADDR to REG(DEVADDR) & REG(ADDR)
- 2) Write the DATAout (REG(DATAOUT)) for write operation.
- 3) Write the operation cfg by REG(STARTXFR) to kick off the command.
- 4) Read the BUSY status by REG(STATUS) to monitor if the operation is done.
- 5) Read back the REG(DATAIN) for read operation.

Multiple Data Transfer: (write operation.)

E.g. we want to write (n+1) beats data by I2C



Burst Write Operation:

- 1) Write the DEV_ADDR and SUB_ADDR to REG(DEVADDR) & REG(ADDR)
- 2) Write (N) to REG(BYTECNT).
- 3) Write the REG(DATAOUT) for write operation.
- 4) Write the operation cfg by REG(STARTXFR) to kick off the command.
- 5) Read the SDOEMPTY bit by REG(STATUS) to monitor if the data is sent.
- 6) quit as all data is written, otherwise put the new data to the REG(DATAOUT) for write operation.
- 7) continue step 4.

Multiple Data Transfer: (read operation.)

E.g. we want to read (n+1) beats data by I2C



Burst Read Operation:

- 1) Write the DEV_ADDR and SUB_ADDR to REG(DEVADDR) & REG(ADDR)
- 2) Write (N) to REG(BYTECNT).
- 3) Write the operation cfg by REG(STARTXFR) to kick off the command.
- 4) Read the DATARDY bit by REG(STATUS) to monitor if the data is obtained.
- 5) Read REG(DATAIN) and continue step-4 until all bytes are read.

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3.19 PCM Controller

3.5.7 Features

- PCM module provides PBUS interface for register configuration and data transfer
- Two clock sources are reserved for PCM circuit. (From internal clock generator, int_pcm_clk, and from external clock source, ext_pcm_clk)
- PCM module can drive a clock out to external codec ($\text{out_clk_freq} = \text{int_pcm_clk}/n$, n = configurable by register, $1 \leq n \leq 64$).
- 2 channels PCM are available. 4~128 slots are configurable.
- Each channel supports a-law(8-bits)/u-law(8-bits)/raw-PCM(16-bits) transfer.
- Hardware converter of a-law?raw-16 and u-law ? raw-16 are implemented in design.
- Support long(8 cycle)/short(1 cycles)/configurable(interval & start point are configurable) FSYNC.
- All signals are driven by rising edge and latched by falling edge.
- Last bit of DTX will be tri-stated on falling edge.
- Begin of slot is configurable by 10 bits registers each channel.
- 32 bytes FIFO are available for each channel
- PCM interface can emulate I2S interface (16-bits data-width only).
- MSB/LSB order is configurable.
- support both of a-law/u-law(8-bits) → linear PCM(16-bits) and linear PCM(16bits) → a-law/u-law(8-bits)

3.5.8 Block Diagram

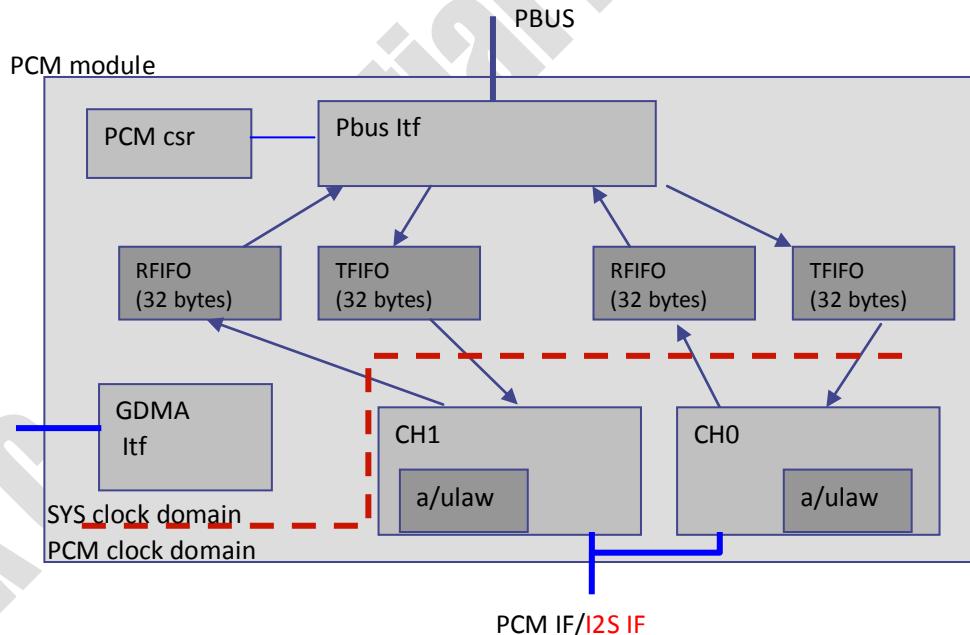


Fig. 3-12-1 3.12 PCM Controller Block Diagram

Two clocks domains are partitioned in this design. PCM converter (ulaw?raw-16bit and alaw?raw-16bit) are implemented in PCM mxDmx. The threshold of FIFO is configurable. As the threshold reaches, PCM will (a) trigger the DMA interface to notify external DMA engine to transfer data. (b) trigger the interrupts to host.

The interrupt sources include :

- threshold is reached
- FIFO under run or overrun.

- fault is detected at DMA interface.

The A-law and u-law converter is implemented base on ITU-G.711 A-law and u-law table. In this design, support both of a-law/u-law(8-bits) → linear PCM(16-bits) and linear PCM(16bits) → a-law/u-law(8-bits)

The data-flow from codec to PCM-controller (RX-flow) is shown as below:

- PCM-controller latches the data from DRX at indicated time slot and then writes it to FIFO. If FIFO full, the data will be lost.
- As the RX-FIFO reach the threshold, two actions may be taken
- As DMA_ENA=1, DMA_REQ will be asserted to request a burst transfer. And it will re-check the FIFO threshold after DMA_END is asserted by GDMA. (GDMA should be configured before channel is enabled.)
- Assert the Interrupt source to notify HOST. HOST can check RFIFO_AVAIL information then get back the data from FIFO.

The data-flow from PCM-controller to codec (TX-flow) is shown as below:

- After GDMA is configured, software should configure and enable the PCM channel.
- The empty FIFO should
- As DMA_ENA=1, DMA_REQ will be triggered to request a burst transfer. And it will re-check the FIFO threshold after DMA_END is asserted by GDMA (a burst is completed.).
- Assert the Interrupt source to notify HOST. HOST will write down the data to TX-FIFO. After that, HOST will recheck TFIFO_EMPTY information then write more data if available.

NOTICE: As DMA_ENA=1, the burst size of GDMA should less than the threshold value.

3.5.9 Register Description (base: 0x1000.2000)

GLB_CFG: GLB_CFG Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31	RW	PCM_EN	PCM enable, 1: enable 0: disable, all FSM and control register of PCM_mxDmx will be clear to default value.	0
30	RW	DMA_EN	DMA enable 1: enable DMA interface, transfer data with DMA 0: disable DMA interface, transfer data with software.	0
29:23	-	-	Reserved	0
22:20	RW	RFF_THRES	RXFIFO threshold, As threshold reach, host/dma will be notified to fill FIFO. (unit = word) It should be >2 and <6 As data in FIFO under the threshold, interrupt & DMA will be triggered.	4
19	-	-	Reserved	0
18:16	RW	TFF_THRES	TXFIFO threshold, As threshold reach, host/dma will be notified to fill FIFO. (unit = word) It should be >2 and <6. As data in FIFO over the threshold, interrupt & DMA will be triggered.	4
15:10	-	-	Reserved	0
9	RW	CH1-TX_EN	Channel-1 TX enable	0
8	RW	CH0-TX_EN	Channel-0 TX enable	0
7:2	-	-	Reserved	0
1	RW	CH1-RX_EN	Channel-1 RX enable	0

0	RW	CHO-RX_EN	Channel-0 RX enable 1: enable 0:disable	0
---	----	-----------	---	---

PCM_CFG: PCM_CFG Register (offset: 0x04)

Bits	Type	Name	Description	Initial value
31	RW	-	Reserved for future.	0
30	RW	CLKOUT_EN	Enable the PCM_CLK_OUT 1: PCM clock is provide from internal divisor. 0: PCM clock is provide from external Codec/OSC (NOTE: Normally, the register should be asserted to '1'. And it should be asserted after divider cfg & divider clock enable)	0
29:28	-	-	Reserved	
27	RW	EXT_FSYNC	FSYNC is provided by external. 1: FSYNC is provided by external 0: FSYNC is generated by internal circuit.	0
26	RW	LONG_FSYNC	FSYNC mode: 1: long FSYNC 0: short FSYNC	0
25	RW	FSYNC_POL	Polarity of FSYNC 1: FSYNC is high active 0: FSYNC is low active	1
24	RW	DTX_TRI	Tristate the DTX as fall edge as last bit. 1: Tristate the DTX 0: non-Tristate the DTX	1
23:3	-	-	Reserved	0
2:0	RW	SLOT_MODE	How many slot each PCM frame 0: 4 slots, PCM clock out/in should be 256KHz. 1: 8 slots, PCM clock out/in should be 512KHz. 2:16 slots, PCM clock out/in should be 1.024MHz. 3:32 slots, PCM clock out/in should be 2.048MHz. 4:64 slots, PCM clock out/in should be 4.096MHz. 5:128 slots, PCM clock out/in should be 8.192MHz. other: reserved. Note: When using the external clock, the frequency clock should be equal to PCM_clock out. Otherwise, the PCM_CLKin should be 8.192 MHz.	0

INT_STATUS: INT_STATUS Register (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:16	RO	-	Reserved	0
15	RW	CH1T_DMA_FAULT	Found any fault of the CH1-TX's DMA signals. (Write '1' to clear)	0
14	RW	CH1T_OVRUN	The FIFO of CH1-TX overrun(Write '1' to clear)	
13	RW	CH1T_UNRUN	The FIFO of CH1-TX underrun(Write '1' to clear)	0
12	RW	CH1T_THRES	The FIFO of CH1-TX lower than the defined threshold. (Write '1' to clear)	0
11	RW	CH1R_DMA_FAULT	Found any fault of the CH1-RX's DMA signals. (Write '1' to clear)	0
10	RW	CH1R_OVRUN	The FIFO of CH1-RX overrun(Write '1' to clear)	
9	RW	CH1R_UNRUN	The FIFO of CH1-RX underrun(Write '1' to clear)	0
8	RW	CH1R_THRES	The FIFO of CH1-RX lower than the defined threshold. (Write '1' to clear)	0
7	RW	CH0T_DMA	Found any fault of the CHO-TX's DMA signals. (Write '1' to clear)	0

		FAULT	
6	RW	CHOT_OVRUN	The FIFO of CH0-TX overrun(Write '1' to clear)
5	RW	CHOT_UNRUN	The FIFO of CH0-TX underrun(Write '1' to clear)
4	RW	CHOT_THRES	The FIFO of CH0-TX lower than the defined threshold. (Write '1' to clear)
3	RW	CHOR_DMA_FAULT	Found any fault of the CH0-RX's DMA signals. (Write '1' to clear)
2	RW	CHOR_OVRUN	The FIFO of CH0-RX overrun(Write '1' to clear)
1	RW	CHOR_UNRUN	The FIFO of CH0-RX underrun(Write '1' to clear)
0	RW	CHOR_THRES	The FIFO of CH0-RX lower than the defined threshold. (Write '1' to clear)

INT_EN: INT_EN Register (offset: 0x0c)

Bits	Type	Name	Description	Initial value
31:16	RO	-	Reserved	0
15	RW	INT15_EN	Enable INT_STATUS[15]	0
14	RW	INT14_EN	Enable INT_STATUS[14]	0
13	RW	INT13_EN	Enable INT_STATUS[13]	0
12	RW	INT12_EN	Enable INT_STATUS[12]	0
11	RW	INT11_EN	Enable INT_STATUS[11]	0
10	RW	INT10_EN	Enable INT_STATUS[10]	0
9	RW	INT9_EN	Enable INT_STATUS[9]	0
8	RW	INT8_EN	Enable INT_STATUS[8]	0
7	RW	INT7_EN	Enable INT_STATUS[7]	0
6	RW	INT6_EN	Enable INT_STATUS[6]	0
5	RW	INT5_EN	Enable INT_STATUS[5]	0
4	RW	INT4_EN	Enable INT_STATUS[4]	0
3	RW	INT3_EN	Enable INT_STATUS[3]	0
2	RW	INT2_EN	Enable INT_STATUS[2]	0
1	RW	INT1_EN	Enable INT_STATUS[1]	0
0	RW	INT0_EN	Enable INT_STATUS[0]	0

FF_STATUS: FF_STATUS Register (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:12	RO	CH1RFF_AVCNT	CH1, Available FIFO space can be read (unit=word)	0
11:8	RO	CH1TFF_EPCNT	CH1, Available FIFO space can be written (unit=word)	8
7:4	RO	CH0RFF_AVCNT	CH0, Available FIFO space can be read (unit=word)	0
3:0	RO	CH0TFF_EPCNT	CH0, Available FIFO space can be written (unit=word)	8

CH0_CFG: CH0_CFG Register (offset: 0x020)

Bits	Type	Name	Description	Initial value
31	RW	LBK_EN	Loopback enable 1: loopback (Asyn-TXFIFO → DTX → DRX → Asyn-RXFIFO) 0: normal mode	0
30	RW	EXT_LBK_EN	External loopback enable 1: external loopback enable (Ext-Codec → DRX → DTX → Ext-Codec) 0: normal mode	0
29:27	RW	CMP_MODE	Compress type select 000: disable HW converter, linear raw-data (16-bits) 010: disable HW converter, linear raw-data(8-bits), A-law or U-law (8-bits) 011: reserved 100: enable HW converter, raw-data(16-bits) → U-law mode (8-	0

			bits) (PCM bus be compress format) 101: enable HW converter, U-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format) 110: enable HW converter, raw-data(16-bits) → A-law mode (8-bits) (PCM bus be compress format) 111: enable HW converter, A-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format)	
26:10	-	-	Reserved	0
9:0	RW	TS_START	Timeslot Starting location	1

CH1_CFG: CH1_CFG Register (offset: 0x24)

Bits	Type	Name	Description	Initial value
31	RW	LBK_EN	Loopback enable 1: loopback (Asyn-TXFIFO → DTX → DRX → Asyn-RXFIFO) 0: normal mode	0
30	RW	EXT_LBK_EN	External loopback enable 1: external loopback enable (Ext-Codec → DRX → DTX → Ext-Codec) 0: normal mode	0
29:27	RW	CMP_MODE	Compress type select 000: disable HW converter, linear raw-data (16-bits) 010: disable HW converter, linear raw-data(8-bits), A-law or U-law (8-bits) 011: reserved 100: enable HW converter, raw-data(16-bits) → U-law mode (8-bits) (PCM bus be compress format) 101: enable HW converter, U-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format) 110: enable HW converter, raw-data(16-bits) → A-law mode (8-bits) (PCM bus be compress format) 111: enable HW converter, A-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format)	0
26:10	-	-	Reserved	
9:0	RW	TS_START	Timeslot Starting location	1

FSYNC_CFG: : FSYNC configuration Register (offset:0x30)

Bits	Type	Name	Description	Initial value
31	RW	Cfg_fsync_en	Enable configurable FSYNC	0
30	RW	Pos_sample	Controller sample data with 1: positive edge of PCM clock 0: negative edge of PCM clock Notice: This configuration should be "0" if DTX_TRI=1	0
29:22	-	-	Reserved	0
21:12	RW	Fsync_start	Start point of configurable FSYNC	0
11:10	-	-	Reserved	0
9:0	RW	Fsync_intv	Interval of configurable FSYNC	0

CH_CFG2: : Extended channel configuration Register (offset:0x34)

Bits	Type	Name	Description	Initial value
31:20	-	-	-	-
19	RW	CH1_RXFF_CLR	CH1 RXFIFO clear, set 1 for clear, 0 for normal operation.	0
18	RW	CH1_TXFF_CLR	CH1 TXFIFO clear, set 1 for clear, 0 for normal operation.	0
17	RW	-	Reserved	0

16	RW	CH1_LSB	Enable CH1 transmit in LSB order	0
15:4	-	-	Reserved	0
3	RW	CHO_RXFF_CLR	CHO RXFIFO clear, set 1 for clear, 0 for normal operation.	0
2	RW	CHO_TXFF_CLR	CHO TXFIFO clear, set 1 for clear, 0 for normal operation.	0
1	RW	-	Reserved	0
0	RW	CHO_LSB	Enable CH0 transmit in LSB order	0

RSV_REG16: RSV_REG16 Register (offset: 0x38)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:0	RW	SPARE_REG	Spare Register for future	0

DIVCOMP_Cfg: Integer part of Dividor Register (offset: 0x50)

Bits	Type	Name	Description	Initial value
31	RW	CLK_EN	Enable the clock divisor.	0
30:8	-	-	Reserved	0
7:0	RW	DIVCOMP	fraction part of divisor.	0

DIVINT_Cfg: Integer part of Dividor Register (offset: 0x54)

Bits	Type	Name	Description	Initial value
31:10	-	-	Reserved	0
9:0	RW	DIVINT	Integer part of divisor. Formula : $FreqOut = 1/(FreqIn * 2^8 * (DIVINT + DIVCOMP / (2^8)))$ FreqIn is always fixed to 40MHz.	0

DIGDELAY_Cfg: Digital delay configuration Register (offset: 0x60)

Bits	Type	Name	Description	Initial value
31	RW	TXD_CLR_GLT	Clear the detected glitch flag for TXD. 1:clear, 0:nothing	0
30	RW	CHEN_CLR_GLT	Clear the detected glitch flag for CHEN. 1:clear, 0:nothing	0
29:27	-	-	Reserved.	0
26	RO	TXD_GLT_ST	Status if detect glitch in TXD signal. It can be cleared by bit[31]	0
25:24	-	-	Reserved.	0
23	RO	CHEN1N_GLT_ST	Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (negedge sample)	0
22	RO	CHENON_GLT_ST	Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (negedge sample)	0
21:20	-	-	Reserved.	0
19	RO	CHEN1P_GLT_ST	Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (posedge sample)	0
18	RO	CHENOP_GLT_ST	Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (posedge sample)	0
17	RO	CHEN1PD_GLT_ST	Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (posedge sample, delay 1 cycle)	0
16	RO	CHENOPD_GLT_ST	Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (posedge sample, delay 1 cycle)	0
15	RW	TXD_DIGDLY_EN	Enable digital delay path. 1: enable, 0 disable.	0
14:13	-	-	Reserved	0
12:8	RW	TXD_DLYVAL	Delay count value, the description is same to CHEN_DLYVAL field in this register.	2
7	RW	CHEN_DIGDLY_EN	Enable digital delay path. 1: enable, 0 disable.	0
6:5	-	-	Reserved	0
4:0	RW	CHEN_DLYVAL	Delay count value,	2

			the error of delay $= \text{clk_period} * (\text{sync_delay} + \text{sync_delta} + (\text{dlycnt_cfg}) + 1)$ e.g. dlycnt_cfg=4, (sync_delay always fixes to 4), final delay = $\text{clk_period} * (2 + (-1/0/+1) + (4) + 1)$ $= \text{clk_period} * (6/7/8) = \text{clk_period} * (6^{~8})$ $= 25\text{ns} \sim 33.3\text{ns}$ NOTE: Period is $1/240\text{MHz} = 4.1667\text{ns}$ in RT3352	
--	--	--	--	--

CH0_FIFO: CH0_FIFO Register (offset: 0x80)

Bits	Type	Name	Description	Initial value
31:0	RW	CH0_FIFO	FIFO access point	0

CH1_FIFO: : CH1_FIFO Register (offset:0x84)

Bits	Type	Name	Description	Initial value
31:0	RW	CH1_FIFO	FIFO access point	0

PCM initialization flow:

Step #1: Set PCM_CFG

Step #2: Set CH0/1_CFG

Step #3: Write PCM data to FIFO CH0/1_FIFO

Step #4: Set GLB_CFG to enable the PCM and channel.

Step #5: Set divisor clock

Step #6: enable clock

Step #7: Monitor FF_STATUS to receive/transmit the other PCM data.

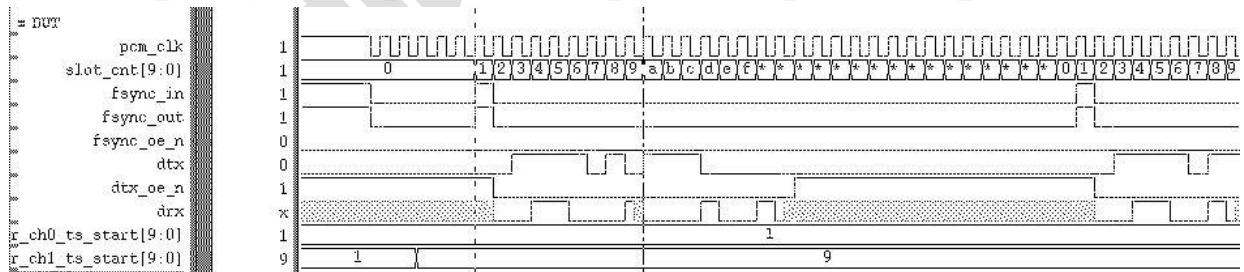
Example of PCM configuration
Case1 :

Cfg_fsync Register: Cfg_fsync_en = 0 (PS: fsync is always driven at slot_cnt=1)

CH0_CFG Register: ts_start=1

CH1_CFG Register: ts_start=9

PCM_CFG Register: LONG_FSYNC=1'b0, FSYNC_POL=1'b1, DRX_TRI=1'b0, SLOT_MODE=3'b0

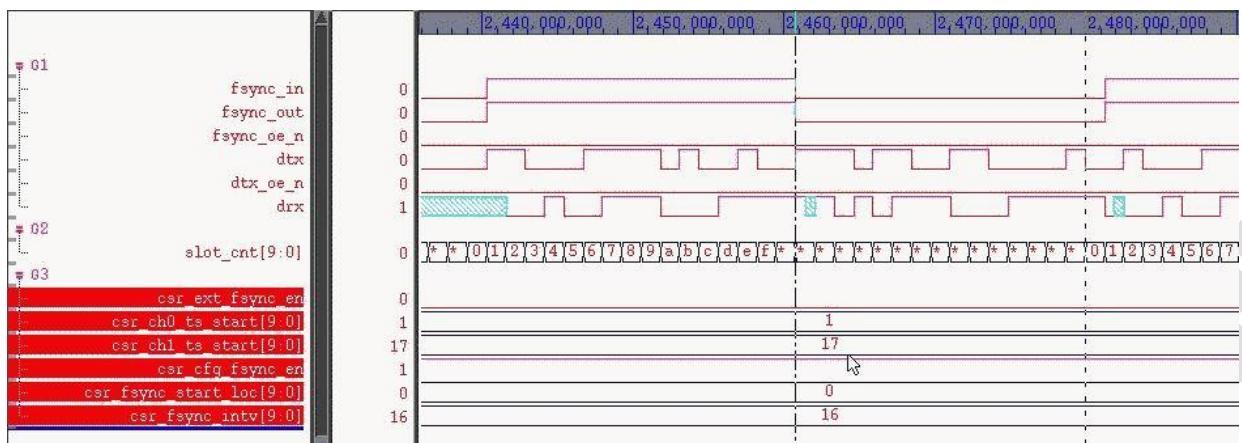

Case2 :

Cfg_fsync Register: Cfg_fsync_en = 1, start_loc=0, interval=16

CH0_CFG Register: ts_start=1

CH1_CFG Register: ts_start=17

PCM_CFG Register: LONG_FSYNC=1'b0, FSYNC_POL=1'b1, DRX_TRI=1'b0, SLOT_MODE=3'b0, RAW16-bits

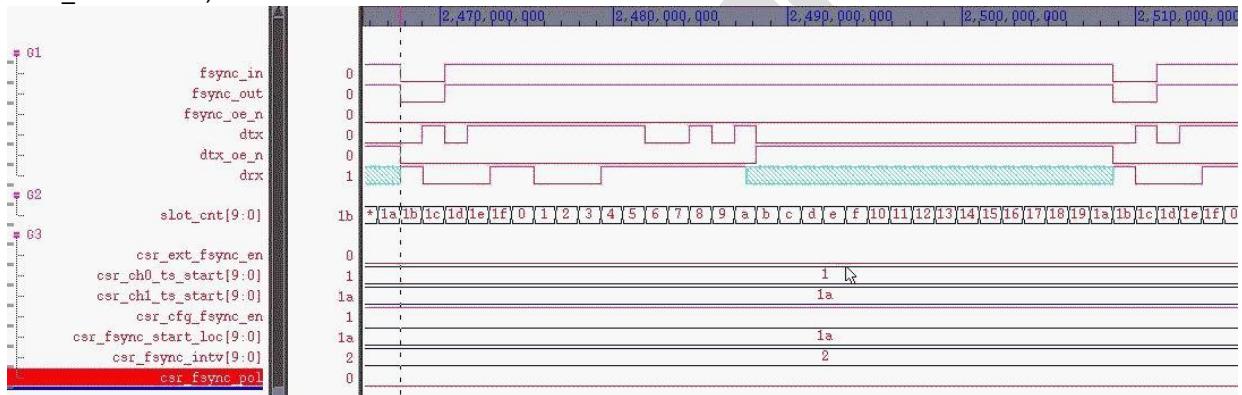

Case3 :

Cfg_fsync Register: Cfg_fsync_en = 1, start_loc=0x1A, interval=2

CHO_CFG Register: ts_start=1 (disable)

CH1_CFG Register: ts_start=0x1A

PCM_CFG Register: LONG_FSYNC=1'b0, FSYNC_POL=1'b0 (LOW active), DRX_TRI=1'b0,
 SLOT_MODE=3'b0, RAW16-bits



3.20 Generic DMA Controller

3.5.10 Features

- Support 16 DMA channels
- Support 16 DMA requests
- Programmable hardware channel priority
- Programmable DMA Burst Size (1,2,4,8,16 burst transfer)
- Support 32 bit wide transaction
- Big-endian and Little-endian support
- Support memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral transfers.
- Interrupts for each channel. They also can be masked, independently.
- Each channel transaction can be masked temporarily by the software, and released by the hardware automatically

3.5.11 Block Diagram

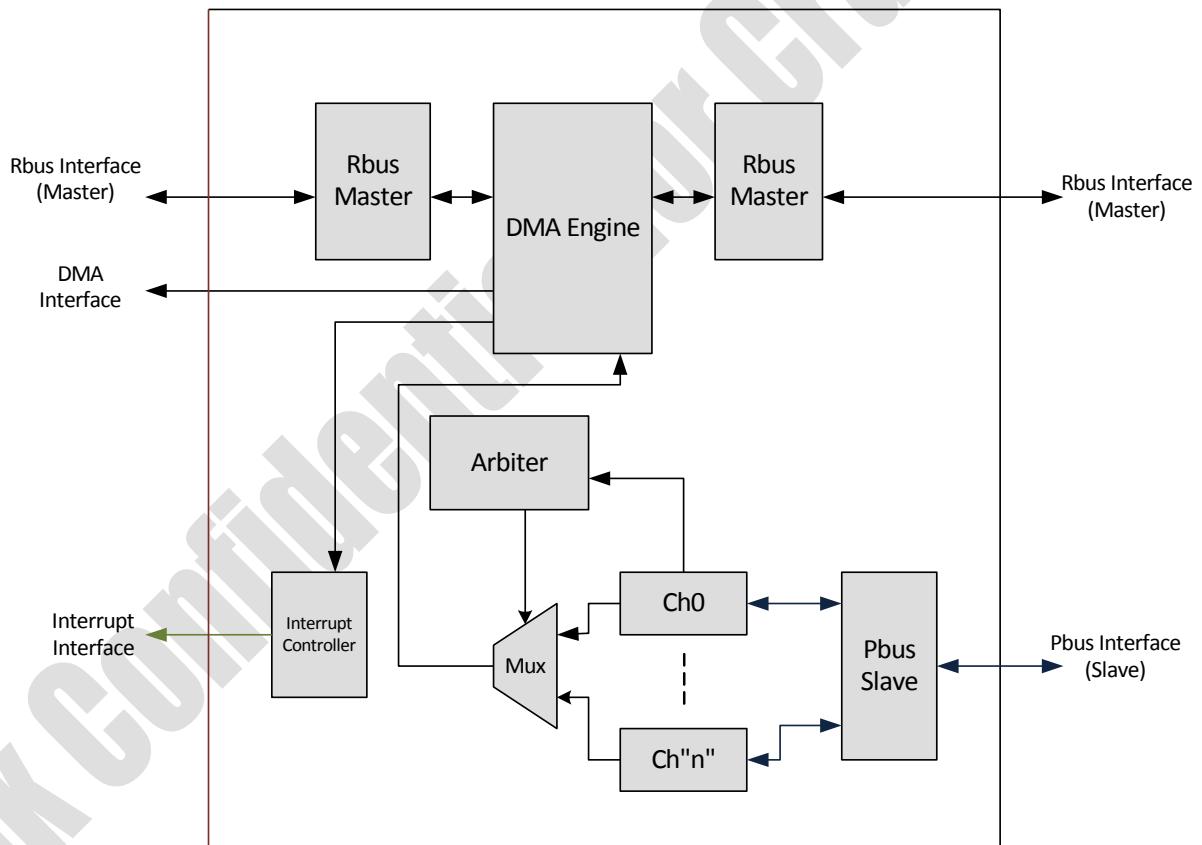


Fig.3-13-1 Generic DMA controller block diagram

3.5.12 Peripheral Channel Connection

Channel number	Peripheral
0~1	Reserved
2	I2S Controller (TXDMA)
3	I2S Controller (RXDMA)
4	PCM Controller (RDMA, channel-0)
5	PCM Controller (RDMA, channel-1)
6	PCM Controller (TDMA, channel-0)
7	PCM Controller (TDMA, channel-1)
8~15	Reserved

3.5.13 Register Description (Base: 0x1000.2800)

GDMA_SAn: GDMA Channel n Source Address

(offset: 0x000, 0x010, 0x020, 0x030, 0x040, 0x050, 0x060, 0x070, 0x080, 0x090, 0x0A0, 0x0B0, 0x0C0, 0x0D0, 0x0E0, 0x0F0)
(n:0~15)

Bits	Type	Name	Description	Initial value
31:0	R/W	CHANNEL SOURCE ADDRESS	Channel Source Address: This register contains the source address information	32'b0

GDMA_DAn: GDMA Channel n Destination Address

(offset: 0x004, 0x014, 0x024, 0x034, 0x044, 0x054, 0x064, 0x074, 0x084, 0x094, 0x0A4, 0x0B4, 0x0C4, 0x0D4, 0x0E4, 0x0F4)
(n:0~15)

Bits	Type	Name	Description	Initial value
31:0	R/W	CHANNEL DESTINATION ADDRESS	Channel Destination Address: This register contains the destination address information	32'b0

GDMA_CT0n: GDMA Channel n Control Register 0

(offset: 0x008, 0x018, 0x028, 0x038, 0x048, 0x058, 0x068, 0x078, 0x088, 0x098, 0x0A8, 0x0B8, 0x0C8, 0x0D8, 0x0E8, 0x0F8)
(n:0~15)

Bits	Type	Name	Description	Initial value
31:16	R/W	Transfer Count	These registers contain the number of the data bytes needed to be transfer.	16'b0
15:8	--	-	Reserved	8'b0
7	R/W	Source Burst Mode	The value represents the source burst mode 'b0: incremental mode 'b1: fix mode	1'b0
6	R/W	Destination Burst Mode	The value represents the destination burst mode 'b0: incremental mode 'b1: fix mode	1'b0

5:3	R/W	Burst Size	The number of the transfer for burst transaction. 'b000: 1 transfer 'b001: 2 transfer 'b010: 4 transfer 'b011: 8 transfer 'b100: 16 transfer others: undefined	3'b0
2	R/W	Transmit Done Interrupt Enable	Transmit done interrupt enable. 'b1:Enable 'b0:Disable	1'b0
1	R/W	Channel Enable	Enable the channel 'b1: Enable 'b0: Disable This bit will be de-asserted by the hardware when the transaction is done.	1'b0
0	R/W	Hardware/Software Mode Select	Hardware/Software Mode Select 'b1: Software Mode 'b0: Hardware Mode In software mode, the data transfer will start when the Channel Enable bit is set. In hardware mode, the data transfer will start when the DMA Request is asserted.	1'b0

GDMA_CT1n: GDMA Channel n Control Register 1

(offset: 0x00C, 0x01C, 0x02C, 0x03C, 0x04C, 0x05C, 0x06C, 0x07C, 0x08C, 0x09C, 0x0AC, 0x0BC, 0x0CC, 0x0DC, 0x0EC, 0x0FC)

(n:0~15)

Bits	Type	Name	Description	Initial value
31:22	--	-	Reserved	10'b0
21:16	R/W	Source DMA Request	The value represents the source DMA request. 0: DMA_REQ0 1: DMA_REQ1 2: DMA_REQ2 ... n: DMA_REQn 32: The source of the transfer is memory others: undefined	6'b0
15:14	--	-	Reserved	2'b0
13:8	R/W	Destination DMA Request	The value represents the destination DMA request. 0: DMA_REQ0 1: DMA_REQ1 2: DMA_REQ2 ... n: DMA_REQn 32: The destination of the transfer is memory others: undefined	6'b0
7:3	R/W	Next Unmasked Channel	The value represents the next unmasked channel. When the transaction is done, the hardware will clear the Channel Mask bit of the next unmasked channel. 0: Channel 0 1: Channel 1 2: Channel 2 ...	5'b0

			n: Channel n If the hardware doesn't need to clear any Channel Mask bit, these bits must be set to their own channel.	
2	R/W	Coherent Interrupt Enable	When set to 1'b1, GDMA will issue a dummy READ to Destination after last WRITE to Destination. This can ensure the last WRITE arrived at MEM and avoid race problem between interrupt and data to MEM. (please don't set this to 1'b1 if destination is not MEM).	1'b0
1	R/W	Channel Unmasked Interrupt Enable	Channel unmasked interrupt enable. 'b1:Enable 'b0:Disable When this bit is set, an interrupt will be asserted when the hardware wants to clear the Channel Mask bit and the Channel Mask bit is 0 originally.	1'b0
0	R/W	Channel Mask	Channel Mask 'b1: This channel is masked 'b0: This channel is not masked When this channel mask is set, the GDMA transaction will not start until this bit is clear by the hardware.	1'b0

GDMA_UNMASKINT: GDMA Unmasked Interrupt Status Register (offset: 0x200)

Bits	Type	Name	Description	Initial value
31:0	R/W1C	Unmasked Interrupt Status	This register contains the unmasked interrupt status. This bit will be set when the hardware wants to clear the Channel Mask bit and the Channel Mask bit is 0 originally. Bitn~bit0 is for channel-n ~ channel-0, respectively.	32'b0

GDMA_DONEINT: GDMA Interrupt Status Register (offset: 0x204)

Bits	Type	Name	Description	Initial value
31:0	R/W1C	Transmit Done Interrupt Status	This register contains the transmit-done interrupt status. Bitn~bit0 is for channel-n ~ channel-0, respectively.	32'b0

GDMA_GCT: GDMA Global Control Register (offset: 0x220)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	-
4:3	RO	Total channel number	2'b0: 8 channel 2'b1: 16 channel 2'b2: 32 channel 2'b3: Reserved	2'b1
2:1	RO	IP version	Version of GDMA core	2'b2
0	R/W	Arbitration Selection	Select the channel arbitration method. 1'b0: Channel-0 has the highest priority. Channel-1~ Channel-n are round-robin. 1'b1: Channel-0 doesn't have the highest priority. Channel-0~Channel-n are round-robin.	1'b0

GDMA_REQSTS: GDMA Request Status Register (offset: 0x2A0)

Bits	Type	Name	Description	Initial value
31:0	R	GDMA Request Signal Status	This register contains the GDMA Request Signals status Bitn~bit0 is for GDMA_REQn ~ GDMA_REQ0, respectively.	32'b0

GDMA_ACKSTS: GDMA Acknowledge Status Register (offset: 0x2A4)

Bits	Type	Name	Description	Initial value
31:0	R	GDMA Acknowledge Signal Status	This register contains the GDMA Acknowledge Signals status Bitn~bit0 is for GDMA_ACKn ~ GDMA_ACK0, respectively.	32'b0

GDMA_FINSTS: GDMA Finish Status Register (offset: 0x2A8)

Bits	Type	Name	Description	Initial value
31:0	R	GDMA Finish Signal Status	This register contains the GDMA Finish Signals status Bitn~bit0 is for GDMA_FINISHn ~ GDMA_FINISH0, respectively.	32'b0

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3.21 SPI Controller

3.5.14 Features

- Supports up to 2 SPI master operations
- Programmable clock polarity
- Programmable interface clock rate
- Programmable bit ordering
- Firmware-controlled SPI enable
- Programmable payload (address + data) length

3.5.15 Block Diagram

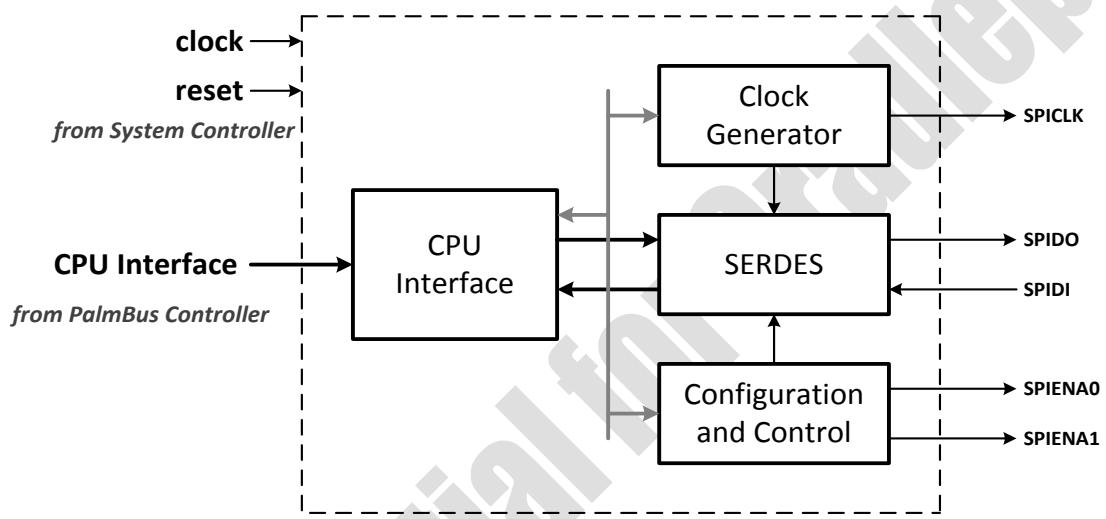


Fig. 3-14-1 SPI controller Block Diagram

3.5.16 Register Description (base: 0x1000.0B00)

SPISTAT0: SPI Interface 0 Status (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	31'b0
0	RO	BUSY	SPI transfer in progress 0: The SPI interface is inactive. 1: An SPI transfer is in progress. Note: This bit must be '0' before initiating a transfer. Any attempt to start a data transfer will be ignored if this bit is a '1'.	1'b0

SPICFG0: SPI Interface 0 Configuration (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:9	-	-	Reserved	23'b0
8	R/W	MSBFIRST	Bit transfer order 0: LSB bits of data sent/received first. 1: MSB bits of data sent/received first. Note: This bit applies to both the command and data.	1'b1
7	-	-	Reserved	1'b0
6	R/W	SPICLKPOL	SPI clock default state 0: The default state of the SPICLK is logic '0'. 1: The default state of the SPICLK is logic '1'. Note: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).	1'b0
5	R/W	RXCKEDGE	SPI clock default state	1'b0

			0: Data is captured on the rising edge of the SPICLK signal. 1: Data is captured on the falling edge of the SPICLK signal.	
4	R/W	TXCKEDGE	SPI clock default state 0: Data is transmitted on the rising edge of the SPICLK signal. 1: Data is transmitted on the falling edge of the SPICLK signal.	1'b0
3	R/W	HIZSPI	Tri-state all SPI pin 0: SPICLK and SPIENA pin are driven. 1: SPICLK and SPIENA pin are tri-stated. Note: This bit overrides all normal functionality.	1'b0
2:0	R/W	SPICLK[2:0]	SPI clock divide control (the rate in following table should be change in the future) 0: SPICLK rate is system clock rate / 2 1: SPICLK rate is system clock rate / 4 2: SPICLK rate is system clock rate / 8 3: SPICLK rate is system clock rate / 16 4: SPICLK rate is system clock rate / 32 5: SPICLK rate is system clock rate / 64 6: SPICLK rate is system clock rate / 128 7: SPICLK is disabled	3'b0

SPICTL0: SPI Interface 0 Control (offset: 0x14)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	28'b0
3	R/W	HIZSDO	Tri-state data out 0: The SPIDO pin remains driven after the cycle is complete. 1: The SPIDO pin is tri-stated after the cycle is complete. Note: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.	1'b0
2	W	STARTWR	Start SPI write transfer When this bit is written with a '1', the contents of the SPIDATA register are transferred to the SPI slave device. Writing a '0' to this register has no effect. Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	1'b0
1	W	STARTRD	When this bit is written with a '1', a read from the SPI slave is started; the read data is placed in the SPIDATA register. Writing a '0' to this register has no effect. Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	1'b0
0	R/W	SPIENA	0: The SPIENA pin is negated. 1: The SPIENA pin is asserted.	1'b0

SPIDATA0: SPI Interface 0 Data (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	SPIDATA[7:0]	This register is used for command/data transfers on the SPI interface. The use of this register is given below: Write: the bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA	8'b0

		[0];bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits. Read: the command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register.	
--	--	---	--

SPISTAT1: SPI Interface 1 Status (offset: 0x40)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	30'b0
0	RO	BUSY	SPI transfer in progress 0: The SPI interface is inactive. 1: An SPI transfer is in progress. Note: This bit must be '0' before initiating a transfer. Any attempt to start a data transfer will be ignored if this bit is a '1'.	1'b0

SPICFG1: SPI Interface 1 Configuration (offset: 0x50)

Bits	Type	Name	Description	Initial value
31:9	-	-	Reserved	23'b0
8	R/W	MSBFIRST	Bit transfer order 0: LSB bits of data sent/received first. 1: MSB bits of data sent/received first. Note: This bit applies to both the command and data.	1'b1
7	-	-	Reserved	1'b0
6	R/W	SPICLKPOL	SPI clock default state 0: The default state of the SPICLK is logic '0'. 1: The default state of the SPICLK is logic '1'. Note: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).	1'b0
5	R/W	RXCKEDGE	SPI clock default state 0: Data is captured on the rising edge of the SPICLK signal. 1: Data is captured on the falling edge of the SPICLK signal.	1'b0
4	R/W	TXCKEDGE	SPI clock default state 0: Data is transmitted on the rising edge of the SPICLK signal. 1: Data is transmitted on the falling edge of the SPICLK signal.	1'b0
3	R/W	HIZSPI	Tri-state all SPI pin 0: SPICLK and SPIENA pin are driven. 1: SPICLK and SPIENA pin are tri-stated. Note: This bit overrides all normal functionality.	1'b0
2:0	R/W	SPICLK[2:0]	SPI clock divide control (the rate in following table should be change in the future) 0: SPICLK rate is system clock rate / 2 1: SPICLK rate is system clock rate / 4 2: SPICLK rate is system clock rate / 8 3: SPICLK rate is system clock rate / 16 4: SPICLK rate is system clock rate / 32 5: SPICLK rate is system clock rate / 64 6: SPICLK rate is system clock rate / 128 7: SPICLK is disabled	3'b0

SPICTL1: SPI Interface 1 Control (offset: 0x54)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	28'b0

3	R/W	HIZSDO	Tri-state data out 0: The SPIDO pin remains driven after the cycle is complete. 1: The SPIDO pin is tri-stated after the cycle is complete. Note: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.	1'b0
2	W	STARTWR	Start SPI write transfer When this bit is written with a '1', the contents of the SPIDATA register are transferred to the SPI slave device. Writing a '0' to this register has no effect. Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	1'b0
1	W	STARTRD	When this bit is written with a '1', a read from the SPI slave is started; the read data is placed in the SPIDATA register. Writing a '0' to this register has no effect. Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	1'b0
0	R/W	SPIENA	0: The SPIENA pin is negated. 1: The SPIENA pin is asserted.	1'b0

SPIDATA1: SPI Interface 1 Data (offset: 0x60)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	SPIDATA[7:0]	This register is used for command/data transfers on the SPI interface. The use of this register is given below: Write: the bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA [0]; bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits. Read: the command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register.	8'b0

SPIARB SPI Interface ARBITER (offset: 0xF0) (Note: This register must be configured when SPI interface 1 want to be activated)

Bits	Type	Name	Description	Initial value
31	R/W	ARB_EN	Arbiter Enable 0: Only SPI interface 0 will work. 1: SPI Interface 0/1 will work concurrently.	1'b0
30:2	-	-	Reserved	29'b0
1	R/W	SPI1_POR	The chip enable polarity indicator for SPI interface 1 0: Indicate the chip enable is low active 1: Indicate the chip enable is high active	1'b0
0	R/W	SPIO_POR	The chip enable polarity indicator for SPI interface 0 0: Indicate the chip enable is low active 1: Indicate the chip enable is high active	1'b0

3.6 I²S Controller

3.6.1 Features

- I²S transmitter/Receiver, which can be configured as master or slave.
- Support 16-bit data, sample rate 8Khz, 16Khz, 22.05Khz, 44.1Khz, and 48Khz
- Support stereo audio data transfer.
- 32 bytes FIFO are available for data transmission.
- Support GDMA access
- Support 12Mhz bit clock from external (as slave mode)

3.6.2 Block Diagram

The block diagram of I²S Transmitter is shown as below.

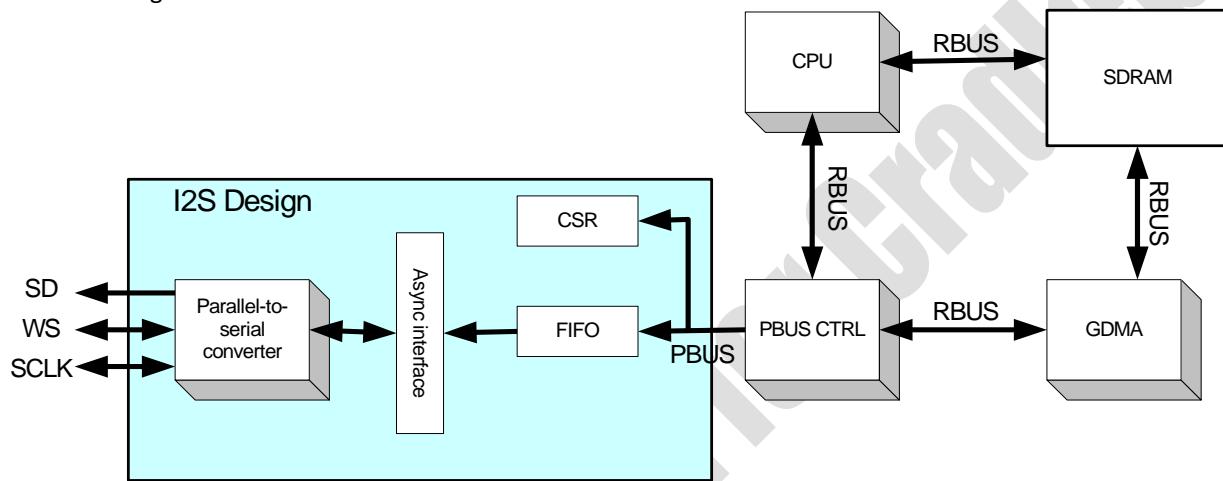


Fig. 3-15-1 The block diagram of I²S Transmitter

The I²S interface consists of two separate cores, a transmitter and a receiver. Both can operate in either master or slave mode. Here we will design only the transmitter in master or slave mode.

I²S signal timing for I²S data format:

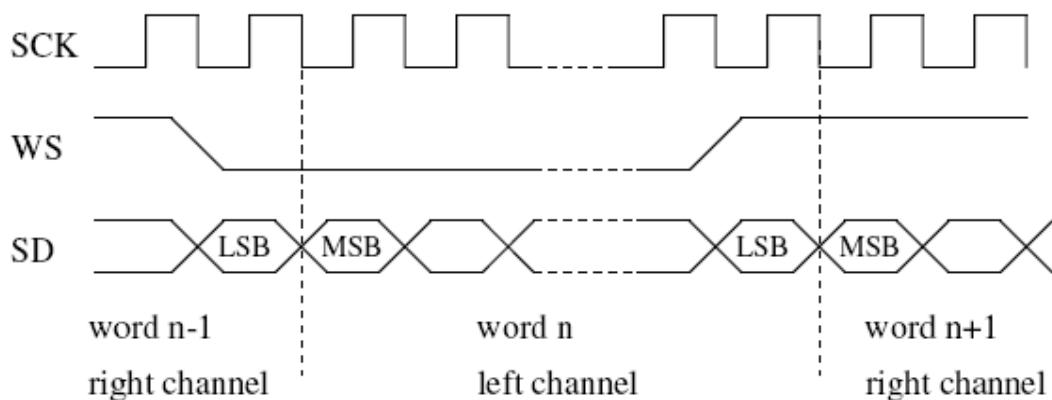


Fig. 3-15-2 I²S Transmitter/Receiver

Serial data is transmitted in 2's complement with the MSB first. The transmitter always sends the MSB of the next word one clock period after the WS changes. Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The word select line indicates the channel being transmitted:

- WS = 0; channel 1 (left);
- WS = 1; channel 2 (right).

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next Word.

3.6.3 Register Description of I2S (base:1000.0A00)

I2S_CFG (offset: 0x00, default: 0x0000_0840)

Bits	Type	Name	Description	Initial value
31	R/W	I2S_EN	I2S enable, 1: enable 0: disable, all control registers of I2S will be clear to default value.	0
30	R/W	DMA_EN	DMA Enable 1: enable dma access 0: disable dma access	0
29:25		Reserved	Reserved	
24	R/W	TX_EN	Transmitter on/off control 1: Enable transmitter 0: Disable transmitter	0
23:21		Reserved	Reserved	
20	R/W	RX_EN	Receiver on/off control 1: Enable receiver 0: Disable receiver	0
19:17	-	Reserved	Reserved	
16	R/W	SLAVE_MODE	Master os Slave 0: Master: using internal clock 1: Slave: using external clock	1
15		Reserved	Reserved	
14:12	R/W	RX_FF_THRES	FIFO threshold, As threshold reach, host/dma will notify to fill FIFO. (Unit = word) It should be >2 and <6	4
11	-	Reserved	Reserved	0
10	-	Reserved	Reserved	0
9	-	Reserved	Reserved	0
8:7	-	Reserved	Reserved	
6:4	R/W	TX_FF_THRES	FIFO threshold, As threshold reach, host/dma will notify to fill FIFO. (Unit = word) It should be >2 and <6	4
3	-	Reserved	Reserved	0
2	-	Reserved	Reserved	0
1	-	Reserved	Reserved	0
0	-	Reserved	Reserved	0

INT_STATUS (offset: 0x04, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	RO	Reserved	Reserved	0
7	R/W	RX_DMA_FAULT	Find any fault in RX's DMA signals	0
6	R/W	RX_OVRUN	The RX FIFO is overflow (Write '1' to clear)	0
5	R/W	RX_UNRUN	The RX FIFO is underflow (Write '1' to clear)	0
4	R/W	RX_THRES	The RX FIFO is lower than the defined threshold. (Write '1' to clear)	0
3	R/W	TX_DMA_FAULT	Find any fault in TX's DMA signals	0
2	R/W	TX_OVRUN	The TX FIFO is overflow (Write '1' to clear)	0
1	R/W	TX_UNRUN	The TX FIFO is underflow (Write '1' to clear)	0
0	R/W	TX_THRES	The FIFO is lower than the defined threshold. (Write '1' to clear)	0

INT_EN (offset: 0x08, default: 0x0)

Bits	Type	Name	Description	Initial value
31:9	RO	Reserved	Reserved	0
7	R/W	RX_INT3_EN	Enable INT_STATUS[7]	0
6	R/W	RX_INT2_EN	Enable INT_STATUS[6]	0
5	R/W	RX_INT1_EN	Enable INT_STATUS[5]	0
4	R/W	RX_INTO_EN	Enable INT_STATUS[4]	0
3	R/W	TX_INT3_EN	Enable INT_STATUS[3]	0
2	R/W	TX_INT2_EN	Enable INT_STATUS[2]	0
1	R/W	TX_INT1_EN	Enable INT_STATUS[1]	0
0	R/W	TX_INTO_EN	Enable INT_STATUS[0]	0

FF_STATUS (offset: 0xc, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	Reserved	Reserved	0
7:4	RO	RX_AV_CNT	Available FIFO space can be read	0
3:0	RO	TX_EP_CNT	Available FIFO space can be written	4'h8

TX_FIFO_WREG(offset: 0x10, default:0x0)

Bits	Type	Name	Description	Initial value
31:0	W	TX_FIFO_WDATA	Write data buffer	0

RX_FIFO_RREG(offset: 0x14, default:0x0)

Bits	Type	Name	Description	Initial value
31:0	R	RX_FIFO_WDATA	Read data buffer	0

I2S_CFG1 (offset: 0x18, default:0x0)

Bits	Type	Name	Description	Initial value
31	R/W	LBK_EN	Loop Back Enable 0: normal mode 1: loop back mode Async_txFifio → Tx → Rx → Async_rxFifio	0
30	R/W	EXT_LBK_EN	External Loop Back Enable 0: normal mode	0

			1: external loop back enable External A/D → Rx → Tx → External D/A	
29:2	-	Reserved	Reserved	
1:0	-	Reserved	Reserved	0

DIVCOMP_Cfg: Integer part of Dividor Register (offset: 0x20)

Bits	Type	Name	Description	Initial value
31	RW	CLK_EN	Enable the clock divisor.	0
30:9	-	-	Reserved	0
8:0	RW	DIVCOMP	fraction part of divisor.	0

DIVINT_Cfg: Integer part of Dividor Register (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:10	-	-	Reserved	0
9:0	RW	DIVINT	Integer part of divisor. Formula : $FreqOut = FreqIn * (1/2) * \{1 / [DIVINT+DIVCOMP/(512)]\}$ FreqIn is always fixed to 40MHz.	0

3.7 Memory Controller

3.7.1 Features

- Support 1 SDRAM/DDR2 (16b/32b) chip selects
- Support 128MB(SDRAM)/256MB(DDR2) per chip select
- Support SDRAM transaction overlapping by early active and hidden pre-charge
- Support user SDRAM Init commands
- Support 4 banks per SDRAM chip select
- SDRAM burst length: 4 (fixed)
- DDR2 burst length: 4/8(programmable)
- Support Wrap-4 transfer
- Support Bank-Raw-Column and Raw-Bank-Column address mapping

3.7.2 Block Diagram

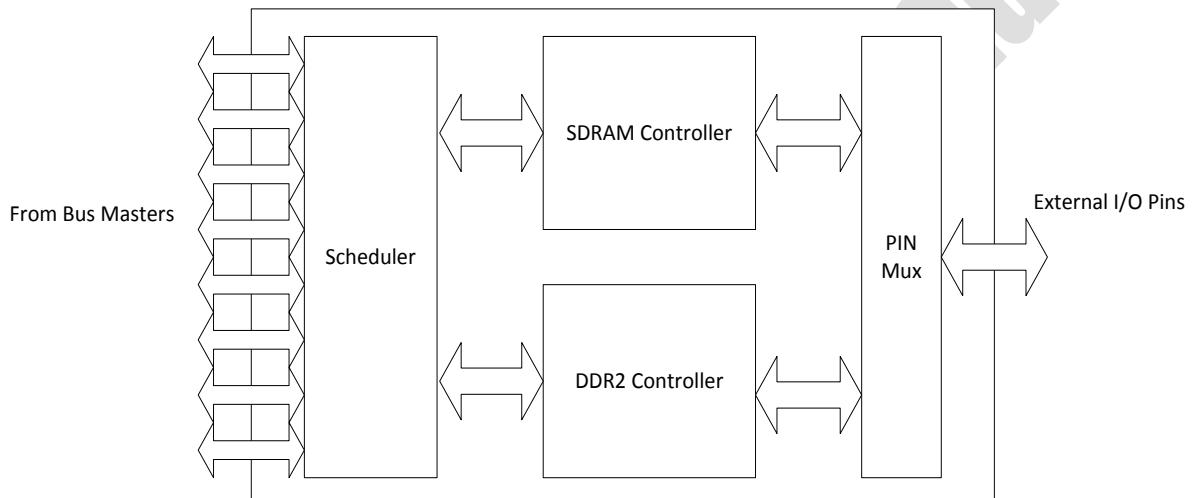


Fig. 3-16-1 SRAM/SDRAM controller Block Diagram

3.7.2.1 SDRAM Initialization Sequence

SDRAMs require an initialization sequence before they are ready for reading and writing. The initialization sequence is described below.

- Step #1: setting SDRAM related timing in SDRAM_CFG0
- Step#2: setting SDRAM size and refresh time in SDRAM_CFG1 register with
SDRAM_INIT_START = 1
- Step#3: Read SDRAM_INIT_DONE in SDRAM_CFG1 register
- Step#4: if SDRAM_INIT_DONE !=1, go to Step#3, else SDRAM initialization sequence finished

Turn off power saving

Size	DRAM width (16bit), total bus width 16	DRAM width (16bit), total bus width 32	DRAM width (32bit), total bus width 32
16Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0000600	SDRAM0: 0xD1825272, SDRAM1: 0xA1000600	N/A
64Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0010600	SDRAM0: 0xD1825272, SDRAM1: 0xA1010600	SDRAM0: 0xD1825272, SDRAM1: 0xA1000600
128Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0110600	SDRAM0: 0xD1825272, SDRAM1: 0xA1110600	SDRAM0: 0xD1825272, SDRAM1: 0xA1010600
256Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0120600	SDRAM0: 0xD1825272, SDRAM1: 0xA1120600	SDRAM0: 0xD1825272, SDRAM1: 0xA1110600
512Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0220600	SDRAM0: 0xD1825272, SDRAM1: 0xA1220600	SDRAM0: 0xD1825272, SDRAM1: 0xA1120600
1024Mb	N/A	N/A	N/A
2048Mb	N/A	N/A	N/A

Turn on power saving with precharge power down mode

Size	DRAM width (16bit), total bus width 16	DRAM width (16bit), total bus width 32	DRAM width (32bit), total bus width 32
16Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0000600	SDRAM0: 0xD1825272, SDRAM1: 0xB1000600	N/A
64Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0010600	SDRAM0: 0xD1825272, SDRAM1: 0xB1010600	SDRAM0: 0xD1825272, SDRAM1: 0xB1000600
128Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0110600	SDRAM0: 0xD1825272, SDRAM1: 0xB1110600	SDRAM0: 0xD1825272, SDRAM1: 0xB1010600
256Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0120600	SDRAM0: 0xD1825272, SDRAM1: 0xB1120600	SDRAM0: 0xD1825272, SDRAM1: 0xB1110600
512Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0220600	SDRAM0: 0xD1825272, SDRAM1: 0xB1220600	SDRAM0: 0xD1825272, SDRAM1: 0xB1120600
1024Mb	N/A	N/A	N/A
2048Mb	N/A	N/A	N/A

Turn on power saving with active power down mode

Size	DRAM width (16bit), total bus width 16	DRAM width (16bit), total bus width 32	DRAM width (32bit), total bus width 32
16Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8000600	SDRAM0: 0xD1825272, SDRAM1: 0xB9000600	N/A (ISSI have no this size)
64Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8010600	SDRAM0: 0xD1825272, SDRAM1: 0xB9010600	SDRAM0: 0xD1825272, SDRAM1: 0xB9000600
128Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8110600	SDRAM0: 0xD1825272, SDRAM1: 0xB9110600	SDRAM0: 0xD1825272, SDRAM1: 0xB9010600
256Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8120600	SDRAM0: 0xD1825272, SDRAM1: 0xB9120600	SDRAM0: 0xD1825272, SDRAM1: 0xB9110600
512Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8220600	SDRAM0: 0xD1825272, SDRAM1: 0xB9220600	SDRAM0: 0xD1825272, SDRAM1: 0xB9120600
1024Mb	N/A	N/A	N/A
2048Mb	N/A	N/A	N/A

3.7.2.2 DDR2 Initialization Sequence

DDR require an initialization sequence before they are ready for reading and write.
Initialization sequence is described below.

- Step #1: Wait for 200us to set "0" in bit10 in address "0x1000_0034"
- Step #2: Read bit[21] of DDR_CFG1 and wait for it become "1"
- Step #3: Set DDR size and data width in DDR_CFG1 (Please refer the table)

DDR SIZE	DDR WIDTH	DDR Total Width	DDR_CFG1	DDR2
256Mb	8	16	32'h222D2323	V
256Mb	8	32	32'h222D3323	V
256Mb	16	16	32'h222E2323	V
256Mb	16	32	32'h222E3323	V
512Mb	8	16	32'h22312323	V
512Mb	8	32	32'h22313323	V
512Mb	16	16	32'h22322323	V
512Mb	16	32	32'h22323323	V
1Gb	8	16	32'h22352323	V
1Gb	16	16	32'h22362323	V
1Gb	16	32	32'h22363323	V
2Gb	16	16	32'h223A2323	V

For DDR2 Performance, need to follow this CFG0 table for different DDR2 size
DDR Frequency: 133MHz

DDR SIZE	DDR WIDTH	DDR Total Width	DDR_CFG0(tRFC/tREFI)	DDR2
256Mb	8	16	32'h2498E400	V
256Mb	8	32	32'h2498E400	V
256Mb	16	16	32'h2498E400	V
256Mb	16	32	32'h2498E400	V
512Mb	8	16	32'h24992400	V
512Mb	8	32	32'h24992400	V
512Mb	16	16	32'h24992400	V
512Mb	16	32	32'h24992400	V
1Gb	8	16	32'h24996400	V
1Gb	16	16	32'h24996400	V
1Gb	16	32	32'h24996400	V
2Gb	16	16	32'h249A2400	V

Note: The system only have 256MB(2Gb) memory space for DRAM, so there are no some types of combination of DDR2 (Please refer the list table)

DDR SIZE	DDR WIDTH	DDR Total Width
1Gb	8	32
2Gb	8	16
2Gb	8	32
2Gb	16	32

3.7.3 Register Description (base: 0x1000.0300)

SDRAM_CFG0: SDRAM Configuration 0 (offset: 0x00)

Bits	Type	Name	Description	Initial value
31	RO	ALWAYS_ONE	Use as an identification for Rbus controller	1'b1
30-29	-	-	Reserved	2'b00
28	R/W	TWR	Write Recovery time number of system clock cycles – 1.	1'b1
27:24	R/W	TMRD	LOAD MODE to any other command delay number of system clock cycles – 1.	4'b0001
23:20	R/W	TRFC	AUTO REFRESH period number of system clock cycles – 1.	4'b1001
19:18	-	-	Reserved	2'b00
17:16	R/W	TCAS	READ command to data valid delay (CAS latency) in number of system clock cycles – 1.	2'b10
15:12	R/W	TRAS	ACTIVE to PRECHARGE command delay in number of system clock cycles – 1.	4'b0101
11:10	-	-	Reserved	2'b00
9:8	R/W	TRCD	ACTIVE to READ or WRITE delay in number of system clock cycles – 1.	2'b10
7:4	R/W	TRC	ACTIVE to ACTIVE command period in number of system clock cycles -1	4'b1000
3:2	-	-	Reserved	2'b00
1:0	R/W	TRP	PRECHARGE command period in number of system clock cycles –1.	2'b10

SDRAM_CFG1: SDRAM Configuration 1 (offset: 0x04)

Bits	Type	Name	Description	Initial value
31	R/W	SDRAM_INIT_START	Write 1 to perform SDRAM initialization sequence. Can not set it to zero after initialization.	1'b0
30	RO	SDRAM_INIT_DONE	0: SDRAM has not been initialized 1: SDRMA has been initialized	1'b0
29	R/W	RBC_MAPPING	1 : {ROW ADDR, BANK ADDR, COL ADDR} address mapping scheme 0 : {BANK ADDR, ROW ADDR, COL ADDR} address mapping scheme	1'b0
28	R/W	PWR_DOWN_EN	1 : Enable SDRAM precharge power down mode to save standby power. When enabled, SDRAM will go 0 : Disable SDRAM precharge power down mode	1'b0
27	R/W	PWR_DOWN_MODE	1 : Reserved 0 : Precharge power down mode	1'b0
26:25	-	-	Reserved	2'b0
24	R/W	SDRAM_WIDTH	Number of SDRAM data bus bits : (#TBD#) 0 : 16 bits 1 : 32 bits (default)	1'b1
23:22	-	-	Reserved	2'b0
21:20	R/W	NUMCOLS	Number of Column address bits : 0 : 8 Column address bits 1 : 9 Column address bits (default) 2 : 10 Column address bits 3: 11 Column address bits	2'b01
19:18	-	-	Reserved	2'b00
17:16	R/W	NUMROWS	Number of Row address bits : 0 : 11 Row address bits 1 : 12 Row address bits (default) 2 : 13 Row address bits 3: 14 Row address bits (not allocable if boot from NAND flash is enabled)	2'b10
15:0	R/W	TREFR	AUTO REFRESH period in number of SDRAM clock cycles – 1.	16'h0600

*PS: SDRAM Self Refresh Mode and Power Down will be supported later.

DRAM_ARB_CFG: DRAM arbiter configuration (offset: 0x08)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	1'b0
30	R/W	Round_Robin_EN	Enable round-robin policy for arbiter 0: Disable 1: Enable	1'b0
29	R/W	CPU_POST_LOCK_EN	Enable arbiter to lock cpu for a while after service cpu 0: Disable 1: Enable	1'b0
28	R/W	CPU_PRE_LOCK_EN	Enable arbiter to lock cpu when detect the cpu command present in OCP bus 0: Disable 1: Enable	1'b0
27:16	-	0	Reserved	12'b0
15:8	R/W	DMA_PENDING_CNT	The counter is used to cancel the cpu lock when DMA request was pending for specified period clock count. The valid value is 1~255, "0" means to cancel the cpu pre/post lock function	8'b0
7:4	-	-	Reserved	
3:0	R/W	CPU_LOCK_CNT	The counter is used to count the period of cpu post lock after service the cpu. The valid value is 1~15. "0" means post lock is 0 cycles	4'b0

Reserved (offset: 0x0C)
ILL_ACC_ADDR: Illegal Access Address Capture (offset: 0x10)

Bits	Type	Name	Description	Initial value
31: 0	RO	ILL_ACC_ADDR	If any bus masters (including CPU) issue illegal accesses (e.g. accessing to reserved memory space, non-double-word accessing to configuration registers), the address of the illegal transaction is captured in this register. An illegal interrupt will generate to indicate this exception.	32'b0

ILL_ACC_TYPE: Illegal Access TYPE Capture (offset: 0x14)

Bits	Type	Name	Description	Initial value
31	RO, W1C	ILL_INT_STATUS	1 : Indicate the illegal access interrupt is pending 0 : Indicate the illegal access interrupt is cleared Write 1 to this bit will clear both ILL_ACC_ADDR and ILL_ACC_TYPE registers and thus clear the ILL_INT_STATUS.	1'b0
30	RO	ILL_ACC_WR	Indicate the access type of the illegal access 1 : illegal access is write 0 : illegal access is read This value is reset to 0 when ILL_ACC_ADDR is written	1'b0
29:20	-	-	Reserved	1'b0
19:16	RO	ILL_ACC_BSEL	Indicate the byte select of the illegal access This value is reset to 0 when ILL_ACC_ADDR is written	1'b0
15:11	-	-	Reserved	1'b0
10:8	RO	ILL_IID	Indicate the initiator ID of the illegal access. 0 : CPU 1 : DMA 2 : PPE 3 : Ethernet PDMA RX 4 : Ethernet PDMA TX 5: PCI/PCIE 6: Embedded WLAN MAC/BBP 7: USB This value is reset to 0 when ILL_ACC_ADDR is written	3'b0

7:0	RO	ILL_ACC_LEN	Indicate the access size of the illegal access. The unit is byte This value is reset to 0 when ILL_ACC_ADDR is written.	8'b0
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DDR_SELF_REFRESH: (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	27'b0
4	R/W	SR_AUTO_EN	Auto self-refresh enable for power saving 0: Disable auto self-refresh feature 1: Enable auto self-refresh feature	1'b0
3:2	-	-	Reserved	2'b0
1	RO	SRACK_B	Self refresh acknowledge status. 0: The DDR2 is under self refresh mode 1: The DDR2 has been exit from the self refresh mode (when DDR2 from self refresh mode to normal mode, it will take about 200 clock cycles)	1'b1
0	R/W	SRREQ_B	Self refresh request control. It is low active. 0: Request DDR2 to enter into self refresh mode. 1: Request DDR to exit the self refresh mode.	1'b1

SDR_DDR_PWR_SAVE_CNT: (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:24	RO	PD_CNT	A counter to show the times of entering self-refresh mode(only for DDR2)	8'h00
23:0	R/W	SR_TAR_CNT	This counter only was referenced when the SDR(PWR_DOWN_EN) or DDR2(SR_AUTO_EN) is set. This counter is use to count the period of the SDR or DDR2 IDLE status. When the IDLE period reach to the specified time period The SDR or DDR2 will be automatically enter power saving or self-refresh mode. Software can configure it for suitable value according to following equation. DRAM_CLK_FREQ is PLL_CLK(384MHz or 400MHz) divided by 3 DDR2: (SR_TAR_CNT *256 +255)/DRAM_CLK_FREQ SDR: (SR_TAR_CNT *256)/DRAM_CLK_FREQ Here is reference table for SDRAM 166MHz: 24'h03FFFF * 256* 6.02ns ~ = 404ms 160MHz: 32'h03FFFF * 256* 6.25ns ~ = 419ms 125MHz: 32'h03FFFF * 256* 8.0ns ~ =536ms	24'h03FFFF

Reserved: (offset: 0x20~3C)

DDR_CFG0: (offset: 0x40)

Bits	Type	Name	Description	Initial value
31:28	R/W	Active-to-Active delay of different banks[3:0]	The minimum number of clock cycles from an active command to the next active command for different banks (T_{RRD}). For DDR2 devices, this is required to be a minimum of 2 regardless of the cycle time.	4'b0010
27:23	R/W	Active to Pre-charge time [4:0]	It is the number of clock cycles from an active command until a pre-charge command is allowed. To obtain this value, one should divide the minimum RAS# to pre-charge delay of the SDRAM by the clock cycle time (T_{RAS}). The sum of Active-to-Pre-charge and Pre-charge-to-Active should be equal or larger than active-to-active delay of the same bank (T_{RC})	5'b01001

22:19	R/W	Pre-charge to Active command time [3:0]	The number of clock cycles needed for the SDRAM to recover from a pre-charge command and ready to accept the next active command. To obtain this value, one should divide the RAS# pre-charge time of the SDRAM (T_{RP}) by the clock cycle time. The sum of Active-to-Pre-charge and Pre-charge-to-Active should be equal or larger than active-to-active delay of the same bank (T_{RC})	4'b0011
18:13	R/W	Refresh to Refresh or Active command delay [5:0]	This field is half the number of clock cycles needed for the SDRAM to recover from a refresh signal to be ready to take the next command. To obtain this value, one should divide the SDRAM row cycle time (T_{RFC}) by the clock cycle time.	6'b011010
12:0	R/W	Refresh Interval [12:0]	The number of clock cycles from one refresh command to the next refresh command. To obtain this value, one should divide the periodic refresh interval (T_{REFI}) by the clock cycle time. The actual timing of issuing a pre-charge command may be delayed by if the SDRAM is processing a normal access. However, the delay is not accumulative so there is no need to shorten the refresh interval to account for memory access time. The non-accumulative refresh delay typically increases memory bandwidth by a few percentage points.	13'b000100 1011000

DDR_CFG1: (offset: 0x44)

Bits	Type	Name	Description	Initial value
31:28	R/W	Write-to-Read delay [3:0]	The write-to-read delay (T_{WTR}) (last write data to the next read command) as specified by the DDR2 data sheet	4'b0010
27:24	R/W	Read-to-Pre-charge delay	The read-to-pre-charge delay (T_{RTP}) as specified by the DDR2 data sheet. Note that this is a DDR2 requirement, and requires a minimum of 2 cycles. These bits are ignored in DDR mode	4'b0010
23:22	-	-	Reserved	2'b00
21	R/W	User data width	This bit is 1 to indicate 64-bit user data width and 0 to indicate 32-bit user data width. When user data width is 32-bits, DDR2 width (bit 13:12) must be "10" to indicate DDR2 data width "16". Note: Our system is always 64-bits. Don't modify it.	1'b1
20:18	R/W	DDR2 size	000: Reserved, 001: individual DDR2 is 64Mbit, (DDR only) 010: individual DDR2 is 128Mbit, (DDR only) 011: individual DDR2 is 256Mbit. 100: individual DDR2 is 512Mbit. 101: individual DDR2 is 1Gbit. 110: individual DDR2 is 2Gbit, (DDR2 only) 111: Reserved	3'b101
17:16	R/W	DDR2 width	00: Reserved 01: individual DDR2 is 8-bit wide 10: individual DDR2 is 16-bit wide 11: Reserved	2'b01
15:14	R/W	External banks	00: 1 external bank, 1 module. (CS#[0]) 01: 2 external bank, 1 module. (CS#[1:0]), 10: Reserved 11: 2 external banks, 2 modules. (CS#[1:0]) Note: In RT3352, we only have one CS pin.	2'b00
13:12	R/W	Total DDR2 data path width	00: Reserved 01: Reserved 10: 16-bits 11: 32-bits. Allowed only when user data width is 64-bits (bit 21 is	2'b10

			"1"). This field specifies the total data width to the DDR2. For example, if four 8-bit wide DDR2 chips are used in parallel to form a 32-bit DDR2 data width, this field should be defined as "11" to indicate 32-bit width. In this case, bit 17:16 should define as "01".	
11:8	R/W	Write Recovery Time [3:0]	The clock cycles needed for the DDR to recover from a write command and be able to accept a pre-charge command. To obtain this value, one should divide the SDRAM write recovery time by the clock cycle time (T_{WR})	4'b0011
7:4	R/W	Mode register set to active [3:0]	The number of clock cycles after the setting of the mode registers in the DDR and before the issue of the next command. To obtain this value, one should divide the Mode Register Set Cycle time (T_{MRD}) by the clock cycle time.	4'b0010
3:0	R/W	RAS# to CAS# delay time[3:0]	The number of clock cycles from an active command to a read/write assertion. To obtain this value, one should divide the RAS# to CAS# delay time (T_{RCD}) by the clock cycle time.	4'b0011

DDR_CFG2: (offset: 0x48)

Bits	Type	Name	Description	Initial value
31	R/W	REGE	This bit should be high when external registers are inserted in the control and address signals between the controller and the DDR SDRAM. One example of such instance is when register mode SDRAM DIMM is used. This bit should be low when the control and address signals from the controller is connected to the SDRAM without register delay	1'b0
30	R/W	DDR2 Mode	This bit determines whether the controller is in DDR or DDR2 mode 0: DDR mode 1: DDR2 mode	1'b1
29:28	R/W	DQS window control for DQS0	Control the mask of DQS0 window leading and trailing edge 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No any extended cycle for leading and trailing edge of DQS window (minimum window)	2'b00
27:26	R/W	DQS window control for DQS1	Control the mask of DQS1 window leading and trailing edge 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No any extended cycle for leading and trailing edge of DQS window (minimum window)	2'b00
25:24	R/W	DQS window control for DQS2	Control the mask of DQS2 window leading and trailing edge 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No any extended cycle for leading and trailing edge of DQS window (minimum window)	2'b00
23:22	R/W	DQS window control for DQS3	Control the mask of DQS3 window leading and trailing edge 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No any extended cycle for leading and trailing edge of DQS window	2'b00

			window (minimum window)	
21:13	-	-	Reserved	9'b0
12	R/W	PD	Active Power Down Exit Time 0: Fast exit time (T_{XARD}) 1: Slow exit time(T_{XARDS}) This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR SDRAM	1'b0
11:9	R/W	WR	Auto Pre-charge Write Recovery (T_{DAL}). These bits must be 0 for DDR SDRAM	3'b010
8	R/W	DLLRESET	0: Normal operation. 1: Normal operation with DLL reset.	1'b0
7	R/W	TESTMODE	0: Normal operation. 1: Test mode. The user must keep this bit at "0" if the SDRAM does not support the TESTMODE bit.	1'b0
6:4	R/W	CAS Latency [2:0]	This register specifies the number of the clock cycles from the assertion of a read/write signal to the SDRAM until the first valid data on the output from the SDRAM. The valid numbers are: "101": 1.5 for DDR or 5 for DDR2. "010": 2 "110": 2.5 (DDR only) "011": 3 "100": 4 (DDR2 only)	3'b011
3	RO	Burst Type	This register is hardwired to "0" to indicate sequential burst type.	1'b0
2:0	R/W	Burst Length [2:0]	This register indicates the burst length of the read/write transaction. "010" is a burst of 4. "011" is a burst of 8. Burst of 4 is not allowed when user data is 64-bit while SDRAM data is 16-bit. Burst of 8 is allowed in all user/SDRAM data width combination. Other values of burst length are not allowed.	3'b011

DDR_CFG3: (offset: 0x4C)

Bits	Type	Name	Description	Initial value
31:13	-	-	Reserved	19'b0
12	R/W	Qoff	Output buffer disable 0: output buffer is enabled 1: output buffer is disabled This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR SDRAM.	1'b0
11	R/W	RDQS	This bit enables the redundant DQS function if supported by the SDRAM. This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR SDRAM.	1'b0
10	R/W	Differential DQS	0: enable differential DQS 1: disable differential DQS This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR SDRAM.	1'b1
9:7	R/W	OCD	These bits support the OCD function if supported by the SDRAM. Value programmed in these register bits will be programmed into the SDRAM at EMR1 programming. This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR SDRAM.	3'b000
6	R/W	RTT bit 1	Used together with bit 2 (RTT0) to control ODT. RTT1, RTT0 00 ODT disabled. 01 75 ohm 10 150 ohm	1'b0

			11 Reserved This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR SDRAM.	
5:3	R/W	Additive Latency	Additive Latency. 000: 0 cycle 001: 1 cycle 010: 2 cycles 011: 3 cycles 100: 4 cycles 101: 5 cycles others: reserved This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR SDRAM.	3'b010
2	R/W	RTT bit 0	Used together with bit 6 (RTT1) to control ODT. This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR SDRAM.	1'b0
1	R/W	DS	Drive Strength 0: 100% drive strength. 1: 60% drive strength.	1'b1
0	R/W	DLL	0: Enable. 1: Disable.	1'b0

DDR_CFG4: (offset: 0x50)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	27'b0
4:0	R/W	FAW	DDR2 devices imposes a restriction in that no more than 4 ACTIVE commands may be issued in a given FAW period. To obtain this value, one should divide the Four Bank Activate period (T_{FAW}) of the DDR by the clock cycle time. These bits are ignored in 4 bank devices.	5'b10100

Reserved: (offset: 0x54~0x5C)

DDR_CFG8: (offset: 0x60)

Bits	Type	Name	Description	Initial value
31:24	R/W	DQ_GROUP3_DELAY_SEL	Data output delay path selection for group3(MD24~MD31) 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0000_1111
23:16	R/W	DQ_GROUP2_DELAY_SEL	Data output delay path selection for group2(MD16~MD23) 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0000_1111

15:8	R/W	DQ_GROUP1_DELAY_SEL	Data output delay path selection for group1(MD8~MD15) 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0000_1111
7:0	R/W	DQ_GROUP0_DELAY_SEL	Data output delay path selection for group0(MD0~MD7) 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0000_1111

DDR_CFG9: (offset: 0x64)

Bits	Type	Name	Description	Initial value
31:24	R/W	DQS3_DELAY_SEL	DQS3 input delay path selection 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0001_1111
23:16	R/W	DQS2_DELAY_SEL	DQS2 input delay path selection 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0001_1111
15:8	R/W	DQS1_DELAY_SEL	DQS1 input delay path selection 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0001_1111

7:0	R/W	DQSO_DELAY_SEL	DQSO input delay path selection 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0001_11 11
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3.8 USB Host Controller & PHY

3.8.1 Features

- Complies with the USB 2.0 Specification
- Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports ping and split transactions
- Descriptor and data prefetching.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- UTMI (legacy), UTMI+ to the PHY

3.8.2 Block Diagram

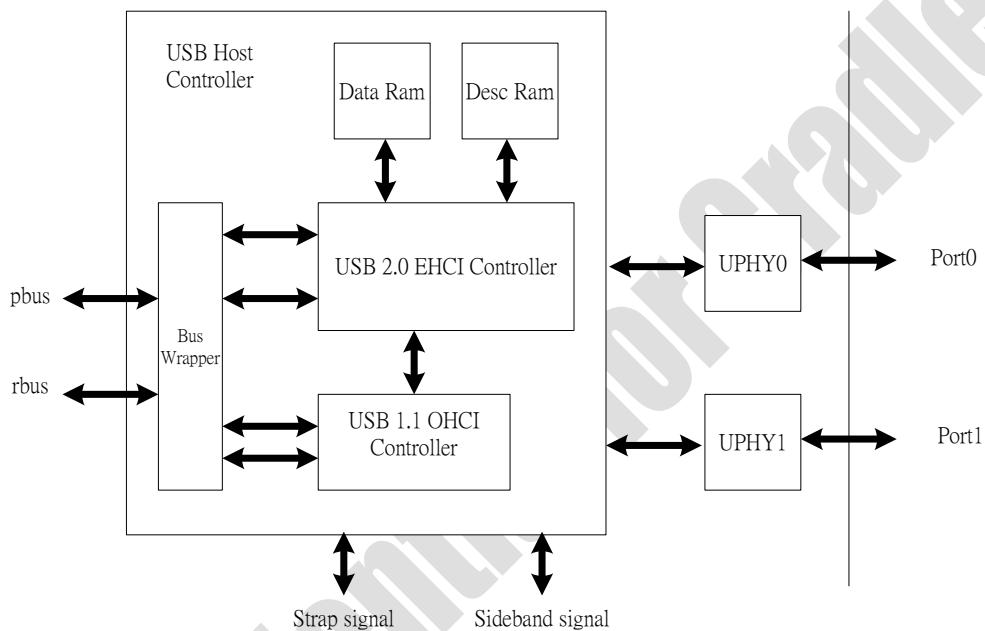


Fig. 3-17-1 USB Host Controller & PHY Block Diagram

3.8.3 Register Description (base: 0x101C.0000)

NOTE: To program EHCI and OHCI registers and initialize the core, refer to the Enhanced Host Controller Interface Specification for Universal Serial Bus and Open Host Controller Interface Specification for USB, respectively.

3.8.3.1 EHCI Operation register (BASE: 0x101C.0000)

EHCI Capability Register

Mnemonic	Register Name	Offset From EHCI AHB Slave Start Address	Default Value
HCCAPBASE	Capability Register	USBBASE ¹ + 00h	32'h01000010
HCSPARAMS	Structural Parameter	USBBASE + 04h	32'h00001116
HCCPARAMS	Capability Parameter	USBBASE + 08h	32'h0000A010 Note: The Isochronous Scheduling Threshold value is set to 1 by default. If Descriptor/Data Prefetch is selected, the value is set 2.

USBBASE is fixed to EHCI slave start address = 0x101C.0000

EHCI Operational Registers

Mnemonic	Register Name	Offset From EHCI AHB Slave Start Address ¹	Default Value
USBCMD	USB Command	USBOPBASE ¹ + 00h	32'h00080000 or 32'h00080B00 ²
USBSTS	USB Status	USBOPBASE + 04h	32'h00001000
USBINTR	USB Interrupt Enable	USBOPBASE + 08h	32'h00000000
FRINDEX	USB Frame Index	USBOPBASE + 0ch	32'h00000000
CTRLDSSEGMENT	4G Segment Selector	USBOPBASE + 10h	32'h00000000
PERIODICLISTBASE	Periodic Frame List Base Address Register	USBOPBASE + 14h	32'h00000000
ASYNCLISTADDR	Asynchronous List Address	USBOPBASE + 18h	32'h00000000

1. USBOPBASE is fixed to the EHCI slave start address + 'h10 (offset = 'h10).
2. The default value depends on whether Async park capability is enabled. Disabled = 32'h0008_0000 and enabled = 32'h0008_0B00.

The default value is:

32'h0008_0000 if Async park capability is disabled (through coreConsultant)
32'h0008_0B00 if Async park capability is enabled.

EHCI Auxiliary Power Well Registers

Mnemonic	Register Name	Offset From EHCI AHB Slave Start Address	Default Value
CONFIGFLAG	Configured Flag Register	USBOPBASE + 40h	32'h00000000
PORTSC_1 to PORTSC_15	Port Status/Control	USBOPBASE + 44h	32'h00002000

- Support USB Host/Device Dual mode
- Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 1.0a)
- Operates in High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes
- Supports up to 4 bidirectional endpoints, including control endpoint 0
- Supports up to 4 host channels.
- Supports a generic root hub
- Includes automatic ping capabilities
- Supports Internal DMA modes
- Includes USB power management features

- Includes power-saving features (clock gating, two power rails for advanced power management)
- Supports packet-based, Dynamic FIFO memory allocation for endpoints for small FIFOs , and flexible, efficient use of RAM provides support to change an endpoint's FIFO memory size during transfers

3.8.3.2 OHCI Operation register (BASE: 0x101C.1000)

Offset	3	0
	1	0
0	HcRevision	
4	HcControl	
8	HcCommandStatus	
C	HcInterruptStatus	
10	HcInterruptEnable	
14	HcInterruptDisable	
18	HcHCCA	
1C	HcPeriodCurrentED	
20	HcControlHeadED	
24	HcControlCurrentED	
28	HcBulkHeadED	
2C	HcBulkCurrentED	
30	HcDoneHead	
34	HcFmInterval	
38	HcFmRemaining	
3C	HcFmNumber	
40	HcPeriodicStart	
44	HcLSThreshold	
48	HcRhDescriptorA	
4C	HcRhDescriptorB	
50	HcRhStatus	
54	HcRhPortStatus[1]	
...	...	
54+4*NDP	HcRhPortStatus[NDP]	

3.9 USB Device Controller

3.9.1 Features

- the USB 2.0 Specification (Revision 1.0a), operates in High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes
- Supports up to 2 bulk-in and bulk out endpoints, including control endpoint 0
- Packet DMA (PDMA) is integrated for efficient data transfer.
- Support bulk-out aggregation features. More than one packet can be aggregated to single bulk transfer.
- Support two RX descriptor rings and two TX descriptor rings for QoS service.

3.9.1.1 PDMA descriptor format

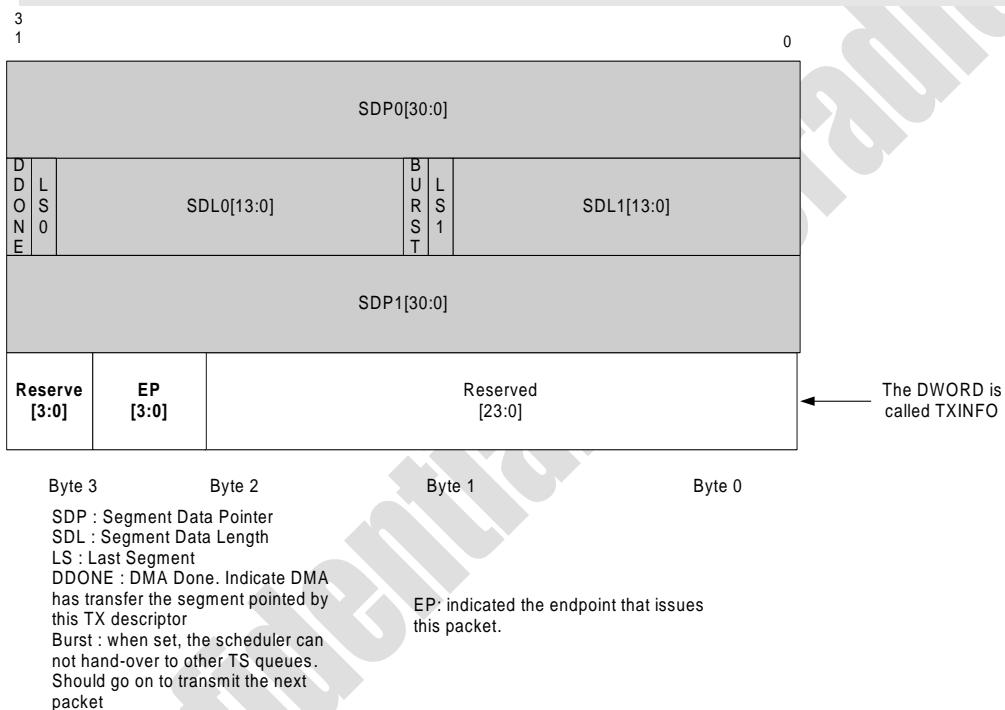


Fig. 3-18-1 PDMA TX descriptor format

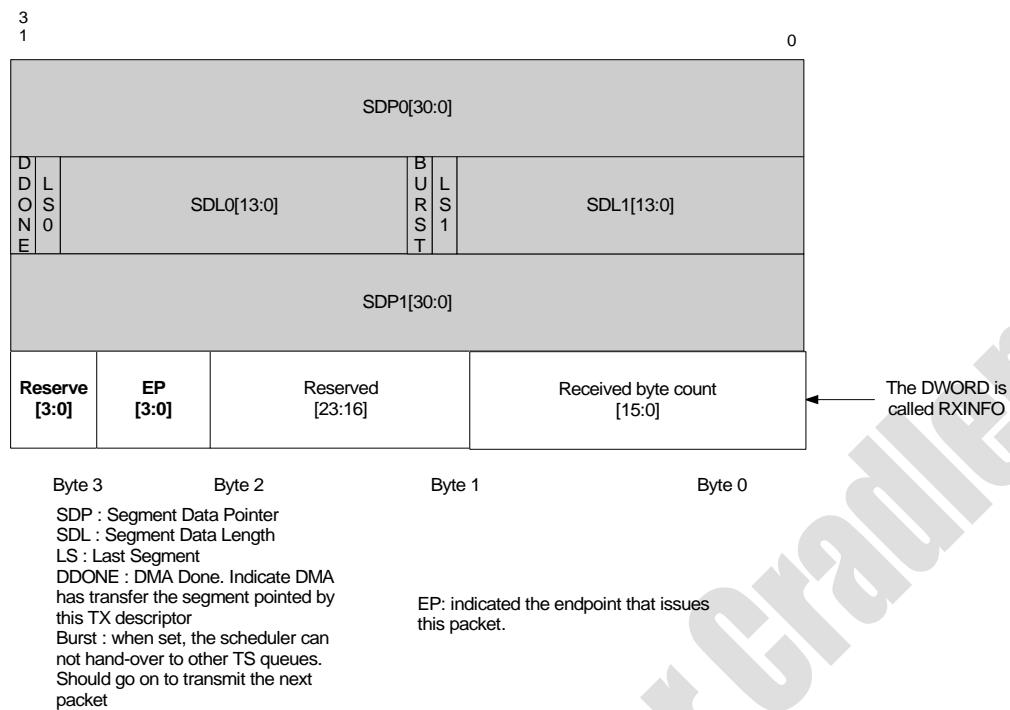
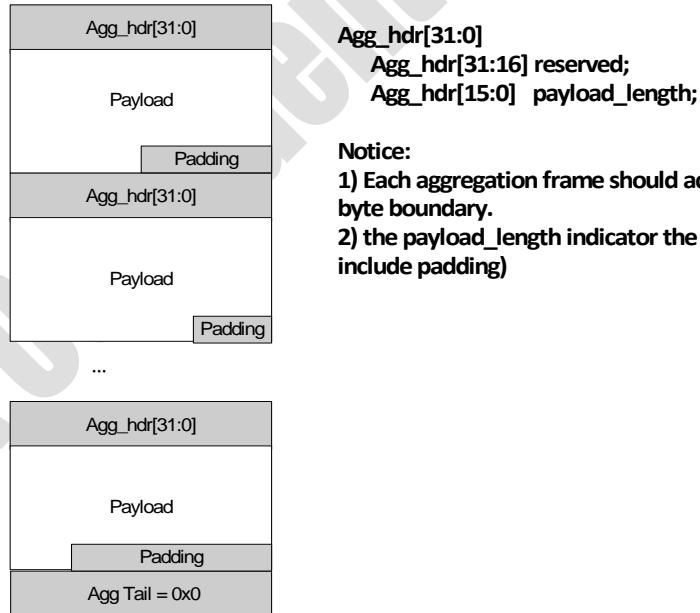


Fig. 3-18-2 PDMA RX descriptor format

3.9.1.2 Bulk-out aggregation format

 3
1


3.9.2 Register Description (base: 0x1012.0000)

3.9.2.1 USB control registers

Refer to *case_cusb2_spec.pdf*.

Registers address = Byte address * 4.

3.9.2.2 UDMA registers

UDMA_CTRL (offset: 0x0800, default :0x00000000)

Bits	Type	Name	Description	Init Value
31:26			Reserved	
25	R/W	EPOUT1_DMAEN	EPOUT1 UDMA enable.	0
24	R/W	EPOUT0_DMAEN	EPOUT0 UDMA enable.	0
23:18				
17	R/W	EPOUT1_AGGEN	EPOUT1 UDMA de-aggregation enable.	0
16	R/W	EPOUT0_AGGEN	EPOUT0 UDMA de-aggregation enable.	0
15:10	-	-	Reserved	-
9	R/W	EPOUT1_QSEL	EPOUT1 Rx ring mapping.	0
8	R/W	EPOUT0_QSEL	EPOUT0 Rx ring mapping.	0
7:5	-	-	Reserved	-
4	R/W	WAKEUP_EN	USB wakeup host enable.	0
3:2	-	-	Reserved	0
1	R/W	UDMA_RX_EN	UDMA Rx enable.	0
0	R/W	UDMA_TX_EN	UDMA Tx enable.	0

UDMA_WRR (offset: 0x0804, default :0x00000000)

Bits	Type	Name	Description	Init Value
31:30	-	-	RESERVED	-
29:28	R/W	SCH_MODE	SCHEDULING MODE 00: WRR 01: strict priority, EP1 > EP2 > EP3 > EP4 > EP5 > EP6 10: mixed mode, EP1 > EP2 > WRR(EP3, EP4, EP5, EP6)	2'b00
27:23	-	-	RESERVED	-
22:20	R/W	SCH_WT_EP6	SCHEDULING WEIGHT OF EPOUT6	0
19	-	-	RESERVED	-
18:16	R/W	SCH_WT_EP5	SCHEDULING WEIGHT OF EPOUT5	0
15	-	-	RESERVED	-
14:12	R/W	SCH_WT_EP4	SCHEDULING WEIGHT OF EPOUT4	0
11	-	-	RESERVED	-
10:8	R/W	SCH_WT_EP3	SCHEDULING WEIGHT OF EPOUT3	0
7	-	-	RESERVED	-

6:4	R/W	SCH_WT_EP2	SCHEDULING WEIGHT OF EPOUT2	0
3	-	-	RESERVED	-
2:0	R/W	SCH_WT_EP1	SCHEDULING WEIGHT OF EPOUT1	0

3.9.2.3 PDMA registers

TX_BASE_PTR0 (offset:0x1000,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16	-	-	Reserved	-
15:0	R/W	TX_BASE_PTR0	Point to the base address of TX_Ring0 (4-DWORD aligned address)	0

TX_MAX_CNT0 (offset:0x1004,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	R/W	TX_MAX_CNT0	The maximum number of TXD count in TXD_Ring0.	0

TX_CTX_IDX0 (offset:0x1008,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	R/W	TX_CTX_IDX0	Point to the next TXD CPU wants to use	0

TX_DTX_IDX0 (offset:0x100C,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	Reserved	-0
7:0	RO	TX_DTX_IDX0	Point to the next TXD DMA wants to use	0

TX_BASE_PTR1 (offset:0x1010,default :0x00000000)

TX_MAX_CNT1 (offset:0x1014,default :0x00000000)

TX_CTX_IDX1 (offset:0x1018,default :0x00000000)

TX_DTX_IDX1 (offset:0x101C,default :0x00000000)

RX_BASE_PTR0 (offset:0x1100,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16	-	-	Reserved	-
15:0	R/W	RX_BASE_PTR0	Point to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address	0

RX_MAX_CNT0 (offset:0x1104,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	R/W	RX_MAX_CNT0	The maximum number of RXD count in RXD Ring #0.	0

RX_CALC_IDX0 (offset:0x1108,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	R/W	RX_CALC_IDX0	Point to the next RXD CPU wants to allocate to RXD Ring #0.	0

FS_DRX_IDX0 (offset:0x110C,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	

7:0	R/W	RX_DRX_IDX0	Point to the next RXD DMA wants to use in FDS Ring#0. It should be a 4-DWORD aligned address.	0
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RX_BASE_PTR1 (offset:0x1110,default :0x00000000)

RX_MAX_CNT1 (offset:0x1114,default :0x00000000)

RX_CALC_IDX1 (offset:0x1118,default :0x00000000)

RX_DRX_IDX1 (offset:0x111C,default :0x00000000)

PDMA_INFO (offset:0x1200,default :0x1008020E)

Bits	Type	Name	Description	Init Value
31:28	RO	VERSION	PDMA controller version.	0x1
27:24	RO	INDEX_WIDTH	Ring index width	0xC
23:16	RO	BASE_PTR_WIDTH	Base pointer width, x Base_addr[31:32-x] is shared with all ring base addr. Only ring0's base address [31:32-x] field is writable.	0x10
15:8	RO	RX_RING_NUM	Rx ring number	0x2
7:0	RO	TX_RING_NUM	Tx ring number	0x2

PDMA_GLO_CFG (offset:0x1204,default :0x000000050)

Bits	Type	Name	Description	Init Value
31:29			Reserved	
28:16		HDR_SEG_LEN	Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value. When set to zero, the header/payload scattering feature is disabled.	8'b0
15:8	-	-	Reserved	-
7	R/W	BIG_ENDIAN	The endian mode selection. DMA applies the endian rule to convert payload and TX/RX information. DMA won't apply endian rule to register or descriptor. 1: big endian. 0: little endian.	0
6	R/W	TX_WB_DDONE	0 :Disable TX_DMA writing back DDONE into TXD 1 : Enable TX_DMA writing back DDONE into TXD	1'b1
5	-	-	Reserved	-
4	R/W	WPDMA_BT_SIZE	Define the burst size of WPDMA 0 : 4 DWORD (16bytes) 1 : 8 DWORD (32 bytes)	1'b1
3	RO	RX_DMA_BUSY	1 : RX_DMA is busy 0 : RX_DMA is not busy	0
2	R/W	RX_DMA_EN	1 : Enable RX_DMA 0 : Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop.)	0
1	RO	TX_DMA_BUSY	1 : TX_DMA is busy 0 : TX_DMA is not busy	0
0	R/W	TX_DMA_EN	1 : Enable TX_DMA 0 : Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)	0

PDMA_RST_IDX (offset:0x1208,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:18			Reserved	
17	W1C	RST_DRX_IDX1	Write 1 to reset to RX_DMARX_IDX1 to 0	1'b0
16	W1C	RST_DRX_IDX0	Write 1 to reset to RX_DMARX_IDX0 to 0	1'b0
15:2	-	-	Reserved	-

1	W1C	RST_DTX_IDX1	Write 1 to reset to TX_DMATX_IDX1 to 0	1'b0
0	W1C	RST_DTX_IDX0	Write 1 to reset to TX_DMATX_IDX0 to 0	1'b0

DELAY_INT_CFG (offset:0x120C,default :0x00000000)

Bits	Type	Name	Description	Init Value
31	RW	TXDLY_INT_EN	1: Enable TX delayed interrupt mechanism. 0: Disable TX delayed interrupt mechanism.	1'b0
30:24	RW	TXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final TX_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'b0
23:16	RW	TXMAX_PTIME	Specified Max pending time for the internal TX_DONE_INT0-5. When the pending time equal or grater TXMAX_PTIME x 20us or the # of pended TX_DONE_INT0-5 equal or grater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'b0
15	RW	RXDLY_INT_EN	1: Enable RX delayed interrupt mechanism. 0: Disable RX delayed interrupt mechanism.	1'b0
14:8	RW	RXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final RX_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'b0
7:0	RW	RXMAX_PTIME	Specified Max pending time for the internal RX_DONE_INT. When the pending time equal or grater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or grater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'b0

INT_STATUS (offset: 0x1220,default :0x00000000)

Bits	Type	Name	Description	Init Value
31	R/W	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0
30	R/W	RX_DLY_INT	Summary of the whole WPDMA RX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0
29	R/W	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0
28	R/W	TX_DLY_INT	Summary of the whole WPDMA TX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0
27:18	-	-	Reserved	-
17	R/W	RX_DONE_INT1	RX Queue#1 packet receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0

16	R/W	RX_DONE_INT0	RX Queue#0 packet receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
15:2	-	-	Reserved	-
1	R/W	TX_DONE_INT1	TX Queue#1 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
0	R/W	TX_DONE_INT0	TX Queue#0 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0

INT_MASK (offset:0x1228,default :0x00000000)

Bits	Type	Name	Description	Init Value
31	R/W	RX_COHERENT_INT_MSK	Interrupt enable for RX_DMA data coherent event.. 1: Enable the interrupt 0: Disable the interrupt	0
30	R/W	RX_DLY_INT_MSK	Summary of the whole WPDMA RX related interrupts 1 : Enable the interrupt 0 : Disable the interrupt	0
29	R/W	TX_COHERENT_INT_MSK	Interrupt enable for TX_DMA data coherent even 1: Enable the interrupt 0: Disable the interrupt	0
28	R/W	TX_DLY_INT_MSK	Summary of the whole WPDMA TX related interrupts 1 : Enable the interrupt 0 : Disable the interrupt	0
27:18	-	-	Reserved	-
17	R/W	RX_DONE_INT_MSK1	RX Queue#1 packet receive interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
16	R/W	RX_DONE_INT_MSK0	RX Queue#0 packet receive interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
15:2	-	-	Reserved	-
1	R/W	TX_DONE_INT_MSK1	TX Queue#1 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
0	R/W	TX_DONE_INT_MSK0	TX Queue#0 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0

PDMA_WRR (offset: 0x1280,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:30	-	-	RESERVED	-
29:28	R/W	SCH_MODE	SCHEDULING MODE 00: WRR 01: strict priority, Q0 > Q1 > Q2 > Q3 10: mixed mode, Q0 > Q1 > WRR(Q2, Q3)	2'b00
27:15	-	-	RESERVED	-

14:12	R/W	SCH_WT_Q3	SCHEDULING WEIGHT OF TX Q3	0
11	-	-	RESERVED	-
10:8	R/W	SCH_WT_Q2	SCHEDULING WEIGHT OF TX Q2	0
7	-	-	RESERVED	-
6:4	R/W	SCH_WT_Q1	SCHEDULING WEIGHT OF TX Q1	0
3	-	-	RESERVED	-
2:0	R/W	SCH_WT_Q0	SCHEDULING WEIGHT OF TX Q0	0

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3.10 Frame Engine

3.10.1 Features

- Wire-speed (1000Mbps) Ethernet LAN/WAN NAT/NAPT routing
- L1-L7(content aware) policy table
- Stateful packet inspection firewall
- QoS support for multimedia traffic
- Support per flow/rule accounting/rate limiting
- Checksum/VLAN/PPPoE offload

3.10.1.1 Network Interface

- One 10/100/1000Mbps Ethernet MACs with RGMII/MII interfaces
- One Scatter-Gather packet DMA with Rbus master interface
 - (Note : Although there are two gigabit Ethernet ports, only one packet DMA is existed. From software point of view, only one software driver instance is used. The software driver could assign the TX packet destination by assign the PN filed in the TX descriptor)
- One special port for packet processing engine

3.10.1.2 PSE (Packet Switch Engine) Features

- Four external ports and one special PPE port (for packet bridging/routing)
- Efficient page-based buffer management (256 pages, each page is 128 bytes)
- QoS-aware queue management
- Supports 4 output queues per gigabit Ethernet port
- WRR/Strict priority scheduling
- Egress rate limiting/shaping
- Non-blocking, wire-speed packet switching
- Supports Jumbo frames up-to 12KB
- Flow control for no-packet-loss guarantee
- Emulated multicast support (can mirror a TX packet to CPU)
- Checksum offload, VLAN & PPPOE header insertion (by CDMA)
- Auto-Padding for sub-64B packets

3.10.1.3 PPE Features

- Supports 512 policy rules for ACL, accounting and rate limiting
- The policy rules can base on pre-route/post-route L1-L7 headers & contents (up-to 16 bytes)
- DDoS avoidance by rate limiting
- Supports stateful packet filtering (SPI)
- Supports IPv4 NAT/NAPT routing
- Supports 1/2/4/8/16K IPv4 NAPT flows
- Supports virtual server, port-triggering & port forwarding
- Supports any kind of IPv4 NAT(NAPT, Twice NAT)
- Supports 16 PPPoE sessions
- Supports cone-NAT, port-restricted NAT & Symmetric NAT
- Supports per rule or per flow accounting or rate limiting

- Patent-pending Flow Offloading technology for flexible/high performance packet L3/L4 packet processing
- Supports double VLAN tagging (Q-in-Q)
- Support VID Swapping
- Support multi-WAN load balancing with H/W S/W cooperation
- PS : All the PPE features mentioned above require software porting to enable

3.10.1.4 QoS Related Features

- Packets can be classified based on L1-L7 headers/content
- Supports 4 TX queues
- Supports WRR scheduling for GE ports
- Supports egress rate limiting for each network port
- Powerful buffer reservation scheme to reserve packet buffer resources for multi-media traffic

3.10.1.5 Packet DMA (PDMA) Features

- Supports 2 TX descriptor rings and one RX descriptor ring
- Scatter/Gather DMA
- Delayed interrupt
- Configurable 4/8/16 32-bit word burst length

3.10.2 Block Diagram

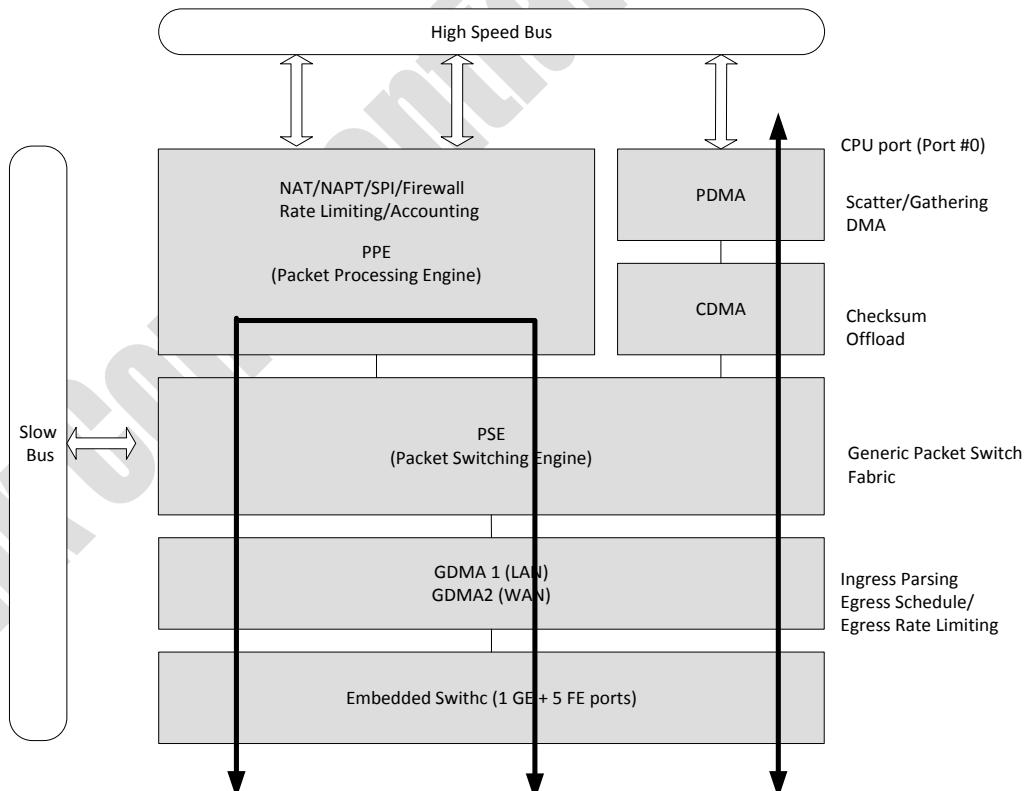
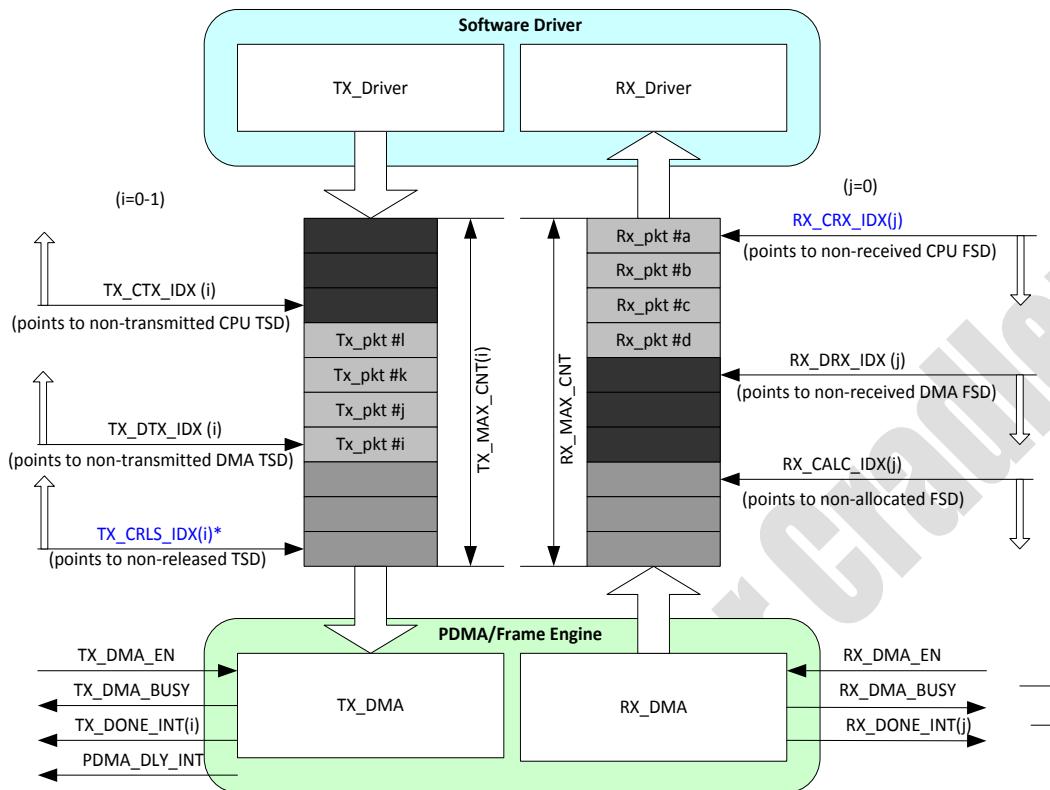


Fig. 3-19-1 Frame Engine block diagram

3.10.2.1 PDMA FIFO-like Ring Concept



Note 1 : TX_CRLS_IDX(i) and RX_CRX_IDX(j) are not in
PDMA hardware, they are resident in CPU's local memory

Note 2:

TXQ0 : GE MAC low priority queue

RXQ0 : For GE MAC receive

TXQ1 : GE MAC high priority queue

Fig. 3-19-2 PDMA FIFO-like ring concept

3.10.2.2 PDMA Descriptor Format

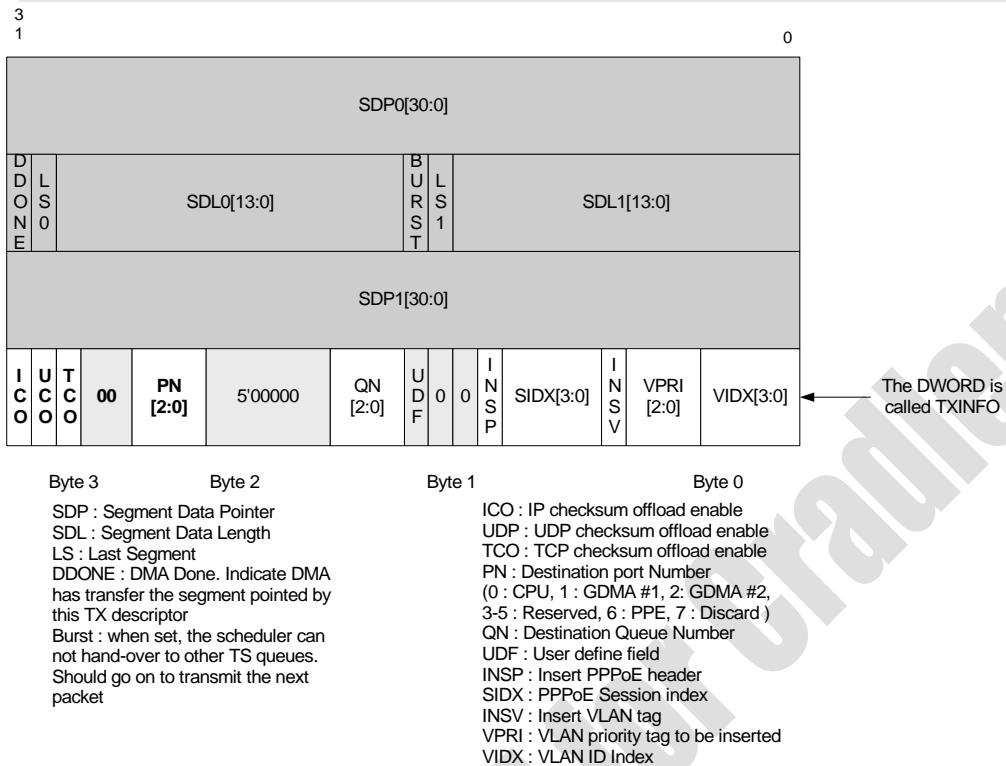


Fig. 3-19-3 PDMA TX descriptor format

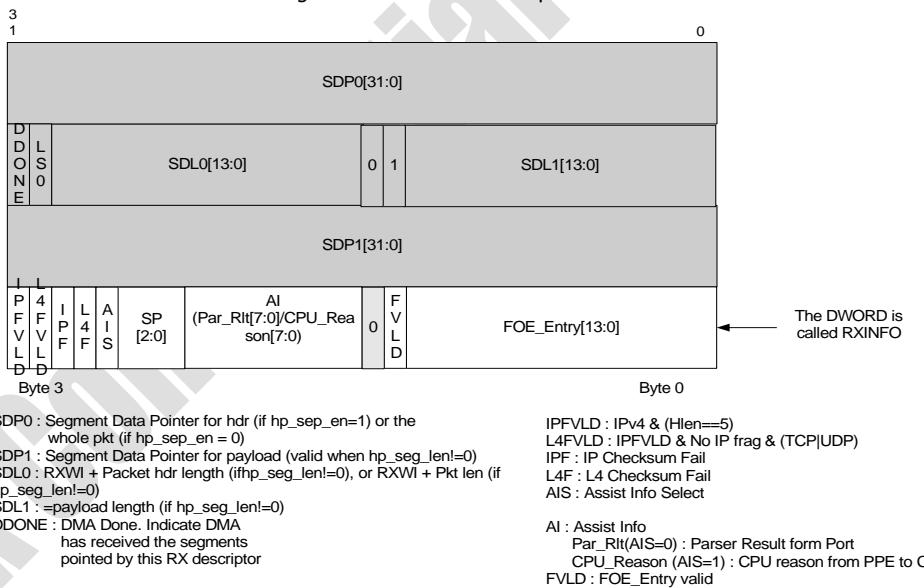


Fig. 3-19-4 PDMA RX descriptor format

3.10.3 Register Description (base: 0x1010.0000)

MDIO_ACCESS : Reserved (offset: 0x00)

MDIO_CFG1 : Reserved (offset: 0x04)

FE_GLO_CFG : Frame Engine Global Configuration (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:16	R/W	EXT_VLAN	Extended VLAN type	16'h8100
15:8	-		Reserved	16'd125
7:4	R/W	L2_SPACE	L2 space. Unit is 8 bytes	4'h8
3:1	-	-	Reserved	3'b0
0	R/W	RATE_MINUS	Minus byte counts for incoming frame 1'b0 : a specific byte count is added to the frame length according to FOE_TS_T.RATE_BYTE 1'b1: a specific byte count is subtracted from the incoming frame length.	1'b0

FE_RST_GLO : Frame Engine Global Reset (offset: 0x0C)

Bits	Type	Name	Description	Initial value
31:16	RC	FC_DROP_CNT	Flow control drop packet count.	16'b0
15:1	-	-	Reserved	15'b0
0	WO	PSE_RESET	PSE reset Write 1 to reset PSE Write 0 to disable reset PSE	1'b0

FE_INT_STATUS : Frame Engine Interrupt Status (offset: 0x10)

Bits	Type	Name	Description	Initial value
31	R/W	CNT_PPE_AF	PPE Counter Table Almost Full Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
30	-	-	Reserved	1'b0
29	R/W	CNT_GDM1_AF	GDMA1 Counter Table Almost Full Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
28:26	-	-	Reserved	3'b000
25	R/W	GE1_CRC_DROP	GE1 discards a packet due to CRC error Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
24	R/W	PSE_BUF_DROP	PSE discards a packet due to buffer sharing limitation (flow control) Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
23	R/W	GE1_OTHER_DROP	GE1 discards a packet due to other reason (e.g. too short, too long, FIFO overflow, checksum error,.., etc.) Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
22	R/W	PSE_P1_FC	PSE port1 (GDMA1) flow control asserted. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
21	R/W	PSE_P0_FC	PSE port0 (CDMA) flow control asserted. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
20	R/W	PSE_FQ_EMPTY	PSE free Q empty threshold reached & forced drop condition occurred. Write 1 to clear the interrupt.	1'b0

			Read to get the raw interrupt status	
19	-	-	Reserved	1'b0
18	R/W	GE1_STA_CHG	GE port #1 link status changes (link, speed, flow control) Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
17	R/W	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
16	R/W	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
15:12	-	-	Reserved	4'b0
11	R/W	TX_DONE_INT3	Tx queue#3 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
10	R/W	TX_DONE_INT2	Tx queue#2 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
9	R/W	TX_DONE_INT1	Tx queue#1 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
8	R/W	TX_DONE_INT0	Tx queue#0 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
7:3	-	-	Reserved	5'b0
2	R/W	RX_DONE_INT0	Packet receive interrupt. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
1	R/W	TX_DLY_INT	Delayed version of TX_DONE_INT0 and TX_DONE_INT1. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
0	R/W	RX_DLY_INT	Delayed version of RX_DONE_INT0. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0

FE_INT_ENABLE : Frame Engine Interrupt Enable (offset: 0x14)

Bits	Type	Name	Description	Initial value
31	R/W	CNT_PPE_AF	PPE Counter Table Almost Full 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
30	-	-	Reserved	1'b0
29	R/W	CNT_GDM1_AF	GDMA1 Counter Table Almost Full Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
28:26	-	-	Reserved	3'b0
25	R/W	GE1_CRC_DROP	GE1 discards a packet due to CRC error 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
24	R/W	PSE_BUF_DROP	PSE discards a packet due to buffer sharing limitation (flow control) 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
23	R/W	GE1_OTHER_DROP	GE1 discards a packet due to other reason (e.g. too short, too long, FIFO overflow, checksum error, etc.) 1 : Enable the interrupt	1'b0

			0 : Disable the interrupt	
22	R/W	PSE_P1_FC	PSE port1 (GDMA1) flow control asserted. 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
21	R/W	PSE_P0_FC	PSE port0 (CDMA) flow control asserted. 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
20	R/W	PSE_FQ_EMPTY	PSE free Q empty threshold reached & forced drop condition occurred. 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
19	-	-	Reserved	1'b0
18	R/W	GE1_STA_CHG	GE port #1 link status changes (link, speed, flow control) 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
17	R/W	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit. 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
16	R/W	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit. 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
15:12	-	-	Reserved	4'b0
11	R/W	TX_DONE_INT3	Tx queue#3 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
10	R/W	TX_DONE_INT2	Tx queue#2 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
9	R/W	TX_DONE_INT1	Tx queue#1 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
8	R/W	TX_DONE_INT0	Tx queue#0 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
7:3	-	-	Reserved	5'b0
2	R/W	RX_DONE_INT0	Packet receive interrupt. 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
1	R/W	TX_DLY_INT	Delayed version of TX_DONE_INT0 and 1 : Enable the interrupt 0 : Disable the interrupt	1'b0
0	R/W	RX_DLY_INT	Delayed version of RX_DONE_INT0. 1 : Enable the interrupt 0 : Disable the interrupt	1'b0

FOE_TS_T : Time Stamp (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:24	R	PSE_FQ_PCNT	PSE free Q page count	8'hff
23:16	R/W	ADD_RATE_BYTE	Byte number should be added to frame while calculate the rate limit.	8'd24
15:0	R/W	FOE_TS_T	Time stamp Note: Time Stamp unit is 1 sec.	16'b0

3.10.3.1 Register Description – GDMA1

GDMA1_FWD_CFG : GDMA1 Forwarding Configuration (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:28	-	GDM1_JMB_LEN	When GDM1_JMB_EN=1, this parameter define the maximum packet length(including CRC) that GDMA1 could receive in 1024-byte unit. The valid value is from 0 ~12.	4'd12
27:26	-	-	Reserved	
25	R/W	GDM1_20US TICK_SLT	0: GDM1 shaper add token every 1ms. 1: GDM1 shaper add token every 20us. Please refer to GDM1_TK_RATE in GDMA1_SHPR_CFG register.	1'b0
24	R/W	GDM1_TCI_81xx	0: Check VLAN tag with EXT_VLAN[15:0] 1: Check VLAN tag with EXT_VLAN[15:8] only	1'b0
23	R/W	GDM1_DROP_256B	A Special mode to drop packets with payload > 256 bytes. 0 : Drop packets according to standard Ethernet frame length limitation. 1 : Drop packets with payload >256 bytes	1'b0
22	R/W	GDM1_ICS_EN	IPv4 header checksum check enable	1'b1
21	R/W	GDM1_TCS_EN	TCP checksum check enable	1'b1
20	R/W	GDM1_UCS_EN	UDP checksum check enable	1'b1
19	R/W	GDM1_JMB_EN	0 : Drop received frames if length is great than 1518 (1522 for VLAN frames, and 1526 for double VLAN frames) 1 : Allow receiving jumbo frames length up to 12kB.	1'b0
18	R/W	GDM1_DISPAD	0 : Enable GMAC1 Tx padding function. 1 : Disable GMAC1 Tx padding function.	1'b0
17	R/W	GDM1_DISCRC	0 : Enable GMAC1 Tx CRC generation. 1 : Disable GMAC1 Tx CRC generation.	1'b0
16	R/W	GDM1_STRPCRC	0 : Disable GDMA1 automatic Rx CRC stripping 1 : Enable GDMA1 automatic Rx CRC stripping	1'b1
15	-	-	Reserved	1'b0
14:12	R/W	GDM1_UFRC_P	GDMA1 My MAC uni-cast frames destination port 3'd0 : CPU 3'd1 : GDMA1 3'd2 : GDMA2 3'd6 : PPE 3'd7 : Discard Others: Reserved	3'b111
11	-	-	Reserved	1'b0
10:8	R/W	GDM1_BFRC_P	GDMA1 broad-cast MAC address frames destination port 3'd0 : CPU 3'd1 : GDMA1 3'd2 : GDMA2 3'd6 : PPE 3'd7 : Discard Others: Reserved	3'b111
7	-	-	Reserved	1'b0
6:4	R/W	GDM1_MFRC_P	GDMA1 multi-cast MAC address frames destination port 3'd0 : CPU 3'd1 : GDMA1 3'd2 : GDMA2 3'd6 : PPE 3'd7 : Discard Others: Reserved	3'b111

3	-	-	Reserved	1'b0
2:0	R/W	GDM1_OFRC_P	GDMA1 other MAC address frames destination port 3'd0 : CPU 3'd1 : GDMA1 3'd2 : GDMA2 3'd6 : PPE 3'd7 : Discard Others: Reserved	3'b111

GDMA1_SCH_CFG : GDMA1 Scheduling Configuration (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	7'b0
25:24	R/W	GDM1_SCH_MOD	2'b00 : WRR 2'b01 : Strict Priority, Q3>Q2>Q1>Q0 2'b10 : Mixed, Q3>WRR(Q2,Q1,Q0) 2'b11 : Mixed, Q3>Q2>WRR(Q1,Q0)	2'b00
23:15	-	-	Reserved	1'b0
14:12	R/W	GDM1_WT_Q3	Q3's weight 3'd0 : weight = 1 3'd1 : weight = 2 3'd7 : weight = 8	3'b111
11	-	-	Reserved	1'b0
10:8	R/W	GDM1_WT_Q2	Q2's weight 3'd0 : weight = 1 3'd1 : weight = 2 3'd7 : weight = 8	3'b011
7	-	-	Reserved	1'b0
6:4	R/W	GDM1_WT_Q1	Q1's weight 3'd0 : weight = 1 3'd1 : weight = 2 3'd7: weight = 8	3'b001
3	-	-	Reserved	1'b0
2:0	R/W	GDM1_WT_Q0	Q0's weight 3'd0 : weight = 1 3'd1 : weight = 2 3'd7: weight = 8	3'b000

GDMA1_SHPR_CFG : GDMA1 Output Shaper Configuration (offset: 0x28)

Bits	Type	Name	Description	Initial value
31:25	-	-	Reserved	7'b0
24	R/W	GDM1_SHPR_EN	GDMA1 output shaper enable. 0 : Disable 1 : Enable	1'b0
23:16	R/W	GDM1_BK_SIZE	GDMA1 output shaper maximum bucket size. Unit is 1kB.	8'b0
15:14	-	-	Reserved	2'b0
13:0	R/W	GDM1_TK_RATE	GDMA1 output shaper token rate. Unit is 8B/ms or 8B/20us. According to GDM1_20US_TICK_SLT.	14'b0

GDMA1_MAC_ADRL : GDMA1 MAC Address LSB (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:0	R/W	GDM1_MY_MAC_L	GMAC1 MAC address bit 31-0	32'b0

GDMA1_MAC_ADRH : GDMA1 MAC Address MSB (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	GDM1_MY_MAC_H	GMAC1 MAC address bit 47-32	16'b0

3.10.3.2 Register Description - PSE
PSE_FQ_CFG (offset:0x40)

Bits	Type	Name	Description	Initial value
31:24	R/W	FQ_MAX_PCNT	Maximum free Q page count. Please reset PSE after re-programming this register.	8'hFF
23:16	R/W	FQ_FC_RLS	Free Q flow control release threshold.	8'hA1
15:8	R/W	FQ_FC_ASRT	Free Q flow control assertion threshold.	8'hA0
7:0	R/W	FQ_FC_DROP	Free Q empty threshold. If one input port is FC asserted and this threshold is reached, PSE will drop any new coming frame from this port.	8'h00

CDMA_FC_CFG (offset:0x44)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'h1
27:24	R/W	P0_HQ_DEF	Bit map definition of high priority Q. '1' presents high priority Q, and '0' presents low priority Q. bit 27: Q3 priority definition bit 26: Q2 priority definition bit 25: Q1 priority definition bit 24: Q0 priority definition	4'b1100
23:16	R/W	P0_HQ_RESV	Reserved page count for high priority Q.	8'h40
15:8	R/W	P0_LQ_RESV	Reserved page count for low priority Q.	8'h10
7:0	R/W	P0_IQ_ASRT	Virtual input Q FC assertion threshold.	8'h10

GDMA1_FC_CFG (offset:0x48)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'h1
27:24	R/W	P1_HQ_DEF	Bit map definition of high priority Q. '1' presents high priority Q, and '0' presents low priority Q. bit 27: Q3 priority definition bit 26: Q2 priority definition bit 25: Q1 priority definition bit 24: Q0 priority definition	4'b1100
23:16	R/W	P1_HQ_RESV	Reserved page count for high priority Q.	8'h40
15:8	R/W	P1_LQ_RESV	Reserved page count for low priority Q.	8'h10
7:0	R/W	P1_IQ_ASRT	Virtual input Q FC assertion threshold.	8'h10

GDMA2_FC_CFG (offset:0x4C)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'h1
27:24	R/W	P2_HQ_DEF	Bit map definition of high priority Q. '1' presents high priority Q, and '0' presents low priority Q. bit 27: Q3 priority definition bit 26: Q2 priority definition bit 25: Q1 priority definition bit 24: Q0 priority definition	4'b1100
23:16	R/W	P2_HQ_RESV	Reserved page count for high priority Q.	8'h40
15:8	R/W	P2_LQ_RESV	Reserved page count for low priority Q.	8'h10
7:0	R/W	P2_IQ_ASRT	Virtual input Q FC assertion threshold.	8'h10

CDMA_OQ_STA (offset:0x50)

Bits	Type	Name	Description	Initial value
31:24	RO	P0_OQ3_PCNT	CDMA output Q3 page count.	8'b0

23:16	RO	P0_OQ2_PCNT	CDMA output Q2 page count.	8'b0
15:8	RO	P0_OQ1_PCNT	CDMA output Q1 page count.	8'b0
7:0	RO	P0_OQ0_PCNT	CDMA output Q0 page count.	8'b0
GDMA1_OQ_STA (offset:0x54)				
Bits	Type	Name	Description	Initial value
31:24	RO	P1_OQ3_PCNT	GDMA1 output Q3 page count.	8'b0
23:16	RO	P1_OQ2_PCNT	GDMA1 output Q2 page count.	8'b0
15:8	RO	P1_OQ1_PCNT	GDMA1 output Q1 page count.	8'b0
7:0	RO	P1_OQ0_PCNT	GDMA1 output Q0 page count.	8'b0
GDMA2_OQ_STA (offset:0x58)				
Bits	Type	Name	Description	Initial value
31:24	RO	P2_OQ3_PCNT	GDMA2 output Q3 page count.	8'b0
23:16	RO	P2_OQ2_PCNT	GDMA2 output Q2 page count.	8'b0
15:8	RO	P2_OQ1_PCNT	GDMA2 output Q1 page count.	8'b0
7:0	RO	P2_OQ0_PCNT	GDMA2 output Q0 page count.	8'b0
PSE_IQ_STA (offset:0x5C)				
Bits	Type	Name	Description	Initial value
31:24	RO	P6_OQ0_PCNT	PPE output Q0 page count.	8'b0
23:16	RO	P2_IQ_PCNT	GDMA2 virtual input Q page count.	8'b0
15:8	RO	P1_IQ_PCNT	GDMA1 virtual input Q page count.	8'b0
7:0	RO	P0_IQ_PCNT	CDMA virtual input Q page count.	8'b0

3.10.3.3 Register Description – GDMA2

GDMA2_FWD_CFG : GDMA2 Forwarding Configuration (offset: 0x60)

Bits	Type	Name	Description	Initial value
31:28	R/W	GDM2_JMB_LEN	When GDM2_JMB_EN=1, this parameter define the maximum packet length(including CRC) that GDMA2 could receive in 1024-byte unit. The valid value is from 0 ~12.	4'd12
27:26	-	-	Reserved	
25	R/W	GDM2_20US_TICK_SLT	0: GDM2 shaper add token every 1ms. 1: GDM2 shaper add token every 20us. Please refer to GDM2_TK_RATE in GDMA2_SHPR_CFG register.	1'b0
24	R/W	GDM2_TCI_81xx	0: Check VLAN tag with EXT_VLAN[15:0] 1: Check VLAN tag with EXT_VLAN[15:8] only	1'd0
23	R/W	GDM2_DROP_256B	A Special mode to drop packets with payload > 256 bytes. 0 : Drop packets according to standard Ethernet frame length limitation. 1 : Drop packets with payload >256 bytes	1'b0
22	R/W	GDM2_ICS_EN	IPv4 header checksum check enable	1'b1
21	R/W	GDM2_TCS_EN	TCP checksum check enable	1'b1
20	R/W	GDM2_UCS_EN	UDP checksum check enable	1'b1
19	R/W	GDM2_JMB_EN	0 : Drop received frames if length is great than 1518 (1522 for VLAN frames, and 1526 for double VLAN frames) 1 : Allow receiving jumbo frames length up to 12kB.	1'b0
18	R/W	GDM2_DISPAD	0 : Enable GDMA2 Tx padding function. 1 : Disable GDMA2 Tx padding function.	1'b0
17	R/W	GDM2_DISCRC	0 : Enable GDMA2 Tx CRC generation. 1 : Disable GDMA2 Tx CRC generation.	1'b0
16	R/W	GDM2_STRPCRC	0 : Disable GDMA2 automatic Rx CRC stripping 1 : Enable GDMA2 automatic Rx CRC stripping	1'b1
15	-	-	Reserved	1'b0
14:12	R/W	GDM2_UFRC_P	GDMA2 My MAC uni-cast frames destination port 3'd0 : CPU	3'b111

			3'd1 : GDMA1 3'd2 : GDMA2 3'd6 : PPE 3'd7 : Discard Others: Reserved	
11	-	-	Reserved	1'b0
10:8	R/W	GDM2_BFRC_P	GDMA2 broad-cast MAC address frames destination port 3'd0 : CPU 3'd1 : GDMA1 3'd2 : GDMA2 3'd6 : PPE 3'd7 : Discard Others: Reserved	3'b111
7	-	-	Reserved	1'b0
6:4	R/W	GDM2_MFRC_P	GDMA2 multi-cast MAC address frames destination port 3'd0 : CPU 3'd1 : GDMA1 3'd2 : GDMA2 3'd6 : PPE 3'd7 : Discard Others: Reserved	3'b111
3	-	-	Reserved	1'b0
2:0	R/W	GDM2_OFRC_P	GDMA2 other MAC address frames destination port 3'd0 : CPU 3'd1 : GDMA1 3'd2 : GDMA2 3'd6 : PPE 3'd7 : Discard Others: Reserved	3'b111

GDMA2_SCH_CFG : GDMA2 Scheduling Configuration (offset: 0x64)

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	7'b0
25:24	R/W	GDM2_SCH_MOD	2'b00 : WRR 2'b01 : Strict Priority, Q3>Q2>Q1>Q0 2'b10 : Mixed, Q3>WRR(Q2,Q1,Q0) 2'b11 : Mixed, Q3>Q2>WRR(Q1,Q0)	2'b00
23:15	-	-	Reserved	1'b0
14:12	R/W	GDM2_WT_Q3	Q3's weight 3'd0 : weight = 1 3'd1 : weight = 2 3'd7 : weight = 8	3'b111
11	-	-	Reserved	1'b0
10:8	R/W	GDM2_WT_Q2	Q2's weight 3'd0 : weight = 1 3'd1 : weight = 2 3'd7 : weight = 8	3'b011
7	-	-	Reserved	1'b0
6:4	R/W	GDM2_WT_Q1	Q1's weight 3'd0 : weight = 1 3'd1 : weight = 2 3'd7 : weight = 8	3'b001

3	-	-	Reserved	1'b0
2:0	R/W	GDM2_WT_Q0	Q0's weight 3'd0 : weight = 1 3'd1 : weight = 2 3'd7 : weight = 8	3'b0

GDMA2_SHPR_CFG : GDMA2 Output Shaper Configuration (offset: 0x68)

Bits	Type	Name	Description	Initial value
31:25	-	-	Reserved	7'b0
24	R/W	GDM2_SHPR_EN	GDMA2 output shaper enable. 0 : Disable 1 : Enable	1'b0
23:16	R/W	GDM2_BK_SIZE	GDMA2 output shaper maximum bucket size. Unit is 1kB.	8'b0
15:14	-	-	Reserved	2'b0
13:0	R/W	GDM2_TK_RATE	GDMA2 output shaper token rate. Unit is 8B/ms or 8B/20us. According to GDM2_20US_TICK_SLT.	14'b0

GDMA2_MAC_ADRL : GDMA2 MAC Address LSB (offset: 0x6C)

Bits	Type	Name	Description	Initial value
31:0	R/W	GDM2_MY_MAC_L	GMAC2 MAC address bit 31-0	32'b0

GDMA2_MAC_ADRH : GDMA1 MAC Address MSB (offset: 0x70)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	GDM2_MY_MAC_H	GMAC2 MAC address bit 47-32	16'b0

3.10.3.4 Register Description - CPU Port

CDMA_CSG_CFG (offset: 0x80)

Bits	Type	Name	Description	Initial value
31:16	R/W	INS_VLAN_	Inserted VLAN type	16'h8100
15:3	-	-	Reserved	13'b0
2	R/W	ICS_GEN_EN	IPv4 header checksum generation enable	1'b0
1	R/W	UCS_GEN_EN	UDP checksum generation enable	1'b0
0	R/W	TCS_GEN_EN	TCP checksum generation enable	1'b0

CDMA_SCH_CFG (offset: 0x84)

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	6'b0
25:24	R/W	CDM_SCH_MOD	2'b00: WRR 2'b01: Strict Priority, Q3>Q2>Q1>Q0 2'b10: Mixed, Q3>WRR(Q2,Q1,Q0) 2'b11: Mixed, Q3>Q2>WRR(Q1,Q0)	2'b00
23:15	-	-	Reserved	9'b0
14:12	R/W	CDM_WT_Q3	Q3's weight 3'd0: weight = 1 3'd1: weight = 2 3'd7: weight = 8	3'b111
11	-	-	Reserved	1'b0
10:8	R/W	CDM_WT_Q2	Q2's weight 3'd0: weight = 1 3'd1: weight = 2 3'd7: weight = 8	3'b011
7	-	-	Reserved	1'b0
6:4	R/W	CDM_WT_Q1	Q1's weight 3'd0: weight = 1	3'b001

			3'd1: weight = 2 3'd7: weight = 8	
3	-	-	Reserved	1'b0
2:0	R/W	CDM_WT_Q0	Q0's weight 3'd0: weight = 1 3'd1: weight = 2 3'd7: weight = 8	3'b000

PPPOE_SID_0001 (offset: 0x88)

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID1	PPPoE Session ID for SID INDEX#1	16'b0
15:0	R/W	PPPOE_SID0	PPPoE Session ID for SID INDEX#0	16'b0

PPPOE_SID_0203 (offset: 0x8C)

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID3	PPPoE Session ID for SID INDEX#3	16'b0
15:0	R/W	PPPOE_SID2	PPPoE Session ID for SID INDEX#2	16'b0

PPPOE_SID_0405 (offset: 0x90)

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID5	PPPoE Session ID for SID INDEX#5	16'b0
15:0	R/W	PPPOE_SID4	PPPoE Session ID for SID INDEX#4	16'b0

PPPOE_SID_0607 (offset: 0x94)

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID7	PPPoE Session ID for SID INDEX#7	16'b0
15:0	R/W	PPPOE_SID6	PPPoE Session ID for SID INDEX#6	16'b0

PPPOE_SID_0809 (offset: 0x98)

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID9	PPPoE Session ID for SID INDEX#9	16'b0
15:0	R/W	PPPOE_SID8	PPPoE Session ID for SID INDEX#8	16'b0

PPPOE_SID_1011 (offset: 0x9C)

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID11	PPPoE Session ID for SID INDEX#11	16'b0
15:0	R/W	PPPOE_SID10	PPPoE Session ID for SID INDEX#10	16'b0

PPPOE_SID_1213 (offset: 0xa0)

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID13	PPPoE Session ID for SID INDEX#13	16'b0
15:0	R/W	PPPOE_SID12	PPPoE Session ID for SID INDEX#12	16'b0

PPPOE_SID_1415 (offset: 0xa4)

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID15	PPPoE Session ID for SID INDEX#15	16'b0
15:0	R/W	PPPOE_SID14	PPPoE Session ID for SID INDEX#14	16'b0

VLAN_ID_0001 (offset: 0xa8)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID0	VLAN ID of VLAN1	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID1	VLAN ID of VLAN0	12'b0

VLAN_ID_0203 (offset: 0xAC)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID2	VLAN ID of VLAN2	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID3	VLAN ID of VLAN3	12'b0

VLAN_ID_0405 (offset: 0xb0)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID4	VLAN ID of VLAN4	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID5	VLAN ID of VLAN5	12'b0

VLAN_ID_0607 (offset: 0xb4)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID6	VLAN ID of VLAN6	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID7	VLAN ID of VLAN7	12'b0

VLAN_ID_0809 (offset: 0xb8)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID8	VLAN ID of VLAN8	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID9	VLAN ID of VLAN9	12'b0

VLAN_ID_1011 (offset: 0xbC)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID10	VLAN ID of VLAN10	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID11	VLAN ID of VLAN11	12'b0

VLAN_ID_1213 (offset: 0xc0)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID12	VLAN ID of VLAN12	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID13	VLAN ID of VLAN13	12'b0

VLAN_ID_14_15 (offset: 0xc4)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID_14	VLAN ID of VLAN14	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID_15	VLAN ID of VLAN15	12'b0

FE_COS_MAP : Frame engine class of service mapping (offset: 0xc8)

Bits	Type	Name	Description	Initial value
31	R/W	PORT_PRI_EN	0: use VLAN priority 1: use source port priority	1'b0
30	R/W	EXT_SW_EN	0 : There is no external Ethernet switch which supports Ralink special tag on the frame engine's GE port #1. 1 : There is an external Ethernet switch which supports Ralink special tag on the frame engine's GE port #1. If both EXT_SW_EN and GDM1_TCI_81xx are set to 1, the frame engine will apply the following mapping to for identifying the source port of an incoming frame. This source port (SP[2:0]) will be attached to the RX descriptor when the frame 's destination port is CPU. It is also used for PPE's policy engine process to classify frames based frame headers and source port.	

			<table border="1"> <thead> <tr> <th>Incoming port</th><th>Frame Engine SP[2:0] (when EXT_SW_EN=1)</th><th>Frame Engine SP[2:0] (when EXT_SW_EN=0)</th></tr> </thead> <tbody> <tr><td>Ethernet SW P0</td><td>0</td><td>1</td></tr> <tr><td>Ethernet SW P1</td><td>1</td><td>1</td></tr> <tr><td>Ethernet SW P2</td><td>2</td><td>1</td></tr> <tr><td>Ethernet SW P3</td><td>3</td><td>1</td></tr> <tr><td>Ethernet SW P4</td><td>4</td><td>1</td></tr> <tr><td>Ethernet SW P5</td><td>5</td><td>1</td></tr> <tr><td>Frame Engine PDMA</td><td>6</td><td>0</td></tr> <tr><td>Frame Engine GE1</td><td>N/A</td><td>1</td></tr> <tr><td>Frame Engine GE2</td><td>5</td><td>2</td></tr> </tbody> </table>	Incoming port	Frame Engine SP[2:0] (when EXT_SW_EN=1)	Frame Engine SP[2:0] (when EXT_SW_EN=0)	Ethernet SW P0	0	1	Ethernet SW P1	1	1	Ethernet SW P2	2	1	Ethernet SW P3	3	1	Ethernet SW P4	4	1	Ethernet SW P5	5	1	Frame Engine PDMA	6	0	Frame Engine GE1	N/A	1	Frame Engine GE2	5	2	
Incoming port	Frame Engine SP[2:0] (when EXT_SW_EN=1)	Frame Engine SP[2:0] (when EXT_SW_EN=0)																																
Ethernet SW P0	0	1																																
Ethernet SW P1	1	1																																
Ethernet SW P2	2	1																																
Ethernet SW P3	3	1																																
Ethernet SW P4	4	1																																
Ethernet SW P5	5	1																																
Frame Engine PDMA	6	0																																
Frame Engine GE1	N/A	1																																
Frame Engine GE2	5	2																																
			<pre> graph TD subgraph Frame_Engine [Frame Engine] direction TB PPE[PPE (P6)] --- FE[Frame Engine] PDMA[PDMA (P0)] --- FE GE1[GE1 (P1)] --- FE GE2[GE2 (P5)] --- FE P6[Port 6 (GE)] --- FE end subgraph External_Switch [External Ethernet Switch] direction LR P5[P5 (GE)] --- ES[External Ethernet Switch] P4[P4] --- ES P3[P3] --- ES P2[P2] --- ES P1[P1] --- ES P0[P0] --- ES end FE --- P5 FE --- P6 </pre>																															
			<p>Porting issues for software :</p> <ol style="list-style-type: none"> 1. In this external switch mode, packets come from CPU (PDMA) and loopbacked by PPE back to CPU will be denoted as coming from port "6" (see the mapping table above) 2. In this external switch mode, packets come from GE2 will be denoted as coming from port "5" (see the mapping table above) 3. There are two port #5 in the mapping table. It is because we just assume if customers want to use port#5 of the external switch, they might not want to use the GE2 of the frame engine. The reason for not using "port #7" to denote GE2 is we reserve "7" as "don't care source port" in the policy table of the PPE. 																															
29:28	-	-	Reserved																															
27:26	R/W	Port5_QUEUE	Dest. queue # for frames with source port=5	2'b00																														
25:24	R/W	Port4_QUEUE	Dest. queue # for frames with source port=4	2'b00																														
23:22	R/W	Port3_QUEUE	Dest. queue # for frames with source port=3	2'b00																														
21:20	R/W	Port2_QUEUE	Dest. queue # for frames with source port=2	2'b00																														

19:18	R/W	Port1_QUEUE	Dest. queue # for frames with source port=1	2'b00
17:16	R/W	Port0_QUEUE	Dest. queue # for frames with source port=0	2'b00
15:14	R/W	VPRI7_QUEUE	Dest. queue # for frames with VLAN priority=7	2'b00
13:12	R/W	VPRI6_QUEUE	Dest. queue # for frames with VLAN priority=6	2'b00
11:10	R/W	VPRI5_QUEUE	Dest. queue # for frames with VLAN priority=5	2'b00
9:8	R/W	VPRI4_QUEUE	Dest. queue # for frames with VLAN priority=4	2'b00
7:6	R/W	VPRI3_QUEUE	Dest. queue # for frames with VLAN priority=3	2'b00
5:4	R/W	VPRI2_QUEUE	Dest. queue # for frames with VLAN priority=2	2'b00
3:2	R/W	VPRI1_QUEUE	Dest. queue # for frames with VLAN priority=1	2'b00
1:0	R/W	VPRI0_QUEUE	Dest. queue # for frames with VLAN priority=0	2'b00

3.10.3.5 Register Description - PDMA

PDMA_GLO_CFG (offset:0x100)

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	2'b0
29:16	R/W	HDR_SEG_LEN	Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value. When set to zero, the header/payload scattering feature is disabled.	14'b0
15:8	-	-	Reserved	8'b0
7	-	-	Reserved	1'b0
6	R/W	TX_WB_DDONE	0 : Disable TX_DMA writing back DDONE into TXD 1 : Enable TX_DMA writing back DDONE into TXD	1'b1
5:4	R/W	PDMA_BT_SIZE	Define the burst size of PDMA 0 : 4 DWORD (16bytes) 1 : 8 DWORD (32 bytes) 2 : Reserved 3 : Reserved	2'd1
3	RO	RX_DMA_BUSY	1 : RX_DMA is busy 0 : RX_DMA is not busy	1'b0
2	R/W	RX_DMA_EN	1 : Enable RX_DMA 0 : Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop.)	1'b0
1	RO	TX_DMA_BUSY	1 : TX_DMA is busy 0 : TX_DMA is not busy	1'b0
0	R/W	TX_DMA_EN	1 : Enable TX_DMA 0 : Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)	1'b0

PDMA_RST_IDX (offset:0x104)

Bits	Type	Name	Description	Initial value
31:17	-	-	Reserved	15'b0
16	W1C	RST_DRX_IDX0	Write 1 to reset to RX_DRX_IDX0 to 0	1'b0
15:4	-	-	Reserved	12'b0
3	W1C	RST_DTX_IDX3	Write 1 to reset to TX_DTX_IDX3 to 0	1'b0
2	W1C	RST_DTX_IDX2	Write 1 to reset to TX_DTX_IDX2 to 0	1'b0
1	W1C	RST_DTX_IDX1	Write 1 to reset to TX_DTX_IDX1 to 0	1'b0
0	W1C	RST_DTX_IDX0	Write 1 to reset to TX_DTX_IDX0 to 0	1'b0

DLY_INT_CFG (offset 0x10C)

Bits	Type	Name	Description	Initial value
31	RW	TXDLY_INT_EN	1: Enable TX delayed interrupt mechanism. 0: Disable TX delayed interrupt mechanism.	1'b0
30:24	RW	TXMAX_PINT	Specified Max # of pended interrupts.	7'b0

			When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final TX_DLY_INT is generated. Set to 0 will disable this feature	
23:16	RW	TXMAX_PTIME	Specified Max pending time for the internal TX_DONE_INT0 and TX_DONE_INT1. When the pending time equal or grater TXMAX_PTIME x 20us or the # of pended TX_DONE_INT0 and TX_DONE_INT1 equal or grater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated. Set to 0 will disable this feature	8'b0
15	RW	RXDLY_INT_EN	1: Enable RX delayed interrupt mechanism. 0: Disable RX delayed interrupt mechanism.	1'b0
14:8	RW	RXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final RX_DLY_INT is generated. Set to 0 will disable this feature	7'b0
7:0	RW	RXMAX_PTIME	Specified Max pending time for the internal RX_DONE_INT. When the pending time equal or grater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or grater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated Set to 0 will disable this feature.	8'b0

TX_BASE_PTR0 (offset: 0x110)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_BASE_PTR0	Point to the base address of TX_Ring0 (4-DWORD aligned address)	32'b0

TX_MAX_CNT0 (offset: 0x114)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_MAX_CNT0	The maximum number of TXD count in TXD_Ring0.	12'b0

TX_CTX_IDX0 (offset:0x118)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_CTX_IDX0	Point to the next TXD in TXD_Ring0 CPU wants to use	12'b0

TX_DTX_IDX0 (offset:0x11C)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	RO	TX_DTX_IDX0	Point to the next TXD in TXD_Ring0 DMA wants to use	12'b0

TX_BASE_PTR1(offset:0x120)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_BASE_PTR1	Point to the base address of TX_Ring1 (4-DWORD aligned address)	32'b0

TX_MAX_CNT1 (offset:0x124)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_MAX_CNT1	The maximum number of TXD count in TXD_Ring1.	12'b0

TX_CTX_IDX1(offset:0x128)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_CTX_IDX1	Point to the next TXD in TXD_Ring1 CPU wants to use	12'b0

TX_DTX_IDX1 (offset:0x12C)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	RO	TX_DTX_IDX1	Point to the next TXD in TXD_Ring1 DMA wants to use	0

RX_BASE_PTR0 (offset:0x130)

Bits	Type	Name	Description	Initial value
31:0	R/W	RX_BASE_PTR0	Point to the base address of RXD Ring #0. It should be a 4-DWORD aligned address	0

RX_MAX_CNT0 (offset:0x134)

Bits	Type	Name	Description	Initial value
31:12	R-	-	Reserved	0
11:0	R/W	RX_MAX_CNT0	The maximum number of RXD count in RXD Ring #0.	0

ALC_IDX0 (offset:0x138)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0
11:0	R/W	RX_CALC_IDX0	Point to the next RXD CPU wants to allocate to RXD Ring #0.	0

RX_DRX_IDX0 (offset:0x13C)

Bits	Type	Name	Description	Initial value
31:12	RO	Reserved	Reserved	0
11:0	RO	RX_DRX_IDX0	Point to the next RXD DMA wants to use in RXD Ring#0. It should be a 4-DWORD aligned address.	0

TX_BASE_PTR2(offset:0x140)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_BASE_PTR2	Point to the base address of TX_Ring2 (4-DWORD aligned address)	32'b0

TX_MAX_CNT2 (offset:0x144)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_MAX_CNT2	The maximum number of TXD count in TXD_Ring2.	12'b0

TX_CTX_IDX2(offset:0x148)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_CTX_IDX2	Point to the next TXD in TXD_Ring2 CPU wants to use	12'b0

TX_DTX_IDX2 (offset:0x14C)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	RO	TX_DTX_IDX2	Point to the next TXD in TXD_Ring2 DMA wants to use	0

TX_BASE_PTR3(offset:0x150)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_BASE_PTR3	Point to the base address of TX_Ring3 (4-DWORD aligned address)	32'b0

TX_MAX_CNT3 (offset:0x154)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_MAX_CNT3	The maximum number of TXD count in TXD_Ring3.	12'b0

TX_CTX_IDX3(offset:0x158)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_CTX_IDX3	Point to the next TXD in TXD_Ring3 CPU wants to use	12'b0

TX_DTX_IDX3 (offset:0x15C)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	RO	TX_DTX_IDX3	Point to the next TXD in TXD_Ring3 DMA wants to use	0

PDMA_FC_CFG1 (offset:0x1EC)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	PDM_FC_DEF_Q1	TXRING Q1 flow control pause condition Bit[11]: pause Q1 when PSE P2 Q3 full Bit[10]: pause Q1 when PSE P2 Q2 full Bit[9]: pause Q1 when PSE P2 Q1 full Bit[8]: pause Q1 when PSE P2 Q0 full Bit[7]: pause Q1 when PSE P1 Q3 full Bit[6]: pause Q1 when PSE P1 Q2 full Bit[5]: pause Q1 when PSE P1 Q1 full Bit[4]: pause Q1 when PSE P1 Q0 full Bit[3]: pause Q1 when PSE P0 Q3 full Bit[2]: pause Q1 when PSE P0 Q2 full Bit[1]: pause Q1 when PSE P0 Q1 full Bit[0]: pause Q1 when PSE P0 Q0 full	12'hFFF
15:12	-	-	Reserved	4'b0
11:0	R/W	PDM_FC_DEF_Q0	TXRING Q0 flow control pause condition Bit[11]: pause Q0 when PSE P2 Q3 full Bit[10]: pause Q0 when PSE P2 Q2 full Bit[9]: pause Q0 when PSE P2 Q1 full Bit[8]: pause Q0 when PSE P2 Q0 full Bit[7]: pause Q0 when PSE P1 Q3 full Bit[6]: pause Q0 when PSE P1 Q2 full Bit[5]: pause Q0 when PSE P1 Q1 full Bit[4]: pause Q0 when PSE P1 Q0 full Bit[3]: pause Q0 when PSE P0 Q3 full Bit[2]: pause Q0 when PSE P0 Q2 full Bit[1]: pause Q0 when PSE P0 Q1 full Bit[0]: pause Q0 when PSE P0 Q0 full	12'hFFF

PDMA_FC_CFG2 (offset:0x1F0)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	PDM_FC_DEF_Q1	TX RING Q3 flow control pause condition Bit[11]: pause Q3 when PSE P2 Q3 full Bit[10]: pause Q3 when PSE P2 Q2 full Bit[9]: pause Q3 when PSE P2 Q1 full Bit[8]: pause Q3 when PSE P2 Q0 full Bit[7]: pause Q3 when PSE P1 Q3 full Bit[6]: pause Q3 when PSE P1 Q2 full Bit[5]: pause Q3 when PSE P1 Q1 full Bit[4]: pause Q3 when PSE P1 Q0 full Bit[3]: pause Q3 when PSE P0 Q3 full Bit[2]: pause Q3 when PSE P0 Q2 full Bit[1]: pause Q3 when PSE P0 Q1 full Bit[0]: pause Q3 when PSE P0 Q0 full	12'hFFF
15:12	-	-	Reserved	4'b0
11:0	R/W	PDM_FC_DEF_Q0	TX RING Q2 flow control pause condition Bit[11]: pause Q2 when PSE P2 Q3 full Bit[10]: pause Q2 when PSE P2 Q2 full Bit[9]: pause Q2 when PSE P2 Q1 full Bit[8]: pause Q2 when PSE P2 Q0 full Bit[7]: pause Q2 when PSE P1 Q3 full Bit[6]: pause Q2 when PSE P1 Q2 full	12'hFFF

			Bit[5]: pause Q2 when PSE P1 Q1 full Bit[4]: pause Q2 when PSE P1 Q0 full Bit[3]: pause Q2 when PSE P0 Q3 full Bit[2]: pause Q2 when PSE P0 Q2 full Bit[1]: pause Q2 when PSE P0 Q1 full Bit[0]: pause Q2 when PSE P0 Q0 full	
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SCH_Q01_CFG : Scheduler configuration for queue #0 and #1 (offset: 0x1F4)

Bits	Type	Name	Description	Initial value
31	R/W	MAX_BKT_SIZE1	When set to 0, the max bucket size (burst size allowed in byte) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us. When set to 1, the max bucket size (burst size allowed in byte) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us + 2048 bytes.	1'b0
30	R/W	MAX_RATE_ULMT1	When set to 1, the max rate limitation function for queue #1 is disabled. The max rate for queue #1 is unlimited. The scheduler would allocate bandwidth to queue #1 based on MAX_WEIGHT1. When set to 0, the max rate limitation function for queue #1 is enabled. The max rate for queue #1 is defined by MAX_RATE1.	1'b1
29:28	R/W	MAX_WEIGHT1	Define the auto-reload bucket size if MAX_RATE_ULMT1 is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue #1. 2'b00 : 1023 bytes 2'b01 : 2047 bytes 2'b10 : 4095 bytes 2'b11: 8191 bytes	2'd1
27:26	R/W	MIN_RATE_RATI01	Define the guaranteed Min rate based on MAX_RATE1. 2'b00 : MIN_RATE1 = MAX_RATE1 2'b01 : MIN_RATE1 = 1/2 MAX_RATE1 2'b10 : MIN_RATE1 = 1/4 MAX_RATE1 2'b11 : MIN_RATE1 = 0	2'd3
25:16	R/W	MAX_RATE1	Define the limited Max rate for queue # 1 if MAX_RATE_ULMT1 is 0. The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example, If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps	10'd0
15	R/W	MAX_BKT_SIZE0	When set to 0, the max bucket size (burst size allowed in byte) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us. When set to 1, the max bucket size (burst size allowed in byte) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us + 2048 bytes.	1'b0
14	R/W	MAX_RATE_ULMT0	When set to 1, the max rate limitation function for queue #0 is disabled. The max rate for queue #0 is unlimited. The scheduler would allocate bandwidth to queue #0 based on MAX_WEIGHT0. When set to 0, the max rate limitation function for queue #0 is	1'b1

			enabled. The max rate for queue #0 is defined by MAX_RATE0.	
13:12	R/W	MAX_WEIGHT0	<p>Define the auto-reload bucket size if MAX_RATE_ULMT0 is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue #0.</p> <p>2'b00 : 1023 bytes 2'b01 : 2047 bytes 2'b10 : 4095 bytes 2'b11: 8191 bytes</p>	2'd0
11:10	R/W	MIN_RATE_RATI00	<p>Define the guaranteed Min rate based on MAX_RATE0.</p> <p>2'b00 : MIN_RATE0 = MAX_RATE0 2'b01 : MIN_RATE0 = 1/2 MAX_RATE0 2'b10 : MIN_RATE0 = 1/4 MAX_RATE0 2'b110 : MIN_RATE0 = 0</p>	2'd3
9:0	R/W	MAX_RATE0	<p>Define the limited Max rate for queue #0 if MAX_RATE_ULMT0 is 0.</p> <p>The value specified represents the amount of 4-byte quota to be added into the queue #0 bucket per 125us.</p> <p>For example, If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\mu\text{s} = 16.384 \text{M bytes/sec or } 131 \text{Mbps}$</p>	10'd0

SCH_Q23_CFG : Scheduler configuration for queue #2 and #3 (offset: 0x1f8)

Bits	Type	Name	Description	Initial value
31	R/W	MAX_BKT_SIZE3	<p>When set to 0, the max bucket size (burst size allowed) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us.</p> <p>When set to 1, the max bucket size (burst size allowed) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us + 2048 bytes.</p>	1'b0
30	R/W	MAX_RATE_ULMT3	<p>When set to 1, the max rate limitation function for queue #3 is disabled. The max rate for queue #3 is unlimited. The scheduler would allocate bandwidth to queue #3 based on MAX_WEIGHT3.</p> <p>When set to 0, the max rate limitation function for queue #3 is enabled. The max rate for queue #3 is defined by MAX_RATE3.</p>	1'b1
29:28	R/W	MAX_WEIGHT3	<p>Define the auto-reload bucket size if MAX_RATE_ULMT3 is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue #3.</p> <p>2'b00 : 1023 bytes 2'b01 : 2047 bytes 2'b10 : 4095 bytes 2'b11: 8191 bytes</p>	2'd3
27:26	R/W	MIN_RATE_RATI03	<p>Define the guaranteed Min rate based on MAX_RATE3.</p> <p>2'b00 : MIN_RATE3 = MAX_RATE3 2'b01 : MIN_RATE3 = 1/2 MAX_RATE3 2'b10 : MIN_RATE3 = 1/4 MAX_RATE3 2'b11 : MIN_RATE3 = 0</p>	2'd3
25:16	R/W	MAX_RATE3	<p>Define the limited Max rate for queue #3 if MAX_RATE_ULMT3 is 0. The value specified represents the amount of 4-byte quota to be</p>	10'd0

			added into the queue #1 bucket per 125us. For example,: If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec or } 131\text{Mbps}$	
15	R/W	MAX_BKT_SIZE2	When set to 0, the max bucket size (burst size allowed) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us. When set to 1, the max bucket size (burst size allowed) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us + 2048 bytes.	1'b0
14	R/W	MAX_RATE_ULMT2	When set to 1, the max rate limitation function for queue #2 is disabled. The max rate for queue #2 is unlimited. The scheduler would allocate bandwidth to queue #2 based on MAX_WEIGHT2. When set to 0, the max rate limitation function for queue #2 is enabled. The max rate for queue #2 is defined by MAX_RATE0.	1'b1
13:12	R/W	MAX_WEIGHT2	Define the auto-reload bucket size if MAX_RATE_ULMT0 is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue #2. 2'b00 : 1023 bytes 2'b01 : 2047 bytes 2'b10 : 4095 bytes 2'b11: 8191 bytes	2'd2
11:10	R/W	MIN_RATE_RATI02	Define the guaranteed Min rate based on MAX_RATE0. 2'b00 : MIN_RATE2 = MAX_RATE2 2'b01 : MIN_RATE2 = 1/2 MAX_RATE2 2'b10 : MIN_RATE2 = 1/4 MAX_RATE2 2'b11 : MIN_RATE2 = 0	2'd3
9:0	R/W	MAX_RATE2	Define the limited Max rate for queue # 2 if MAX_RATE_ULMT2 is 0. The value specified represents the amount of 4-byte quota to be added into the queue #0 bucket per 125us. For example : If 512 is programmed, then the max rate limited is : $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec or } 131\text{Mbps}$	10'd0

3.10.3.6 Register Description – Frame Engine Counters (base: 0x1010.0400)

0x300	GDMA_TX_GBCNT1	Transmit good byte count for GDMA port#1&2
0x304	GDMA_TX_GPCNT1	Transmit good pkt count for GDMA port#1&2 (not including flow control frames)
0x308	GDMA_TX_SKIPCNT1	Transmit skip count for GDMA port#1&2
0x30C	GDMA_TX_COLCNT1	Transmit collision count for GDMA port#1&2
0x310 – 0x31C	Reserved	
0x320	GDMA_RX_GBCNT1	Received good byte count for GDMA port#1&2
0x324	GDMA_RX_GPCNT1	Received good pkt count for GDMA port#1&2 (not including flow control frames)
0x328	GDMA_RX_OERCNT1	Received overflow error pkt count for GDMA port#1&2
0x32C	GDMA_RX_FERCNT1	Received FCS error pkt count for GDMA port#1&2
0x330	GDMA_RX_SERCNT1	Received too short error pkt count for GDMA port#1&2

0x334	GDMA_RX_LERCNT1	Received too long error pkt count for GDMA port#1&2
0x338	GDMA_RX_CERCNT1	Received ip/tcp/udp checksum error pkt count for GDMA port#1&2
0x33C	GDMA_RX_FCCNT1	Received flow control pkt count for GDMA port#1&2

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3.11 Ethernet Switch

3.11.1 Features

- Support IEEE 802.3 full duplex flow control
- 5 10/100Mbps PHY
- Support Spanning Tree port states
- Support 1K-MAC address table with direct or XOR hash
- QoS
 - Four priorities queues per port
 - Packet classification based on incoming port, IEEE 802.1p or IP ToS/DSCP
 - Strict-Priority Queue (PQ) and Weighted Round Robin (WRR)
- VLAN
 - Port Base VLAN
 - Double VLAN tagging
 - 802.1q tag VLAN
 - 16 VIDs
- MAC address table read and write-able
- MAC security – Locking a MAC address to an incoming port
- MAC clone support – hash with VID
- IGMP support
- Broadcast storm prevention

Draft

3.11.2 Block Diagram

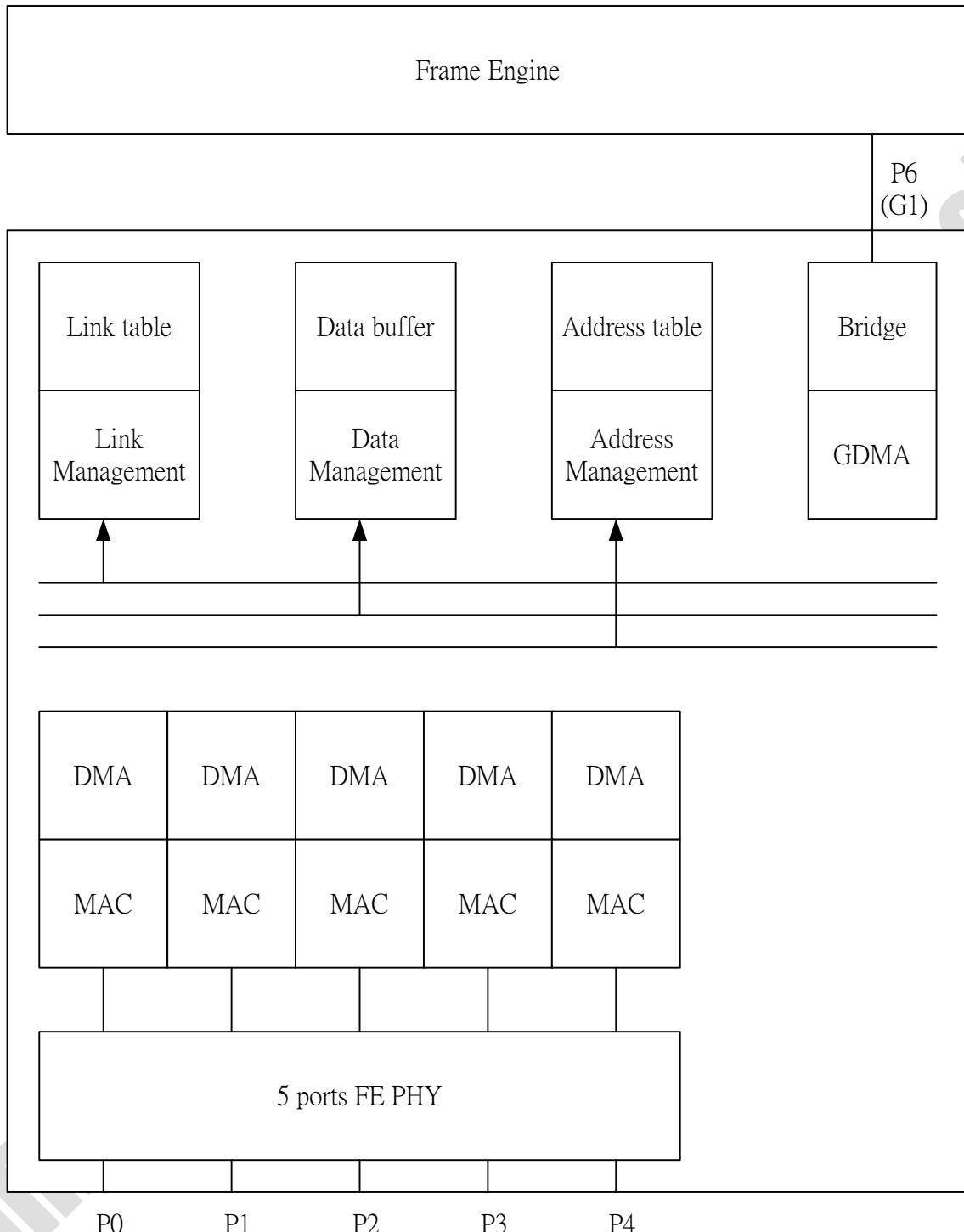


Fig. 3-20-1 Ethernet Switch Block Diagram

3.11.3 Frame Classification

FTAG	DA	Type	IPv4/IPv6 Protocol	Description
BC	FF-FF-FF-FF-FF-FF	-	-	Broadcast Frames
MC	Bit.40=1'b1	-	-	Multicast Frames
IGMP	01-00-5E-xx-xx-xx	08-00	0x02	IGMP Message Packet
IP_MULT	01-00-5E-xx-xx-xx	-		IP Multicast Frames
MLD	33-33-xx-xx-xx-xx	86-DD	0x00 (Hop_by_Hop) 0x3A (ICMPv6)	MLD/ICMPv6 Message Packet
IPV6_MULT	33-33-xx-xx-xx-xx	-		IPv6 Multicast Frames
PAUSE	-	88-08	-	Discarded
	01-80-C2-00-00-01 Or Unicast DA	88-08	Followed by 00-01	MAC Control Pause Frame (< 1518 bytes) Discarded
RMC	01-80-C2-00-00-00	-	-	BPDU
	01-80-C2-00-00-02 ~ 01-80-c2-00-00-xx			Reserved Group/Multicast Frames

Fig. 3-18-2 Reserved Multicast Address Frames

3.11.4 Register Description (base: 0x1011.0000)

Note : In RT3350, the registers realted P5 (port 5) are not applicable. Please keep them as default settings

ISR: Interrupt Status Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:30		-	Reserved	2'b0
29	RO	WATCHDOG1_TMR_EXPIRED	P5 no transmit packet alert. This bit indicating that P5 don't transmit packet for 3 seconds when P5 need to transmit packet.	1'b0
28	R/W	WATCHDOG0_TMR_EXPIRED	Abnormal Alert This bit indicating that global queue block counts is less than buf_starvation_th for 3 seconds. Write one clear.	1'b0
27	R/W	HAS_INTRUDER	Intruder Alert This bit indicating that an unsecured packet is coming into a secured port. Write one clear.	1'b0
26	R/W	PORT_ST_CHG	Port status change Any port from link status change. Write one clear.	1'b0
25	R/W	BC_STORM	BC storm The device is undergoing broadcast storm. Write one clear.	1'b0
24	R/W	MUST_DROP_LAN	Queue exhausted The global queue is used up and all packets are dropped. Write one clear.	1'b0
23	R/W	GLOBAL_QUE_FULL	Global Queue Full. Write one clear.	1'b0
22:21	-	Reserved		2'b0
20	R/W	LAN_QUE_FULL[6]	Port6 out queue full. Write one clear.	1'b0
19	R/W	LAN_QUE_FULL[5]	Port5 out queue full. Write one clear.	1'b0
18	R/W	LAN_QUE_FULL[4]	Port4 out queue full. Write one clear.	1'b0
17	R/W	LAN_QUE_FULL[3]	Port3 out queue full. Write one clear.	1'b0
16	R/W	LAN_QUE_FULL[2]	Port2 out queue full. Write one clear.	1'b0
15	R/W	LAN_QUE_FULL[1]	Port1 out queue full. Write one clear.	1'b0
14	R/W	LAN_QUE_FULL[0]	Port0 out queue full. Write one clear.	1'b0
13:0	-	Reserved		14'b0

IMR: Interrupt Mask Register (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:30	-		Reserved	2'b01
29	R/W	SW_INT_MASK_29	P5 no transmit packet alert. This bit indicating that P5 don't transmit packet for 3 seconds when P5 need to transmit packet.	1'b1
28	R/W	SW_INT_MASK_28	Abnormal Alert This bit indicating that global queue block counts is less than buf_starvation_th for 3 seconds.	1'b1
27	R/W	SW_INT_MASK_27	Intruder Alert This bit indicating that an unsecured packet is coming into a secured port.	1'b1
26	R/W	SW_INT_MASK_26	Port status change Any port from link status change	1'b1
25	R/W	SW_INT_MASK_25	BC storm The device is undergoing broadcast storm	1'b1
24	R/W	SW_INT_MASK_24	Queue exhausted The global queue is used up and all packets are dropped	1'b1
23	R/W	SW_INT_MASK_23	Shared queue full	1'b1
22:21			Reserved	2'b11
20	R/W	SW_INT_MASK_20	port6 queue full	1'b1
19	R/W	SW_INT_MASK_19	port5 queue full	1'b1
18	R/W	SW_INT_MASK_18	port4 queue full	1'b1
17	R/W	SW_INT_MASK_17	port3 queue full	1'b1
16	R/W	SW_INT_MASK_16	port2 queue full	1'b1
15	R/W	SW_INT_MASK_15	port1 queue full	1'b1
14	R/W	SW_INT_MASK_14	port0 queue full	1'b1
13	R/W	SW_INT_MASK_13	Reserved	1'b1
12	R/W	SW_INT_MASK_12	Reserved	1'b1
11	R/W	SW_INT_MASK_11	Reserved	1'b1
10	R/W	SW_INT_MASK_10	Reserved	1'b1
9	R/W	SW_INT_MASK_9	Reserved	1'b1
8	R/W	SW_INT_MASK_8	Reserved	1'b1
7	R/W	SW_INT_MASK_7	Reserved	1'b1
6	R/W	SW_INT_MASK_6	Reserved	1'b1
5	R/W	SW_INT_MASK_5	Reserved	1'b1
4	R/W	SW_INT_MASK_4	Reserved	1'b1
3	R/W	SW_INT_MASK_3	Reserved	1'b1
2	R/W	SW_INT_MASK_2	Reserved	1'b1
1	R/W	SW_INT_MASK_1	Reserved.	1'b1
0	R/W	SW_INT_MASK_0	Reserved	1'b1

FCT0: Flow Control Threshold 0 (offset:0x08)

Bits	Type	Name	Description	Initial value
31:24	R/W	FC_RLS_TH	Flow Control Release Threshold Flow control will be disabled when the global queue block counts is greater than the release threshold	8'd255
23:16	R/W	FC_SET_TH	Flow Control Set Threshold Flow control will be enabled when the global queue block counts is less than the set threshold	8'd200
15:8	R/W	DROP_RLS_TH	Drop Release Threshold Switch will stop dropping packets when the global queue block counts is greater than the drop-release threshold	8'd110

7:0	R/W	DROP_SET_TH	Drop Set Threshold Switch will start dropping packets when the global queue block counts is less than the drop-set threshold.	8'd90
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FCT1: Flow Control Threshold 1 (offset: 0x0C)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'd0
7:0	R/W	PORT_TH	Per Port Output Threshold When the global queue reaches the flow control or drop threshold on register FCT0, per port output threshold will be checked to enable flow-control or packet-drop depending on per queue minimum reserved blocks of the register PFC2.	8'd20

PFC0: Priority flow control – 0 (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'd0
27:24	R/W	MTCC_LMT	MTCC LIMIT The maximum Back-off count limit to drop excessive collision packets.	4'd15
23			Reserved	-
22:16	R/W	TURN_OFF_FC	Turn off FC When Receiving High Packet Auto-turn-off FC when the programmed ports receive one of the highest priority packet. <u>0: disable</u> <u>1: enable</u>	7'd0
15:12	R/W	VO_NUM	The proportional number of WRR for Voice Queue After transmit exactly the number of packets then proceed to next queue. If equal to 0, only this queue is forced to the strict priority mode	4'd0
11:8	R/W	CL_NUM	The proportional number of WRR for Control-Load Queue After transmit exactly the number of packet then proceed to next queue.	4'd0
7:4	R/W	BE_NUM	The proportional number of WRR for Best-Effort Queue After transmit exactly the number of packet then proceed to next queue.	4'd0
3:0	R/W	BK_NUM	The proportional number of WRR for Background Queue After transmit exactly the number of packet then proceed to next queue.	4'd0

PFC1: Priority Flow control –1 (offset: 0x14)

Bits	Type	Name	Description	Initial value
31	R/W	CPU_USE_Q1_EN	CPU Port only use q1 enable 0: default priority resolution 1: packets forwarded to CPU port uses Best-Effort Queue.	1'b0
30:24	R/W	EN_TOS[7:0]	Port6 ~ port0 TOS_en. Check TOS field of IP packets for priority resolution. 0: disable 1 :enable	7'd0
23	R/W	IGMP_to_CPU	IGMP forward to CPU enable 1'b0 : IGMP message will be flooded to all ports 1'b1 : IGMP message will be forwarded to CPU port only.	1'b0

22:16	R/O	EN_VLAN	Enable per port VLAN ID and priority tag check. 0: disable. 1: enable	8'd0
15	R/W	PRIORITY_OPTION	Priority Resolution Option 0 : 802.1p → TOS → Per port 1 : TOS → 802.1p → Per port	1'b0
14			Reserved	1'b0
13:12	R/W	PORT_PRI6	Port priority By setting this register to force per port's default priority.	2'b01
11:10	R/W	PORT_PRI5	Port priority By setting this register to force per port's default priority.	2'b01
9:8	R/W	PORT_PRI4	Port priority By setting this register to force per port's default priority.	2'b01
7:6	R/W	PORT_PRI3	Port priority By setting this register to force per port's default priority.	2'b01
5:4	R/W	PORT_PRI2	Port priority By setting this register to force per port's default priority.	2'b01
3:2	R/W	PORT_PRI1	Port priority By setting this register to force per port's default priority.	2'b01
1:0	R/W	PORT_PRIO	Port priority By setting this register to force per port's default priority.	2'b01

PFC2: Priority flow control –2 (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:24	R/W	PRI_TH_VO	Voice Threshold – Highest Priority The minimum reserved packet block count which outout queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the queued blocks exceed the threshold, the incoming packet will be paused or dropped.	8'd3
23:16	R/W	PRI_TH_CL	Control Load Threshold The minimum reserved packet block count which outout queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the queued blocks exceed the threshold, the incoming packet will be paused or dropped.	8'd3
15:8	R/W	PRI_TH_BE	Best Effort threshold The minimum reserved packet block count which outout queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the queued blocks exceed the threshold, the incoming packet will be paused or dropped.	8'd3
7:0	R/W	PRI_TH_BK	Background Threshold – Lowest Priority The minimum reserved packet block count which outout queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the queued blocks exceed the threshold, the incoming packet will be paused or dropped.	8'd3

GQS0: Global Queue Status – 0 (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:9		-	Reserved	23'd0
8:0	RO	EMPTY_CNT	Global Queue Block Counts This field indicates the number of block count left in the global free queue.	9'h16b

GQS1: Global Queue Status – 1 (offset: 0x20)

Bits	Type	Name	Description	Initial value
31			Reserved	-
30:24	RO	OUTQUE_FULL_VO	Congested Voice Queue The corresponding queue is congested	7'd0
24			Reserved	-
23:16	RO	OUTQUE_FULL_CL	Congested Control Load Queue The corresponding queue is congested	7'd0
15			Reserved	-
14:8	RO	OUTQUE_FULL_BE	Congested Best Effort Queue The corresponding queue is congested	7'd0
7			Reserved	-
6:0	RO	OUTQUE_FULL_BK	Congested Background Queue The corresponding queue is congested	7'd0

ATS: Address Table Search (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:3		-	Reserved	29'b0
2	RO	AT_LKUP_IDLE	Address Lookup Idle This field indicates that Address Table engine is in IDLE state.	1'b0
1	R/W	SEARCH_NXT_ADDR	Search For The Next Address (Self_Clear)	1'b0
0	R/W	BEGIN_SEARCH_ADDR	Start Searching The Address Table (Self_Clear)	1'b0

ATSO: Address Table Status 0 (offset: 0x28)

Bits	Type	Name	Description	Initial value
31:22	RO	HASH_ADD_LU	Address table lookup address	10'd0
21:19		-	Reserved	3'd0
18:12	RO	R_PORT_MAP	Port map The MAC existing in the bit =1.	7'd0
11		-	Reserved	-
10:7	RO	R_VID	VLAN index	4'd0
6:4	RO	R_AGE_FIELD	Aging field	3'd0
3			Reserved	-
2	RO	R_MC_INGRESS	MC Ingress	1'b0
1	RO	AT_TABLE_END	Search to the end of address table	1'b0
0	RO	SEARCH_RDY	Data is ready (read clear)	1'b0

ATS1: Address Table Status 1 (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:16		-	Reserved	16'b0
15:0	RO	MAC_AD_SER0	Read MAC address [15:0]	16'bx

ATS2: Address Table Status 2 (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:0	RO	MAC_AD_SER1	Read MAC address [47:16]	32'b0

WMAD0: WT_MAC_AD0 (offset: 0x34)

Bits	Type	Name	Description	Initial value
31:22	RO	HASH_ADD_CFG	Address table configuration address	10'd0
21:19		-	Reserved	3'd0
19	RO	AT_CFG_IDLE	Address table configuration SM idle	1'b1
18:12	R/W	W_PORT_MAP	Write Port Bit-map	7'b0
11		-	Reserved	-

10:7	R/W	W_INDEX	Write VLAN Index 0: VLAN 0 ~ 15: VLAN 15	4'b0
6:4	R/W	W_AGE_FIELD	Write aging field, 111b : static address, 001b ~110b: the entry is valid and will be aged out 000b : default, entry is invalid	3'b0
3	R/W	-SA_FILTER	SA_FILTER 0: defult 1: the corresponding packet will be dropped when the SA is matched.	1'b0
2	R/W	W_MC_INGRESS	Write Mc_Ingress Bit	1'b0
1	RO	W_MAC_DONE	MAC Write Done 0: default 1: MAC address write OK, (read_clear)	1'b0
0	R/W	W_MAC_CMD	MAC Address Write Command 0: default 1: the MAC write data is ready and write to MAC table now, self_clear	1'b0

WMAD1: WT_MAC_AD1 (offset: 0x38)

Bits	Type	Name	Description	Initial value
31:16		-	Reserved	16'b0
15:0	R/W	W_MAC_15_0	Write MAC address [15:0]	16'h0

WMAD2: WT_MAC_AD2 (offset: 0x3C)

Bits	Type	Name	Description	Initial value
31:0	R/W	W_MAC_47_16	Write MAC address [47:16]	32'b0

PVIDC0: PVID Configuration 0 (offset: 0x40)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	P1_PVID	Port1 PVID setting	12'd1
11:0	R/W	P0_PVID	Port0 PVID setting	12'd1

PVIDC1: PVID Configuration 1 (offset: 0x44)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	P3_PVID	Port3 PVID setting	12'd1
11:0	R/W	P2_PVID	Port2 PVID setting	12'd1

PVIDC2: PVID Configuration 2 (offset: 0x48)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	P5_PVID	Port5 PVID setting	12'd1
11:0	R/W	P4_PVID	Port4 PVID setting	12'd1

PVIDC3: PVID Configuration 3 (offset: 0x4C)

Bits	Type	Name	Description	Initial value
31:12		-	Reserved	20'd0
11:0	R/W	P6_PVID	Port6 PVID setting	12'd1

VLANO0: VLAN Identifier 0 (offset: 0x50)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	VID1	VLAN field Identifier for VLAN 1	12'd2
11:0	R/W	VID0	VLAN field Identifier for VLAN 0	12'd1

VLANI1: VLAN Identifier 1 (offset: 0x54)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	VID3	VLAN field Identifier for VLAN 3	12'd4
11:0	R/W	VID2	VLAN field Identifier for VLAN 2	12'd3

VLANI2: VLAN Identifier 2 (offset: 0x58)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	VID5	VLAN field Identifier for VLAN 5	12'd6
11:0	R/W	VID4	VLAN field Identifier for VLAN 4	12'd5

VLANI3: VLAN Identifier 3 (offset: 0x5C)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	VID7	VLAN field Identifier for VLAN 7	12'd8
11:0	R/W	VID6	VLAN field Identifier for VLAN 6	12'd7

VLANI4: VLAN Identifier 4 (offset: 0x60)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	VID9	VLAN field Identifier for VLAN 9	12'd10
11:0	R/W	VID8	VLAN field Identifier for VLAN 8	12'd9

VLANI5: VLAN Identifier 5 (offset: 0x64)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	VID11	VLAN field Identifier for VLAN 11	12'd12
11:0	R/W	VID10	VLAN field Identifier for VLAN 10	12'd11

VLANI6: VLAN Identifier 6 (offset: 0x68)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	vid13	VLAN field Identifier for VLAN 13	12'd14
11:0	R/W	vid12	VLAN field Identifier for VLAN 12	12'd13

VLANI7: VLAN Identifier 7 (offset: 0x6C)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'd0
23:12	R/W	VID15	VLAN Identifier for VLAN 15	12'd16
11:0	R/W	VID14	VLAN Identifier for VLAN 14	12'd15

VMSC0: VLAN Member Port Configuration 0 (offset: 0x70)

Bits	Type	Name	Description	Initial value
30:24	R/W	VLAN_MEMSET_3	VLAN 3 member port	8'hff
22:16	R/W	VLAN_MEMSET_2	VLAN 2 member port	8'hff
15:8	R/W	VLAN_MEMSET_1	VLAN 1 member port	8'hff
7:0	R/W	VLAN_MEMSET_0	VLAN 0 member port	8'hff

VMSC1: VLAN Member Port Configuration 1 (offset: 0x74)

Bits	Type	Name	Description	Initial value
30:24	R/W	VLAN_MEMSET_7	VLAN 7 member port	8'hff
22:16	R/W	VLAN_MEMSET_6	VLAN 6 member port	8'hff
15:8	R/W	VLAN_MEMSET_5	VLAN 5 member port	8'hff
7:0	R/W	VLAN_MEMSET_4	VLAN 4 member port	8'hff

VMSC2: VLAN Member Port Configuration 2 (offset: 0x78)

Bits	Type	Name	Description	Initial value
30:24	R/W	VLAN_MEMSET_11	VLAN 11 member port	8'hff

22:16	R/W	VLAN_MEMSET_10	VLAN 10 member port	8'hff
15:8	R/W	VLAN_MEMSET_9	VLAN 9 member port	8'hff
7:0	R/W	VLAN_MEMSET_8	VLAN 8 member port	8'hff

VMSC3: VLAN Member Port Configuration 3 (offset: 0x7C)

Bits	Type	Name	Description	Initial value
30:24	R/W	VLAN_MEMSET_15	VLAN 15 member port	8'hff
22:16	R/W	VLAN_MEMSET_14	VLAN 14 member port	8'hff
15:8	R/W	VLAN_MEMSET_13	VLAN 13 member port	8'hff
7:0	R/W	VLAN_MEMSET_12	VLAN 12 member port	8'hff

POA: Port Ability (offset: 0x80)

Bits	Type	Name	Description	Initial value
31	RO	G1_LINK	Port 6 Link Status 1: Link up 0: Link down	1'b0
30	RO	G0_LINK	Port 5 Link Status 1: Link up 0: Link down	1'b0
29:25	RO	LINK	Port 4 ~ port 0 Link Status 1: Link up 0: Link down	5'b0
24:23	RO	G1_XFC	Flow Control Status of Port 6 The flow control capability status bit after Auto-negotiation force mode. 1xb: full duplex and tx flow control ON x1b: full duplex and rx flow control ON 00b: flow control off	2'b0
22:21	RO	G0_XFC	Flow Control Status of Port 5 The flow control capability status bit after Auto-negotiation force mode. 1xb: full duplex and tx flow control ON x1b: full duplex and rx flow control ON 00b: flow control off	2'b0
20:16	RO	XFC	Flow Control Status of port 0 ~ 4 The flow control capability status bit after Auto-negotiation force mode. 0: flow control off 1 : full duplex and 802.3x flow control ON (after AN or forced)	5'b0
15:9	RO	DUPLEX	Port6 ~ port0 Duplex Mode 0: half duplex 1: full duplex	7'h0
8:7	RO	G1_SPD	MII port 6 Speed Mode 10: 1GHz, 01: 100M, 00: 10M	2'b0
6:5	RO	G0_SPD	MII port 5 Speed:Mode 10: 1GHz, 01: 100M, 00: 10M	2'b0
4:0	RO	SPEED	Port4 ~ port0 Speed Mode 0 : 10M 1 : 100M	5'b0

FPA: Force Port4 ~ Port0 Ability (offset: 0x84)

Bits	Type	Name	Description	Initial value
31:27	R/W	FORCE_MODE	Port4 ~ port 0 force mode 0: default 1: force mode. Auto-negotiation status is ignored. All the port ability are forced according to the following fields of the register FPA.	5'd0
26:22	R/W	FORCE_LNK	Port 4 ~ port 0 PHY Link This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 0: link down 1: linkup	5'b0
21	-		Reserved	1'd0
20:16	R/W	FORCE_XFC	Port 4 ~ port 0 Flow control of PHY port This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 0: default OFF 1: 802.3x flow control ON	5'd0
15:13	-		Reserved	3'd0
12:8	R/W	FORCE_DPX	Port4 ~ port0 Duplex, This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 0: half duplex 1: full duplex	5'd0
7:6	-		Reserved	2'd0
5	R/W	XTAL_COMP	Crystal rate compensation 0 : Disable 1 : When the switch has transmitted 20000 bytes, the switch will compensate for the loss of crystal rate.	1'b0
4:0	R/W	FORCE_SPD	Port4 ~ port0 Speed: This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 0: 10M 1: 100M	5'b0

PTS: Port Status (offset: 0x88)

Bits	Type	Name	Description	Initial value
31:10	-		Reserved	22'b0
9	RO	G1_TXC_STATUS	Port 6 TXC status port 6 TXC status, 1= error, no TXC	1'b0
8	RO	G0_TXC_STATUS	Port 5 TXC status port 5 TXC status, 1= error, no TXC	1'b0
7	-		Reserved	1'b0
6:0	RO	SECURED_ST	Security Status 1= has intruder coming if turn on the SA_secured mode, read clear	7'b0

SOCPC: SoC Port Control (offset: 0x8C)

Bits	Type	Name	Description	Initial value
31:26	-		Reserved	6'b0
25	R/W	CRC_PADDING	CRC padding from CPU If this bit is set , all packets from CPU don't need to append CRC and the outgoing LAN/WAN port will calculate and append CRC. 0: packets from CPU need CRC appending 1: packets from CPU without CRC appending	1'b1

24:23	R/W	CPU_SELECTION -	CPU Selection 00b : Port 6 01b : Port 0 10b : Port 4 11b : Port 5	2'b0
22:16	R/W	DISBC2C PU	When this bit = 1, BC frames from the corresponding port will not be forward to CPU. 1'b0 : Includes CPU port. 1'b1 : Excludes CPU port	7'h7f
15	R/W	UNI_FCBP_OPTI ON-	Unicast Frame Flow control/Back pressure option 0 : When all ports are fc/bp disable, the switch will use drop_threshold to drop frames only. If not, the switch will use fc_threshold and drop_threshold. 1 : When only the destination TX port is fc/bp disable, the switch will use drop_threshold to drop frames only . If not, that TX port uses fc_threshold and drop_threshold.	1'b0
14:8	R/W	DISMC2C PU	When this bit =1, MC frames from the corresponding port will not forward to CPU. 1'b0 : Includes CPU port. 1'b1 : Excludes CPU port	7'h7f
7		-	Reserved	1'b0
6:0	R/W	DISUN2C PU	When this bit is =1 , unknown UC frames from the corresponding port will not forwarded to CPU 1'b0 : Includes CPU port. 1'b1 : Excludes CPU port	7'h7f

POC1: Port Control 0 (offset: 0x90)

Bits	Type	Name	Description	Initial value
31:30	R/W	HASH_ADDR_SHIFT	Address table hashing algorithm option for member set index	2'b0
29	R/W	DIS_GMII_PORT_1	Disable port 6 0: port enable 1: port disable	1'b1
28	R/W	DIS_GMII_PORT_0	Disable port 5 0 port enable 1: port disable	1'b1
27:23	R/W	DIS_PORT	Disable phy port 0: port enable 1: port disable	5'h1f
22:16	R/W	DISRMC2 CPU	Unknown Reserved Multicast Frame Excludes CPU 1'b0: Unknown Reserved Multicast Forward Rule (SGC.RMC_RULE) 1'b1: Excludes CPU port	7'h0
15		-	Reserved	1'b0
14:8	R/W	EN_FC	Apply 802.3x status after Auto-negotiation This field can individually control the 802.3x capability after Auto-negotiation is done. 0: ignore the AN stats for 802.3x capability 1: follow the AN status for 802.3x capability	7'h7f

7	R/W	MC_FCBP_OPTION-	Multicast Flow control/Backpressure option 0 : When all ports are fc/bp disable, the switch will use drop_threshold to drop frames only. If not, the switch will use fc_threshold and drop_threshold. 1 : When only the destination TX port is fc/bp disable, switch will use drop_threshold to drop frames only . If that TX port uses fc_threshold and drop_threshold.	1'b0
6:0	R/W	EN_BP	Apply back pressure capability 0: ignore the back pressure mode (default OFF) 1: apply back pressure based on SGC.BP_MODE.	7'h7f

POC1: Port Control 1 (offset: 0x94)

Bits	Type	Name	Description	Initial value
31:23		-	Reserved	9'd0
29:23	R/W	DisIPMC2CPU	Unknown IP Multicast Frame Excludes CPU 1'b0: Unknown IP Multicast Forward Rule (SGC.IP_MULT_RULE) 1'b1: Excludes CPU port	7'h0
22:16	R/W	BLOCKING_STATE	Port State for Spanning Tree Protocol 0 : normal state 1 : blocking state, forwarding rmc packet to cpu(need programming address table)	7'd0
15		-	Reserved	1'd0
14:8	R/W	DIS_LRNING	Disable SA learning 0: default enabled 1: disable Source MAC learning	7'b0
7		-	Reserved	1'd0
6:0	R/W	SA_SECURED_PORT	SA secured mode 0: don't care SA match, 1: the packets' SA needs match, otherwise discard the packets (Note: Must set dis_learn and sa_secured at the same Time).	7'b0

POC2: Port control 2 (offset: 0x98)

Bits	Type	Name	Description	Initial value
31		-	Reserved	1'b0
30	R/W	G1_TXC_CHECK	Check the Port 6 TXC if no txc clock, then disable MII port 1: enable, check TXC	1'b0
29	R/W	G0_TXC_CHECK	Check the port 5 TXC if no txc clock, then disable MII port 1: enable, check TXC	1'b0
28:26		-	Reserved	3'b0
25	R/W	MLD2CPU_EN	MLD Message Packets forward to CPU 1'b0 : MLD message will be flooded to all ports 1'b1 : MLD message will be forwarded to CPU port only.	1'b0
24:23	R/W	IPV6_MULT_RULE	Unknown IPV6 Multicast Frame Forward Rule If no match in the address table, then following the rule 00: BC 01: to cpu 10: drop 11: Reserved	2'b0

22:16	R/W	DIS_UC_PAUSE	Disable Unicast Pause Frame 0: switch will consider pause frame when DA!=0180c20001 but unicast to CPU, 1: switch will not consider pause frame when DA!=0180c20001 and unicast to CPU	7'b0
15	R/W	PER_VLAN_UNTAG_EN	Per port per vlan untag enable VLAN tag removal option. 0 : Use per port UNTAG_EN 1 : Use untag enable bitmap in VLAN table	1'b0
14:8	R/W	ENAGING_PORT	Port aging 0: disable aging that the MAC address is belong to programmed port(s) 1: enable aging	7'h7f
7		-	Reserved	-
6:0	R/W	UNTAG_EN	Per Port VLAN Tag Removal 0: disable 1: enable VLAN tag field removal.	7'h0

SGC: Switch Global Control (offset: 0x9C)

Bits	Type	Name	Description	Initial value
31		-	Reserved	1'b0
30	R/W	BKOFF_ALG	Backoff Algorithm Option 0: default 1: comply with UNH test	1'b1
29	R/W	LEN_ERR_CHK	Length of Received Frame Check Enable When the bit is set, the received packet length will be checked for length encapsulated frames. 0: default disabled 1: comply with UNH test	1'b1
28:27	R/W	IP_MULT_RULE	Unknown IP Multicase Frame Forward Rule If no match in the address table, then following the rules, 00: BC 01: to cpu 10: drop 11: reserved	2'b0
26:25	R/W	RMC_RULE	Unknown Reserved Multicast Frame Forward Rule If no match in the address table, then follow the rules, 00: to all port(not include blocking state port) 01: to cpu 10: drop 11: reserved	2'b0
24:23	R/W	LED_FLASH_TIME	The Frequency Of LED Flash 00: 30ms 01: 60ms 10: 240ms 11: 480ms	2'b0
22:21	R/W	BISH_TH	The Threshold Of Memory Bisshop 11:skip if fail 8 blocks, 0 00:skip if fail 16 (default, from pins) 01:skip if fail 48 10:skip if fail 64	2'b0
20	RO	BISH_DIS	Build In Self Hop 0: enable skip function (default, from pin)	1'b0

19:18	R/W	BP_MODE	Back Pressure Mode 00: disable 01: BP jam, the jam number is set by bp_num 10: BP jamALL, jam packet until the BP condition is released(default), 11: BP carrier, use carrier insertion to do back pressure	2'b10															
17:16	R/W	DISMIIPORT_WASTX	GMII Port Disable Was_Transmit 1: disable was_transmit (good for late CRS PHY, like HPNA2.0 or power-LAN), 0: enable	2'b0															
15:12	R/W	BP_JAM_CNT	Back Pressure Jam Number The consecutive jam count when back pressure is enabled, The default is 10 packet jam then one no-jam packet.	4'b1010															
11	R/W	DISABLE TX BACKOFF	Disable The Collision Back Off Timer 0: default 1: re-transmit immediately after collision,	1'b0															
10:9	R/W	ADDRESS_HASH_ALG	MAC Address Hashing Algorithm 00: direct mode, using last 10-bit as hashing address 01: XOR48 mode 10: XOR32 mode 11:reserved	2'b0															
8	R/W	DIS_PKT_TX_ABORT	Disable Packet TX Abort 1: Disable collision 16 packet abort and late collision abort 0: enable both abort	1'b0															
7:6	R/W	PKT_MAX_LEN	Maximum Packet Length <table border="1"> <tr> <th></th> <th>Untagged</th> <th>VLAN-taged</th> </tr> <tr> <td>00b</td> <td>1536 Bytes</td> <td>1536 Bytes</td> </tr> <tr> <td>01b</td> <td>1518 Bytes</td> <td>1522 Bytes</td> </tr> <tr> <td>10b</td> <td>1522 Bytes</td> <td>1526 Bytes</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td>Reserved</td> </tr> </table>		Untagged	VLAN-taged	00b	1536 Bytes	1536 Bytes	01b	1518 Bytes	1522 Bytes	10b	1522 Bytes	1526 Bytes	11b	Reserved	Reserved	2'b01
	Untagged	VLAN-taged																	
00b	1536 Bytes	1536 Bytes																	
01b	1518 Bytes	1522 Bytes																	
10b	1522 Bytes	1526 Bytes																	
11b	Reserved	Reserved																	
5:4	R/W	BC_STORM_PROT	Global Broadcast Storm Protection BC will be blocked, if the following number of BC blocks in output queues <u>00: disable</u> 01: 64 10: 96 11: 128	2'b0															
3:0	R/W	AGING INTERVAL	Aging Timer 0000: disable age <u>0001: 300sec</u> 0010 ~ 0111: 600 ~ 38400sec 1xxx: Fast Age (60sec)	4'd1															

STRT: Switch Reset (offset: 0xA0)

Bits	Type	Name	Description	Initial value
31:0	WO	Reset_SW	Reset switch engine, data, address, link memory , cpu port and ahb interface when writing data to the STRT register.	32'b0

LEDP0: LED Port0 (offset: 0xA4)

Bits	Type	Name	Description	Initial value
31:4	-		Reserved	28'd0
3:0	RW	P0_LED	port0 LED state, default = link/activity 4'b0000: link	4'b0101

		4'b0001: 100M speed 4'b0010: duplex 4'b0011: activity 4'b0100: collision 4'b0101: link/activity 4'b0110: duplex/collision 4'b0111: 10M speed/activity 4'b1000: 100M speed/activity 4'b1011: off 4'b1100: on 4'b1010: blink	
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LEDP1: LED Port 1 (offset: 0xA8)

Bits	Type	Name	Description	Initial value
31:4		-	Reserved	28'b0
3:0	RW	P1_LED	Port1 LED state, default = link/activity	4'b0101

LEDP2: LED Port2 (offset: 0xAC)

Bits	Type	Name	Description	Initial value
31:4		-	Reserved	28'b0
3:0	RW	P2_LED	Port2 LED state, default = link/activity	4'b0101

LEDP3: LED Port3 (offset: 0xB0)

Bits	Type	Name	Description	Initial value
31:4		-	Reserved	28'b0
3:0	RW	P3_LED	Port3 LED state, default = link/activity	4'b0101

LEDP4: LED Port4 (offset: 0xB4)

Bits	Type	Name	Description	Initial value
31:4		-	Reserved	28'b0
3:0	RW	P4_LED	Port4 LED state, default = link/activity	4'b0101

WDTR: Watch Dog trigger Reset (offset: 0xB8)

Bits	Type	Name	Description	Initial value
31:8		-	Reserved	24'b0
7:0	RW	BUF_STARV_TH	Buffer starvation threshold Switch will interrupt CPU when the global queue block counts is less than the threshold for 3 seconds.	8'd30

DES: Debug Signal (offset: 0xBC)

Bits	Type	Name	Description	Initial value
31:16		-	Reserved	16'b0
15:0	RO	DEBUG_SIGNAL	Port 5 debug signal	16'b0

PCR0: PHY Control Register 0 (offset: 0xC0)

Bits	Type	Name	Description	Initial value
31:16	RW	WT_NWAY_DATA	The data be written into the PHY	17'b0
15		-	Reserved	1'b0
14	RW	RD_PHY_CMD	Read command To enable read command on PHY, write 1 to this bit . After command is completed, this bit is self-cleared.	1'b0
13	RW	WT_PHY_CMD	Write command To enable write command on PHY, write 1 to this bit . After command is completed, this bit is self-cleared	1'b0
12:8	RW	CPU_PHY_REG_ADDR	PHY register address	5'b0
7:5		-	Reserved	3'b0
4:0	RW	CPU_PHY_ADDR	PHY address (Note: The internal 5-ports PHY reserves the PHY address)	5'b0

			starting from 5'd0 ~ 5'd4. For the external PHY, the PHY address from 5'd5 to 5'd31 can be applied. The default PHY address of Port 5 is 5'd5 for auto-polling function.)	
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PCR1: PHY control register 1 (offset: 0xC4)

Bits	Type	Name	Description	Initial value
31:16	RO	RD_DATA	The Read Data	15'b0
15:2	-	Reserved		14'b0
1	RO	RD_RDY	Read operation isdone, read clear	1'0
0	RO	WT_DONE	Write operation is done, read clear	1'b0

FPA1 : Force Port 5 ~Port 6 ability (offset:0xC8)

Bits	Type	Name	Description	Initial value
31:30	-	Reserved		2'b0
29	R/W	AP_EN	Port 5 Auto polling enable	1'b0
28:24	R/W	EXT_PHY_ADDR_BASE	Port 5 External phy base address	5'd5
23:22	R/W	G0_RXCLK_SKEW_SEL	Port 5 rxclock skew selection	2'b01
21:20	R/W	G0_TXCLK_MODE_SEL	Port 5 txclock skew selection	2'b01
19	-	Reserved		1'b0
18	R/W	TURBO_MII_CLK	Port 5 revMII mode clock selection 0 : 25MHz output clock 1 : 31.25MHz output clock	1'b0
17:14	-	Reserved		4'b0
13	R/W	FORCE_RGMII_LINK1	Force port 6 link This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 0: link down 1: link up	1'b0
12	R/W	FORCE_RGMII_LINK0	Force port 5 link This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 0: link down 1: link up	1'b0
11	R/W	FORCE_RGMII_EN1	Force port 6 enable 0: reserved 1: force mode. Auto-negotiation status is ignored. Port ability is forced according to the following fields of register FPA1.	1'b0
10	R/W	FORCE_RGMII_EN0	Force port 5 enable 0: default 1: force mode. Auto-negotiation status is ignored. Port 5 ability is forced according to the following fields of the register FPA1.	1'b0
9:8	R/W	FORCE_RGMII_XFC1	Force port 6 flow control ability This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 1x: for tx x1: for rx	2'b11
7:6	R/W	FORCE_RGMII_XFC0	Force port 5 flow control ability This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 1x: for tx x1: for rx	2'b00
5	R/W	FORCE_RGMII_DPX1	Force port 6 duplex	1'b1

			This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 0: half duplex 1: full duplex	
4	R/W	FORCE_RGMII_DPX0	Force port 5 duplex This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 0: half duplex 1: full duplex	1'b0
3:2	R/W	FORCE_RGMII_SPD1	Force port 6 speed This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 1x: 1GMhz 01: 100MHz 00: 10MHz	2'b10
1:0	R/W	FORCE_RGMII_SPD0	Force port 5 speed This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register. 1x: 1GMhz 01: 100MHz 00: 10MHz	2'b01

FCT2: Flow Control Threshold 2 (offset: 0xCC)

Bits	Type	Name	Description	Initial value
31:25		-	Reserved	14'd0
24:18	R/W	DIS_IPV6MC2CPU	Unknown IPv6 Multicast Frame Excludes CPU 1'b0: Unknown IPv6 Multicast Forward Rule (POC2.IPV6_MULT_RULE) 1'b1: Excludes CPU port	7'b0
17:13	R/W	MUST_DROP_RLS_TH	If the global queue pointer higher than the threshold. The must drop condition will be released.	5'd5
12:8	R/W	MUST_DROP_SET_TH	If the global queue pointer reach must drop. All incoming packets have to be dropped.	5'd3
7:6		-	Reserved	2'b0
5:0	R/W	MC_PER_PORT_TH	MC packets per port threshold. When the global queue reaches the flow control threshold on register FCT0, per port output threshold for MC packet will be checked to enable flow-control or packet-dop on incoming MC packet.	6'd12

QSS0: Queue_Status_0 (offset: 0x D0)

Bits	Type	Name	Description	Initial value
31:24		-	Reserved	8'b0
23:15	RO	BE_CNT_R	Link control best effort queue block counter monitor	9'b0
14:5	RO	BK_CNT_R	Link control background queue block counter monitor	10'b0

QSS1: Queue_Status_1 (offset: 0x D4)

Bits	Type	Name	Description	Initial value
31:18		-	Reserved	14'b0
17:9	RO	VO_CNT_R	Link control voice queue block counter monitor	9'b0
8:0	RO	CL_CNT_R	Link control control load queue block counter monitor	9'b0

DEC: Debug Control (offset: 0x D8)

Bits	Type	Name	Description	Initial value
31:24	R/W	SW2FE_BRIDGE_IPG	SW2FE Bridge IPG Byte Count Inter-Frame Byte Count between the consecutive frames flowing from Switch to Frame Engine	8'd64
23:16	R/W	FE2SW_BRIDGE_IPG	FE2SW Bridge IPG byte count Inter-Frame Byte Count between the consecutive frames flowing from Frame Engine to Switch	8'd64
15:9		-	Reserved	7'd0
8	R/W	BRIDGE_EN	Enable FE2SW Bridge IPG Prevention 1'b0: Disable 1'b1: Enable IPG Prevention when FE2SW_BRIDGE_IPG is too short (8'd16) to receive the next frame.	1'b1
7:6		-	Reserved	2'd0
5:3	R/W	DEBUG_SW_PORT_SEL	Port 5 debug selection control	3'b0
2:0		-	Reserved	3'd0

MTI: Memory Test Information (offset: 0xDC)

Bits	Type	Name	Description	Initial value
31:16		-	Reserved	16'b0
15:7	RO	SKIP_BLOCKS	Skip block counter This field indicates how many blocks are skipped due to memory bit fault.	9'bx
6	RO	SW_MEM_TEST_DONE	Switch memory test done	1'bx
5	RO	LK_RAM_TEST_DONE	Link ram test done	1'bx
4	RO	LK_RAM_TEST_FAIL	Link ram test fail	1'bx
3	RO	AT_RAM_TEST_DONE	Address table ram test done	1'bx
2	RO	AT_RAM_TEST_FAIL	Address table ram test fail	1'bx
1	RO	DT_RAM_TEST_DONE	Data buffer ram test done	1'bx
0	RO	DT_RAM_TEST_FAIL	Data buffer ram test fail	1'bx

PPC: Port 6 Packet Counter (offset: 0xE0)

Bits	Type	Name	Description	Initial value
31:16	RO	SW2FE_CNT	Switch to frame engine packet counter	16'b0
15:0	RO	FE2SW_CNT	Frame engine to switch packet counter	16'b0

SGC2: Switch Global Control 2 (offset: 0xE4)

Bits	Type	Name	Description	Initial value
31	R/W	P6_RXFC_QUE_EN	Port 6 RX flow control by Frame Engine 4 Queues 0: Port 6 RX flow control is decided by any queue congestion of the Frame Engine 1: Port 6 RX flow control is decided by 4 queues of the Frame Engine congestion independently.	1'b0
30	R/W	P6_TXFC_WL_EN	Port 6 TX flow control by Switch WAN/LAN port 0: Port 6 TX flow control is decided by any port of the Switch congestion 1: Port 6 TX flow control is decided by WAN/LAN port of the Switch congestion independently	1'b0

29:24	R/W	LAN_PMAP	Lan port bit map This field indicates per port attribute used for flow control. 1: Lan port 0: Wan port	6'b0
23	R/W	SPECIAL_TAG_EN	Special Tag enable 0 : default RX special tag is enabled according to the global control bit- CPU_TPID_EN TX special tag is enabled according to the per-port TX_CPU_TPID_BIT_MAP 1 : CPU_TPID_EN is not used Both TX and RX special tag feature are decided by the per-port TX_CPU_TPID_BIT_MAP	1'b0
22:16	R/W	TX_CPU_TPID_BIT_MAP	Transmit CPU TPID(810x) port bit map 0: default (TPID=0x8100) 1: TPID=0x810? depending on TX/RX usages	7'b0
15:13		-	Reserved	3'b0
12	R/W	P6_PER_QUEUE_FC	Port 6 per queue TX flow control This bit is only valid when P6_TXFC_WL_EN is enabled. 0 : 4 Queues Flow control of the Frame Engine is decided by the Switch WAN/LAN all queue full conditions 1 : 4 Queues Flow control of the Frame Engine is decided by the Switch WAN/LAN per queue full condition	1'b0
11	R/W	ARBITER_LAN_EN	Memory arbiter only for P0~P4 enable 0: default 1: memory arbiter only for P0~P4.	1'b0
10	R/W	CPU_TPID_EN	CPU TPID(81xx) enable 0: disable. CPU TPID=8100 1: enable. CPU TPID=810x.	1'b0
9	R/W	ARBITER_GPT_EN	Memory Arbiter only for P5 and P6	1'b0
8	R/W	SLOT_4TO1	Memory Arbitter Ratio Selection 0: (P5,P6) : (P0-P4) = 3:2 1: (P5,P6) : (P0-P4) = 4:1	1'b0
7		-	Reserved	3'b0
6:0	R/W	DOUBLE_TAG_EN	Insert double tag field When this bit is set , the incoming packet is allowed to insert outer or double tag. 1: enable double tag field 0: disable the double tag field.	7'b0

POPC: Port 0 Packet Counter (offset: 0xE8)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT0	Port 0 receive bad packet counter	16'b0
15:0	RO	GOOD_PKT_CNT0	Port 0 receive good packet counter	16'b0

P1PC: Port 1 Packet Counter (offset: 0xEC)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT1	Port 1 receive bad packet counter	16'b0
15:0	RO	GOOD_PKT_CNT1	Port 1 receive good packet counter	16'b0

P2PC: Port 2 Packet Counter (offset: 0xF0)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT2	Port 2 receive bad packet counter	16'b0
15:0	RO	GOOD_PKT_CNT2	Port 2 receive good packet counter	16'b0

P3PC: Port 3 Packet Counter (offset: 0xF4)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT3	Port 3 receive bad packet counter	16'b0
15:0	RO	GOOD_PKT_CNT3	Port 3 receive good packet counter	16'b0

P4PC: Port 4 packet counter (offset: 0xF8)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT4	Port 4 receive bad packet counter	16'b0
15:0	RO	GOOD_PKT_CNT4	Port 4 receive good packet counter	16'b0

P5PC: Port 5 packet counter (offset: 0xFC)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT5	Port 5 receive bad packet counter	16'b0
15:0	RO	GOOD_PKT_CNT5	Port 5 receive good packet counter	16'b0

VUB0: VLAN Untag Block 0 (offset: 0x100)

Bits	Type	Name	Description	Initial value
31:28			Reserved	4'd0
27:21	R/W	VLAN_3_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 3	7'd0
20:14	R/W	VLAN_2_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 2	7'd0
13:7	R/W	VLAN_1_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 1	7'd0
6:0	R/W	VLAN_0_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 0	7'd0

VUB0: VLAN Untag Block 1 (offset: 0x104)

Bits	Type	Name	Description	Initial value
31:28			Reserved	4'd0
27:21	R/W	VLAN_7_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 7	7'd0
20:14	R/W	VLAN_6_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 6	7'd0
13:7	R/W	VLAN_5_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 5	7'd0
6:0	R/W	VLAN_4_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 4	7'd0

VUB0: VLAN Untag Block 2 (offset: 0x108)

Bits	Type	Name	Description	Initial value
31:28			Reserved	4'd0
27:21	R/W	VLAN_11_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 11	7'd0
20:14	R/W	VLAN_10_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 10	7'd0
13:7	R/W	VLAN_9_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 9	7'd0
6:0	R/W	VLAN_8_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 8	7'd0

VUB0: VLAN Untag Block 3 (offset: 0x10C)

Bits	Type	Name	Description	Initial value
31:28			Reserved	4'd0
27:21	R/W	VLAN_15_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 15	7'd0

20:14	R/W	VLAN_14_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 14	7'd0
13:7	R/W	VLAN_13_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 13	7'd0
6:0	R/W	VLAN_12_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 12	7'd0

BMU_CTRL: Broadcast/Multicast/Unknown Rate Limit Control (offset: 0x110)

Bits	Type	Name	Description	Initial value
31			Reserved	1'b0
30:24	R/W	ONE_US_CYCLE_NUM	One micro-second cycle number This field is used to calculate 1us period.	7'd124
23			Reserved	1'd0
22:20	R/W	P5_RATE_LIMIT_CTRL	Port 5 rate limit control	3'd0
19			Reserved	1'd0
18:16	R/W	P4_RATE_LIMIT_CTRL	Port 4 rate limit control	3'd0
15			Reserved	1'd0
14:12	R/W	P3_RATE_LIMIT_CTRL	Port 3 rate limit control	3'd0
11			Reserved	1'd0
10:8	R/W	P2_RATE_LIMIT_CTRL	Port 2 rate limit control	3'd0
7			Reserved	1'd0
6:4	R/W	P1_RATE_LIMIT_CTRL	Port 1 rate limit control	3'd0
3			Reserved	1'd0
2:0	R/W	P0_RATE_LIMIT_CTRL	Port 0 rate limit control [2] : Broadcast frame enable [1] : Multicast frame enable [0] : Unknown frame enable	3'd0

BMU_LMT_NUM_1: Broadcast/Multicast/Unknown Rate Limit Frame Number 1 (offset: 0x114)

Bits	Type	Name	Description	Initial value
31:16	R/W	RATE_LIMIT_NUM_BER_100M	Rate Limit received Broadcast / Multicast / Unknown frame number in 100M in 100 ms duration	16'hFFFF
15:0	R/W	RATE_LIMIT_NUM_BER_10M	Rate Limit received Broadcast / Multicast / Unknown frame number in 10M in 1 sec duration.	16'hFFFF

RL_NUM_10M: Rate Limit Frame Number 2 (offset: 0x118)

Bits	Type	Name	Description	Initial value
31	R/W	INGRESS_RATE_BY_TE_OPTION	Ingress Rate Byte Option 0 : Add 1 : Minus	1'd0
30:24	R/W	INGRESS_RATE_BY_TE_NUM	Ingress Rate Byte number	7'h18
23	-	RES	Reserved	1'd0
22:16	-	RES	Reserved	7'h18
15:0	-	RES	Reserved	16'hFFFF

P01_ING_CTRL: Port 0 & 1 Ingress Rate Limit Control(offset: 0x11C)

Bits	Type	Name	Description	Initial value
31			Reserved	1d0

30	R/W	P1_INGRESS_Ctrl	P1 Ingress Limit Control 1:ON 0:OFF	1'd0
29	R/W	P1_MNG_PKT_BY_PASS	P1 Management Packet Bypass Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set. (Only bypass BPDU, IGMP & MLD packets) 0: all packet included 1: Management Frame excluded	1'd0
28	R/W	P1_INGRESS_FLOW_CTRL_ON	Port 1 Ingress rate flow control When the bit is set, the pause frame is used prior to packet dropped according to P1_ING_THRES. If the bucket is empty, then P1 will start to discard the received packets except those specific packet in P1_MNG_PKY_BYPASS mode. 0: OFF 1: ON	1'b0
27:26	R/W	P1_TIMER_TICK	Port 1 Timer Tick 0 : 512 us 1 : 128 us 2 : 32 us 3 : 8 us	2'd0
25:16	R/W	P1_TOKEN	Port 1 Token Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte) The maximum space of this bucket is 16'hFFFF bytes	10'd0
15			Reserved	1'd0
14	R/W	P0_INGRESS_CTRL	P0 Ingress Limit Control 1:ON 0:OFF	1'd0
13	R/W	P0_MNG_PKT_BY_PASS	P0 Management Packet Bypass Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set. (Only bypass BPDU, IGMP & MLD packets) 0: all packet included 1: Management Frame excluded	1'd0
12	R/W	P0_INGRESS_FLOW_CTRL_ON	Port 0 Ingress rate flow control When the bit is set, the pause frame is used prior to packet dropped according to P0_ING_THRES. If the bucket is empty, then P0 will start to discard the received packets except those specific packet in P0_MNG_PKY_BYPASS mode. 0: OFF 1: ON	1'b0
11:10	R/W	P0_TIMER_TICK	Port 0 Timer Tick 0 : 512 us 1 : 128 us 2 : 32 us 3 : 8 us	2'd0
9:0	R/W	P0_TOKEN	Port 0 Token Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte) The maximum space of the bucket is 16'hFFFF bytes.	10'd0

P23_ING_CTRL: Port 2 & 3 Ingress Rate Limit Control(offset: 0x120)

Bits	Type	Name	Description	Initial value
31			Reserved	1'd0
30	R/W	P3_INGRESS_CTRL	P3 Ingress Limit Control 1:ON 0:OFF	1'd0
29	R/W	P3_MNG_PKT_BY_PASS	P3 Management Packet Bypass Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set. (Only bypass BPDU, IGMP & MLD packets) 0: all packet included 1: Management Frame excluded	1'd0
28	R/W	P3_INGRESS_FLOW_CTRL_ON	Port 3 Ingress rate flow control When the bit is set, the pause frame is used prior to packet dropped according to P3_ING_THRES. If the bucket is empty, then P3 will start to discard the received packets except those specific packet in P3_MNG_PKY_BYPASS mode. 0: OFF 1: ON	1'b0
27:26	R/W	P3_TIMER_TICK	Port 3 Timer Tick 0 : 512 us 1 : 128 us 2 : 32 us 3 : 8 us	2'd0
25:16	R/W	P3_TOKEN	Port 3 Token Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte) The maximum space of this bucket is 16'hFFFF bytes	10'd0
15			Reserved	1'd0
14	R/W	P2_INGRESS_CTRL	P2 Ingress Limit Control 1:ON 0:OFF	1'd0
13	R/W	P2_MNG_PKT_BY_PASS	P2 Management Packet Bypass Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set. (Only bypass BPDU, IGMP & MLD packets) 0: all packet included 1: Management Frame excluded	1'd0
12	R/W	P2_INGRESS_FLOW_CTRL_ON	Port 2 Ingress rate flow control When the bit is set, the pause frame is used prior to packet dropped according to P2_ING_THRES. If the bucket is empty, then P2 will start to discard the received packets except those specific packet in P2_MNG_PKY_BYPASS mode. 0: OFF 1: ON	1'b0
11:10	R/W	P2_TIMER_TICK	Port 2 Timer Tick 0 : 512 us 1 : 128 us 2 : 32 us 3 : 8 us	2'd0

9:0	R/W	P2_TOKEN	Port 2 Token Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte) The maximum space of this bucket is 16'hFFFF bytes	10'd0
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P45_ING_CTRL: Port 4 & 5 Ingress Rate Limit Control(offset: 0x124)

Bits	Type	Name	Description	Initial value
31:			Reserved	1'd0
30	R/W	P5_INGRESS_CTRL	P5 Ingress Limit Control 1:ON 0:OFF	1'd0
29	R/W	P5_MNG_PKT_BY_PASS	P5_Management Packet Bypass Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set. (Only bypass BPDU, IGMP & MLD packets) 0: all packet included 1: Management Frame excluded	1'd0
28	R/W	P5_INGRESS_FLOW_CTRL_ON	Port 5 Ingress rate flow control When the bit is set, the pause frame is used prior to packet dropped according to P5_ING_THRES. If the bucket is empty, then P5 will start to discard the received packets except those specific packet in P5_MNG_PKY_BYPASS mode. 0: OFF 1: ON	1'b0
27:26	R/W	P5_TIMER_TICK	Port 5 Timer Tick 0 : 512 us 1 : 128 us 2 : 32 us 3 : 8 us	2'd0
25:16	R/W	P5_TOKEN	Port 5 Token Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte) The maximum space of this bucket is 16'hFFFF bytes	10'd0
15			Reserved	1'd0
14	R/W	P4_INGRESS_CTRL	P4 Ingress Limit Control 1:ON 0:OFF	1'd0
13	R/W	P4_MNG_PKT_BY_PASS	P4 Management Packet Bypass Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set. (Only bypass BPDU, IGMP & MLD packets) 0: all packet included 1: Management Frame excluded etc	1'd0
12	R/W	P4_INGRESS_FLOW_CTRL_ON	Port 4 Ingress rate flow control When the bit is set, the pause frame is used prior to packet dropped according to P4_ING_THRES. If the bucket is empty, then P4 will start to discard the received packets except those specific packet in P4_MNG_PKY_BYPASS mode. 0: OFF 1: ON	1'b0

11:10	R/W	P4_TIMER_TICK	Port 4 Timer Tick 0 : 512 us 1 : 128 us 2 : 32 us 3 : 8 us	2'd0
9:0	R/W	P4_TOKEN	Port 4 Token Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte) The maximum space of this bucket is 16'hFFFF bytes	10'd0

P0_ING_THRES: Port 0 Ingress Rate Limit Threshold(offset: 0x128)

Bits	Type	Name	Description	Initial value
31:16	R/W	P0_IN_FC_OFF_THRESHOLD	Port 0 ingress rate limit flow control off. If P0_INGRESS_FLOW_CTRL_ON = 1 and P0 Flow control capability is on (XFC status in 0x80), then P0 will initiate PAUSE OFF frame or stop backpressure.	16'dAAAAA
15:0	R/W	P0_IN_FCON_THRESH	Port 0 ingress rate limit flow control on. If P0_INGRESS_FLOW_CTRL_ON = 1 and P0 Flow control capability is on (XFC status in 0x80), then P0 will initiate PAUSE ON frame or backpressure.	16'd5555

P1_ING_THRES: Port 1 Ingress Rate Limit Threshold(offset: 0x12C)

Bits	Type	Name	Description	Initial value
31:16	R/W	P1_IN_FC_OFF_THRESHOLD	Port 1 ingress rate limit flow control off.	16'dAAAAA
15:0	R/W	P1_IN_FCON_THRESH	Port 1 ingress rate limit flow control on.	16'd5555

P2_ING_THRES: Port 2 Ingress Rate Limit Threshold(offset: 0x130)

Bits	Type	Name	Description	Initial value
31:16	R/W	P2_IN_FC_OFF_THRESHOLD	Port 2 ingress rate limit flow control off.	16'dAAAAA
15:0	R/W	P2_IN_FCON_THRESH	Port 2 ingress rate limit flow control on.	16'd5555

P3_ING_THRES: Port 3 Ingress Rate Limit Threshold(offset: 0x134)

Bits	Type	Name	Description	Initial value
31:16	R/W	P3_IN_FC_OFF_THRESHOLD	Port 3 ingress rate limit flow control off.	16'dAAAAA
15:0	R/W	P3_IN_FCON_THRESH	Port 3 ingress rate limit flow control on.	16'd5555

P4_ING_THRES: Port 4 Ingress Rate Limit Threshold(offset: 0x138)

Bits	Type	Name	Description	Initial value
31:16	R/W	P4_IN_FC_OFF_THRESHOLD	Port 4 ingress rate limit flow control off.	16'dAAAAA
15:0	R/W	P4_IN_FCON_THRESH	Port 4 ingress rate limit flow control on.	16'd5555

P5_ING_THRES: Port 5 Ingress Rate Limit Threshold(offset: 0x13C)

Bits	Type	Name	Description	Initial value
31:16	R/W	P5_IN_FC_OFF_THRESHOLD	Port 5 ingress rate limit flow control off.	16'hAAAAA
15:0	R/W	P5_IN_FCON_THRESH	Port 5 ingress rate limit flow control on.	16'h5555

3.11.5 MII control register

These registers could be accessed by PCR0 (PHY Control Register 0) and PCR1 indirectly.

Among them, PHY reg0~1 and 4~6 are unique for each port. PHY reg2~3 are common for all 5 ports.

Legend:

SC: Self-clearing, RC: Read-clearing

LL: Latching Low, LH: Latching High

R/W: Read/write, RO: Read-Only

CR Address:00(d00) Reset State:3100

Bit	Read/Write	Name	Description	Default
15	R/ W; SC	MR_MAIN_RESET	1=Reset: 0=Normal, reset all digital logic, except phy_reg	1'h0
14	R/W	LOOPBACK_MII	Mii loop back	1'h0
13	R/W	FORCE_SPEED	1 = 100Mbps: 0=10Mbps, when mr_autoneg_enable = 1'b0	1'h1
12	R/W	MR_AUTONEG_ENABLE	1= Enabled: 0=Normal	1'h1
11	R/W	POWERDOWN	phy into power down (power down analog TX analog RX, analog AD)	1'h0
10		-	Reserved	1'h0
9	R/W; SC	MR_RESTART_NEGOTIATION	1 = Restart Auto-Negotiation: 0 = Normal	1'h0
8	R/W	FORCE_DUPLEX	1 = Full Duplex: 0 = Half Duplex, when mr_autoneg_enable = 1'b0	1'h1
7:0		-	Reserved	8h00

MII status register

CR Address:01(d01) Reset State: 7849

Bit	Read/Write	Name	Description	Default
15		100 BASE T4	Not supported	1'h0
14	RO	100BASE-X Full Duplex	1 = PHY is 100BASE-X full duplex capable 0 = PHY is not 100BASE-X full duplex capable	1'h1
13	RO	100BASE-X Half Duplex	1 = PHY is 100BASE-X half duplex capable 0 = PHY is not 100BASE-X half duplex capable	1'h1
12	RO	10Mbps/s Full Duplex	1 = PHY is 10Mbps/s Full duplex capable 0 = PHY is not 10Mbps/s Full duplex capable	1'h1
11	RO	10 Mb/s Half Duplex	1 = PHY is 10Mbps/s Half duplex capable 0 = PHY is not 10Mbps/s Half duplex capable	1'h1
10		100BASE-T2 full duplex	Not supported	1'h0
9		100BASE-T2 half duplex	Not supported	1'h0
8:7		-	Reserved	2'h0
6	RO	MF Preamble Suppression	1 = PHY can accept management frames with preamble suppression 0 = PHY cannot accept management frames with	1'h1

			preamble suppression	
5	RO	mr_autoneg_complete	1 = auto-negotiate completed, 0 = auto-negotiate incomplete	1'h0
4		-	Reserved	1'h0
3	RO	Autoneg Ability	1 = PHY can auto-negotiate, 0 = PHY cannot auto-negotiate	1'h1
2	RO/LL	Link Status	1 = link is up, 0 = link is down	1'h0
1	RO/LH; RC	Jabber Detect	1 = jabber condition detected	1'h0
0	RO	Extended Capability	1=extended register capabilities, 0=basic register set capabilities only	1'h1

PHY identifier register

CR Address:02(d02) Reset State: 00c3

Bit	Read/Write	Name	Description	Default
15:0	RO	PHY_ID[31-16]	OUI (bits 3-18). Ralink OUI =000C43	16'h00c3

PHY version register

CR Address:03(d03) Reset State: 0800

Bit	Read/Write	Name	Description	Default
15:10	RO	PHY_ID[15-10]	OUI (bits 19-24)	6'h02
9:4	RO	PHY_ID[9-4]	Manufacturer's Model Number (bits 5-0)	6'h00
3:0	RO	PHY_ID[3-0]	Revision Number (bits3-0); Register 3, bit 0 is LS bit of PHY Identifier	4'h0

Auto-Negotiation advertisement register

CR Address:04(d04) Reset State: 05e1

Bit	Read/Write	Name	Description	Default
15	RO	Next Page Enable	1=Set to use Next Page: 0=Not to use Next Page	1'h0
14		-	Reserved	1'h0
13	R/W	Remote Fault Enable	1 = Auto Negotiation Fault Detected 0 = No Remote Fault	1'h0
12:11	RO	Not Implemented	Technology Ability A7-A6	2'h0
10	R/W	Pause	Technology Ability A5	1'h1
9	RO	Not Implemented	Technology Ability A4	1'h0
8	R/W	100Base-TX Full Duplex Capable	1 = Capable of Full Duplex 0 = Not Capable	1'h1
7	R/W	100 Base-TX Half Duplex Capable	1 = Capable of Half Duplex 0 = Not Capable	1'h1
6	R/W	10 Base-T Full Duplex Capable	1 = Capable of Full Duplex 10BASE-T 0 = Not Capable	1'h1
5	R/W	10 Base-T Half Duplex Capable	1 = Capable of Half Duplex 10BASE-T 0 = Not Capable	1'h1
4:0	R/W	Selector Field	Identifies type of message	5'h01

Auto-Negotiation Link partner (LP) ability register

CR Address:05(d05) Reset State: 0000

Bit	Read/Write	Name	Description	Default
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15	RO	Next Page	1=Link Partner is requesting Next Page function 0=Base Page is requested.	1'h0
14	RO	Acknowledge	1= Link partner acknowledge Received Successfully 0 =Not Received	1'h0
13	RO	Remote Fault	1 = Auto Negotiation Fault Detected 0 = No Remote Fault	1'h0
12:1 1	RO	Not implemented	Technology Ability A7-A6	2'h0
10	RO	Pause	Technology Ability A5	1'h0
9	RO	Not Implemented	Technology Ability A4	1'h0
8	RO	100Base-TX Full Duplex Capable	1 = Capable 0 = Not Capable	1'h0
7	RO	100 Base-TX Half Duplex Capable	1 = Capable 0 = Not Capable	1'h0
6	RO	10 Base-T Full Duplex Capable	1 = Capable 0 = Not Capable	1'h0
5	RO	10 Base-T Half Duplex Capable	1 = Capable 0 = Not Capable	1'h0
4:0	RO	Selector Field	Identifies type of message	5'h00

Auto-Negotiation expansion register

CR Address:06(d06) Reset State: 0000

Bit	R/W/Type	Name	Description	Default
15:5	RO	RESERVED	No Meaning	11'h0
4	RO/LH; RC	Parallel Detection Fault	1 = Local Device Parallel Detection Fault 0 = No fault detected	1'h0
3	RO	Link Partner Next Page Able	1 = Link Partner is Next Page Able 0 = Link Partner is not Next Page Able	1'h0
2	RO	mr_np_able	1 = Local device is Next Page Able 0 = Local device is not Next Page Able	1'h0
1	RO/LH; RC	Page Received	1 = A New Page has been received 0 = A New Page has not been received	1'h0
0	RO	Link Partner Auto-negotiation Able	1 = Link Partner is Auto-negotiation able 0 = Link Partner is not Auto-negotiation able	1'h0

3.11.6 Function Description

3.11.6.1 Flow control settings

For both FE or GE ports, flow control enable/disable is decided by :

1. Force mode is the highest priority,

 1.1 GE ports use FPA : Force Port 5 ~Port 6 ability (offset:0xC8)

 [11:10] Enable port6 or 5 force mode

 [9:8] Port 6 flow control ability (Support asymmetric flow control [9]:TX [8]:RX)

 [7:6] Port 5 flow control ability

 1.2 FE ports use FPA: Force Port4 ~ Port0 Ability (offset: 0x84)

 [31:27] Enable port 4 ~ 0 force mode

 [26:22] Port 4 ~ 0 flow control ability (Only support symmetric flow control)

2. If the force mode is disabled, then use the flow control status after auto-negotiation.

 But there is one exception for flow control : when POC1: Port Control 0 (offset: 0x90) [14:8]

 “EN_FC” pause flow control is disabled, then flow control will be disabled without regard to the AN result.

 (For GE ports, Port5 or 6, EN_FC[port_num] = 0 will disable both TX and RX flow control)

 No matter using force or AN mode, the final flow control enable/disable value will show on POA: Port Ability (offset: 0x80) [24:16] for port 0 ~ 6

3. Another exception on PFC0: Priority flow control – 0 (offset: 0x10) [23:16] Turn off flow control, For Q3 traffic, the user can use this register to turn off the flow control.

3.11.6.2 VID and Tagging

3.11.6.2.1 VID and VLAN member set

RT3352 supports 16 VLANs. It can be configured to identify any 16 out of 4096 possible VIDs.

These 16 VIDs could be configured by setting VIDx (X=0~15) registers. To configure the member set ports of a given VLAN, one can set the VLAN_MEMSET_x (x=0~15) register. Each bit of the VLAN_MEMSET_x register is corresponding to the associated port. For example, to configure port #1 and port #3 as the member ports of VLAN 5, one can set VLAN_MEMSET_5 as 8'b00001010.

3.11.6.2.2 Tag and Untag

There is a per port register to configure the egress tag and untag setting. If one does not want VLAN tagged frame transmitted from a given port x, he could set UNTAG_EN[x]=1; If one wants VLAN tagged frame transmitted from port y, he could set UNTAG_EN[y]=0. RT3352 supports VLAN tag/untag by per egress port basis. It does not support per VLAN per port basis.

3.11.6.2.3 Port VID

There is per port Px_PVID register to support PVID. The Px_PVID is assigned to a incoming frame which is untagged or priority tagged (i.e. VID filed =0).

3.11.6.2.4 Double Tag

RT3352 supports double VLAN tags by setting a per ingress port register – DOUBLE_TAG_EN[x].

When RT3352 receives a frame from a port with DOUBLE_TAG_EN = 1, it will ignore the VLAN tag filed, if any, and insert the associated PVID in front of the frame after the MAC SA field. Then,

it will go on the frame forwarding decision based on this PVID. When this frame is finally be transmitted to an egress port with UNTAG_EN=0, the egress packet will be double VLAN tagged if its incoming format is single VLAN tag; it will be single VLAN tagged if its incoming format is non-VLAN tagged. Please see the following figure for some examples.

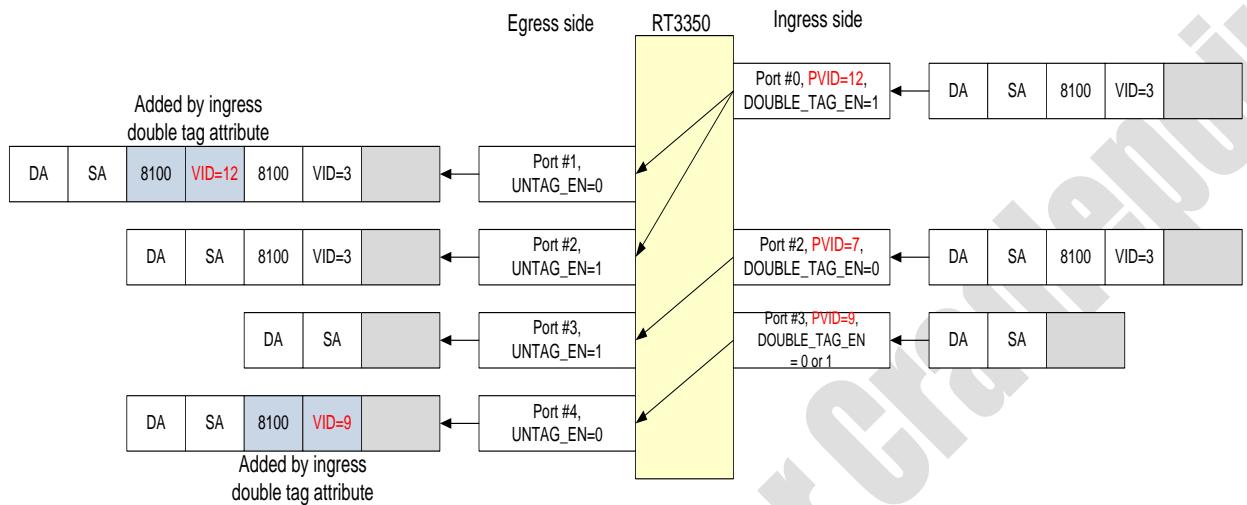


Fig. 3-20-2 Double Tag

3.11.6.2.5 Special Tag

In order to let the recipient (e.g. RT3352 internal CPU or external 3rd party CPU) knows the incoming port number of a received frame, a special tag is supported to rewrite the TPID (0x8100) filed with the incoming port number. The format of this rewritten TPID is : 810x, where x specifies the incoming port number. To enable this feature, one should set CPU_TPID_EN=1 first and specify output ports that need incoming port number to be carried by TPID by setting the associated ports in TX_CPU_TPID_BIT_MAP[6:0]. Please be noted, this special tag feature is a supplement to the existing VLAN tag feature. If the egress frame does not have VLAN tag, there is no way for RT3352 to put incoming port number into the modified TPID field. If the egress frame is double VLAN tagged, the special tag applies to the outer VLAN tag only. Please see the following figure for some examples.

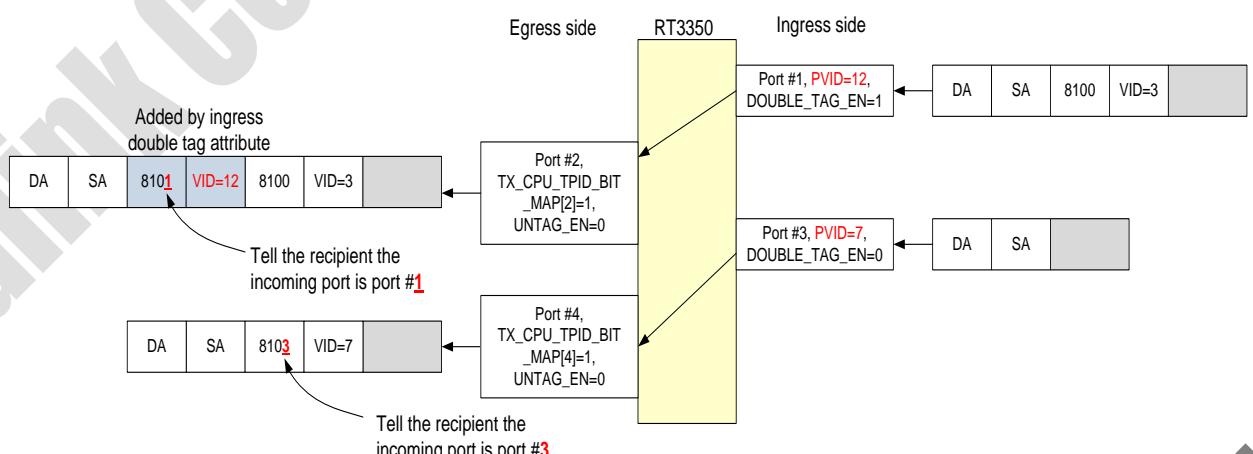


Fig. 3-20-3 Special Tag

3.11.6.3 Packet Classification, QoS, Scheduling and Buffer control

RT3352 supports 4 CoS queues per egress port. When a frame is received, it is classified by IP DSCP, 802.1p tag and incoming port priority. The classify sequence is 802.1p tag first , then IP DSCP, and finally the incoming port priority. To enable IP DSCP classification for port x, one has to set EN_TOS[x] to 1; To enable 802.1p tag classification for port x, one has to set EN_VLAN[x] to 1. If both EN_TOS[x] and EN_VLAN[x] are zero or could not be applied (for non-IP or non-VLAN frames), frame will be classified by the PORT_PRIx register. The IP DSCP and 802.1p user priority to CoS queue mapping are specified by the following tables :

IP DSCP (decimal value)	CoS Queue Mapping
0~15	BK_q
16~31	BE_q
32~47	CL_q
48~63	VO_q

802.1p priority (decimal value)	CoS Queue Mapping
1, 2	BK_q
0, 3	BE_q
4, 5	CL_q
6, 7	VO_q

At the egress side, there is a SP/WRR scheduler for each output port to schedule the frame transmission opportunity. One can assign the weight for each of the VO/CL/BE/BK queues to specify the service ratio. It also support a mixed schedule mode to treat VO queue as the strict priority by assigning its weight (VO_NUM) to zero.

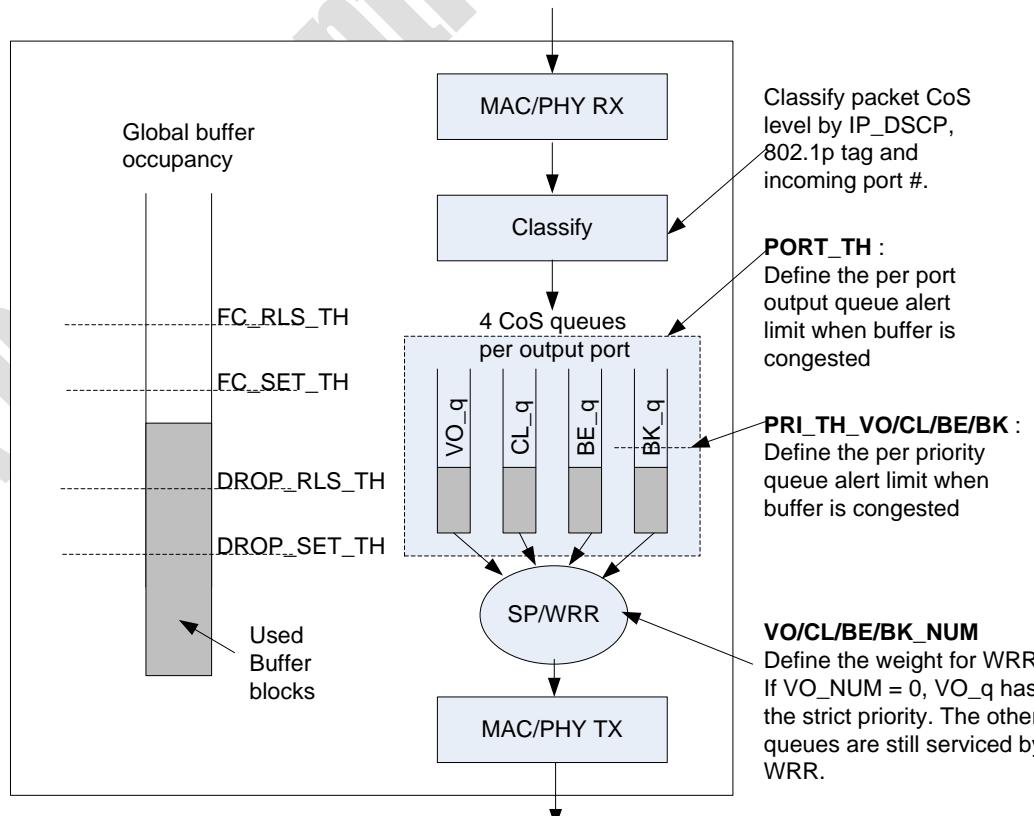


Fig. 3-20-4 Packet Classification, QoS, Scheduling and Buffer control

To support QoS-aware flow control, there is a global per CoS queue threshold setting to define the alert threshold when global packet buffer is getting congested. When the global buffer block count is lower than FC_SET_TH, an incoming frame will trigger a pause_ON frame to be transmitted if the PORT_TH of the destination port and PRI_TH_xx (xx = VO or CL or BE or BK) are both reached. By this sophisticated buffer control mechanism, the high priority traffic (e.g. VoIP) will not get dropped or paused if it is put in strict priority VO_q and its source rate is controlled.

The above description for QoS-aware flow control could be worked even well if we turn on SW2FE_WL_FC_EN (Switch to Frame Engine WAN-LAN flow control) for one-armed router application. Since there is only a single GE port connecting the frame engine and the embedded Ethernet switch, the traditional 802.3x pause mechanism might block all frames from CPU to the Ethernet switch regardless of frame's destination (LAN or WAN). In other words, there will be HOL (Head-of-Line blocking in this one-armed router case. To relief the HOL, one could tell the Ethernet switch which ports are LAN ports by specifying the ports into LAN_PMAP register. Together with separated LAN/WAN GDMA in the frame engine, a better QoS-aware flow control could be supported.

3.11.6.4 Spanning Tree Protocol

To eliminate the LAN loop , Spanning Tree Protocol(STP) can be used to detect the loop and maintain the spanning tree topology. RT3352 can support different port states, frame forwarding and learning capability to meet the STP requirements. Below table expresses the relative port states and the corresponding capabilities.

Port State	Receive BPDU	Transmit BPDU	Learn Address	Forward Frame
Disabled	-	-	-	-
Blocking	V	-	-	-
Listening	V	V	-	-
Learning	V	V	V	-
Forwarding	V	V	V	V

To emulate the different port behaviors, user can configure the following registers based on which port state the software will apply one port to.

1. Disabled -

- Disable frame transmission(POC1.BLOCKING_STATE=0x1)
- Not participate in the operation of the Spanning Tree Protocol (SGC.RMC_RULE=0x2)
- Disable Source MAC Learning(POC1.DIS_LRNING=0x1)

2. Blocking -

- Disable frame transmission (POC1.BLOCKING_STATE=0x1)
- Participate in the Spanning Tree Protocol (SGC.RMC_RULE=0x1)
- Disable Source MAC Learning(POC1.DIS_LRNING=0x1)

3. Listening -

- Disable frame transmission (POC1.BLOCKING_STATE=0x1)
- Participate in the operation of the Spanning Tree Protocol (SGC.RMC_RULE=0x1)
- Disable Source MAC Learning(POC1.DIS_LRNING=0x1)

4. Learning -

- Discard frame transmission(POC1.BLOCKING_STATE=0x1)
- Participate in the operation of the Spanning Tree Protocol (SGC.RMC_RULE=0x1)
- Enable Source MAC Learning(POC1.DIS_LRNING=0x0)

5. Forwarding -

- Enable frame transmission (POC1.BLOCKING_STATE=0x0)
- Participate in the operation of the Spanning Tree Protocol (SGC.RMC_RULE=0x1)

- Enable Source MAC Learning(POC1.DIS_LRNING=0x0)

3.12 802.11n 2T2R MAC/BBP

3.12.1 Features

- 1x1/1x2/1x3/2x1/2x2 modes
- 300MHz PHY Rate Support
- Legacy and High Throughput Modes
- 20MHz/40MHz bandwidth
- Reverse Direction Data Flow and Frame Aggregation
- WEP 64/128, WPA, WPA2 Support
- QoS – WMM, WMM-PS
- Wake on Wireless LAN
- Multiple BSSID Support
- International Regulation - 802.11d + h
- Cisco CCX V1.0 V2.0 V3.0 Compliance
- Bluetooth Co-existence
- Low Power with Advanced Power Management

3.12.2 Block Diagram

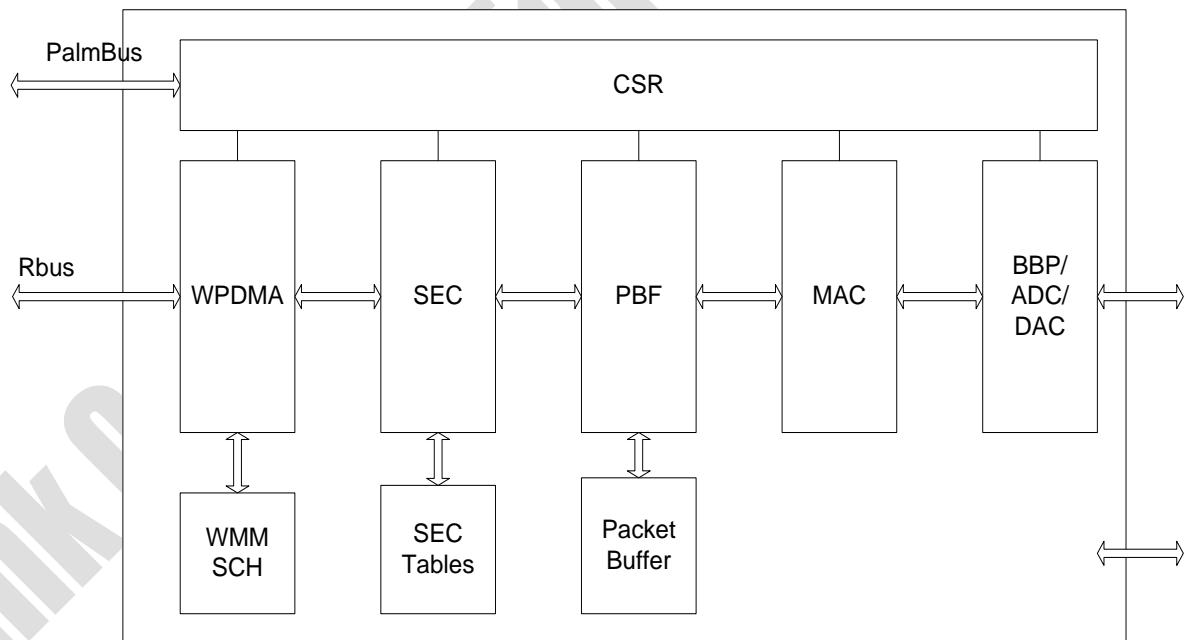


Fig. 3-21-1 802.11n 2T2R MAC/BBP block diagram

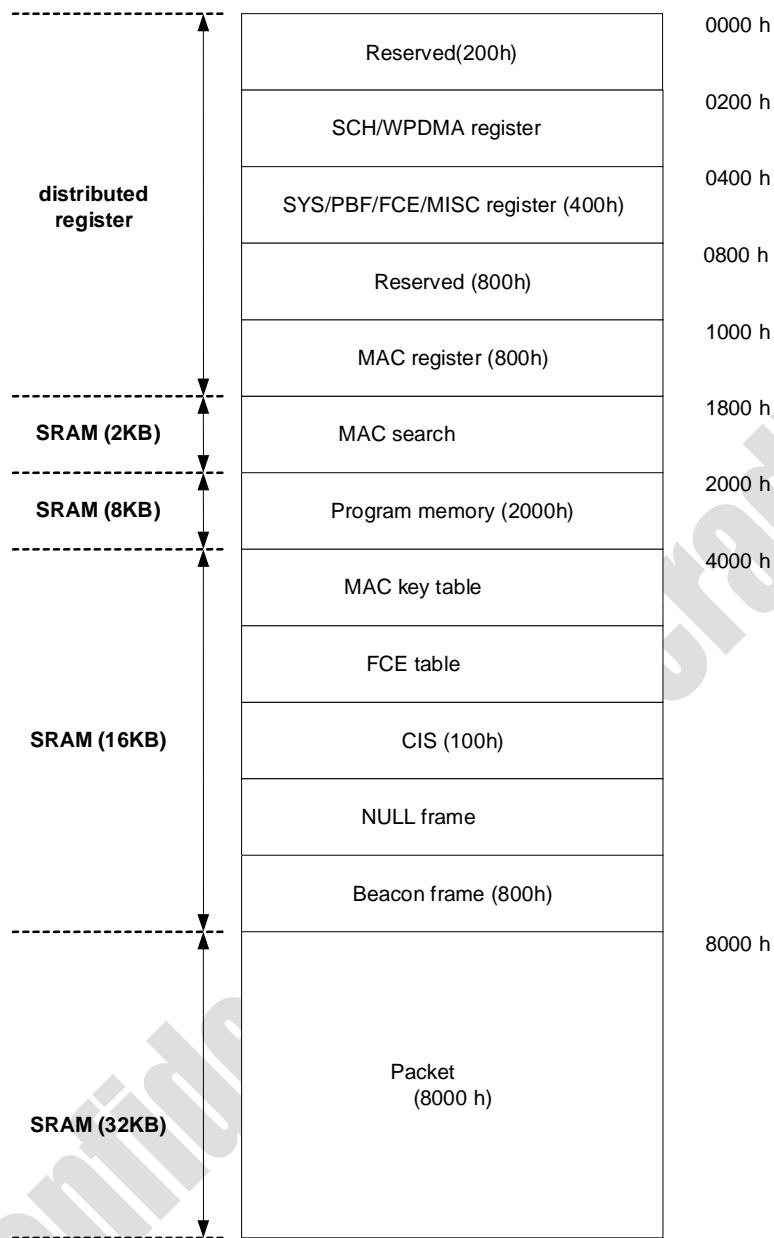


Fig. 3-21-2 802.11n 2T2R MAC/BBP register map

3.12.3 Register Description - SCH/WPDMA (base: 1018.0000)

INT_STATUS (offset: 0x0200)

Bits	Type	Name	Description	Initial value
31:21	-	-	Reserved	0
20	R/W	RADAR_INT	BBP radar detection interrupt	0
19:18	-	-	Reserved	0
17	R/W	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0
16	R/W	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0

15	R/W	MAC_INT_4	MAC interrupt 4: GP timer interrupt	0
14	R/W	MAC_INT_3	MAC interrupt 3: Auto wakeup interrupt	0
13	R/W	MAC_INT_2	MAC interrupt 2: TX status interrupt	0
12	R/W	MAC_INT_1	MAC interrupt 1: Pre-TBTT interrupt	0
11	R/W	MAC_INT_0	MAC interrupt 0: TBTT interrupt	0
10	RO	TX_RX_COHERENT	When TX_COHERENT or RX_COHERENT is on, this bit is set	0
9	R/W	MCU_CMD_INT	MCU command interrupt	0
8	R/W	TX_DONE_INT5	TX Queue#5 packet transmit interrupt Write 1 to clear the interrupt.	0
7	R/W	TX_DONE_INT4	TX Queue#4 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
6	R/W	TX_DONE_INT3	TX Queue#3 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
5	R/W	TX_DONE_INT2	TX Queue#2 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
4	R/W	TX_DONE_INT1	TX Queue#1 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
3	R/W	TX_DONE_INT0	TX Queue#0 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
2	R/W	RX_DONE_INT	RX packet receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
1	R/W	TX_DLY_INT	Summary of the whole WPDMA TX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0
0	R/W	RX_DLY_INT	Summary of the whole WPDMA RX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0

INT_MASK (offset:0x0204)

Bits	Type	Name	Description	Initial value
31:21	-	-	Reserved	0
20	R/W	RADAR_INT_EN	Enable for BBP radar detection interrupt 1: Enable the interrupt 0: Disable the interrupt	0
19:18	-	-	Reserved	0
17	R/W	TX_COHERENT_EN	Enable for TX_DMA data coherent interrupt 1: Enable the interrupt 0: Disable the interrupt	0
16	R/W	RX_COHERENT_EN	Enable for RX_DMA data coherent interrupt 1: Enable the interrupt 0: Disable the interrupt	0
14	R/W	MAC_INT4_EN	MAC interrupt 4: GP timer interrupt	0
14	R/W	MAC_INT3_EN	MAC interrupt 3: Auto wakeup interrupt	0
13	R/W	MAC_INT2_EN	MAC interrupt 2: TX status interrupt	0
12	R/W	MAC_INT1_EN	MAC interrupt 1: Pre-TBTT interrupt	0
11	R/W	MAC_INT0_EN	MAC interrupt 0: TBTT interrupt	0

10	-	-	Reserved	0
9	R/W	MCU_CMD_INT_MSK	MCU command interrupt enable 1 : Enable the interrupt 0 : Disable the interrupt	0
8	R/W	TX_DONE_INT_MSK5	TX Queue#5 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
7	R/W	TX_DONE_INT_MSK4	TX Queue#4 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
6	R/W	TX_DONE_INT_MSK 3	TX Queue#3 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
5	R/W	TX_DONE_INT_MSK 2	TX Queue#2 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
4	R/W	TX_DONE_INT_MSK 1	TX Queue#1 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
3	R/W	TX_DONE_INT_MSK 0	TX Queue#0 packet transmit interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
2	R/W	RX_DONE_INT_MSK	RX packet receive interrupt 1 : Enable the interrupt 0 : Disable the interrupt	0
1	R/W	TX_DLY_INT_MSK	Summary of the whole WPDMA TX related interrupts 1 : Enable the interrupt 0 : Disable the interrupt	0
0	R/W	RX_DLY_INT_MSK	Summary of the whole WPDMA RX related interrupts 1 : Enable the interrupt 0 : Disable the interrupt	0

WPDMA_GLO_CFG (offset:0x0208)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:8		HDR_SEG_LEN	Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value. When set to zero, the header/payload scattering feature is disabled.	8'b0
7	R/W	BIG_ENDIAN	The endian mode selection. DMA applies the endian rule to convert payload and TX/RX information. DMA won't apply endian rule to register or descriptor. 1: big endian. 0: little endian.	0
6	R/W	TX_WB_DDONE	0 : Disable TX_DMA writing back DDONE into TXD 1 : Enable TX_DMA writing back DDONE into TXD	1'b1
5:4	R/W	WPDMA_BT_SIZE	Define the burst size of WPDMA 0 : 4 DWORD (16bytes) 1 : 8 DWORD (32 bytes) 2 : 16 DWORD (64 bytes) 3 : 32 DWORD (128 bytes)	2'd2
3	RO	RX_DMA_BUSY	1 : RX_DMA is busy 0 : RX_DMA is not busy	0
2	R/W	RX_DMA_EN	1 : Enable RX_DMA 0 : Disable RX_DMA (when disabled, RX_DMA will finish the	0

			current receiving packet, then stop.)	
1	RO	TX_DMA_BUSY	1 : TX_DMA is busy 0 : TX_DMA is not busy	0
0	R/W	TX_DMA_EN	1 : Enable TX_DMA 0 : Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)	0

WPDMA_RST_IDX (offset:0x020C)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	1'b0
16	W1C	RST_DRX_IDX0	Write 1 to reset to RX_DMARX_IDX0 to 0	1'b0
15:6	-	-	Reserved	1'b0
5	W1C	RST_DTX_IDX3	Write 1 to reset to TX_DMATX_IDX5 to 0	1'b0
4	W1C	RST_DTX_IDX2	Write 1 to reset to TX_DMATX_IDX4 to 0	1'b0
3	W1C	RST_DTX_IDX3	Write 1 to reset to TX_DMATX_IDX3 to 0	1'b0
2	W1C	RST_DTX_IDX2	Write 1 to reset to TX_DMATX_IDX2 to 0	1'b0
1	W1C	RST_DTX_IDX1	Write 1 to reset to TX_DMATX_IDX1 to 0	1'b0
0	W1C	RST_DTX_IDX0	Write 1 to reset to TX_DMATX_IDX0 to 0	1'b0

DELAY_INT_CFG (offset:0x0210)

Bits	Type	Name	Description	Initial Value
31	RW	TXDLY_INT_EN	1: Enable TX delayed interrupt mechanism. 0: Disable TX delayed interrupt mechanism.	1'b0
30:24	RW	TXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See below), an Final TX_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'b0
23:16	RW	TXMAX_PTIME	Specified Max pending time for the internal TX_DONE_INT0-5. When the pending time equal or grater TXMAX_PTIME x 20us or the # of pended TX_DONE_INT0-5 equal or grater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'b0
15	RW	RXDLY_INT_EN	1: Enable RX delayed interrupt mechanism. 0: Disable RX delayed interrupt mechanism.	1'b0
14:8	RW	RXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See below), an Final RX_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'b0
7:0	RW	RXMAX_PTIME	Specified Max pending time for the internal RX_DONE_INT. When pending time equal or grater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or grater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'b0

WMM_AIFSN_CFG (offset:0x0214)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	16'b0
15:12	RW	AIFSN3	WMM parameter AIFSN3	4'h0
11:8	RW	AIFSN2	WMM parameter AIFSN2	4'h0
7:4	RW	AIFSN1	WMM parameter AIFSN1	4'h0

3:0	RW	AIFSNO	WMM parameter AIFSNO	4'h0
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WMM_CWMIN_CFG (offset:0x0218)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	16'b0
15:12	RW	CW_MIN3	WMM parameter Cw_min3	4'h0
11:8	RW	CW_MIN2	WMM parameter Cw_min2	4'h0
7:4	RW	CW_MIN1	WMM parameter Cw_min1	4'h0
3:0	RW	CW_MIN0	WMM parameter Cw_min0	4'h0

WMM_CWMAX_CFG (offset:0x021C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	16'b0
15:12	RW	CW_MAX3	WMM parameter Cw_max3	4'h0
11:8	RW	CW_MAX2	WMM parameter Cw_max2	4'h0
7:4	RW	CW_MAX1	WMM parameter Cw_max1	4'h0
3:0	RW	CW_MAX0	WMM parameter Cw_max0	4'h0

WMM_TXOP0_CFG (offset:0x0220)

Bits	Type	Name	Description	Initial Value
31:16	RW	TXOP1	WMM parameter TXOP1	16'h0
15:0	RW	TXOP0	WMM parameter TXOP0	16'h0

WMM_TXOP1_CFG (offset:0x0224)

Bits	Type	Name	Description	Initial Value
31:16	RW	TXOP3	WMM parameter TXOP3	16'h0
15:0	RW	TXOP2	WMM parameter TXOP2	16'h0

TX_BASE_PTR0 (offset:0x0230)

Bits	Type	Name	Description	Initial Value
31:0	R/W	TX_BASE_PTR0	Point to the base address of TX_Ring0 (4-DWORD aligned address)	0

TX_MAX_CNT0 (offset:0x0234)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_MAX_CNT0	The maximum number of TXD count in TXD_Ring0.	0

TX_CTX_IDX0 (offset:0x0238)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_CTX_IDX0	Point to the next TXD CPU wants to use	0

TX_DTX_IDX0 (offset:0x023C)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	20'b0
11:0	RO	TX_DTX_IDX0	Point to the next TXD DMA wants to use	0

TX_BASE_PTR1 (offset:0x0240,default :0x00000000)
TX_MAX_CNT1 (offset:0x0244,default :0x00000000)
TX_CTX_IDX1 (offset:0x0248,default :0x00000000)
TX_DTX_IDX1 (offset:0x024C,default :0x00000000)
TX_BASE_PTR2 (offset:0x0250,default :0x00000000)
TX_MAX_CNT2 (offset:0x0254,default :0x00000000)
TX_CTX_IDX2 (offset:0x0258,default :0x00000000)
TX_DTX_IDX2 (offset:0x025C,default :0x00000000)
TX_BASE_PTR3 (offset:0x0260,default :0x00000000)
TX_MAX_CNT3 (offset:0x0264,default :0x00000000)
TX_CTX_IDX3 (offset:0x0268,default :0x00000000)
TX_DTX_IDX3 (offset:0x026C,default :0x00000000)

TX_BASE_PTR4 (offset:0x0270,default :0x00000000)
 TX_MAX_CNT4 (offset:0x0274,default :0x00000000)
 TX_CTX_IDX4 (offset:0x0278,default :0x00000000)
 TX_DTX_IDX4 (offset:0x027C,default :0x00000000)

TX_BASE_PTR5 (offset:0x0280,default :0x00000000)
 TX_MAX_CNT5 (offset:0x0284,default :0x00000000)
 TX_CTX_IDX5 (offset:0x0288,default :0x00000000)
 TX_DTX_IDX5 (offset:0x028C,default :0x00000000)
 RX_BASE_PTR (offset:0x0290)

Bits	Type	Name	Description	Initial Value
31:0	R/W	RX_BASE_PTR0	Point to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address	0

RX_MAX_CNT (offset:0x0294)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0
11:0	R/W	RX_MAX_CNT0	The maximum number of RXD count in RXD Ring #0.	0

RX_CALC_IDX (offset:0x0298)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0
11:0	R/W	RX_CALC_IDX0	Point to the next RXD CPU wants to allocate to RXD Ring #0.	0

FS_DRX_IDX (offset:0x029C)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0
11:0	R/W	RX_DRX_IDX0	Point to the next RXD DMA wants to use in FDS Ring#0. It should be a 4-DWORD aligned address.	0

US_CYC_CNT (offset:0x02A4)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0
24	R/W	TEST_EN	Test mode enable	0
23:16	R/W	TEST_SEL	Test mode selection	8'hf0
15:9	-	-	Reserved	0
8	R/W	BT_MODE_EN	Blue-tooth mode enable	0
7:0	RW	US_CYC_CNT	Clock cycle count in 1us. It's dependent on the system clock rate. For system clock rate = 125Mhz, set 8'h7D For system clock rate = 133Mhz, set 8'h85	8'h21

3.12.3.1 Register Description - PBF (base: 1018.0000)

SYS_CTRL (offset: 0x0400)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0
19	R/W	SHR_MSEL	Shared memory access selection. 0: address 0x4000 – 0x7FFF mapping to lower 16kB of shared memory 1: address 0x4000 – 0x7FFF mapping to higher 4kB of shared memory	0
18:17	R/W	PBF_MSEL	Packet buffer memory access selection. 00: address 0x8000 – 0xFFFF mapping to 1 st 32kB of packet buffer. 01: address 0x8000 – 0xFFFF mapping to 2 nd 32kB of packet buffer. 10: address 0x8000 – 0xFFFF mapping to 3 rd 32kB of packet buffer.	0
16	R/W	HST_PM_SEL	Host program ram write selection.	0
15			Reserved	
14	R/W	CAP_MODE	Packet buffer capture mode.	0

			0: packet buffer in normal mode. 1: packet buffer in BBP capture mode.	
13	-	-	Reserved	1
12	R/W	CLKSELECT	MAC/PBF clock source selection. 0: from PLL 1: from 40MHz clock input	0
11	R/W	PBF_CLKEN	PBF clock enable.	0
10	R/W	MAC_CLK_EN	MAC clock enable.	0
9	R/W	DMA_CLK_EN	DMA clock enable.	0
8	-	-	Reserved	0
7	R/W	MCU_READY	MCU ready. 8051 writes '1' to this bit to inform host internal MCU is ready.	0
6:5	-	-	Reserved	0
4	R/W	ASY_RESET	ASYNC interface reset. Write '1' to this bit will put ASYNC into reset state.	0
3	R/W	PBF_RESET	PBF hardware reset. Write '1' to this bit will put PBF into reset state.	0
2	R/W	MAC_RESET	MAC hardware reset. Write '1' to this bit will put MAC into reset state.	0
1	R/W	DMA_RESET	DMA hardware reset. Write '1' to this bit will put DMA into reset state.	0
0	W1C	MCU_RESET	MCU hardware reset. This bit will be auto-cleared after several clock cycles.	0

HOST_CMD (offset: 0x0404)

Bits	Type	Name	Description	Initial Value
31:0	R/W	HST_CMD	Host command code. Host write this register will trigger interrupt to 8051.	0

PBF_CFG (offset: 0x0408)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0
23:21	R/W	TX1Q_NUM	Queue depth of Tx1Q. The maximum number is 7.	3'h7
20:16	R/W	TX2Q_NUM	Queue depth of Tx2Q. The maximum number is 20.	5'h14
15	R/W	NULL0_MODE	HCCA NULL0 frame auto mode. In this mode, In this mode, NULL0 frame will be automatically transmitted if TXQ1 is enabled but empty. After NULL0 frame transmitted, TXQ1 will be disabled. 0: disable 1: enable	0
14	R/W	NULL1_MODE	HCCA NULL1 frame auto mode. In this mode, all TXQ (0/1/2) will be disabled after NULL1 frame transmitted. 0: disable 1: enable	0
13	R/W	RX_DROP_MODE	Rx drop mode. When set, PBF will drop Rx packet before into DMA. 0: normal mode 1: drop mode	0
12	R/W	TX0Q_MODE	Tx0Q operation mode. 0: auto mode 1: manual mode	0
11	R/W	TX1Q_MODE	Tx1Q operation mode. 0: auto mode 1: manual mode	0
10	R/W	TX2Q_MODE	Tx2Q operation mode. 0: auto mode 1: manual mode	0

9	R/W	RX0Q_MODE	Rx0Q operation mode. 0: auto mode 1: manual mode	0
8	R/W	HCCA_MODE	HCCA auto mode. In this mode, TXQ1 will be enabled when CF-POLL arriving. 0: disable 1: enable	0
7:5	-	-	Reserved	0
4	R/W	TX0Q_EN	Tx0Q enable 0: disable 1: enable	1
3	R/W	TX1Q_EN	Tx1Q enable 0: disable 1: enable	0
2	R/W	TX2Q_EN	Tx2Q enable 0: disable 1: enable	1
1	R/W	RX0Q_EN	Rx0Q enable 0: disable 1: enable	1
0	-	-	Reserved	0

MAX_PCNT (offset: 0x040C)

Bits	Type	Name	Description	Initial Value
31:24	R/W	MAX_TX0Q_PCNT	Maximum buffer page count of Tx0Q.	8'h1f
23:16	R/W	MAX_TX1Q_PCNT	Maximum buffer page count of Tx1Q.	8'h3f
15:8	R/W	MAX_TX2Q_PCNT	Maximum buffer page count of Tx2Q.	8'h9f
7:0	R/W	MAX_RX0Q_PCNT	Maximum buffer page count of Rx0Q.	8'h9f

BUF_CTRL (offset: 0x0410)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0
11	W1C	WRITE_TX0Q	Manual write Tx0Q.	0
10	W1C	WRITE_TX1Q	Manual write Tx1Q.	0
9	W1C	WRITE_TX2Q	Manual write Tx2Q	0
8	W1C	WRITE_RX0Q	Manual write Rx0Q	0
7	W1C	NULL0_KICK	Kick out NULL0 frame. This bit will be cleared after NULL0 frame is transmitted.	0
6	W1C	NUL1_KICK	Kick out NULL1 frame. This bit will be cleared after NULL1 frame is transmitted.	0
5	W1C	BUF_RESET	Buffer reset.	0
4	-	-	Reserved	0
3	W1C	READ_TX0Q	Manual read Tx0Q.	0
2	W1C	READ_TX1Q	Manual read Tx1Q.	0
1	W1C	READ_TX2Q	Manual read Tx2Q	0
0	W1C	READ_RX0Q	Manual read Rx0Q	0

MCU_INT_STA (offset: 0x0414)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0
27	R/W	MAC_INT_11	MAC interrupt 11: Reserved	0
26	R/W	MAC_INT_10	MAC interrupt 10: Reserved	0
25	R/W	MAC_INT_9	MAC interrupt 9: Reserved	0
24	R/W	MAC_INT_8	MAC interrupt 8: RX QoS CF-Poll interrupt	0

23	R/W	MAC_INT_7	MAC interrupt 7: TXOP early termination interrupt	0
22	R/W	MAC_INT_6	MAC interrupt 6: TXOP early timeout interrupt	0
21	R/W	MAC_INT_5	MAC interrupt 5: Reserved	0
20	R/W	MAC_INT_4	MAC interrupt 4: GP timer interrupt	0
19	R/W	MAC_INT_3	MAC interrupt 3: Auto wakeup interrupt	0
18	R/W	MAC_INT_2	MAC interrupt 2: TX status interrupt	0
17	R/W	MAC_INT_1	MAC interrupt 1: Pre-TBTT interrupt	0
16	R/W	MAC_INT_0	MAC interrupt 0: TBTT interrupt	0
15	R/W	ADCL5H8_INT	RF ADC change from 5-bit to 8-bits interrupt	0
14	R/W	RX_SD_INT	RF RX signal detection interrupt	0
13:12	-	-	Reserved	0
11	R/W	DTX0_INT	DMA to TX0Q frame transfer complete interrupt.	0
10	R/W	DTX1_INT	DMA to TX1Q frame transfer complete interrupt.	0
9	R/W	DTX2_INT	DMA to TX2Q frame transfer complete interrupt.	0
8	R/W	DRX0_INT	RX0Q to DMA frame transfer complete interrupt.	0
7	R/W	HCMD_INT	Host command interrupt.	0
6	R/W	NOTX_INT	NULL0 frame Tx complete interrupt.	0
5	R/W	N1TX_INT	NULL1 frame Tx complete interrupt.	0
4	R/W	BCNTX_INT	Beacon frame Tx complete interrupt.	0
3	R/W	MTX0_INT	TX0Q to MAC frame transfer complete interrupt.	0
2	R/W	MTX1_INT	TX1Q to MAC frame transfer complete interrupt.	0
1	R/W	MTX2_INT	TX2Q to MAC frame transfer complete interrupt.	0
0	R/W	MRX0_INT	MAC to RX0Q frame transfer complete interrupt.	0

*This register is only for 8051

MCU_INT_ENA (offset:0x0418)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0
27	R/W	MAC_INT11_EN	MAC interrupt 11 enable	0
26	R/W	MAC_INT10_EN	MAC interrupt 10 enable	0
25	R/W	MAC_INT9_EN	MAC interrupt 9 enable	0
24	R/W	MAC_INT8_EN	MAC interrupt 8 enable	0
23	R/W	MAC_INT7_EN	MAC interrupt 7 enable	0
22	R/W	MAC_INT6_EN	MAC interrupt 6 enable	0
21	R/W	MAC_INT5_EN	MAC interrupt 5 enable	0
20	R/W	MAC_INT4_EN	MAC interrupt 4 enable	0
19	R/W	MAC_INT3_EN	MAC interrupt 3 enable	0
18	R/W	MAC_INT2_EN	MAC interrupt 2 enable	0
17	R/W	MAC_INT1_EN	MAC interrupt 1 enable	0
16	R/W	MAC_INT0_EN	MAC interrupt 0 enable	0
15:12	-	-	Reserved	0
11	R/W	DTX0_INT_EN	DMA to TX0Q frame transfer complete interrupt enable.	0
10	R/W	DTX1_INT_EN	DMA to TX1Q frame transfer complete interrupt enable.	0
9	R/W	DTX2_INT_EN	DMA to TX2Q frame transfer complete interrupt enable.	0
8	R/W	DRX0_INT_EN	RX0Q to DMA frame transfer complete interrupt enable.	0
7	R/W	HCMD_INT_EN	Host command interrupt enable.	0
6	R/W	NOTX_INT_EN	NULL0 frame Tx complete interrupt enable.	0
5	R/W	N1TX_INT_EN	NULL1 frame Tx complete interrupt enable.	0
4	R/W	BCNTX_INT_EN	Beacon frame Tx complete interrupt enable.	0

3	R/W	MTX0_INT_EN	TX0Q to MAC frame transfer complete interrupt enable.	0
2	R/W	MTX1_INT_EN	TX1Q to MAC frame transfer complete interrupt enable.	0
1	R/W	MTX2_INT_EN	TX2Q to MAC frame transfer complete interrupt enable.	0
0	R/W	MRX0_INT_EN	MAC to RX0Q frame transfer complete interrupt enable.	0

*This register is only for 8051

TX0Q_IO (offset: 0x041C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	TX0Q_IO	TX0Q IO port. This register is used in manual mode.	0

TX1Q_IO (offset: 0x0420)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	TX1Q_IO	TX1Q IO port. This register is used in manual mode.	0

TX2Q_IO (offset: 0x0424)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	TX2Q_IO	TX2Q IO port. This register is used in manual mode.	0

RX0Q_IO (offset: 0x0428)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	RX0Q_IO	RX0Q IO port. This register is used in manual mode.	0

BCN_OFFSET0 (offset: 0x042C)

Bits	Type	Name	Description	Initial Value
31:24	R/W	BCN3_OFFSET	Beacon #3 address offset in shared memory. Unit is 64 byte.	8'hec
23:16	R/W	BCN2_OFFSET	Beacon #2 address offset in shared memory. Unit is 64 byte.	8'he8
15:8	R/W	BCN1_OFFSET	Beacon #1 address offset in shared memory. Unit is 64 byte.	8'he4
7:0	R/W	BCN0_OFFSET	Beacon #0 address offset in shared memory. Unit is 64 byte.	8'he0

Note1: There are two beacon frame buffers on this chip. They are located at 0x4000 - 0x4FFF (SHR_MSEL = 1) and 0x6000 – 0x7FFF (SHR_MSEL = 0).

The physical address of beacon frame is calculated by:

If OFFSET < 0x40

Set SHR_MSEL = 1 (SYS_CTRL[19] = 1)

Beacon frame starting address = OFFSET *64 + 0x4000 (0x4000 – 0x4FFF)

Else if OFFSET >= 0x80

Set SHR_MSEL = 0 (SYS_CTRL[19] = 0)

Beacon frame starting address = OFFSET *64 + 0x4000 (0x6000 – 0x7FFF)

Else

This address can't be beacon buffer

BCN_OFFSET1 (offset: 0x0430)

Bits	Type	Name	Description	Initial Value
31:24	R/W	BCN7_OFFSET	Beacon #7 address offset in shared memory. Unit is 64 byte.	8'hfc
23:16	R/W	BCN6_OFFSET	Beacon #6 address offset in shared memory. Unit is 64 byte.	8'hf8
15:8	R/W	BCN5_OFFSET	Beacon #5 address offset in shared memory. Unit is 64 byte.	8'hf4
7:0	R/W	BCN4_OFFSET	Beacon #4 address offset in shared memory. Unit is 64 byte.	8'hf0

TXRXQ_STA (offset: 0x0434)

Bits	Type	Name	Description	Initial Value
31:24	RO	RX0Q_STA	RxQ status	8'h22
23:16	RO	TX2Q_STA	Tx2Q status	8'h02
15:8	RO	TX1Q_STA	Tx1Q status	8'h02
7:0	RO	TX0Q_STA	Tx0Q status	8'h02

TXRXQ_PCNT (offset: 0x0438)

Bits	Type	Name	Description	Initial Value
31:24	RO	RX0Q_PCNT	Page count in RxQ	8'h00
23:16	RO	TX2Q_PCNT	Page count in Tx2Q	8'h00
15:8	RO	TX1Q_PCNT	Page count in Tx1Q	8'h00
7:0	RO	TX0Q_PCNT	Page count in Tx0Q	8'h00

PBF_DBG (offset: 0x043C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0
7:0	RO	FREE_PCNT	Free page count	8'hFE

CAP_CTRL (offset: 0x0440)

Bits	Type	Name	Description	Initial Value
31	R/W	CAP_ADC_FEQ	Data source. 0: data from the ADC output 1: Data from the FEQ output	0
30	WC	CAP_START	Data capture start 0: No action 1: Start data capture (cleared automatically after capture finished)	0
29	W1C	MAN_TRIGGER	Manual capture trigger	0
28:16	R/W	TRIG_OFFSET	Starting address offset before trigger point.	13'h140
15:13	-	-	Reserved	0
12:0	RO	START_ADDR	Starting address of captured data.	13'h000

3.12.3.2 Register Description – RF TEST (base: 1018.0000)
CSR_RF_CFG (offset: 0x0500)

Bits	Type	Name	Description	Initial Value
31:18	-	-	Reserved	0
17	R/W1	RF_CSR_KICK	Write – kick RF register read/write 0: do nothing 1: kick read/write process Read – Polling RF register read/write 0: idle 1: busy	0
16	R/W	RF_CSR_WR	0: read 1: write	0
15:14	R		Reserved	0
13:8	R/W	TESTCSR_RFACC_REGN	RF register ID R0 ~ R63 UM 0 for R0, 1 for R1 and so on.	0
7:0	R/W	RF_CSR_DATA	Write – DATA written to RF Read – DATA read from RF	0

3.12.3.3 Register Description - MAC (base: 1018.0000)
ASIC_VER_ID (offset:0x1000)

Bits	Type	Name	Description	Initial value
31:16	R	VER_ID	ASIC version ID	16'h2860
15:0	R	REV_ID	ASIC reversion ID	16'h0101

MAC_SYS_CTRL (offset:0x1004)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0

7	R/W	RX_TS_EN	Write 32-bit hardware RX timestamp instead of (RXWI->RSSI), and write (RXWI->RSSI) instead of (RXWI->SNR). Note: For QA RX sniffer mode only. 1: enable 0: disable	0
6	R/W	WLAN_HALT_EN	Enable external WLAN halt control signal 1: enable 0: disable	0
5	R/W	PBF_LOOP_EN	Packet buffer loop back enable (TX->RX) 1: enable 0: disable	0
4	R/W	CONT_TX_TEST	Continuous TX production test; override MAC_RX_EN, MAC_TX_EN 1: enable 0: disable	0
3	R/W	MAC_RX_EN	MAC RX enable 1: enable 0: disable	0
2	R/W	MAC_TX_EN	MAC TX enable 1: enable 0: disable	0
1	R/W	BBP_HRST	BBP hard-reset 1: BBP in reset state 0: BBP in normal state Note: Whole BBP including BBP registers will be reset.	1
0	R/W	MAC_SRST	MAC soft-reset 1: MAC in reset state 0: MAC in normal state Note: MAC registers and tables will NOT be reset.	1

Note: MAC hard-reset is outside the scope of MAC registers.

MAC_ADDR_DW0 (offset:0x1008)

Bits	Type	Name	Description	Initial value
31:24	R/W	MAC_ADDR_3	MAC address byte3	0
23:16	R/W	MAC_ADDR_2	MAC address byte2	0
15:8	R/W	MAC_ADDR_1	MAC address byte1	0
7:0	R/W	MAC_ADDR_0	MAC address byte0	0

MAC_ADDR_DW1 (offset:0x100C)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:8	R/W	MAC_ADDR_5	MAC address byte5	0
7:0	R/W	MAC_ADDR_4	MAC address byte4	0

Note: Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

MAC_BSSID_DW0 (offset:0x1010)

Bits	Type	Name	Description	Initial value
31:24	R/W	BSSID_3	BSSID byte3	0
23:16	R/W	BSSID_2	BSSID byte2	0
15:8	R/W	BSSID_1	BSSID byte1	0
7:0	R/W	BSSID_0	BSSID byte0	0

MAC_BSSID_DW1 (offset: 0x1014)

Bits	Type	Name	Description	Initial value
31:21	-	-	Reserved	0
20:18	R/W	MULTI_BCN_NUM	Multiple BSSID Beacon number 0: one back-off beacon 1-7: SIFS-burst beacon count	0
17:16	R/W	MULTI_BSSID_MODE	Multiple BSSID mode In multiple-BSSID AP mode, BSSID shall be the same as MAC_ADDR, that is, this device owns multiple MAC_ADDR in this mode.	0
			The multiple MAC_ADDR/BSSID are distinguished by [bit2: bit0] of byte5. 0: 1-BSSID mode (BSS index = 0) 1: 2-BSSID mode (byte5.bit0 as BSS index) 2: 4-BSSID mode (byte5.bit1:0 as BSS index) 3: 8-BSSID mode (byte5.bit2:0 as BSS index)	0
15:8	R/W	BSSID_5	BSSID byte5	0
7:0	R/W	BSSID_4	BSSID byte4	0

MAX_LEN_CFG (offset: 0x1018)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19:16	R/W	MIN_MPDU_LEN	Minimum MPDU length (unit: bytes) MAC will drop the MPDU if the length is less than this limitation. Applied only in MAC RX.	10
15:14	-	-	Reserved	0
13:12	R/W	MAX_PSDU_LEN	Maximum PSDU length (power factor) 0: $2^{13} = 8K$ bytes 1: $2^{14} = 16K$ bytes 2: $2^{15} = 32K$ bytes 3: $2^{16} = 64K$ bytes MAC will NOT generate A-MPDU with length greater than this limitation. Applied only in MAC TX.	0
11:0	R/W	MAX_MPDU_LEN	Maximum MPDU length (unit: bytes) MAC will drop the MPDU if the length is greater than this limitation. Applied only in MAC RX.	4095

BBP_CSR_CFG (offset: 0x101C)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	R/W	BBP_RW_MODE	BBP Register R/W mode 1: parallel mode 0: serial mode	1
18	R/W	BBP_PAR_DUR	BBP Register parallel R/W pulse width 0: pulse width = 62.5ns 1: pulse width = 112.5ns	0
			Note: Please set BBP_PAR_DUR=1 in 802.11J mode.	
17	R/W	BBP_CSR_KICK	Write - kick BBP register read/write 0: do nothing 1: kick read/write process Read - Polling BBP register read/write progress 0: idle, 1: busy	0
16	R/W	BBP_CSR_RW	0: Write 1: Read	0
15:8	R/W	BBP_ADDR	BBP register ID 0 for R0, 1 for R1, and so on.	0
7:0	R/W	BBP_DATA	Write - Data written to BBP Read - Data read from BBP	0

RF_CSR_CFG0 (offset: 0x1020)

Bits	Type	Name	Description	Initial value
31	R/W	RF_REG_CTRL	Write: 1 - RF_REG0/1/2 to RF chip Read: 0 – idle, 1 – busy	0
30	R/W	RF_LE_SEL	RF_LE selection 0:RF_LE0 activate 1:RF_LE1 activate	0
29	R/W	RF_LE_STBY	RF_LE standby mode 0: RF_LE is high when standby 1: RF_LE is low when standby	0
28:24	R/W	RF_REG_WIDTH	RF register bit width Default: 22	22
23:0	R/W	RF_REG_0	RF register0 ID and content	0

RF_CSR_CFG1 (offset: 0x1024)

Bits	Type	Name	Description	Initial value
31:25	-	-	Reserved	0
24	R/W	RF_DUR	Gap between BB_CONTROL_RF and RF_LE 0: 3 system clock cycle (37.5usec) 1: 5 system clock cycle (62.5usec)	0
23:0	R/W	RF_REG_1	RF register1 ID and content	0

RF_CSR_CFG2 (offset: 0x1028)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0
23:0	R/W	RF_REG_2	RF register2 ID and content	0

Note: Software should make sure the first bit (MSB in the specified bit number) written to RF is 0 for RF chip mode selection.

LED_CFG (offset: 0x102C)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0
30	R/W	LED_POL	LED polarity 0: active low 1: active high	0
29:28	R/W	Y_LED_MODE	Yellow LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	0
27:26	R/W	G_LED_MODE	Green LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	2
25:24	R/W	R_LED_MODE	Red LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	1
23:22	-	-	Reserved	0
21:16	R/W	SLOW_BLK_TIME	Slow blinking period (unit: 1sec)	3
15:8	R/W	LED_OFF_TIME	TX blinking off period (unit: 1ms)	30
7:0	R/W	LED_ON_TIME	TX blinking on period (unit: 1ms)	70

XIFS_TIME_CFG (offset:0x1100)

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	
29	R/W	BB_RXEND_EN	BB_RX_END signal enable Refer BB_RX_END signal from BBP RX logic to start SIFS defer. 0: disable 1: enable	1
28:20	R/W	EIFS_TIME	EIFS time (unit: 1us) EIFS is the defer time after reception of a CRC error packet. After deferring EIFS, the normal back-off process may proceed.	314
19:16	R/W	OFDM_XIFS_TIME	Delayed OFDM SIFS time compensator (unit: 1us) When BB_RX_END from BBP is a delayed version the SIFS deferred will be (OFDM_SIFS_TIME - OFDM_XIFS_TIME)	4
15:8	R/W	OFDM_SIFS_TIME	OFDM SIFS time (unit: 1us) Applied after OFDM TX/RX.	16
7:0	R/W	CCK_SIFS_TIME	CCK SIFS time (unit: 1us) Applied after CCK TX/RX.	10

Note1: EIFS = SIFS + ACK @ 1Mbps + DIFS = 10us (SIFS) + 192us (long preamble) + 14*8us (ACK) + 50us (DIFS) = 364. However, MAC should start back-off procedure after (EIFS-DIFS).

Note2: EIFS is not applied if MAC is a TXOP initiator that owns the channel.

Note3: EIFS is not started if AMPDU is only partial corrupted.

Caution: It is recommended that both (CCK_SIFS_TIME) and (OFDM_SIFS_TIME) are no less than TX/RX transition time. If the SIFS value is not long enough, a SIFS burst transmission may be replaced with a PIFS burst one.

BKOFF_SLOT_CFG (offset:0x1104)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0
11:8	R/W	CC_DELAY_TIME	Channel clear delay (unit: 1-us) This value specified the TX guard time after channel is clear.	2
7:0	R/W	SLOT_TIME	Slot time (unit: 1-us) This value specified the slot boundary after deferring SIFS time. Note: Default 20us is for 11b/g. 11a and 11g-short-slot-mode is 9us.	20

NAV_TIME_CFG (offset:0x1108)

Bits	Type	Name	Description	Initial value
31	WC	NAV_UPD	NAV timer manual update command 0: Do nothing 1: Update NAV timer with NAV_UPD_VAL	0
30:16	R/W	NAV_UPD_VAL	NAV timer manual update value (unit: 1us)	0
15	R/W	NAV_CLR_EN	NAV timer auto-clear enable When enabled, MAC will auto clear NAV timer after the reception of CF-End frame from previous NAV holder STA. 0: disable 1: enable	1
14:0	R	NAV_TIMER	NAV timer (unit: 1us) The timer is set by other STA and will auto countdown to zero. The STA who set the NAV timer is called the NAV holder. When NAV timer is nonzero, MAC will not send any packet.	0

CH_TIME_CFG (offset:0x110C)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	0
4	R/W	EIFS_AS_CH_BUSY	Count EIFS as channel busy 0: disable 1: enable	1
3	R/W	NAV_AS_CH_BUSY	Count NAV as channel busy 0: disable 1: enable	1
2	R/W	RX_AS_CH_BUSY	Count RX busy as channel busy 0: disable 1: enable	1
1	R/W	TX_AS_CH_BUSY	Count TX busy as channel busy	1

			0: disable 1: enable	
0	R/W	CH_STA_TIMER_EN	Channel statistic timer enable 0: disable 1: enable	0

PBF_LIFE_TIMER (offset:0x1110)

Bits	Type	Name	Description	Initial value
31:0	R	PBF_LIFE_TIMER	TX/RX MPDU timestamp timer (free run) Unit: 1us	0

BCN_TIME_CFG (offset:0x1114)

Bits	Type	Name	Description	Initial value
31:24	R/W	TSF_INS_COMP	TSF insertion compensation value (unit: 1us) When inserting TSF, add this value with local TSF timer as the TX timestamp.	0
23:21	-	-	Reserved	0
20	R/W	BCN_TX_EN	BEACON frame TX enable When enabled, MAC sends BEACON frame at TBTT interrupt. 0: disable 1: enable	0
19	R/W	TBTT_TIMER_EN	TBTT timer enable When enabled, TBTT interrupt will be issued periodically with period specified in (BCN_INTERVAL). 0: disable 1: enable	0
18:17	R/W	TSF_SYNC_MODE	Local 64-bit TSF timer synchronization mode 00: disable 01: (STA infra-structure mode) Upon the reception of BEACON frame from associated BSS, local TSF is always updated with remote TSF. 10: (STA ad-hoc mode) Upon the reception of BEACON frame from associated BSS, local TSF is updated with remote TSF only if the remote TSF is greater than local TSF. 11: (AP mode) SYNC with nobody	0
16	R/W	TSF_TIMER_EN	Local 64-bit TSF timer enable When enabled, TSF timer will re-start from zero. 0: disable 1: enable	0
15:0	R/W	BCN_INTERVAL	BEACON interval (unit: 64us) This value specified the interval between Maximum beacon interval is about 4sec.	1600

TBTT_SYNC_CFG (offset:0x1118)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0
23:20	R/W	BCN_CWMIN	Beacon transmission CWMIN after TBTT interrupt (unit: slot)	4

19:16	R/W	BCN_AIFSN	Beacon transmission AIFSN after TBTT interrupt (unit: slot)	2
15:8	R/W	BCN_EXP_WIN	Beacon expecting window duration (unit: 64us)	
7:0	R/W	TBTT_ADJUST	The window starts from TBTT interrupt. The phase of "TBTT interrupt train" will NOT be adjusted by the beacon arrived within the window. IBSS mode TBTT phase adaptive adjustment step (unit: 1us), default value is 16us. In IBSS mode (Ad hoc), if consecutive TX beacon failures (or consecutive success) happened, TBTT timer will adjust its phase to meet the external Ad hoc TBTT time.	32 16

TSF_TIMER_DW0 (offset:0x111C)

Bits	Type	Name	Description	Initial value
31:0	R	TSF_TIMER_DW0	Local TSF timer LSB 32 bits (unit: 1us)	0

TSF_TIMER_DW1 (offset:0x1120)

Bits	Type	Name	Description	Initial value
31:0	R	TSF_TIMER_DW1	Local TSF timer MSB 32 bits (unit: 1us)	0

TBTT_TIMER (offset:0x1124)

Bits	Type	Name	Description	Initial value
31:17	-	-	Reserved	0
16:0	R	TBTT_TIMER	TBTT Timer (unit: 32us) The time remains till next TBTT. When TBTT_TIMER_EN is enabled, the timer will down count from BCN_INTERVAL to zero. When TBTT_TIMER_EN is disabled, the timer will stay in zero.	0

INT_TIMER_CFG (offset:0x1128)

Bits	Type	Name	Description	Initial value
31:16	R/W	GP_TIMER	Period of general purpose interrupt timer (Unit: 64us)	0
15:0	R/W	PRE_TBTT_TIMER	Pre-TBTT interrupt time (unit: 64us) The value specifies the interrupt timing before TBTT interrupt.	0

INT_TIMER_EN (offset:0x112C)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	0
1	R/W	GP_TIMER_EN	Periodic general purpose interrupt timer enable 0: disable 1: enable	0
0	R/W	PRE_TBTT_INT_EN	Pre-TBTT interrupt enable 0: disable 1: enable	0

CH_IDLE_STA (offset:0x1130)

Bits	Type	Name	Description	Initial value
31:0	RC	CH_IDLE_TIME	Channel idle time Unit: 1us	0

In application, the channel busy time can be derived by the equation:

CH_BUSY_TIME = host polling period – **CH_IDLE_TIME**

Reserved (offset:0x1134)

Bits	Type	Name	Description	Initial value
31:0	RC	Reserved	Reserved	0

MAC_STATUS_REG (offset:0x1200)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	0
1	R	RX_STATUS	RX status 0: Idle 1: Busy	0
0	R	TX_STATUS	TX status 0: Idle 1: Busy	0

PWR_PIN_CFG (offset:0x1204)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	0
3	R/W	IO_ADDA_PD	AD/DA power down	0
2	R/W	IO_PLL_PD	PLL power down	0
1	R/W	IO_RA_PE	RA_PE	1
0	R/W	IO_RF_PE	RF_PE	1

AUTO_WAKEUP_CFG (offset:0x1208, default: 0x0000_0014)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15	R/W	AUTO_WAKEUP_EN	Auto wakeup interrupt enable Auto wakeup interrupt will be issued after #(SLEEP_TBTT_NUM) TBTTs' at WAKEUP_LEAD_TIME before the target wakeup TBTT. 0: disable 1: enable Note: Please make sure TBTT_TIMER_EN is enabled.	0
14:8	R/W	SLEEP_TBTT_NUM	Number of sleeping TBTT	0
7:0	R/W	WAKEUP_LEAD_TIME	Auto wakeup lead time (unit: 1TU=1024us)	20

3.12.3.4 MAC TX configuration registers (offset: 0x1300)

EDCA_ACO_CFG (BE) (offset: 0x1300)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19:16	R/W	AC0_CWMAX	AC0 CWMAX (unit: power of 2)	7
15:12	R/W	AC0_CWMIN	AC0 CWMIN (unit: power of 2)	3
11:8	R/W	AC0_AIFSN	AC0 AIFSN (unit: # of slot time)	2
7:0	R/W	AC0_TXOP	AC0 TXOP limit (unit: 32us)	0

EDCA_AC1_CFG (BK) (offset: 0x1304)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0

19:16	R/W	AC1_CWMAX	AC1 CWMAX (unit: power of 2)	7
15:12	R/W	AC1_CWMIN	AC1 CWMIN (unit: power of 2)	3
11:8	R/W	AC1_AIFSN	AC1 AIFSN (unit: # of slot time)	2
7:0	R/W	AC1_TXOP	AC1 TXOP limit (unit: 32us)	0

EDCA_AC2_CFG (VI) (offset: 0x1308)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19:16	R/W	AC2_CWMAX	AC2 CWMAX (unit: power of 2)	7
15:12	R/W	AC2_CWMIN	AC2 CWMIN (unit: power of 2)	3
11:8	R/W	AC2_AIFSN	AC2 AIFSN (unit: # of slot time)	2
7:0	R/W	AC2_TXOP	AC2 TXOP limit (unit: 32us)	0

EDCA_AC3_CFG (VO) (offset: 0x130C)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19:16	R/W	AC3_CWMAX	AC3 CWMAX (unit: power of 2)	7
15:12	R/W	AC3_CWMIN	AC3 CWMIN (unit: power of 2)	3
11:8	R/W	AC3_AIFSN	AC3 AIFSN (unit: # of slot time)	2
7:0	R/W	AC3_TXOP	AC3 TXOP limit (unit: 32us)	0

EDCA_TID_AC_MAP (offset: 0x1310)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:14	R/W	TID7_AC_MAP	AC value as TID=7	3
13:12	R/W	TID6_AC_MAP	AC value as TID=6	3
11:10	R/W	TID5_AC_MAP	AC value as TID=5	2
9:8	R/W	TID4_AC_MAP	AC value as TID=4	2
7:6	R/W	TID3_AC_MAP	AC value as TID=3	0
5:4	R/W	TID2_AC_MAP	AC value as TID=2	1
3:2	R/W	TID1_AC_MAP	AC value as TID=1	1
1:0	R/W	TID0_AC_MAP	AC value as TID=0	0

Note: default according 802.11e Table 20.23—User priority to Access Category mappings

TX_PWR_CFG_0 (offset: 0x1314, default: 0x6666_6666)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_OFDM_12	TX power for OFDM 12M/18M	0x66
23:16	R/W	TX_PWR_OFDM_6	TX power for OFDM 6M/9M	0x66
15:8	R/W	TX_PWR_CCK_5	TX power for CCK5.5M/11M	0x66
7:0	R/W	TX_PWR_CCK_1	TX power for CCK1M/2M	0x66

TX_PWR_CFG_1 (offset: 0x1318)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_MCS_2	TX power for HT MCS=2,3	0x66
23:16	R/W	TX_PWR_MCS_0	TX power for HT MCS=0,1	0x66
15:8	R/W	TX_PWR_OFDM_48	TX power for OFDM 48M/54M	0x66
7:0	R/W	TX_PWR_OFDM_24	TX power for OFDM 24M/36M	0x66

TX_PWR_CFG_2 (offset: 0x131C)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_MCS_10	TX power for HT MCS=10,11	0x66

23:16	R/W	TX_PWR_MCS_8	TX power for HT MCS=8,9	0x66
15:8	R/W	TX_PWR_MCS_6	TX power for HT MCS=6,7	0x66
7:0	R/W	TX_PWR_MCS_4	TX power for HT MCS=4,5	0x66

TX_PWR_CFG_3 (offset: 0x1320)

Bits	Type	Name	Description	Initial value
31:24	R/W	-	Reserved	0x66
23:16	R/W	-	Reserved	0x66
15:8	R/W	TX_PWR_MCS_14	TX power for HT MCS=14,15	0x66
7:0	R/W	TX_PWR_MCS_12	TX power for HT MCS=12,13	0x66

TX_PWR_CFG_4 (offset: 0x1324)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:8	R/W	-	Reserved	0x66
7:0	R/W	-	Reserved	0x66

TX_PIN_CFG (offset: 0x1328)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	R/W	TRSW_POL	TRSW_EN polarity	0
18	R/W	TRSW_EN	TRSW_EN enable	1
17	R/W	RFTR_POL	RF_TR polarity	0
16	R/W	RFTR_EN	RF_TR enable	1
15	R/W	LNA_PE_G1_POL	LNA_PE_G1 polarity	0
14	R/W	LNA_PE_A1_POL	LNA_PE_A1 polarity	0
13	R/W	LNA_PE_G0_POL	LNA_PE_G0 polarity	0
12	R/W	LNA_PE_A0_POL	LNA_PE_A0 polarity	0
11	R/W	LNA_PE_G1_EN	LNA_PE_G1 enable	1
10	R/W	LNA_PE_A1_EN	LNA_PE_A1 enable	1
9	R/W	LNA_PE_G0_EN	LNA_PE_G0 enable	1
8	R/W	LNA_PE_A0_EN	LNA_PE_A0 enable	1
7	R/W	PA_PE_G1_POL	PA_PE_G1 polarity	0
6	R/W	PA_PE_A1_POL	PA_PE_A1 polarity	0
5	R/W	PA_PE_G0_POL	PA_PE_G0 polarity	0
4	R/W	PA_PE_A0_POL	PA_PE_A0 polarity	0
3	R/W	PA_PE_G1_EN	PA_PE_G1 enable	1
2	R/W	PA_PE_A1_EN	PA_PE_A1 enable	1
1	R/W	PA_PE_G0_EN	PA_PE_G0 enable	1
0	R/W	PA_PE_A0_EN	PA_PE_A0 enable	1

TX_BAND_CFG (offset: 0x132C)

Bits	Type	Name	Description	Initial value
31:3	-	-	Reserved	0
2	R/W	5G_BAND_SEL_N	5G band selection PIN (complement of 5G_BAND_SEL_P)	1
1	R/W	5G_BAND_SEL_P	5G band selection PIN	0
0	R/W	TX_BAND_SEL	0: use lower 40Mhz band in 20Mhz TX 1: use upper 40Mhz band in 20Mhz TX	0

Note1: TX_BAND_SEL is effective only when TX/RX bandwidth control register R4 of BBP is set to 40Mhz.

TX_SW_CFG0 (offset: 0x1330)

Bits	Type	Name	Description	Initial value
31:24	R/W	DLY_RFTR_EN	Delay of RF_TR assertion	0x0
23:16	R/W	DLY_TRSW_EN	Delay of TR_SW assertion	0x4
15:8	R/W	DLY_PAPE_EN	Delay of PA_PE assertion	0x8
7:0	R/W	DLY_TXPE_EN	Delay of TX_PE assertion	0xC

Note1: The timing unit is 0.25us.

Note2: SIFS_TIME should compensate with DLY_TXPE_EN.

TX_SW_CFG1 (offset: 0x1334)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0
23:16	R/W	DLY_RFTR_DIS	Delay of RF_TR de-assertion	0xC
15:8	R/W	DLY_TRSW_DIS	Delay of TR_SW de-assertion	0x8
7:0	R/W	DLY_PAPE_DIS	Delay of PA_PE de-assertion	0x8

Note1: The timing unit is 0.25us.

Note2: The delay is started from TX_END event of BBP.

Note3: TX_PE is de-asserted automatically as last data byte passed to BBP.

TX_SW_CFG2 (offset: 0x1338)

Bits	Type	Name	Description	Initial value
31:24	R/W	DLY_LNA_EN	Delay of LNA* assertion	0x0
23:16	R/W	DLY_LNA_DIS	Delay of LNA* de-assertion	0xC
15:8	R/W	DLY_DAC_EN	Delay of DAC_PE assertion	0x4
7:0	R/W	DLY_DAC_DIS	Delay of DAC_PE de-assertion	0x8

Note1: The timing unit is 0.25us.

Note 2: LNA* includes LNA_A0, LNA_A1, LNA_G0, LNA_G1.

TXOP_THRES_CFG (offset: 0x133C)

Bits	Type	Name	Description	Initial value
31:24	R/W	TXOP_REM_THRES	Remaining TXOP threshold, unit: 32us As the remaining TXOP is less than the threshold, the TXOP is passed silently.	0
23:16	R/W	CF_END_THRES	CF-END threshold, unit: 32us As the remaining TXOP is greater than the threshold, the CF-END will be send to release the remaining TXOP reserved by long NAV. Set 0xFF to disable CF-END transmission.	0
15:8	R/W	RDG_IN_THRES	RX RDG threshold, unit: 32us As the remaining TXOP (specified in the duration field of the RX frame with RDG=1) is greater than or equal to the threshold, the granted reverse direction TXOP may be used.	0
7:0	R/W	RDG_OUT_THRES	TX RDG threshold, unit: 32us As the remaining TXOP is greater than or equal to the threshold, RDG in the TX frame may be set to one.	0

TXOP_CTRL_CFG (offset: 0x1340)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19:16	R/W	EXT_CW_MIN	Cwmin for extension channel backoff When EXT_CCA_EN is enabled, 40Mhz transmission will be suppressed to 20Mhz if the extension CCA is busy or extension channel backoff is not finished. Default: Cwmin=0, disable.	0
15:8	R/W	EXT_CCA_DLY	Extension CCA signal delay time (unit: usec) Create delayed version of extension CCA signal reference time for extension channel IFS. Default: (ofdm SIFS) + (long slot time) = 16 + 20 = 36 (usec)	36
7	R/W	EXT_CCA_EN	Extension CCA reference enable When transmit in 40Mhz mode, defer until extension CCA is also clear. 0: disable 1: enable	0
6	R/W	LSIG_TXOP_EN	L-SIG TXOP protection enable Extension of mix mode L-SIG protection range to following ACK/CTS.	0
5:0	R/W	TXOP_TRUN_EN	TXOP truncation enable Bit5: reserved Bit4: truncation for MIMO power save RTS/CTS Bit3: truncation for user TXOP mode Bit2: truncation for TX rate group change Bit1: truncation for AC change Bit0: TXOP timeout truncation 0: disable 1: enable	0x3F

TX_RTS_CFG (offset: 0x1344)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0
24	R/W	RTS_FBK_EN	RTS rate fallback enable	0
23:8	R/W	RTS_THRES	RTS threshold (unit: byte) MPDU or AMPDU with length greater than RTS threshold will be protected with RTS/CTS exchange at the beginning of the TXOP.	65535
7:0	R/W	RTS_RTY_LIMIT	Auto RTS retry limit	7

TX_TIMEOUT_CFG (offset: 0x1348)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0
23:16	R/W	TXOP_TIMEOUT	TXOP timeout value for TXOP truncation Unit: 1usec	15

			Note: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: For 20us long slot time.	
15:8	R/W	RX_ACK_TIMEOUT	RX ACK/CTS timeout value for TX procedure Unit: 1usec Note: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: For 20us long slot time.	10
7:4	R/W	MPDU_LIFE_TIME	TX MPDU expiration time Expiration time = $2^{(9+MPDU_LIFE_TIME)}$ us Default value is $2^{(9+9)} \approx 256$ ms	9
3:0	-	-	Reserved	0

TX_RTY_CFG (offset: 0x134C)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0
30	R/W	TX_AUTOFB_EN	TX retry PHY rate auto fallback enable 0: disable 1: enable	0
29	R/W	AGG_RTY_MODE	Aggregate MPDU retry mode 0: expired by retry limit 1: expired by MPDU life timer	1
28	R/W	NAG_RTY_MODE	Non-aggregate MPDU retry mode 0: expired by retry limit 1: expired by MPDU life timer	0
27:16	R/W	LONG_RTY_THRES	Long retry threshold MPDU with length over this threshold is applied with long retry limit.	3000
15:8	R/W	LONG_RTY_LIMIT	Long retry limit	4
7:0	R/W	SHORT_RTY_LIMIT	Short retry limit	7

TX_LINK_CFG (offset: 0x1350)

Bits	Type	Name	Description	Initial value
31:24	R	REMOTE_MFS	Remote MCS feedback sequence number	*
23:16	R	REMOTE_MFB	Remote MCS feedback	0x7F
15:13	-	-	Reserved	0
12	R/W	TX_CFACK_EN	Piggyback CF-ACK enable 0: disable 1: enable	0
11	R/W	TX_RDG_EN	RDG TX enable 0: disable 1: enable	0
10	R/W	TX_MRQ_EN	MCS request TX enable 0: disable 1: enable	0

9	R/W	REMOTE_UMFS_EN	Remote un-solicit MFB enable 0: do not apply remote un-solicit MFB (MFS=7) 1: apply un-solicit MFB	0
8	R/W	TX_MFB_EN	TX apply remote MFB 0: disable 1: enable	0
7:0	R/W	REMOTE_MFB_LITE TIME	Remote MFB life time Unit: 32us	32

HT_FBK_CFG0 (offset: 0x1354)

Bits	Type	Name	Description	Initial value
31:28	R/W	HT_MCS7_FBK	Auto fall back MCS as HT MCS =7	6
27:24	R/W	HT_MCS6_FBK	Auto fall back MCS as HT MCS =6	5
23:20	R/W	HT_MCS5_FBK	Auto fall back MCS as HT MCS =5	4
19:16	R/W	HT_MCS4_FBK	Auto fall back MCS as HT MCS =4	3
15:12	R/W	HT_MCS3_FBK	Auto fall back MCS as HT MCS =3	2
11:8	R/W	HT_MCS2_FBK	Auto fall back MCS as HT MCS =2	1
7:4	R/W	HT_MCS1_FBK	Auto fall back MCS as HT MCS =1	0
3:0	R/W	HT_MCS0_FBK	Auto fall back MCS as HT MCS =0	0

HT_FBK_CFG1 (offset: 0x1358)

Bits	Type	Name	Description	Initial value
31:28	R/W	HT_MCS15_FBK	Auto fall back MCS as HT MCS =15	14
27:24	R/W	HT_MCS14_FBK	Auto fall back MCS as HT MCS =14	13
23:20	R/W	HT_MCS13_FBK	Auto fall back MCS as HT MCS =13	12
19:16	R/W	HT_MCS12_FBK	Auto fall back MCS as HT MCS =12	11
15:12	R/W	HT_MCS11_FBK	Auto fall back MCS as HT MCS =11	10
11:8	R/W	HT_MCS10_FBK	Auto fall back MCS as HT MCS =10	9
7:4	R/W	HT_MCS9_FBK	Auto fall back MCS as HT MCS =9	8
3:0	R/W	HT_MCS8_FBK	Auto fall back MCS as HT MCS =8	8

Note1. The MCS is a fallback stopping state, as the fallback MCS is the same as current MCS.

Note2. HT TX PHY rates will not fallback to legacy PHY rates.

LG_FBK_CFG0 (offset: 0x135C)

Bits	Type	Name	Description	Initial value
31:28	R/W	OFDM7_FBK	Auto fall back MCS as previous TX rate is OFDM 54Mbps.	14
27:24	R/W	OFDM6_FBK	Auto fall back MCS as previous TX rate is OFDM 48Mbps.	13
23:20	R/W	OFDM5_FBK	Auto fall back MCS as previous TX rate is OFDM 36Mbps.	12
19:16	R/W	OFDM4_FBK	Auto fall back MCS as previous TX rate is OFDM 24Mbps.	11
15:12	R/W	OFDM3_FBK	Auto fall back MCS as previous TX rate is OFDM 18Mbps.	10
11:8	R/W	OFDM2_FBK	Auto fall back MCS as previous TX rate is OFDM 12Mbps.	9
7:4	R/W	OFDM1_FBK	Auto fall back MCS as previous TX rate is OFDM 9Mbps.	8
3:0	R/W	OFDM0_FBK	Auto fall back MCS as previous TX rate is OFDM 6Mbps.	8

LG_FBK_CFG1 (offset: 0x1360)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:12	R/W	CCK3_FBK	Auto fall back MCS as previous TX rate is CCK 11Mbps.	2

11:8	R/W	CCK2_FBK	Auto fall back MCS as previous TX rate is CCK 5.5Mbps.	1
7:4	R/W	CCK1_FBK	Auto fall back MCS as previous TX rate is CCK 2Mbps.	0
3:0	R/W	CCK0_FBK	Auto fall back MCS as previous TX rate is CCK 1Mbps.	0

Note1. Bit3 of each legacy fallback rate is selection of OFDM/CCK. 0=CCK, 1=OFDM.

CCK_PROT_CFG (offset: 0x1364)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0
26	R/W	CCK_RTSTH_EN	RTS threshold enable on CCK TX 0: disable 1: enable	0
25:20	R/W	CCK_TXOP_ALLO_W	CCK TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	1
19:18	R/W	CCK_PROT_NAV	TXOP protection type for CCK TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	CCK_PROT_CTRL	Protection control frame type for CCK TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	CCK_PROT_RATE	Protection control frame rate for CCK TX (Including RTS/CTS-to-self/CF-END) Default: CCK 11M	0x0003

OFDM_PROT_CFG (offset: 0x1368)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0
26	R/W	OFDM_RTSTH_EN	RTS threshold enable on OFDM TX 0: disable 1: enable	0
25:20	R/W	OFDM_PROT_TX_OP	OFDM TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	2
19:18	R/W	OFDM_PROT_NAV	TXOP protection type for OFDM TX 0: None 1: Short NAV protection	0

			2: Long NAV protection 3: Reserved (None)	
17:16	R/W	OFDM_PROT_CTRL	Protection control frame type for OFDM TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	OFDM_PROT RATE	Protection control frame rate for OFDM TX (Including RTS/CTS-to-self/CF-END) Default: CCK 11M	0x0003

MM20_PROT_CFG (offset: 0x136C)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0
26	R/W	MM20_RTSTH_EN	RTS threshold enable on MM20 TX 0: disable 1: enable	0
25:20	R/W	MM20_PROT_TXOP	MM20 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	4
19:18	R/W	MM20_PROT_NAV	TXOP protection type for MM20 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	MM20_PROT_CTRL	Protection control frame type for MM20 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	MM20_PROT RATE	Protection control frame rate for MM20 TX (Including RTS/CTS-to-self/CF-END) Default: OFDM 24M	0x4004

MM40_PROT_CFG (offset: 0x1370)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0
26	R/W	MM40_RTSTH_EN	RTS threshold enable on MM40 TX 0: disable 1: enable	0
25:20	R/W	MM40_PROT_TXOP	MM40 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX	8

			Bit21: allow OFDM TX Bit20: allow CCK TX	
19:18	R/W	MM40_PROT_NAV	TXOP protection type for MM40 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	MM40_PROT_CTRL	Protection control frame type for MM40 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	MM40_PROT_RATE	Protection control frame rate for MM40 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x4084

GF20_PROT_CFG (offset: 0x1374)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0
26	R/W	GF20_RTSTH_EN	RTS threshold enable on GF20 TX 0: disable 1: enable	0
25:20	R/W	GF20_PROT_TXOP	GF20 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	16
19:18	R/W	GF20_PROT_NAV	TXOP protection type for GF20 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	GF20_PROT_CTRL	Protection control frame type for GF20 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	GF20_PROT RATE	Protection control frame rate for GF20 TX (Including RTS/CTS-to-self/CF-END) Default: OFDM 24M	0x4004

GF40_PROT_CFG (offset: 0x1378)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0
26	R/W	GF40_RTSTH_EN	RTS threshold enable on GF40 TX 0: disable 1: enable	0
25:20	R/W	GF40_PROT_TX	GF40 TXOP allowance	16

		OP	(0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	
19:18	R/W	GF40_PROT_NA V	TXOP protection type for GF40 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	GF40_PROT_CTR L	Protection control frame type for GF40 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	GF40_PROT_RAT E	Protection control frame rate for GF40 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x4084

EXP_CTS_TIME (offset: 0x137C)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0
30:16	R/W	EXP_OFDM_CTS _TIME	Expected time for OFDM CTS response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 6Mbps CTS	56
15	R		Reserved	0
14:0	R/W	EXP_CCK_CTS_TI ME	Expected time for CCK CTS response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 1Mbps CTS	314

EXP_ACK_TIME (offset: 0x1380)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0
30:16	R/W	EXP_OFDM_ACK _TIME	Expected time for OFDM ACK response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 6Mbps ACK preamble	36
15	-	-	Reserved	0
14:0	R/W	EXP_CCK_ACK_TI ME	Expected time for CCK ACK response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 1Mbps ACK preamble	202

3.12.3.5 MAC RX configuration registers (offset: 0x1400)
RX_FILTR_CFG (offset: 0x1400)

Bits	Type	Name	Description	Initial value
31:17	-	-	Reserved	0

16	R/W	DROP_CTRL_RSV	Drop reserve control subtype	1
15	R/W	DROP_BAR	Drop BAR	0
14	R/W	DROP_BA	Drop BA	1
13	R/W	DROP_PSPOLL	Drop PS-Poll	0
12	R/W	DROP RTS	Drop RTS	1
11	R/W	DROP_CTS	Drop CTS	1
10	R/W	DROP_ACK	Drop ACK	1
9	R/W	DROP_CFEND	Drop CF-END	1
8	R/W	DROP_CFACK	Drop CF-END + CF-ACK	1
7	R/W	DROP_DUPL	Drop duplicated frame	1
6	R/W	DROP_BC	Drop broadcast frame	0
5	R/W	DROP_MC	Drop multicast frame	0
4	R/W	DROP_VER_ERR	Drop 802.11 version error frame	1
3	R/W	DROP_NOT_MY_BSS	Drop frame that is not my BSSID	1
2	R/W	DROP_UC_NOME	Drop not to me unicast frame	1
1	R/W	DROP_PHY_ERR	Drop physical error frame	1
0	R/W	DROP_CRC_ERR	Drop CRC error frame	1

Note: 1: enable, 0: disable.

AUTO_RSP_CFG (offset: 0x1404)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0
7	R/W	CTRL_PWR_BIT	Power bit value in control frame	0
6	R/W	BAC_ACK_POLICY	BA frame -> BAC -> Ack policy bit value	0
5	-	-	Reserved	0
4	R/W	CCK_SHORT_EN	CCK short preamble auto response enable 0: disable 1: enable	0
3	R/W	CTS_40M_REF	In duplicate legacy CTS response mode, refer to extension CCA to decide duplicate or not. 0: disable 1: enable	0
2	R/W	CTS_40M_MODE	Duplicate legacy CTS response mode 0: disable 1: enable	0
1	R/W	BAC_ACKPOLICY_EN	BAC ACK policy bit enable 0: disable; don't care this bit 1: enable; no BA auto responding upon reception of BAR with no ACK policy	1
0	R/W	AUTO_RSP_EN	Auto responder enable	1

LEGACY_BASIC_RATE (offset: 0x1408)

Bits	Type	Name	Description	Initial value
31: 12	-	-	Reserved	0

11: 0	R/W	LEGACY_BASIC_RATE	Legacy basic rate bit mask Bit0: 1 Mbps is basic rate Bit1: 2 Mbps is basic rate Bit2: 5.5 Mbps is basic rate Bit3: 11 Mbps is basic rate Bit4: 6 Mbps is basic rate Bit5: 9 Mbps is basic rate Bit6: 12 Mbps is basic rate Bit7: 18 Mbps is basic rate Bit8: 24 Mbps is basic rate Bit9: 36 Mbps is basic rate Bit10: 48 Mbps is basic rate Bit11: 54 Mbps is basic rate 0: disable 1: enable	0
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HT_BASIC_RATE (offset: 0x140C)

Bits	Type	Name	Description	Initial value
31: 16	R/W	-	Reserved	0
15: 0	R/W	HT_BASIC_RATE	HT basic rate for auto responding control frame Bit15 =1, enable MCS feedback	0

HT_CTRL_CFG (offset: 0x1410)

Bits	Type	Name	Description	Initial value
31: 9	-	-	Reserved	0
8: 0	R/W	HT_CTRL_THRES	Remaining TXOP threshold for HT control frame auto responding (unit: us)	256

SIFS_COST_CFG (offset: 0x1414)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:8	R/W	OFDM_SIFS_COST	OFDM SIFS time (unit: 1us) Applied after OFDM TX/RX.	16
7:0	R/W	CCK_SIFS_COST	CCK SIFS time (unit: 1us) Applied after CCK TX/RX.	10

Note: The OFDM_SIFS_COST and CCK_SIFS_COST are used only for duration field calculation. It will not affect the responding timing.

RX_PARSER_CFG (offset: 0x1418)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
0	R/W	NAV_ALL_EN	Set NAV for all received frames 0: disable (unicast to me frame will not set the NAV) 1: enable	0

3.12.3.6 MAC Security Configuration Registers (offset:0x1500)
TX_SEC_CNT0 (offset:0x1500)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_SEC_ERR_CNT	TX SEC packet error count	0

15:0	RC	TX_SEC_CPL_CNT	TX SEC packet complete count	0
RX_SEC_CNT0 (offset:0x1504)				
Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:0	RC	RX_SEC_CPL_CNT	RX SEC packet complete count	0
CCMP_FC_MUTE (offset:0x1508)				
Bits	Type	Name	Description	Initial value
31:16	R/W	HT_CCMP_FC_MUTE	HT rate CCMP FC mute	0xc78f
15:0	R/W	LG_CCMP_FC_MUTE	Legacy rate CCMP FC mute	0xc78f

3.12.3.7 MAC HCCA/PSMP CSR (offset:0x1600)

TXOP_HLDR_ADDR0 (offset:0x1600)

Bits	Type	Name	Description	Initial value
31:24	R/W	TXOP_HOL_3	TXOP holder MAC address byte3	0
23:16	R/W	TXOP_HOL_2	TXOP holder MAC address byte2	0
15:8	R/W	TXOP_HOL_1	TXOP holder MAC address byte1	0
7:0	R/W	TXOP_HOL_0	TXOP holder MAC address byte0	0

TXOP_HLDR_ADDR1 (offset:0x1604)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:8	R/W	TXOP_HOL_5	TXOP holder MAC address byte5	0
7:0	R/W	TXOP_HOL_4	TXOP holder MAC address byte4	0

Note: Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

TXOP_HLDR_ET (offset:0x1608)

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	0
25	R/W	TXOP_ETM1_EN	TXOP holder early termination interrupt enable (Type 1) Upon the reception of QoS data frame from TXOP_HLDR_ADDR (A2) and Queue size (QS) in QOS control field (QC) is equal to zero, "TXOP holder early termination interrupt" will be issue. 0: disable 1: enable	0
24	R/W	TXOP_ETM0_EN	TXOP holder early termination interrupt enable (Type 0) When RX packet is from TXOP holder specified in QOS_CSR0,1 (match with Addr2) and duration value is less than or equal to early termination duration threshold specified below, "TXOP holder early termination" interrupt will be issued after CRC check is ok. Upon the reception of QoS data frame from TXOP_HLDR_ADDR (A2) and Duration (DUR) is less than or equal to early termination duration threshold (TXOP_ETM_THRES), "TXOP holder early termination interrupt" will be issue. 0: disable 1: enable	0
23:16	R/W	TXOP_ETM_THRE	TXOP early termination duration threshold	0

		S	Unit: 1usec	
15:9	-	-	Reserved	0
8	WC	TXOP_ETO_EN	<p>TXOP holder early timeout enable Write 1 to enable early timeout check. (interrupt when timeout)</p> <p>When enabled, hardware will expect CCA event. If hardware didn't sense CCA over the TXOP holder early timeout threshold (TXOP_ETO_THRES), the "TXOP holder early timeout interrupt" will then be issued.</p>	0
7:1	R/W	TXOP_ETO_THRES	<p>TXOP holder early timeout threshold Unit: 1usec</p>	0
0	R/W	PER_RX_RST_EN	Baseband RX_PE per RX reset enable 0: disable, 1: enable	0

Note1: TXOP holder early timeout interrupt (TXOP_ETO_INT) is used by AP for HC purpose.

Note2: TXOP holder early termination interrupt (TXOP_ETM_INT) is used by STA (both AP and non-AP STA) for HC purpose.

QOS_CFPOLL_RA_DW0 (offset:0x160C)

Bits	Type	Name	Description	Initial value
31:24	R	CFPOLL_A1_BYTE3	Byte3 of A1 of received QoS Data (+) CF-Poll frame	X
23:16	R	CFPOLL_A1_BYTE2	Byte2 of A1 of received QoS Data (+) CF-Poll frame	X
15:8	R	CFPOLL_A1_BYTE1	Byte1 of A1 of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_A1_BYTE0	Byte0 of A1 of received QoS Data (+) CF-Poll frame	X

QOS_CFPOLL_A1_DW1 (offset:0x1610)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0
16	R	CFPOLL_A1_TOME	1: QoS CF-Poll to me 0: Qos CF-Poll not to me	X
15:8	R	CFPOLL_A1_BYTE5	Byte5 of A1 of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_A1_BYTE4	Byte4 of A1 of received QoS Data (+) CF-Poll frame	X

QOS_CFPOLL_QC (offset:0x1614)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0
15:8	R	CFPOLL_QC_BYTE1	Byte1 of QC of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_QC_BYTE0	Byte0 of QC of received QoS Data (+) CF-Poll frame	X

Note: CFPOLL_RA_DW0, CFPOLL_RA_DW1, and CFPOLL_QC are updated after the reception of QoS Data (+) CF-Poll frame and RX QoS CF-Poll interrupt (RX_QOS_CFPOLL_INT) is launched then.

3.12.3.8 MAC Statistic Counters (offset:0x1700)

RX_STA_CNT0 (offset:0x1700)

Bits	Type	Name	Description	Initial value
31:16	RC	PHY_ERRCNT	RX PHY error frame count	0

15:0	RC	CRC_ERRCNT	RX CRC error frame count	0
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Note1: RX PHY error means PSDU length is shorter than indicated by PLCP.

Note2: RX PHY error is also treated as CRC error.

RX_STA_CNT1 (offset:0x1704)

Bits	Type	Name	Description	Initial value
31:16	RC	PLPC_ERRCNT	RX PLCP error count	0
15:0	RC	CCA_ERRCNT	CCA false alarm count	0

Note1: CCA false alarm means there is no PLCP after CCA indication.

Note2: RX PLCP error means there is no PSDU after PLCP indication.

RX_STA_CNT2 (offset:0x1708, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	RX_OVFL_CNT	RX FIFO overflow frame count	0
15:0	RC	RX_DUPL_CNT	RX duplicated filtered frame count	0

Note: MAC will NOT auto respond ACK/BA to the frame originator when frame is lost due to RXFIFO overflow.

However, MAC will respond when frame is duplicated filtered.

TX_STA_CNT0 (offset:0x170C)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_BCN_CNT	TX beacon count	0
15:0	RC	TX_FAIL_CNT	Failed TX count	0

TX_STA_CNT1 (offset:0x1710)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_RTY_CNT	TX retransmission count	0
15:0	RC	TX_SUCC_CNT	Successful TX count	0

TX_STA_CNT2 (offset:0x1714)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_UDFL_CNT	TX underflow count	0
15:0	RC	TX_ZERO_CNT	TX zero length frame count	0

TX_STAT_FIFO (offset:0x1718)

Bits	Type	Name	Description	Initial value
31:16	R	TXQ_RATE	TX success rate	*
15:8	R	TXQ_WCID	TX WCID	*
7	R	TXQ_ACKREQ	TX acknowledge required 0: not required 1: required	*
6	R	TXQ_AGG	TX aggregate 0: non-aggregated 1: aggregated	*
5	R	TXQ_OK	TX success 0: failed 1: success	*
4:1	R	TXQ_PID	TX Packet ID (Latched from TXWI)	*
0	RC	TXQ_VLD	TX status queue valid 0: queue empty, 1: valid	0

Note: TX status FIFO size = 16.

TX_NAG_AGG_CNT (offset:0x171C)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_CNT	Aggregate TX count	0
15:0	RC	TX_NAG_CNT	Non-aggregate TX count	0

TX_AGG_CNT0 (offset:0x1720)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_2_CNT	Aggregate Size = 2 MPDU count	0
15:0	RC	TX_AGG_1_CNT	Aggregate Size = 1 MPDU count	0

TX_AGG_CNT1 (offset:0x1724)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_4_CNT	Aggregate Size = 4 MPDU count	0
15:0	RC	TX_AGG_3_CNT	Aggregate Size = 3 MPDU count	0

TX_AGG_CNT2 (offset:0x1728)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_6_CNT	Aggregate Size = 6 MPDU count	0
15:0	RC	TX_AGG_5_CNT	Aggregate Size = 5 MPDU count	0

TX_AGG_CNT3 (offset:0x172C)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_8_CNT	Aggregate Size = 8 MPDU count	0
15:0	RC	TX_AGG_7_CNT	Aggregate Size = 7 MPDU count	0

TX_AGG_CNT4 (offset:0x1730, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_10_CNT	Aggregate Size = 10 MPDU count	0
15:0	RC	TX_AGG_9_CNT	Aggregate Size = 9 MPDU count	0

TX_AGG_CNT5 (offset:0x1734)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_12_CNT	Aggregate Size = 12 MPDU count	0
15:0	RC	TX_AGG_11_CNT	Aggregate Size = 11 MPDU count	0

TX_AGG_CNT6 (offset:0x1738, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_14_CNT	Aggregate Size = 14 MPDU count	0
15:0	RC	TX_AGG_13_CNT	Aggregate Size = 13 MPDU count	0

TX_AGG_CNT7 (offset:0x173C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_16_CNT	Aggregate Size > 16 MPDU count	0
15:0	RC	TX_AGG_15_CNT	Aggregate Size = 15 MPDU count	0

MPDU_DENSITY_CNT (offset:0x1740, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	RX_ZERO_DEL_CNT	RX zero length delimiter count	0
15:0	RC	TX_ZERO_DEL_CNT	TX zero length delimiter count	0

3.12.3.9 MAC search table (base: 1018.0000, offset: 0x1800)
RX WCID search entry format (8 bytes)

Offset	Type	Name	Description	Initial value
0x00	R/W	WC_MAC_AD	Client MAC address byte0	0x00

		DR0		
0x01	R/W	WC_MAC_AD DR1	Client MAC address byte1	0x00
0x02	R/W	WC_MAC_AD DR2	Client MAC address byte2	0x00
0x03	R/W	WC_MAC_AD DR3	Client MAC address byte3	0x00
0x04	R/W	WC_MAC_AD DR4	Client MAC address byte4	0x00
0x05	R/W	WC_MAC_AD DR5	Client MAC address byte5	0x00
0x06	R/W	BA_SESS_MAS K0	BA session mask (lower) Bit0 for TID0 Bit7 for TID7	0x00
0x07	R/W	BA_SESS_MAS K1	BA session mask (upper) Bit8 for TID8 Bit15 for TID15	0x00

RX WCID search table (offset:0x1800)

Offset	Type	Name	Description	Initial value
0x1800	R/W	WC_ENTRY_0	WC MAC address with WCID=0	0
0x1808	R/W	WC_ENTRY_1	WC MAC address with WCID=1	0
....	R/W	WC MAC address with WCID=2~253	0
0x1FF0	R/W	WC_ENTRY_254	WC MAC address with WCID=254	0
0x1FF8	R/W	WC_ENTRY_255	Reserved (shall not be used)	0

Note1: WCID=Wireless Client ID

3.12.4 Security table/CIS/Beacon/NULL frame (base : 1018.0000, offset: 0x4000)

3.12.4.1 Security Key Format (8DW)

Offset	Type	Name	Description	Initial value
0x00	R/W	SECKEY_DW0	Security key byte3~0	*
0x04	R/W	SECKEY_DW1	Security key byte7~4	*
0x08	R/W	SECKEY_DW2	Security key byte11~8	*
0x0C	R/W	SECKEY_DW3	Security key byte15~12	*
0x10	R/W	TXMIC_DW0	TX MIC key byte3~0	*
0x14	R/W	TXMIC_DW1	TX MIC key byte7~4	*
0x18	R/W	RXMIC_DW0	RX MIC key byte3~0	*
0x1C	R/W	RXMIC_DW1	RX MIC key byte7~4	*

Note:

1. For WEP40, CKIP40, only byte4~0 of security key are valid.
2. For WEP104, CKIP104, only byte12~0 of security key are valid.
3. For TKIP, AES, all the bytes of security key are valid.
4. TX/RX MIC key is used only for TKIP MIC calculation.

3.12.4.2 IV/EIV format (2 DW)

When TXINFO.WIV=0, hardware will auto lookup IV/EIV from this table and update IV/EIV after encryption is finished.

Offset	Type	Name	Description	Initial value
0x00	R/W	IV_FIELED	IV field	*
0x04	R/W	EIV_FIELED	EIV field	*

Note1: The key index and extension IV bit shall be initialized by software. The MSB octet of IV will not be modified by hardware.

Note2: IV/EIV packet number (PN) counter modes:

- a. For WEP40, WEP104, CKIP40, CKIP104, CKIP128 mode, PN=IV[23:0]. EIV[31:0] is not used.
- b. For TKIP mode, PN = {EIV[31:0], IV[7:0], IV[23:16]}, IV[15:8]=(IV[7:0] | 0x20) & 0x7f) is generated by hardware.
- c. For AES-CCMP, PN = {EIV[31:0], IV[15:0]}.
- d. PN = PN + 1 after each encryption.

Note3: Software may initialize the PN counter to any value.

3.12.4.3 WCID attribute entry format (1DW)

Offset	Type	Name	Description	Initial value
31:10	-	-	Reserved	*
9:7	R/W	RXWI_UDF	RXWI user define field This field is tagged in the RXWI.UDF fields for the WCID.	*
6:4	R/W	BSS_IDX	Multiple-BSS index for the WCID	*
3:1	R/W	RX_PKEY_MODE	Pair-wise key security mode 0: No security 1: WEP40 2: WEP104 3: TKIP 4: AES-CCMP 5: CKIP40 6: CKIP104 7: CKIP128	*
0	R/W	RX_PKEY_EN	Key table selection 0: shared key table 1: pair-wise key table	*

3.12.4.4 Share key mode entry format (1DW)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	*
30:28	R/W	SKEY_MODE_7+	Shared key7+(8x) mode, x=0~3	*
27	-	-	Reserved	*
26:24	R/W	SKEY_MODE_6+	Shared key6+(8x) mode, x=0~3	*
23	-	-	Reserved	*
22:20	R/W	SKEY_MODE_5+	Shared key5+(8x) mode, x=0~3	*

19	-	-	Reserved	*
18:16	R/W	SKEY_MODE_4+	Shared key4+(8x) mode, x=0~3	*
15	-	-	Reserved	*
14:12	R/W	SKEY_MODE_3+	Shared key3+(8x) mode, x=0~3	*
11	-	-	Reserved	*
10:8	R/W	SKEY_MODE_2+	Shared key2+(8x) mode, x=0~3	*
7	-	-	Reserved	*
6:4	R/W	SKEY_MODE_1+	Shared key1+(8x) mode, x=0~3	*
3	-	-	Reserved	*
2:0	R/W	SKEY_MODE_0+	Shared key0+(8x) mode, x=0~3	*

Key mode definition:

- 0: No security
- 1: WEP40
- 2: WEP104
- 3: TKIP
- 4: AES-CCMP
- 5: CKIP40
- 6: CKIP104
- 7: CKIP128

3.12.4.5 Security Table

Pair-wise key table (offset:0x4000)

Offset	Type	Name	Description	Initial value
0x4000	R/W	PKEY_0	Pair-wise key for WCID0	*
0x4020	R/W	PKEY_1	Pair-wise key for WCID1	*
....	R/W	Pair-wise key for WCID2~253	*
0x5FC0	R/W	PKEY_254	Pair-wise key for WCID254	*
0x5FE0	R/W	PKEY_255	Pair-wise key for WCID255 (not used)	*

IV/EIV table (offset:0x6000)

Offset	Type	Name	Description	Initial value
0x6000	R/W	IVEIV_0	IV/EIV for WCID0	*
0x6008	R/W	IVEIV_1	IV/EIV for WCID1	*
....	R/W	IV/EIV for WCID2~253	*
0x67F0	R/W	IVEIV_254	IV/EIV for WCID254	*
0x67F8	R/W	IVEIV_255	IV/EIV for WCID255 (not used)	*

WCID attribute table (offset:0x6800)

Offset	Type	Name	Description	Initial value
0x6800	R/W	WCID_ATTR_0	WCID Attribute for WCID0	*
0x6804	R/W	WCID_ATTR_1	WCID Attribute for WCID1	*
....	R/W	WCID Attribute for WCID2~253	*
0x6BF8	R/W	WCID_ATTR_254	WCID Attribute for WCID254	*

0x6BFC	R/W	WCID_ATTR_255	WCID Attribute for WCID255	*
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Shared Key Table (offset:0x6C00)

Offset	Type	Name	Description	Initial value
0x6C00	R/W	SKEY_0	Shared key for BSS_IDX=0, KEY_IDX=0	*
0x6C20	R/W	SKEY_1	Shared key for BSS_IDX=0, KEY_IDX=1	*
0x6C40	R/W	SKEY_2	Shared key for BSS_IDX=0, KEY_IDX=2	*
0x6C60	R/W	SKEY_3	Shared key for BSS_IDX=0, KEY_IDX=3	*
0x6C80	R/W	SKEY_4	Shared key for BSS_IDX=1, KEY_IDX=0	*
0x6CA0	R/W	SKEY_5	Shared key for BSS_IDX=1, KEY_IDX=1	*
0x6CC0	R/W	SKEY_6	Shared key for BSS_IDX=1, KEY_IDX=2	*
0x6CE0	R/W	SKEY_7	Shared key for BSS_IDX=1, KEY_IDX=3	*
0x6D00	R/W	SKEY_8	Shared key for BSS_IDX=2, KEY_IDX=0	*
0x6D20	R/W	SKEY_9	Shared key for BSS_IDX=2, KEY_IDX=1	*
0x6D40	R/W	SKEY_10	Shared key for BSS_IDX=2, KEY_IDX=2	*
0x6D60	R/W	SKEY_11	Shared key for BSS_IDX=2, KEY_IDX=3	*
0x6D80	R/W	SKEY_12	Shared key for BSS_IDX=3, KEY_IDX=0	*
0x6DA0	R/W	SKEY_13	Shared key for BSS_IDX=3, KEY_IDX=1	*
0x6DC0	R/W	SKEY_14	Shared key for BSS_IDX=3, KEY_IDX=2	*
0x6DE0	R/W	SKEY_15	Shared key for BSS_IDX=3, KEY_IDX=3	*
0x6E00	R/W	SKEY_16	Shared key for BSS_IDX=4, KEY_IDX=0	*
0x6E20	R/W	SKEY_17	Shared key for BSS_IDX=4, KEY_IDX=1	*
0x6E40	R/W	SKEY_18	Shared key for BSS_IDX=4, KEY_IDX=2	*
0x6E60	R/W	SKEY_19	Shared key for BSS_IDX=4, KEY_IDX=3	*
0x6E80	R/W	SKEY_20	Shared key for BSS_IDX=5, KEY_IDX=0	*
0x6EA0	R/W	SKEY_21	Shared key for BSS_IDX=5, KEY_IDX=1	*
0x6EC0	R/W	SKEY_22	Shared key for BSS_IDX=5, KEY_IDX=2	*
0x6EE0	R/W	SKEY_23	Shared key for BSS_IDX=5, KEY_IDX=3	*
0x6F00	R/W	SKEY_24	Shared key for BSS_IDX=6, KEY_IDX=0	*
0x6F20	R/W	SKEY_25	Shared key for BSS_IDX=6, KEY_IDX=1	*
0x6F40	R/W	SKEY_26	Shared key for BSS_IDX=6, KEY_IDX=2	*
0x6F60	R/W	SKEY_27	Shared key for BSS_IDX=6, KEY_IDX=3	*
0x6F80	R/W	SKEY_28	Shared key for BSS_IDX=7, KEY_IDX=0	*
0x6FA0	R/W	SKEY_29	Shared key for BSS_IDX=7, KEY_IDX=1	*
0x6FC0	R/W	SKEY_30	Shared key for BSS_IDX=7, KEY_IDX=2	*
0x6FE0	R/W	SKEY_31	Shared key for BSS_IDX=7, KEY_IDX=3	*

Shared Key Mode (offset:0x7000)

Offset	Type	Name	Description	Initial value
0x7000	R/W	SKEY_MODE_0_7	Shared mode for SKEY0-SKEY7	*
0x7004	R/W	SKEY_MODE_8_15	Shared mode for SKEY8-SKEY15	*
0x7008	R/W	SKEY_MODE_16_23	Shared mode for SKEY16-SKEY23	*
0x700C	R/W	SKEY_MODE_24_31	Shared mode for SKEY24-SKEY31	*

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3.12.5 Descriptor and Wireless information

3.12.5.1 TX frame information

To transmit a frame, the driver needs to prepare the TX frame information for hardware. The TX frame information contains the transmission control, the header, and the payload. The transmission control information (the “**TXWI**”) is used by the MAC and BBP and is applied for the associated TX frame when transmission. The header and payload is the content of an 802.11 packet.

The TX information could be scattered in several segments. The TX descriptor (the “**TXD**”) specifies the location and length of the TX frame information segment. TX frame information could be linked by use of several TXD. These TXD are arranged in a TXD ring in serial. Below diagram illustrates the linking between TXD and TX frame information.

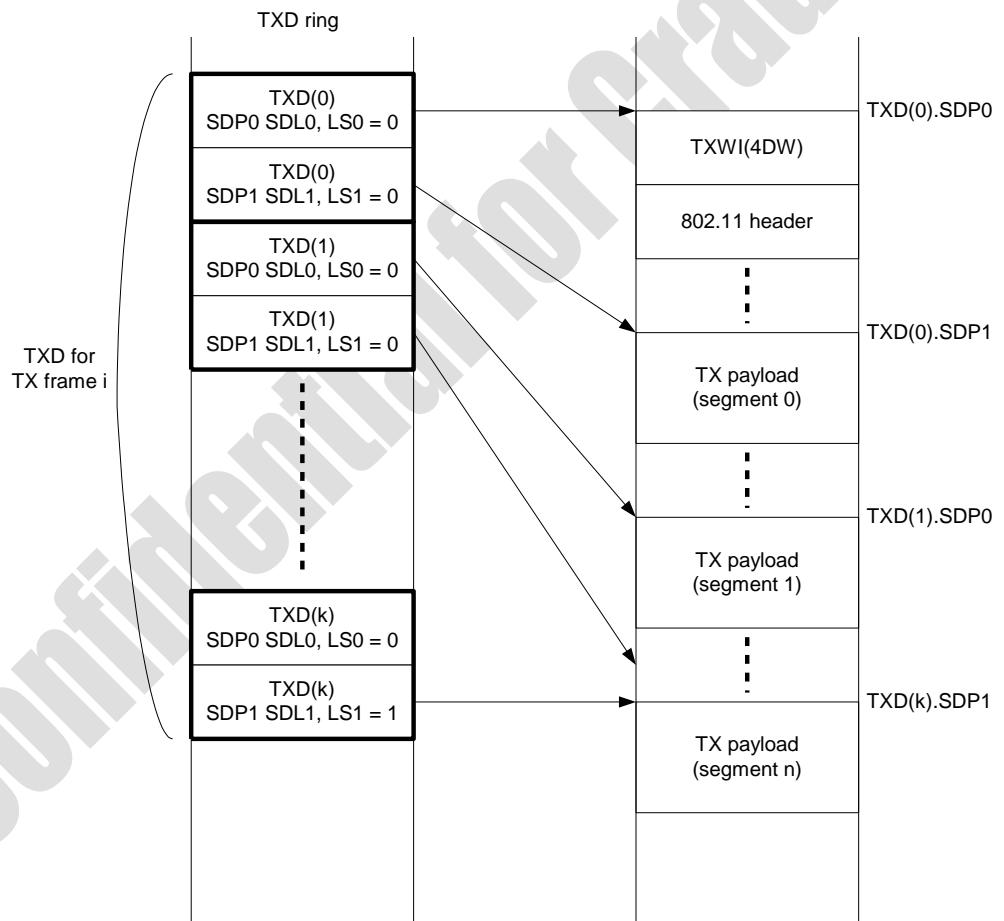


Fig. 3-21-3 TX frame information

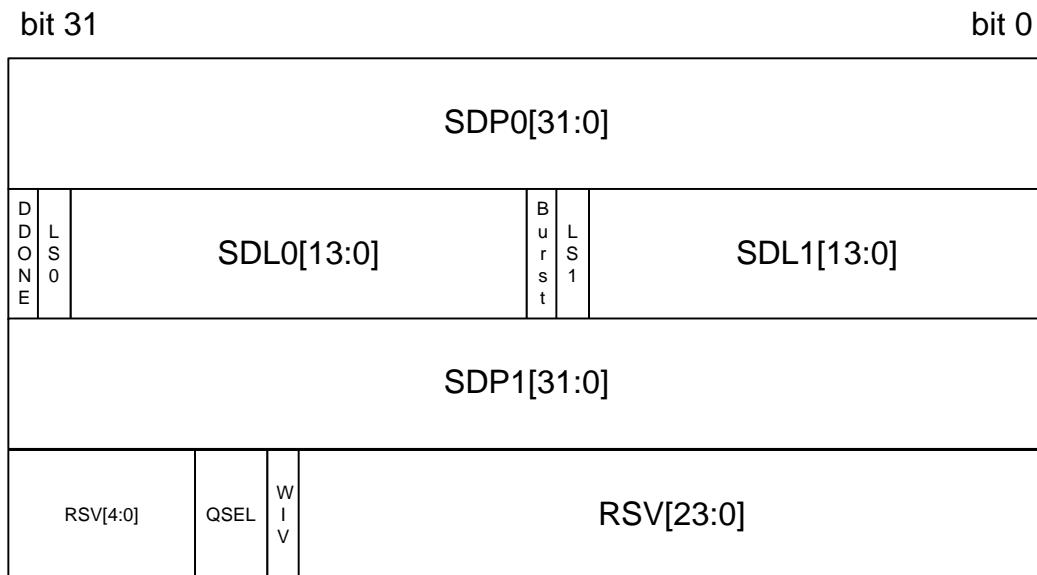
3.12.5.2 TX descriptor format


Fig. 3-21-4 TX descriptor format

- ◆ **SDP0** : Segment Data Pointer 0.
- ◆ **SDL0** : Segment Data Length for the data pointed by SDP0.
- ◆ **SDP1** : Segment Data Pointer 1.
- ◆ **SDL1** : Segment Data Length for the data pointed by SDP1.
- ◆ **LS0** : data pointed by SDP0 is the last segment
- ◆ **LS1** : data pointed by SDP1 is the last segment
- ◆ **DDONE** : DMA Done. DMA has transferred the segments pointed by this TX descriptor
- ◆ **Burst**: force DMA to access next TX frame from the same queue.
- ◆ **QSEL**: the ID of the on-chip queue that the TX frame is moved into. 0: MGMT queue, 1: HCCA queue, 2: EDCA queue, 3: unused.
- ◆ **WIV**: 1: driver prepared all 16-byte TXWI. 0: driver prepared only the first 8-byte TXWI.

3.12.5.3 TXWI format

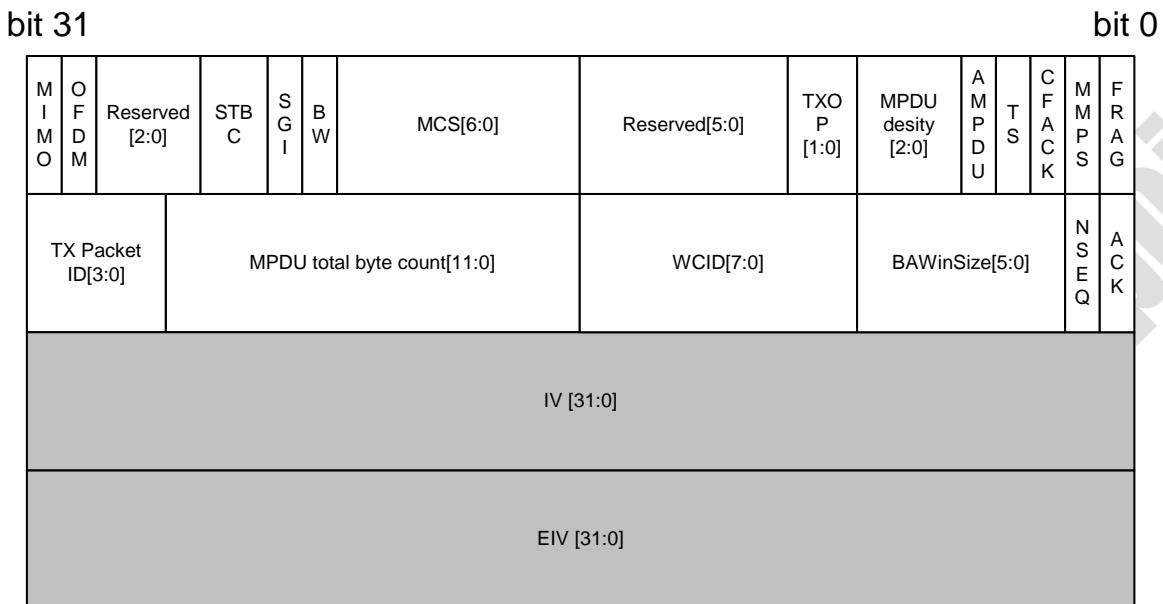


Fig. 3-17-5 TXWI format

- ◆ **FRAG:** 1: to inform TKIP engine this is a fragment, so that TKIP MIC is appended by driver at the last fragment; hardware TKIP engine only need to insert IV/EIV and ICV.
- ◆ **MMPS:** 1: the remote peer is in dynamic MIMO-PS mode
- ◆ **CFACK:** 1: if an ACK is required to the same peer as this outgoing DATA frame, then MAC TX will send a single DATA+CFACK frame instead of separate ACK and DATA frames. 0: no piggyback ACK allowed for the RA of this frame.
- ◆ **TS:** 1: This is a BEACON or ProbeResponse frame and MAC needs to auto insert 8-byte timestamp after 802.11 WLAN header.
- ◆ **AMPDU:** this frame is eligible for AMPDU. MAC TX will aggregate subsequent outgoing frames having <same RA, same TID, AMPDU=1> whenever TXOP allows. Even there's only one DATA frame to be sent, as long as the AMPDU bit in TXWI is ON, MAC will still package it as AMPDU with implicit BAR. This adds only 4-byte AMPDU delimiter overhead into the outgoing frame and imply the response frame is a BA instead of ACK. NOTE: driver should set AMPDU=1 only after a BA session is successfully negotiated, because Block ACK is the only way to acknowledge in AMPDU case.
- ◆ **MPDU density:** 1/4usec ~ 16usec per-peer parameter used in outgoing A-MPDU. (This field complies with the "minimum MDPU Starting Spacing" of the A-MPDU parameter field of draft 1.08).
 - 000- no restriction
 - 001- 1/4 μsec
 - 010- 1/2 μsec
 - 011- 1 μsec
 - 100- 2 μsec
 - 101- 4 μsec
 - 110- 8 μsec
 - 111- 16 μsec
- ◆ **TXOP:** TX back off mode. 0: HT TXOP rule; 1: PIFS TX; 2: SIFS (only when previous frame exchange is successful); 3: Back off.
- ◆ **"MCS/BW/ShortGI/OFDM/MIMO":** TX data rate & MIMO parameters for this outgoing frame to be filled into BBP
- ◆ **ACK:** this bit informs MAC to wait for ACK or not after transmission of the frame. Event though QOD DATA frame has ACK policy in its QOS CONTROL field, MAC TX solely depends on

this ACK bit to decide waiting of ACK or not.

- ◆ **NSEQ**: 1: to use the special h/w SEQ number register in MAC block.
- ◆ **BA window size**: tell MAC the maximum number of to-be-BAed frames is allowed of the RA (RA's BA re-ordering buffer size)
- ◆ **WCID (Wireless Client Index)** : lookup result of ADDR1 in the peer table (255=not found). This index is also used to find all the attributes of the wireless peer (e.g. TX rate, TX power, pair-wise KEY, IV, EIV,). This index has consistent meaning in both driver and hardware.
- ◆ **MSDU total byte count**: total length of this frame.
- ◆ **Packet ID**: as a cookie specified by driver and will be latched into the TX result register stack. Driver use this field to identify special frame's TX result.
- ◆ **IV**: used by encryption engine.
- ◆ **EIV**: used by encryption engine.

3.12.5.4 RX descriptor ring

The RX descriptor (the “**RXD**”) specifies the location to place the payload of the received frame (the RX payload) and the associated receiving information (the “**RXWI**”). One RXD serves for one receiving frame. Only SDP0 and SDL0 are useful in the RXD. The RXD is arranged in the RXD ring in serial. The hardware links the RXWI and RX payload in serial and place it to the location specified in SDP0. See below diagram.

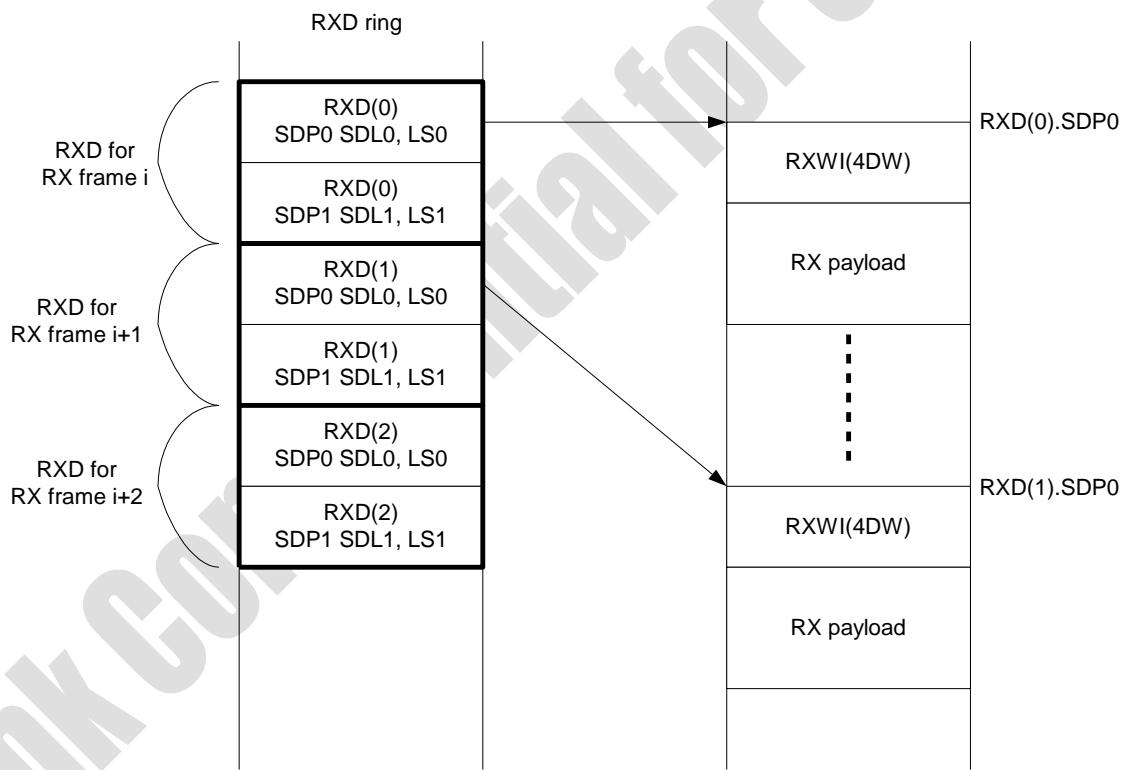


Fig. 3-21-6 RX descriptor ring

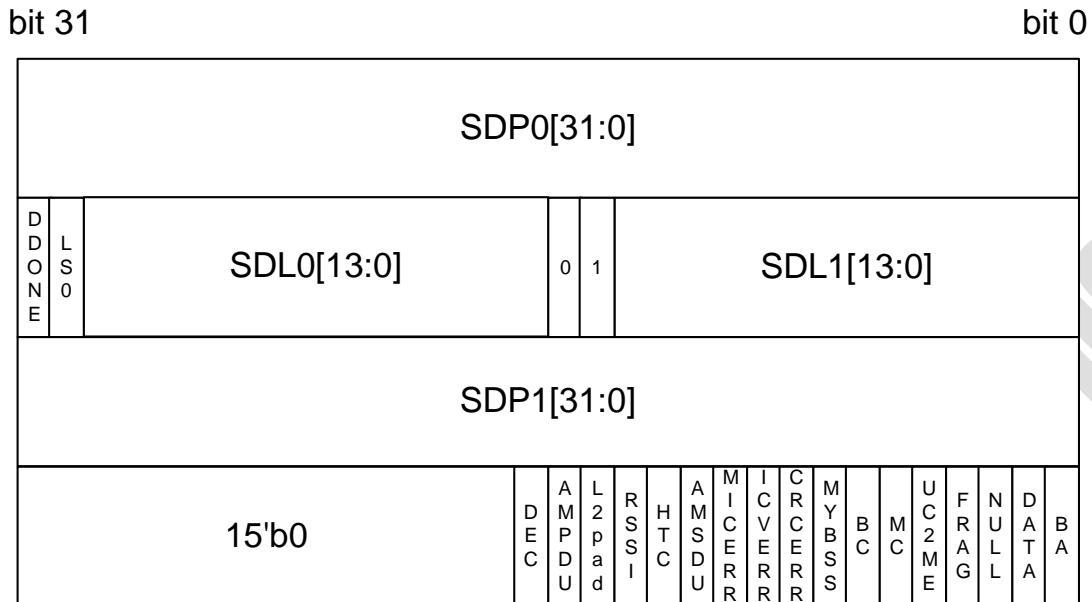
3.12.5.5 RX descriptor format


Fig. 3-21-7 RX descriptor format

Following fields are driver-specified.

- ◆ **SDP0** : Segment Data Pointer 0.
- ◆ **SDL0** : Segment Data Length for the data pointed by SDP0.
- ◆ **SDP1** : Segment Data Pointer 1.
- ◆ **SDL1** : Segment Data Length for the data pointed by SDP1.
- ◆ **DDONE** : DMA Done. DMA has moved the RX frame to the specified location. Set by hardware and cleared by driver.

Following fields are filled by hardware.

- ◆ **BA**: the received frame is part of BA session, need to do re-ordering
- ◆ **DATA**: 1: the received frame is DATA type
- ◆ **NULL**: 1: the received frame has sub-type NULL/QOS-NUL
- ◆ **FRAG**: 1: the receive frame is a fragment
- ◆ **UC2ME**: 1: the received frame ADDR1 = my MAC address
- ◆ **MC**: 1: the received frame ADDR1 = multicast
- ◆ **BC**: 1: the received frame ADDR1 = ff:ff:ff:ff:ff
- ◆ **MyBSS**: 1: the received frame BSSID is one of my BSS (as an AP, max 4 BSSID supported)
- ◆ **CRC error**: 1: the received frame is CRC error
- ◆ **ICV error**: 1: the received frame is ICV error
- ◆ **MIC error**: 1: the received frame is MIC error (RX CNRL register should support individual pass-up error frame to driver in order to implement MIC error detection feature)
- ◆ **AMSDU**: the received frame is in A-MSDU sub frame format which is <802.3 + MSDU + padding>
- ◆ **HTC**: 1: this received frame came with HTC field, 0: no HTC field
- ◆ **RSSI**: 1: RSSI information available in RSSI0, RSSI1, RSSI2 fields
- ◆ **L2Pad**: 1: the L2 header is recognizable and been 2-byte-padded to ensure payload to align at 4-byte boundary. 0: L2 header not extra padded
- ◆ **AMPDU**: 1: this is an AMPDU segregated frame
- ◆ **DEC**: 1: this is a decrypted frame

3.12.5.6 RXWI format

bit 31								bit 0	
TID [3:0]		MPDU total byte count[11:0]				UDF [2:0]	BSS idx [2:0]	Key idx [1:0]	WCID[7:0]
PHY mode [1:0]	RSV [2:0]	STBC [1:0]	S G I	B W	MCS[6:0]	SN[11:0]			FN[3:0]
RSV[7:0]			RSSI_2[7:0]			RSSI_1[7:0]	RSSI_0[7:0]		
RSV[15:0]					SNR_1[7:0]		SNR_0[7:0]		

Fig. 3-21-8 RXWI format

- ◆ **WCID:** index of ADDR2 in the pair wise KEY table. This value uniquely identifies the TA. WCID=255 means not found.
- ◆ **KEY Index:** 0~3 extracted from IV field. For driver reference only, no particular usage so far.
- ◆ **BSSID index:** 0~7 for BSSID0~7. Extract from 802.11 header (the last three bits of BSSID field).
- ◆ **UDF:** User Defined Field.
- ◆ **MPDU total byte count:** the entire MPDU length.
- ◆ **TID:** extracted from 8002.11 QOS control field.
- ◆ **FN:** fragment number of the received MPDU. Extract from 802.11 header.
- ◆ **SN:** sequence number of the received MPDU. Used for BA re-ordering especially that AMSDU are auto segregated by hardware and lost the 802.11 header.
- ◆ **"MCS/BW/SGI/PHYmode":** RX data rate & related MIMO parameters of this frame got from PLCP header. See next section for the detail.
- ◆ **RSSIO, RSSI1, RSSI2:** BBP reported RSSI information of the received frame.
- ◆ **SNR0, SNR1:** BBP reported SNR information of the received frame.

3.12.5.7 Brief PHY rate format and definition

A 16-bit brief PHY rate is used in MAC hardware.

It is the same PHY rate field described in TXWI and RXWI.

Bit	Name	Description
15:14	PHY MODE	Preamble mode 0: Legacy CCK, 1: Legacy OFDM, 2: HT mix mode, 3: HT green field
13:11	-	Reserved
10:9	-	Reserved
8	SGI	Short Guard Interval, only support for HT mode 0: 800ns, 1: 400ns
7	BW	Bandwidth Support both legacy and HT modes 40Mhz in legacy mode means duplicate legacy 0: 20Mhz, 1: 40Mhz

6:0	MCS	Modulation Coding Scheme
-----	-----	--------------------------

Table. Brief PHY rate format

MODE = Legacy CCK	
MCS = 0	Long Preamble CCK 1Mbps
MCS = 1	Long Preamble CCK 2Mbps
MCS = 2	Long Preamble CCK 5.5Mbps
MCS = 3	Long Preamble CCK 11Mbps
MCS = 8	Short Preamble CCK 1Mbps * illegal rate
MCS = 9	Short Preamble CCK 2Mbps
MCS = 10	Short Preamble 5.5Mbps
MCS = 11	Short Preamble 11Mbps
Other MCS codes are reserved in legacy CCK mode.	
BW and SGI are reserved in legacy CCK mode.	
MODE = Legacy OFDM	
MCS = 0	6Mbps
MCS = 1	9Mbps
MCS = 2	12Mbps
MCS = 3	18Mbps
MCS = 4	24Mbps
MCS = 5	36Mbps
MCS = 6	48Mbps
MCS = 7	54Mbps
Other MCS code in legacy CCK mode are reserved	
When BW = 1, duplicate legacy OFDM is sent.	
SGI is reserved in legacy OFDM mode.	
MODE = HT mix mode / HT green field	
MCS = 0 (1S)	(BW=0, SGI=0) 6.5Mbps
MCS = 1	(BW=0, SGI=0) 13Mbps
MCS = 2	(BW=0, SGI=0) 19.5Mbps
MCS = 3	(BW=0, SGI=0) 26Mbps
MCS = 4	(BW=0, SGI=0) 39Mbps
MCS = 5	(BW=0, SGI=0) 52Mbps
MCS = 6	(BW=0, SGI=0) 58.5Mbps
MCS = 7	(BW=0, SGI=0) 65Mbps
MCS = 8 (2S)	(BW=0, SGI=0) 13Mbps
MCS = 9	(BW=0, SGI=0) 26Mbps
MCS = 10	(BW=0, SGI=0) 39Mbps

MCS = 11	(BW=0, SGI=0) 52Mbps
MCS = 12	(BW=0, SGI=0) 78Mbps
MCS = 13	(BW=0, SGI=0) 104Mbps
MCS = 14	(BW=0, SGI=0) 117Mbps
MCS = 15	(BW=0, SGI=0) 130Mbps
MCS = 32	(BW=1, SGI=0) HT duplicate 6Mbps
When BW=1, PHY_RATE = PHY_RATE * 2	
When SGI=1, PHY_RATE = PHY_RATE * 10/9	
The effects of BW and SGI are accumulative.	
When MCS=0~7(1S), SGI option is supported. BW option is supported.	
When MCS=8~15(2S), SGI option is supported. BW option is supported.	
When MCS=32, only SGI option is supported. BW option is not supported. (BW =1)	
Other MCS code in HT mode are reserved	

3.12.5.8 Driver implementation note

3.12.5.8.1 Instruction of down load 8051 firmware

1. Select on-chip program memory
 - i. SYS_CTRL.HST_PM_SEL (0x0400.bit[16]) = 1
2. Write firmware into program memory space, which starts at 0x2000.
3. Close on-chip program memory:
 - i. SYS_CTRL.HST_PM_SEL (0x0400.bit[16]) = 0
4. 8051 starts.

3.12.5.8.2 Instruction of initialize DMA

1. Set base addresses and total number of descriptors:
 - i. TX_BASE_PTR0~TX_BASE_PTR5
 - ii. RX_BASE_PTR
 - iii. TX_MAX_CNT0~TX_MAX_CNT5
 - iv. RX_MAX_CNT
2. Set WMM parameters:
 - i. WMM_AIFSN_CFG
 - ii. WMM_CWMIN_CFG
 - iii. WMM_CWMAX_CFG
 - iv. WMM_TXOP0_CFG and WMM_TXOP1_CFG
3. Set DMA global configuration except TX_DMA_EN and RX_DMA_EN bits:
 - i. WPDMA_GLO_CFG
4. Set interrupt configuration:
 - i. DELAY_INT_CFG
5. Enable DMA interrupt:
 - i. INT_MASK
6. Enable DMA:
 - i. WPDMA_GLO_CFG.TX_DMA_EN = 1, WPDMA_GLO_CFG.RX_DMA_EN = 1

3.12.5.9 Instruction of clock control

3.12.5.9.1 Clock turn-off sequence

1. Switch 80MHz main clock to PLL clock:
 - i. Set SYS_CTRL.CLKSELECT = 1.
2. Turn clock off:
 - i. Set SYS_CTRL.MAC_CLK_EN = 0.
 - ii. Set SYS_CTRL.DMA_CLK_EN = 0.
3. Turn off PLL:
 - i. Set PWR_PIN_CFG.IO_PLL_PD = 1.

3.12.5.9.2 Clock turn-on sequence

1. Turn on PLL:
 - i. Set PWR_PIN_CFG.IO_PLL_PD = 0.
2. Waiting at least \$bbp_pll_ready for PLL clock stable.
3. Turn on clock:
 - i. Set SYS_CTRL.MAC_CLK_EN = 1.
 - ii. Set SYS_CTRL.DMA_CLK_EN = 1.

3.12.5.10 Instruction of TX/RX control

3.12.5.10.1 Freeze TX and RX sequence

1. Disable DMA TX:
 - i. Set WPDMA_GLO_CFG..TX_DMA_EN = 0.

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2. Polling until DMA TX becomes idle and PBF TX queue becomes empty:
 - i. Polling WPDMA_GLO_CFG.TX_DMA_BUSY = 0.
 - ii. Polling TXRXQ_STA.TX0Q_STA = 2, TXRXQ_STA.TX1Q_STA = 2, polling TXRXQ_STA.TX2Q_STA = 2.
 - iii. If the polling period > \$dma_tx_polling_timeout, abort power saving procedure.
3. Disable MAC TX and RX:
 - i. Set MAC_SYS_CTRL.MAC_RX_EN = 0, MAC_SYS_CTRL.MAC_TX_EN = 0.
4. Polling until MAC TX and RX is disabled:
 - i. Polling MAC_STATUS_REG.TX_STATUS = 0, MAC_STATUS_REG.RX_STATUS = 0
 - ii. If the polling period > \$mac_polling_timeout, abort power saving procedure.
5. Disable DMA RX:
 - i. Set WPDMA_GLO_CFG..RX_DMA_EN = 0.
6. Polling until both DMA RX becomes idle and PBF RX queue becomes empty:
 - i. Polling WPDMA_GLO_CFG.RX_DMA_BUSY = 0.
 - ii. Polling TXRXQ_STA.RX0Q_STA = 0x22.
 - iii. If the polling period > \$dma_rx_polling_timeout, abort power saving procedure.

3.12.5.10.2 Recover TX and RX sequence

1. Enable DMA TX and RX:
 - i. Set WPDMA_GLO_CFG..RX_DMA_EN = 1.
 - ii. Set WPDMA_GLO_CFG..TX_DMA_EN = 1.
2. Enable MAC TX and RX:
 - i. Set MAC_SYS_CTRL.MAC_RX_EN = 1.
 - ii. Set MAC_SYS_CTRL.MAC_TX_EN = 1.

3.12.5.11 Instruction of RF power on/off sequence

1. Power down RF components sequence
 - i. Power down RF component
 1. Set PWR_PIN_CFG.IO_ADDA_PD = 1.
 2. Set PWR_PIN_CFG.IO_RF_PE = 0.
 3. Set TX_PIN_CFG.TRSW_EN = 0.
 4. Set TX_PIN_CFG.RFTR_EN = 0.
 5. Set TX_PIN_CFG.LNA_PE*EN = 0.
 6. Set TX_PIN_CFG.PA_PE*EN = 0.
2. Enable RF components sequence
 - i. Recover the registers in previous sequence.
 - ii. Wait \$rf_pll_ready for RF PLL becomes stable.

3.12.5.12 Power saving procedure

1. Freeze TX and RX
2. Power down LED and RF components
3. Clock turn-off

3.12.5.13 Power recovery procedure

1. Clock turn-on
2. Enable LED and RF components
3. Recover TX and RX

3.12.5.14 Parameters

1. \$rf_pll_ready = TBD.
2. \$bbp_pll_ready = 500 us.

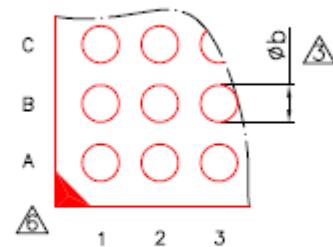
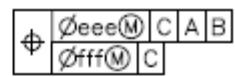
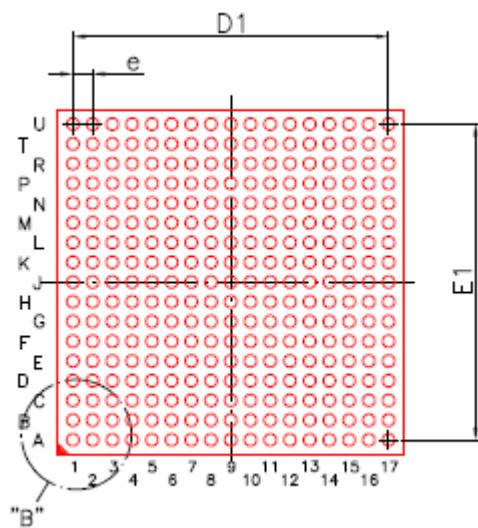
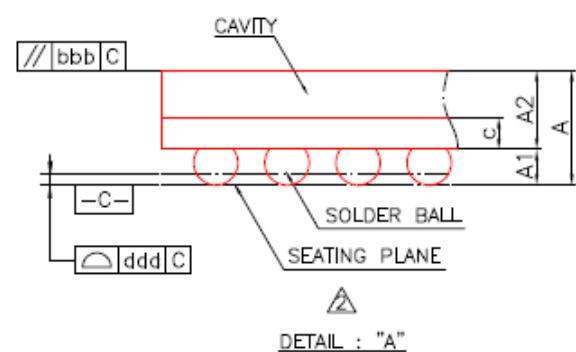
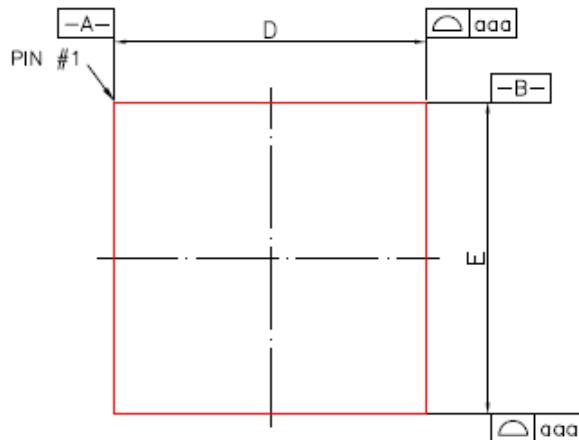
3. \$dma_rx_polling_timeout = TBD.
4. \$dma_tx_polling_timeout = TBD.
5. \$mac_polling_timeout = TBD.

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4. Package Physical Dimension

4.1 TFBGA (14x14x1.4mm)



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.35	0.40	0.45	0.014	0.016	0.018
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
D1	---	12.80	---	---	0.504	---
E1	---	12.80	---	---	0.504	---
e	---	0.80	---	---	0.031	---
b	0.45	0.50	0.55	0.018	0.020	0.022
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.20			0.008		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	17/17			17/17		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2.  PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3.  DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT : JEDEC MO-205.
6.  THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd

5 Revision History

Rev	Date	From	Description
1.0	2010/08/24	James Hu	Initial Release

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