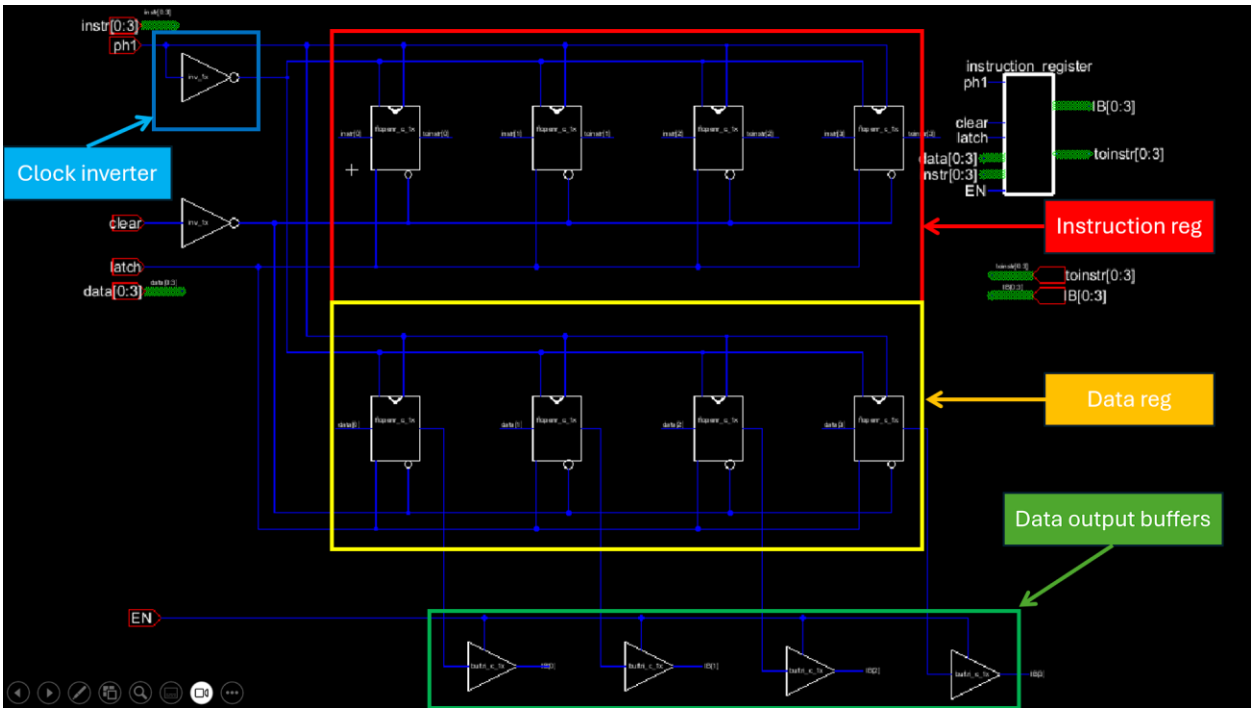
VLSI Final Project – Instruction Register

Matthew Murray – 873525242

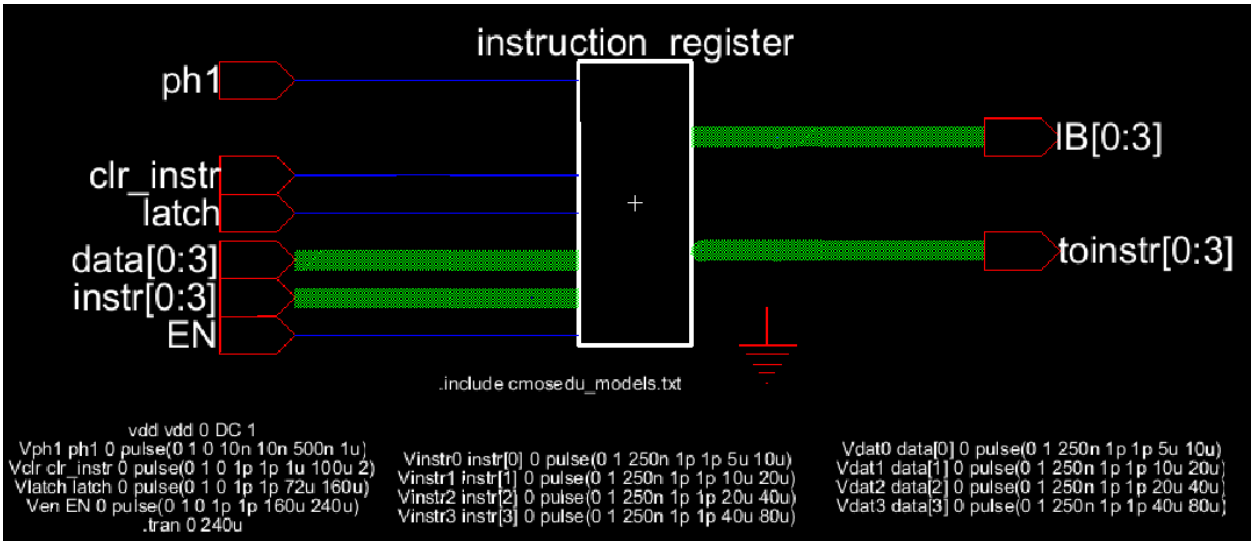
Schematic



The VLSI design mostly matches the reference design with a few exceptions:

- The 2nd clock phase is generated by inverting a single-ended clock input.
- Instead of using clock gating for the latch input, the registers with an enable input were chosen and the latch input was tied to the enables.
- Muddlib offers non-inverting tri-state buffers, so those were used instead of the inverting ones used in the reference design.

Simulation

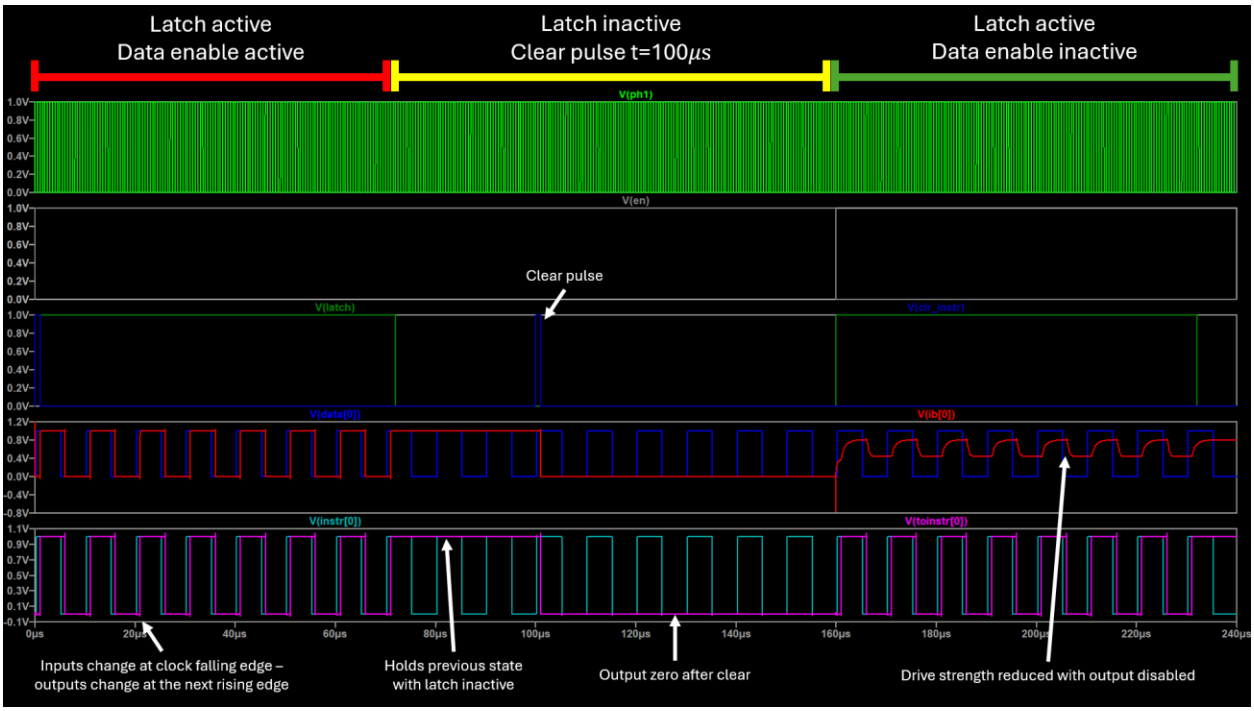


The simulation was done in three phases for 3 different potential modes of operation. During each phase the 4 bit data and 4 bit instruction inputs were cycled through their full 0x0-0xF ranges, although only the LSB is shown in the traces as the other signals are redundant for the purpose of this test. Instr/data inputs change at the falling edge of the clock to be latched on the next rising edge. All registers are initialized to zero with a short clear pulse at the beginning of the simulation.

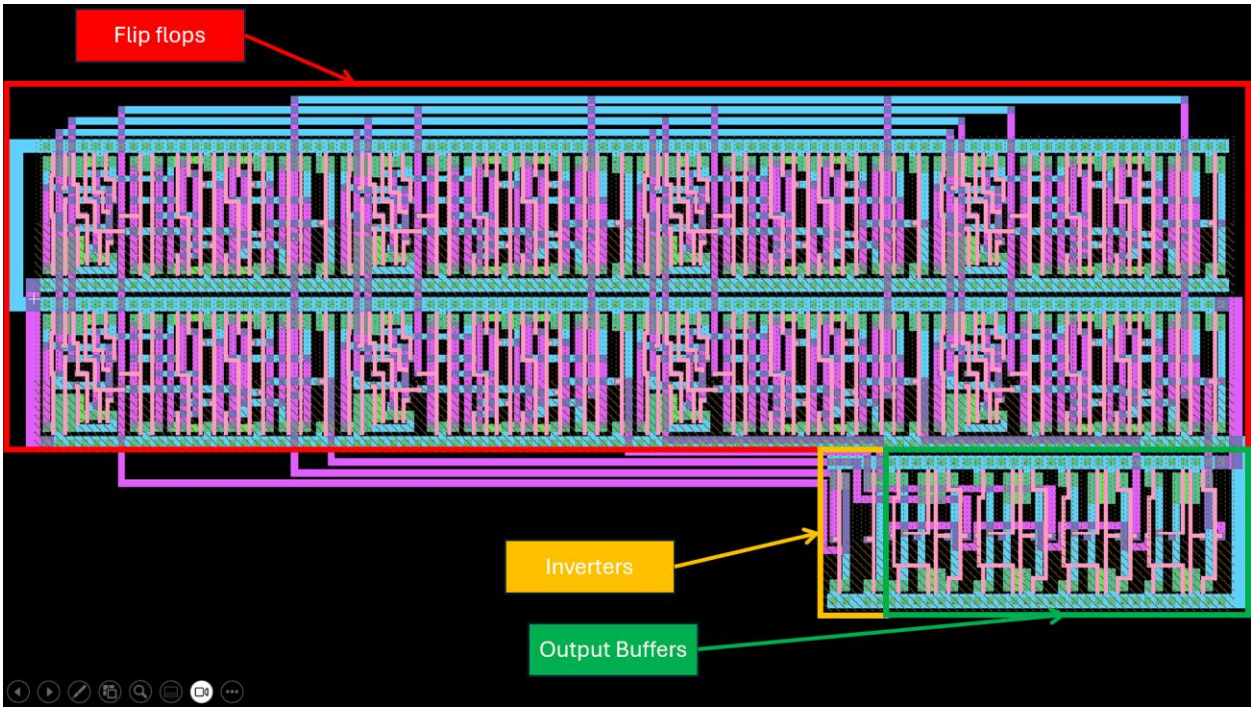
The first phase is “normal operation”. In this phase the latch and enable inputs are both active, and the clear is inactive. In this phase both registers latch the inputs every rising edge of the clock and hold their values on their respective outputs.

In the second phase the latch signal is pulled low, to freeze the state of the registers, then after 20 or so clock cycles, the clear signal is briefly asserted. Because the latch signal is pulled low while the value of both registers is high, the registers hold that value on their outputs regardless of the input. Once the clear signal is pulsed, both registers drop their outputs low.

The last phase is the same as the first but with the enable input inactive. This tri-states the data outputs causing their voltage to stay around 0.5V regardless of the value of the register.



Layout



The layout was designed to be as compact as possible. Most of the space is taken by the flipflops, with the inverters and output buffers at the bottom.