VLSI Lab 5 – Full Adder

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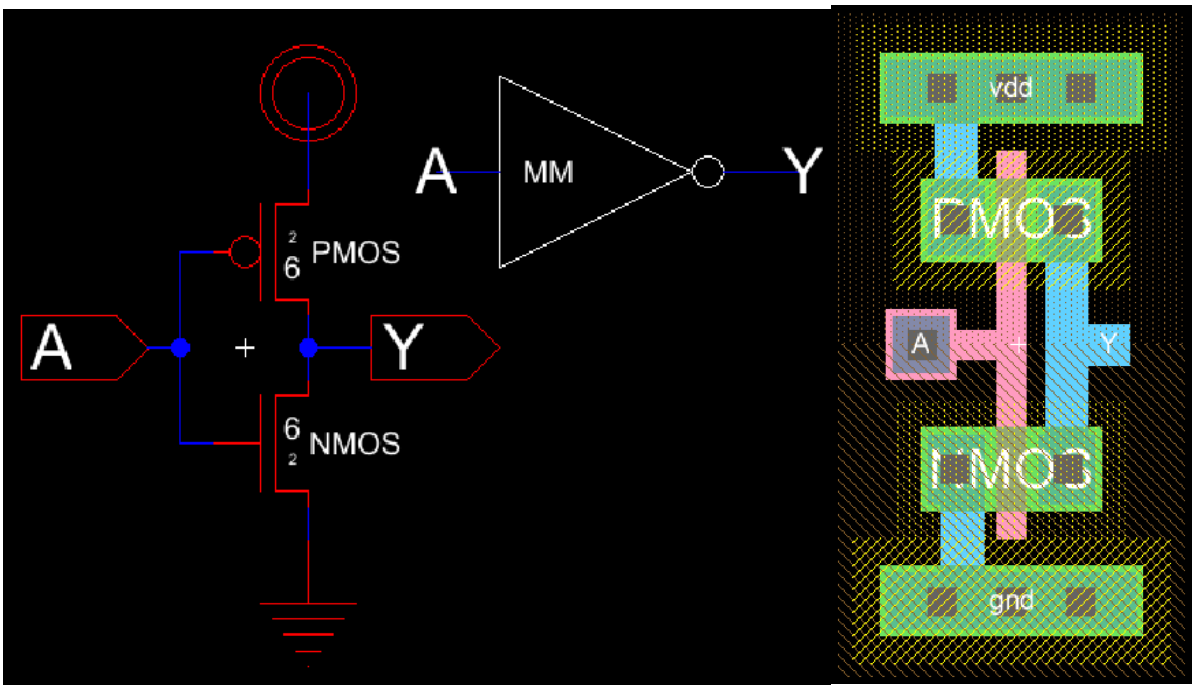
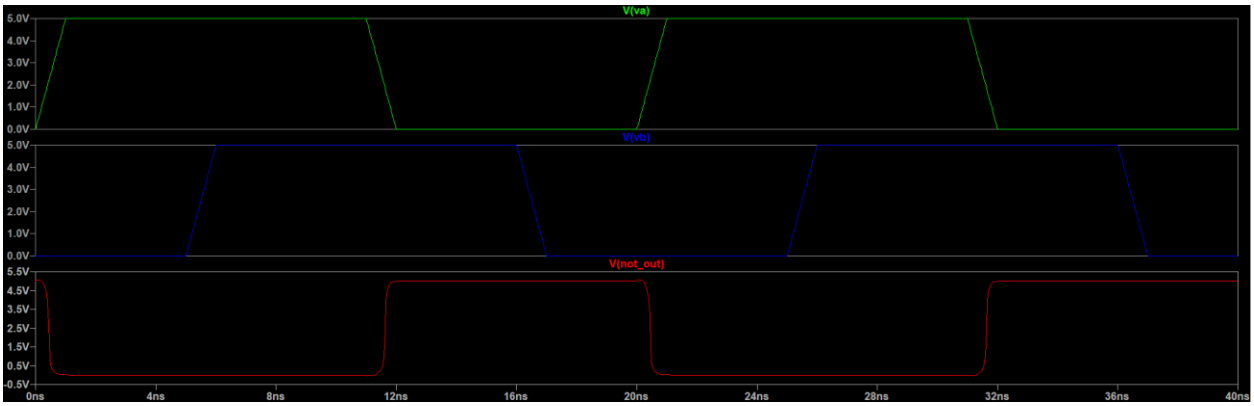
Not

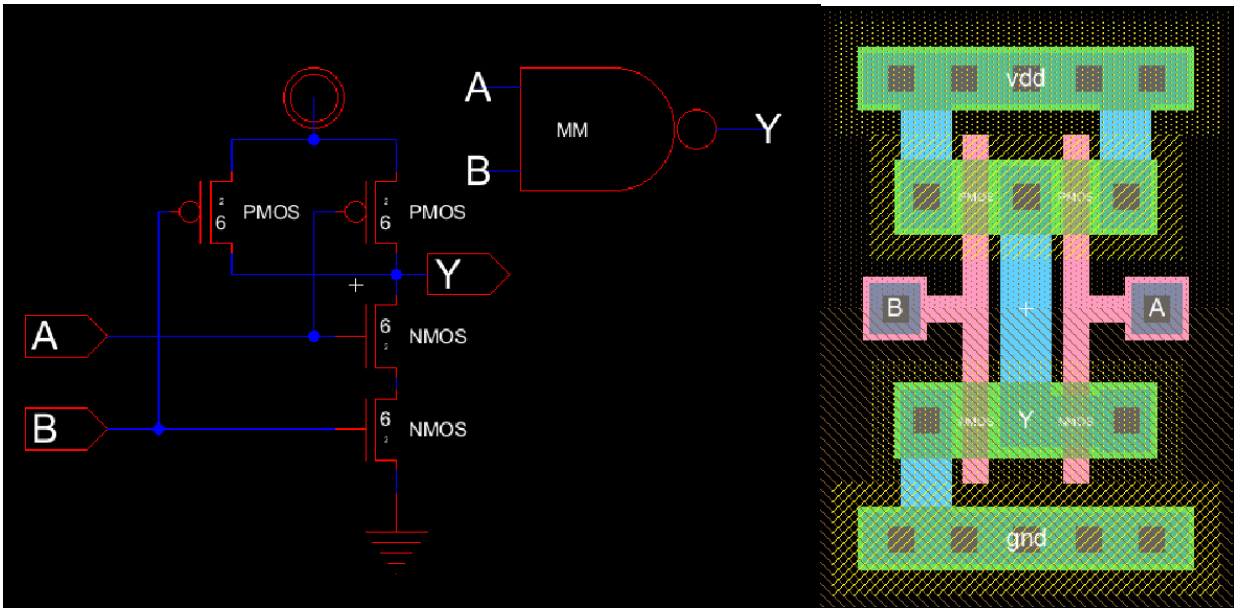


Logic Sim

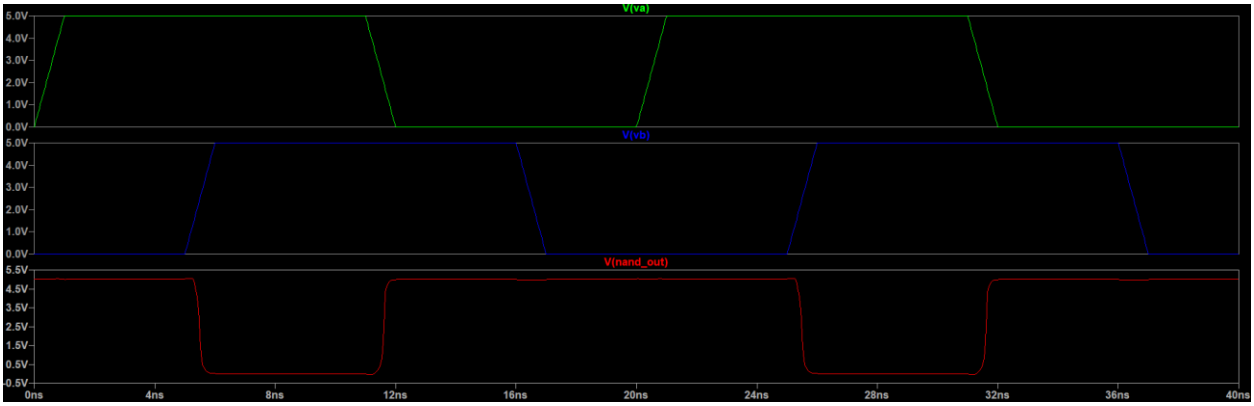


Not_out is high when va is low, and low when va is high.

NAND

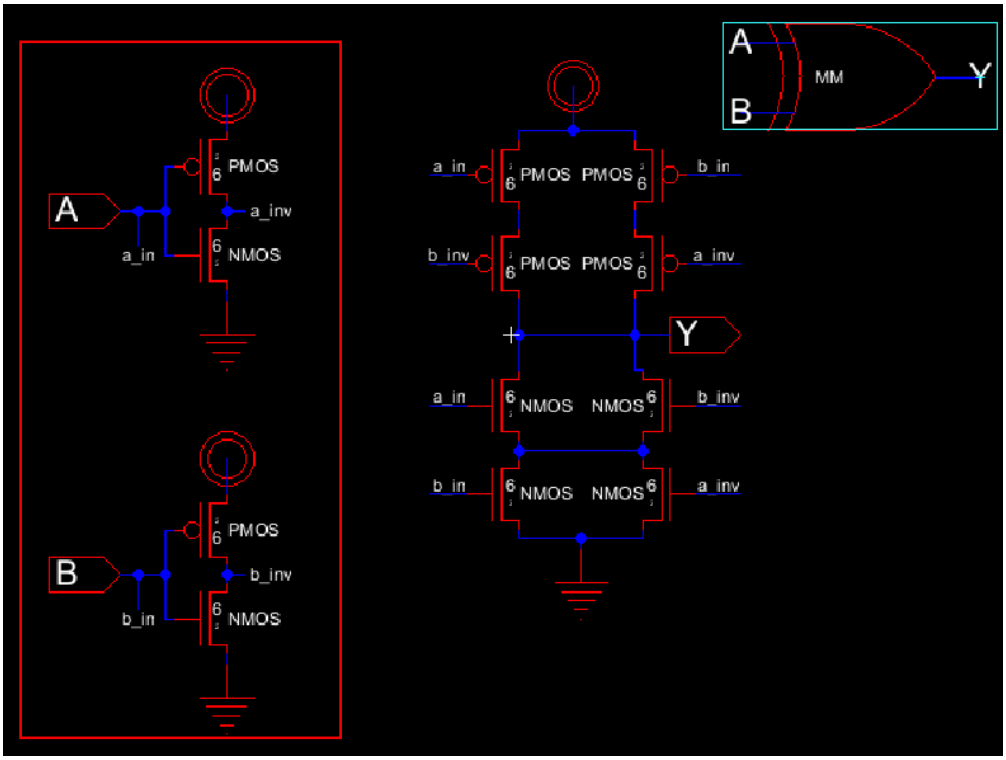


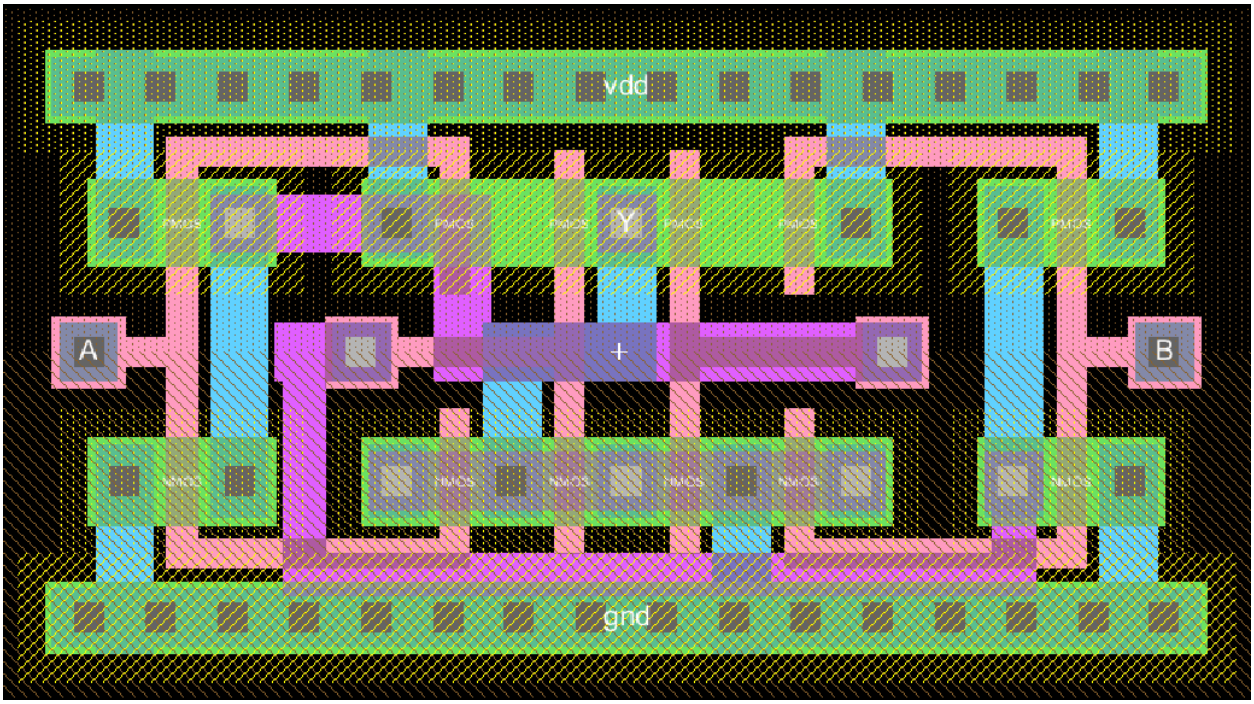
Logic Sim



Nand_out is low when both va and vb are high, and high otherwise.

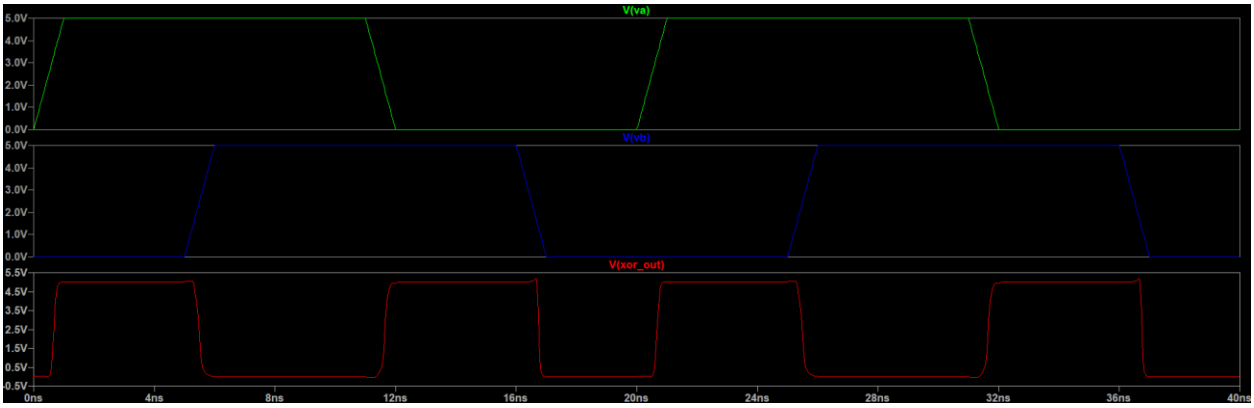
XOR





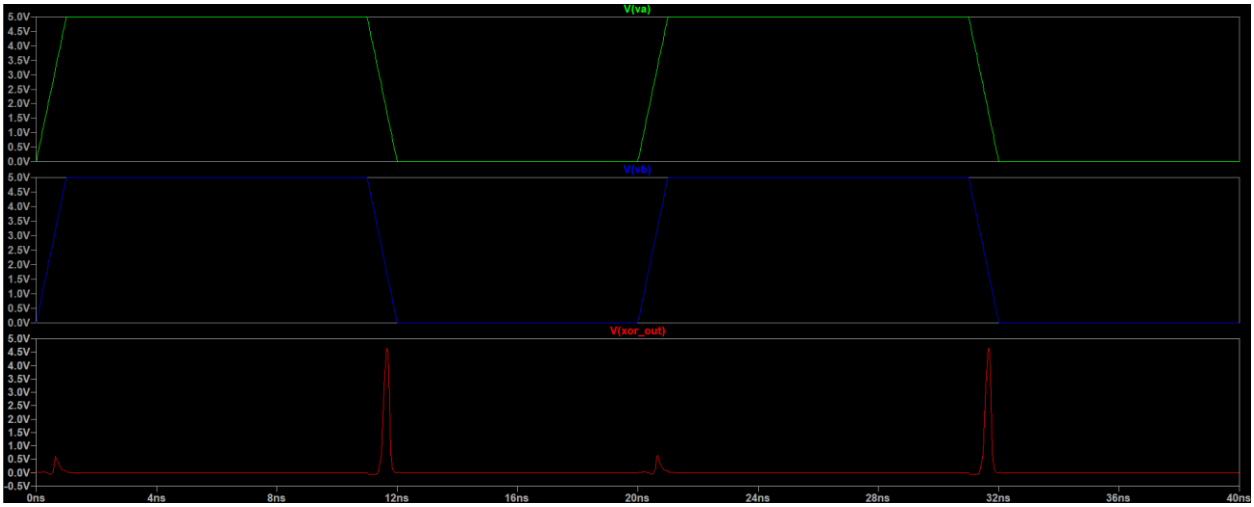
Some nets were routed on metal 2 to keep the design as compact as possible. This way all the bulk connections will line up with the inverter and NAND bulk connections for the full adder.

Logic Sim



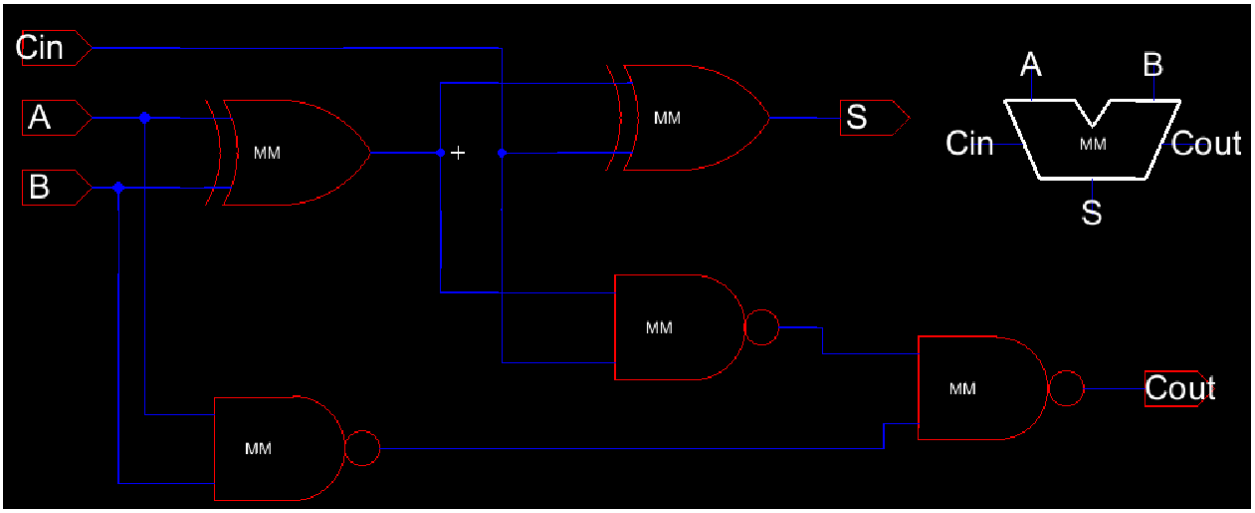
Xor_out is high when either va or vb are high, but not with both or neither or high.

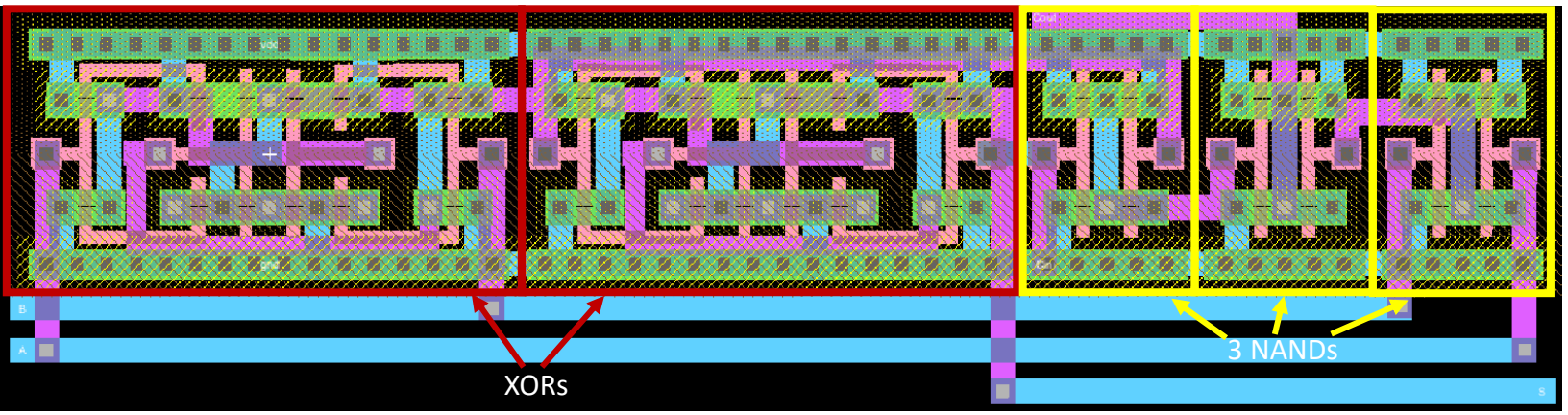
Output Glitches



When both inputs change at the same time, the output can glitch in the transition zone like in the above simulation

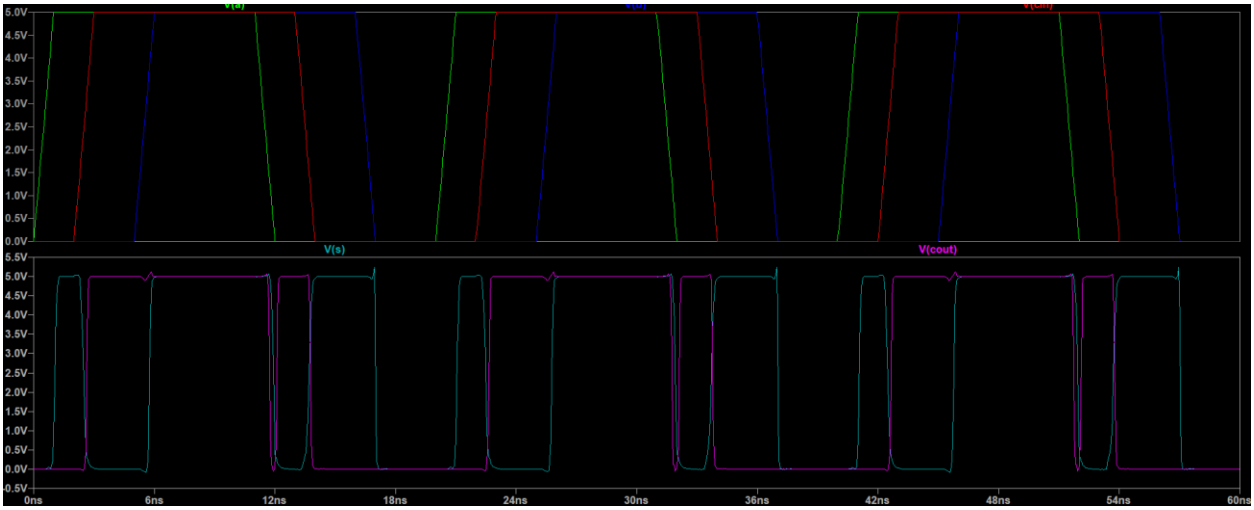
Full Adder





The input and outputs are the bottom 3 metal 1 lines. If these could be placed on metal 3 they could be placed on top of the adder to make a fully tileable design.

Logic Sim



S is high when either 1 or 3 of the inputs (a, b, cin) are high, otherwise its low. Cout is high when 2 or 3 of the inputs are high, otherwise its low.

DRC & NCC

```
================================6================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.026 secs)
================================7================================
Hierarchical NCC every cell in the design: cell 'full_adder{sch}'  cell 'full_adder{lay}'
Comparing: lab5_full_adder:NAND{sch} with: lab5_full_adder:NAND{lay}
  exports match, topologies match, sizes match in 0.058 seconds.
Comparing: lab5_full_adder:XOR{sch} with: lab5_full_adder:XOR{lay}
  exports match, topologies match, sizes match in 0.004 seconds.
Comparing: lab5_full_adder:full_adder{sch} with: lab5_full_adder:full_adder{lay}
  exports match, topologies match, sizes match in 0.013 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.089 seconds.
```