VLSI Lab 4 – Inverters

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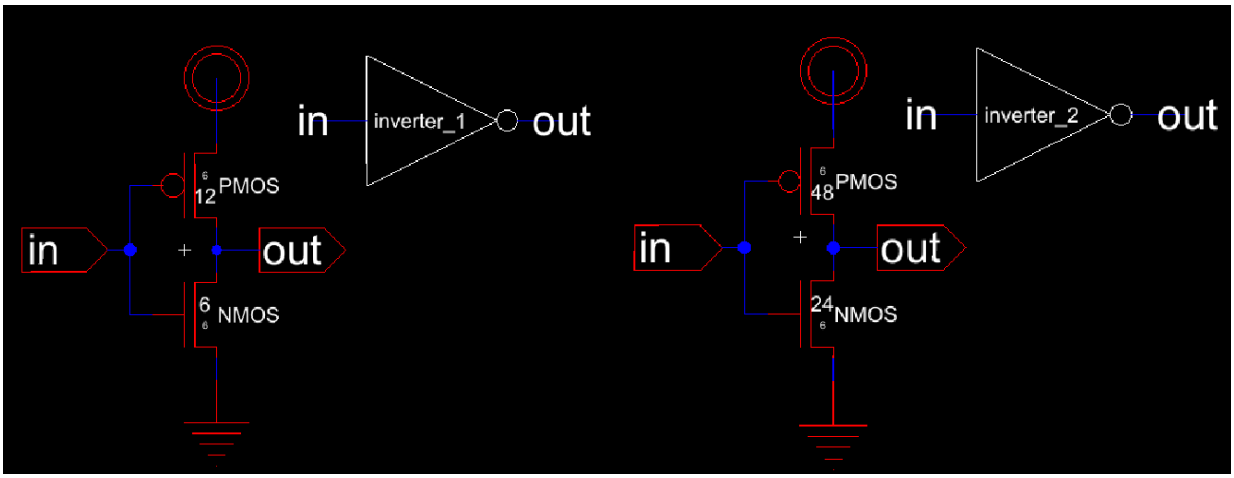
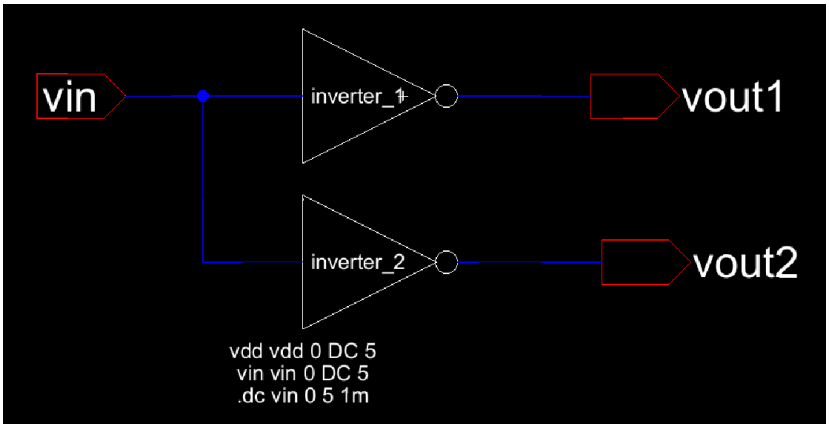
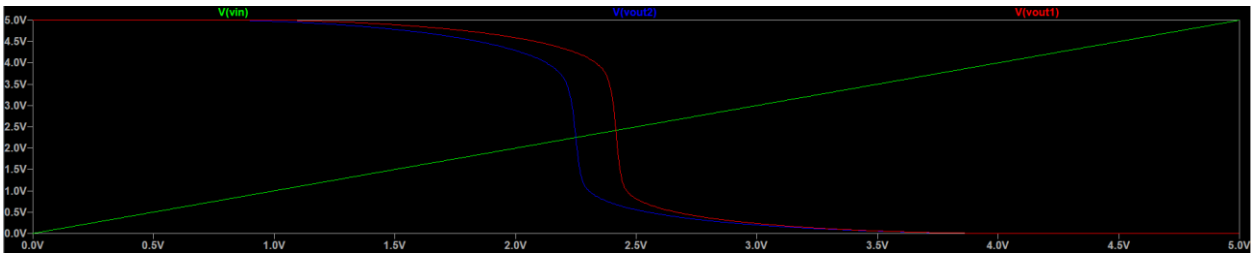
Schematic

Inverter 1/2

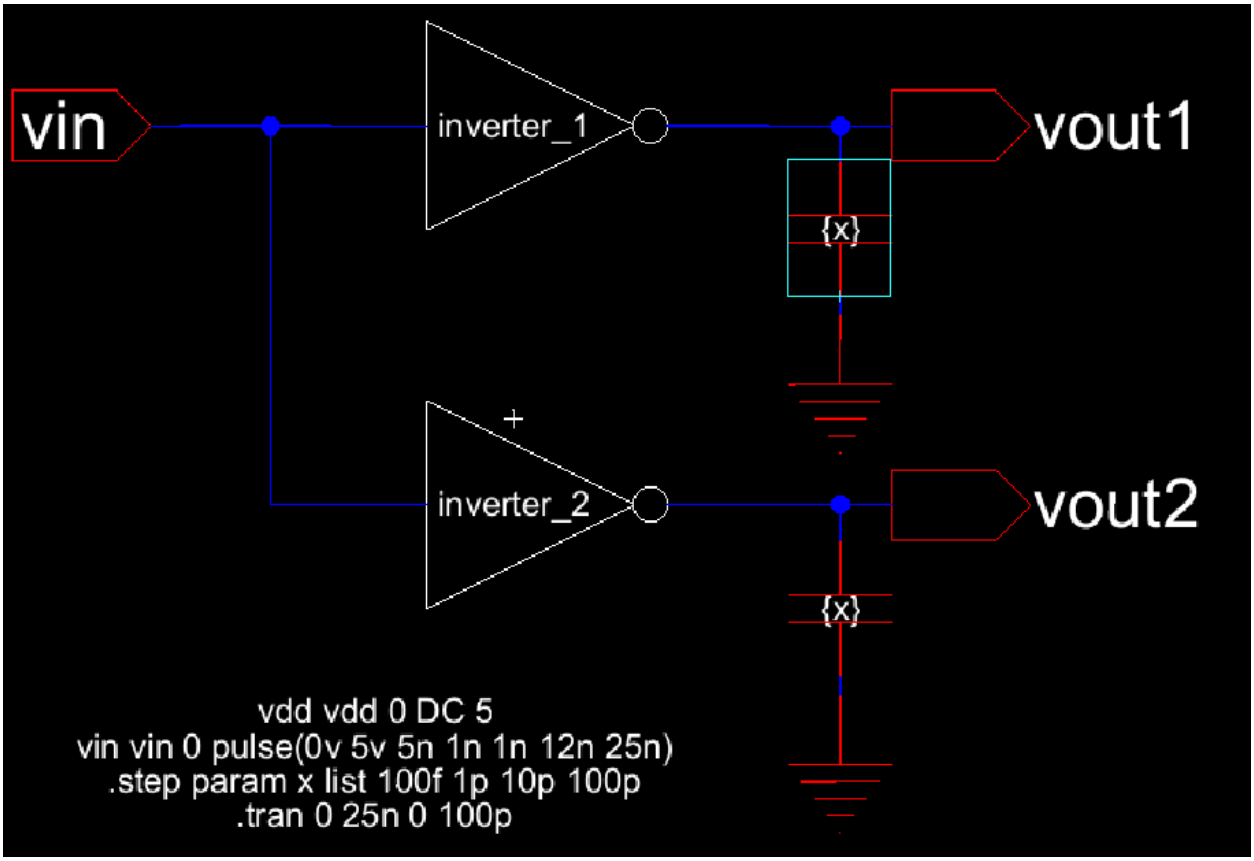


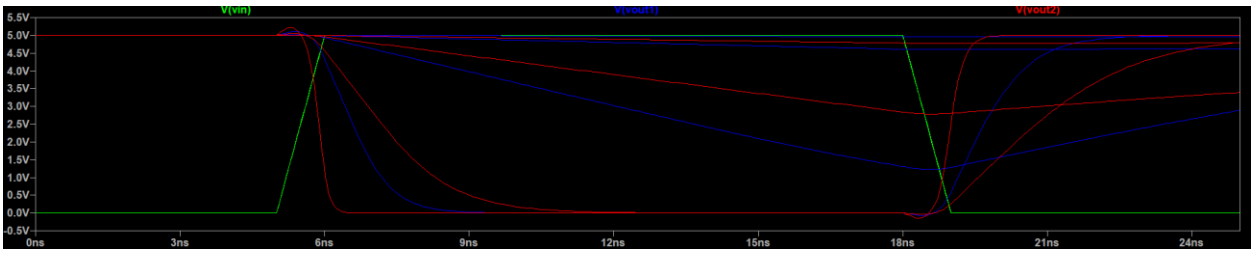
Inverter Sim





Pulse Sim

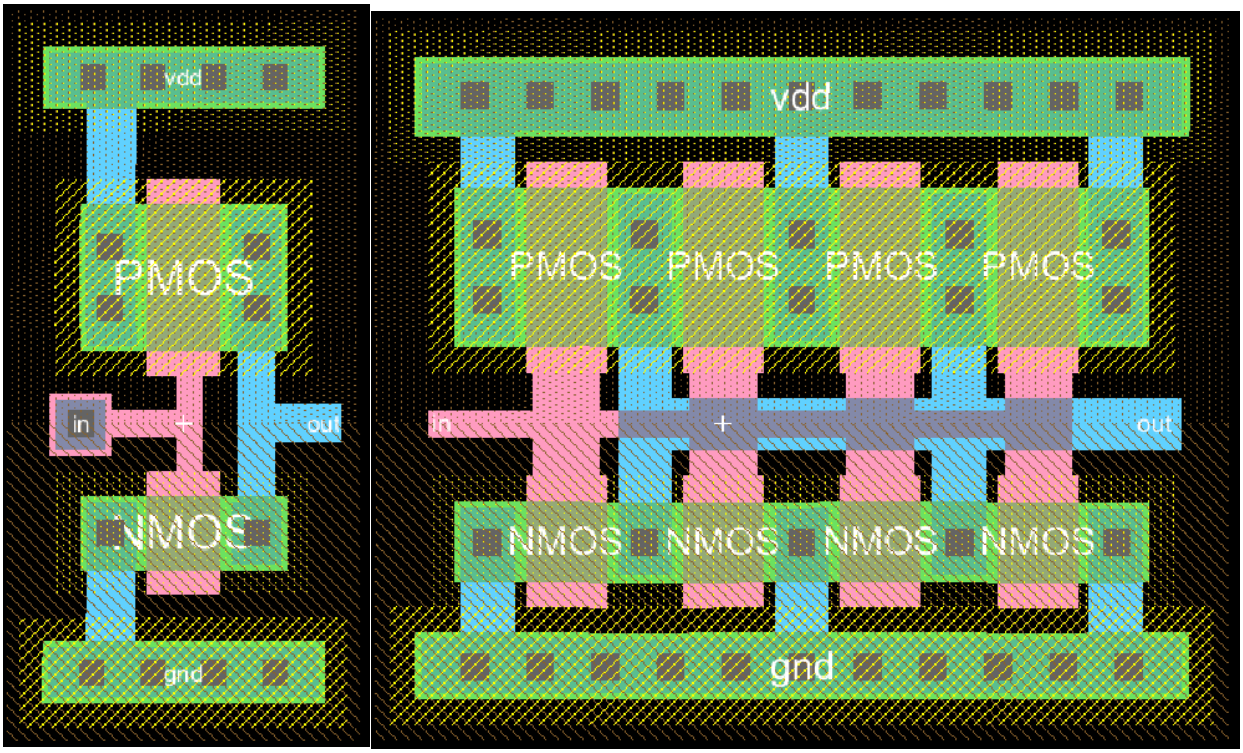




Inverter 2 appears to switch faster in both directions compared to inverter 1. Lower capacitances also appear to cause a little bit of “overshoot” during the transition where voltage goes slightly above 5V or below 0V.

Layout

Inverter ½



Metals and polysilicon wires were made as thick as DRC rules allow, but especially for inverter 1 it wont let it go any thicker than 2 for some reason.