VLSI Lab 1 – DAC

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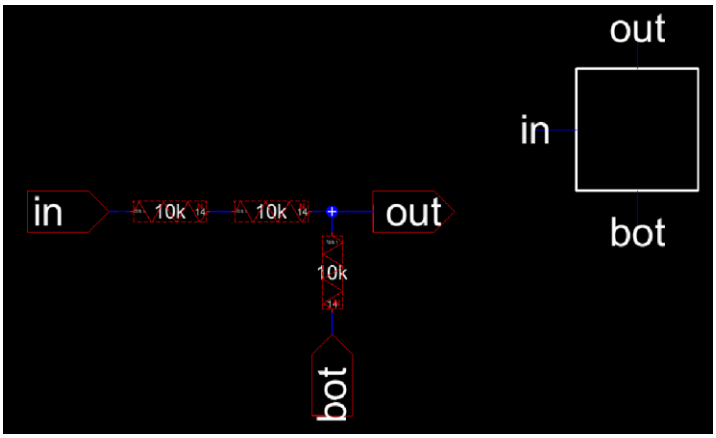
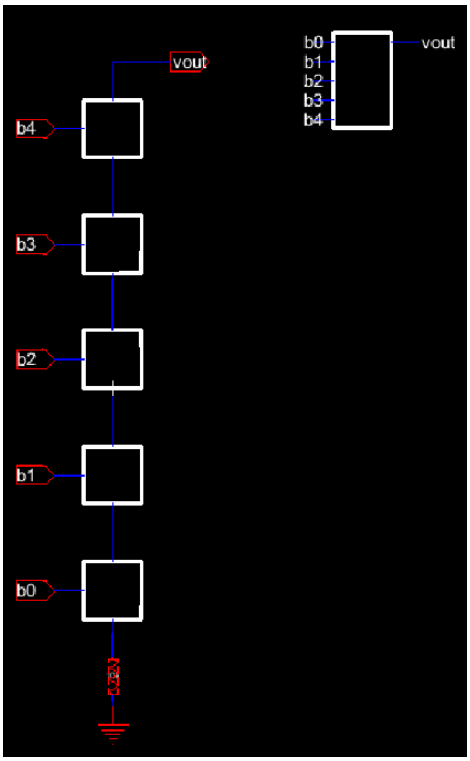
Schematic

Resistor Divider Schematic



5 Bit Dac Schematic



DAC Output Resistance

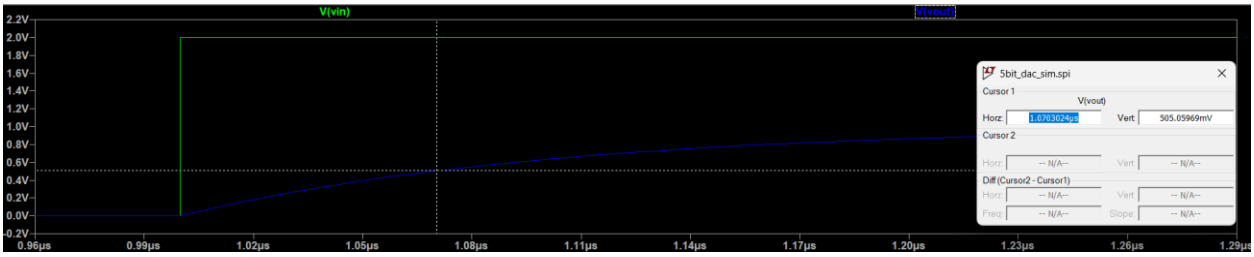
The output resistance of a voltage divider is the resistance of each resistor in parallel ($R_1 \parallel R_2 = \frac{1}{\frac{1}{R_1}+\frac{1}{R_2}}$). Stacking voltage dividers in the way done in this DAC puts the next divider in the chain in series with the lower resistor connected to ”bot” and in parallel with the input resistor connected to “in”. Assuming R_1 is the resistor connected to b1, R_2 is connected to “bot”, and R_N is the calculated output resistance of the next voltage divider, the resistance of a 2 bit DAC would be $R_1 \parallel (R_2 + R_N) = \frac{1}{\frac{1}{R_1}+\frac{1}{R_2+R_N}}$. This can be chained up to N bits, but the resistance of the last extra 10k resistor on the lsb should be added.

It turns out that because $R_1 = 2 * R_2$, $R_2 + R_N$ always evaluates to R_1 and $R_1 \parallel R_1 = R_2$, causing the total output resistance to always be equal to R_2, or 10k in this case.

Delay, driving a load

Predicted output delay: $0.7 * R_o * C_o = 0.7 * 10k * 10\text{e} - 12 = 70ns$

Matches spice sim:



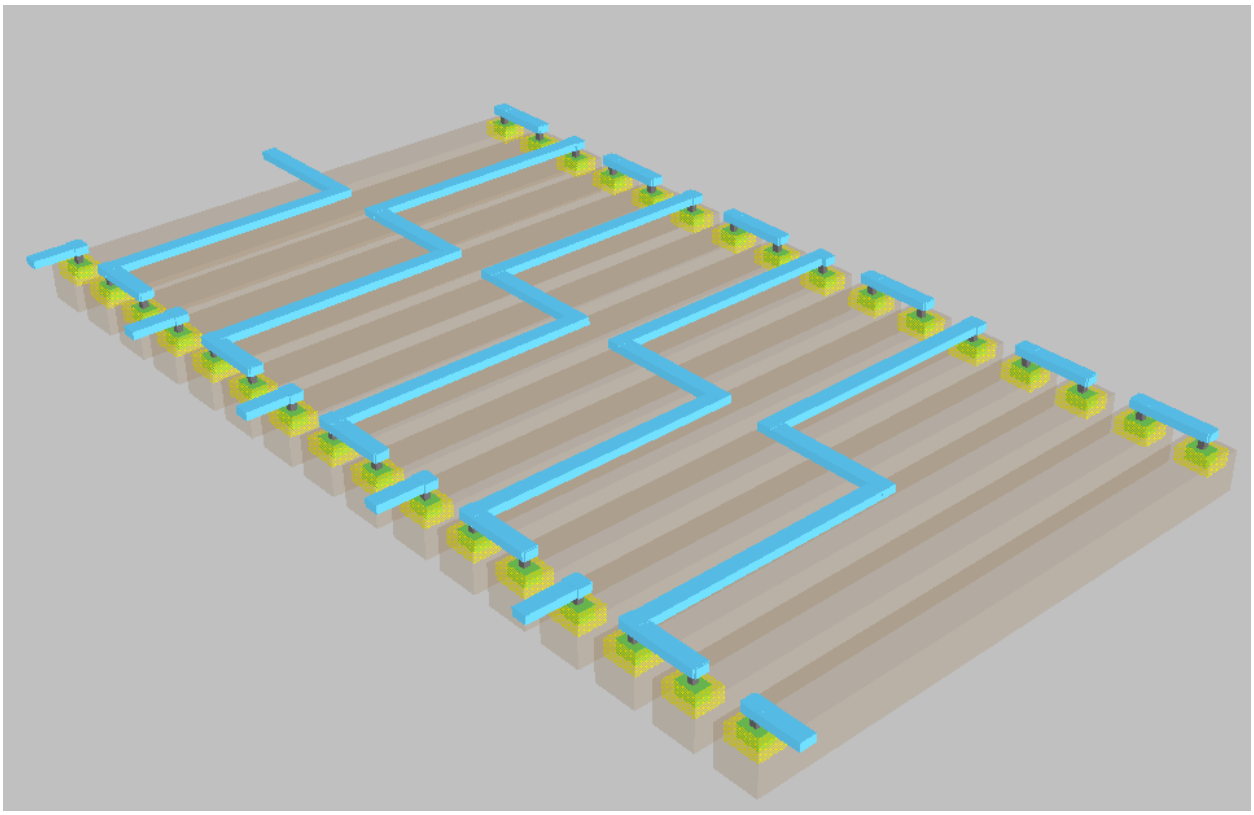
Simulations

If the DAC drives a 10k load its output voltage will get halved since its output resistance is 10k.

Layout

10k Resistor

You select the width of a resistor based on your manufacturers minimum feature width, then calculate your length based on the formula $R = R_{square} * \frac{L}{W}$.



DRC & NCC

```
==================================76==================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 18 networks
0 errors and 0 warnings found (took 0.02 secs)
==================================77==================================
Hierarchical NCC every cell in the design: cell '5bit_dac{sch}'  cell '5bit_dac{lay}'
Comparing: lab_1_dac:5bit_dac{sch} with: lab_1_dac:5bit_dac{lay}
  exports match, topologies match, sizes not checked in 0.074 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.093 seconds.
```