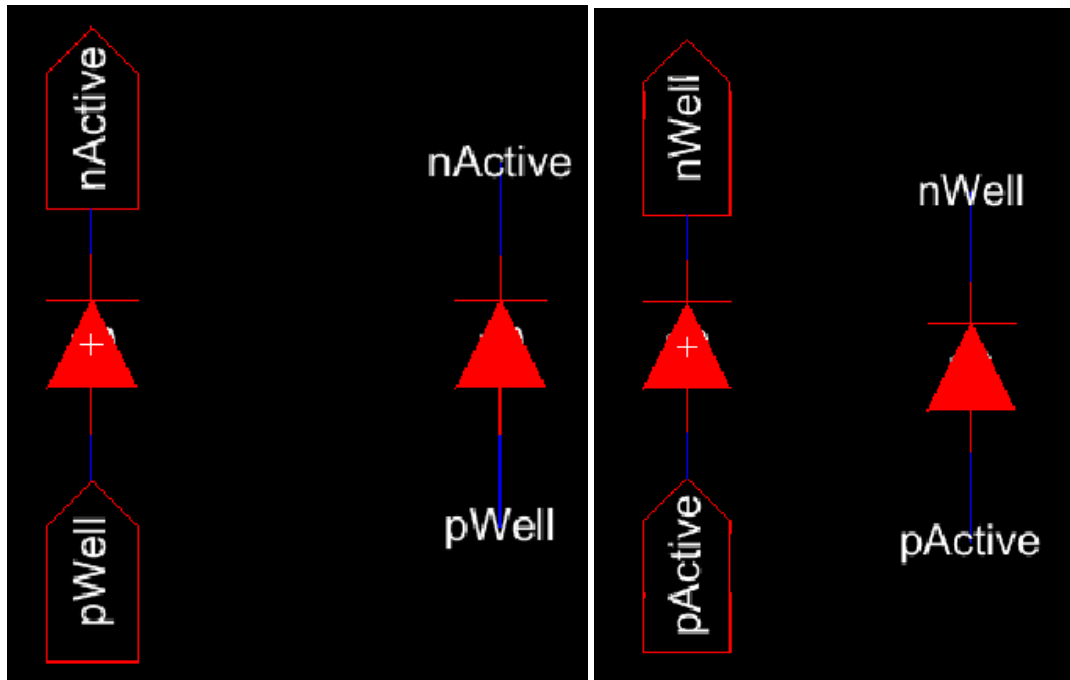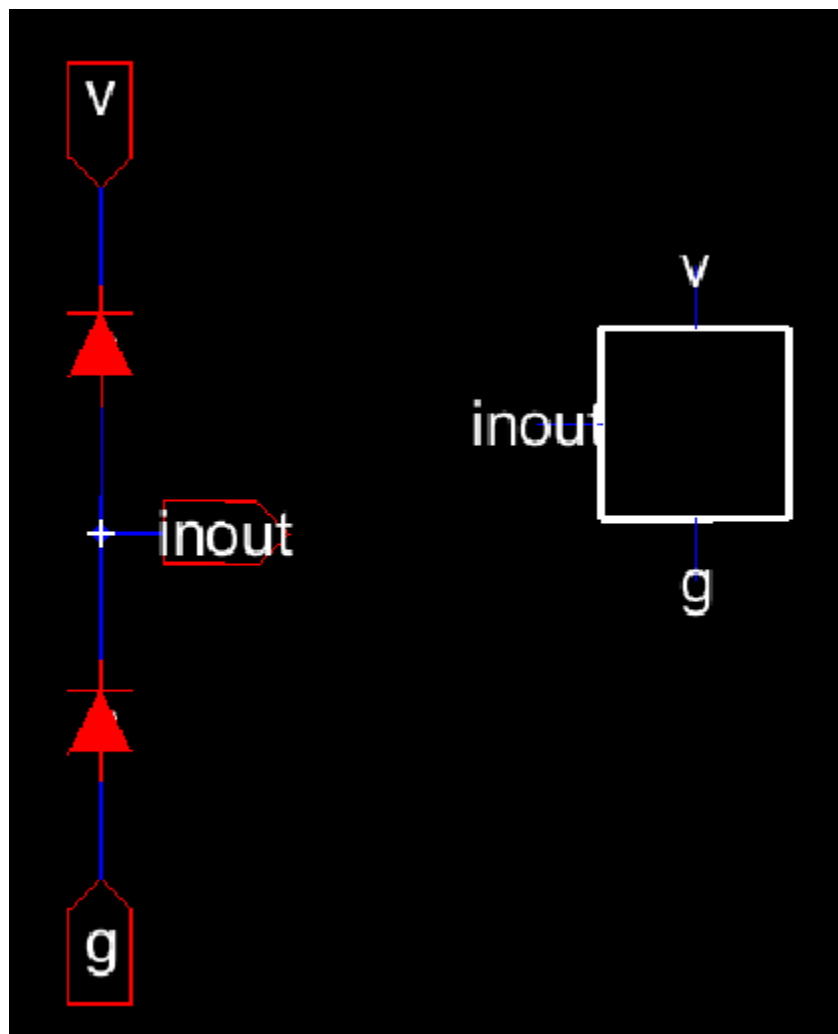# VLSI Lab 3 – NMOS ESD

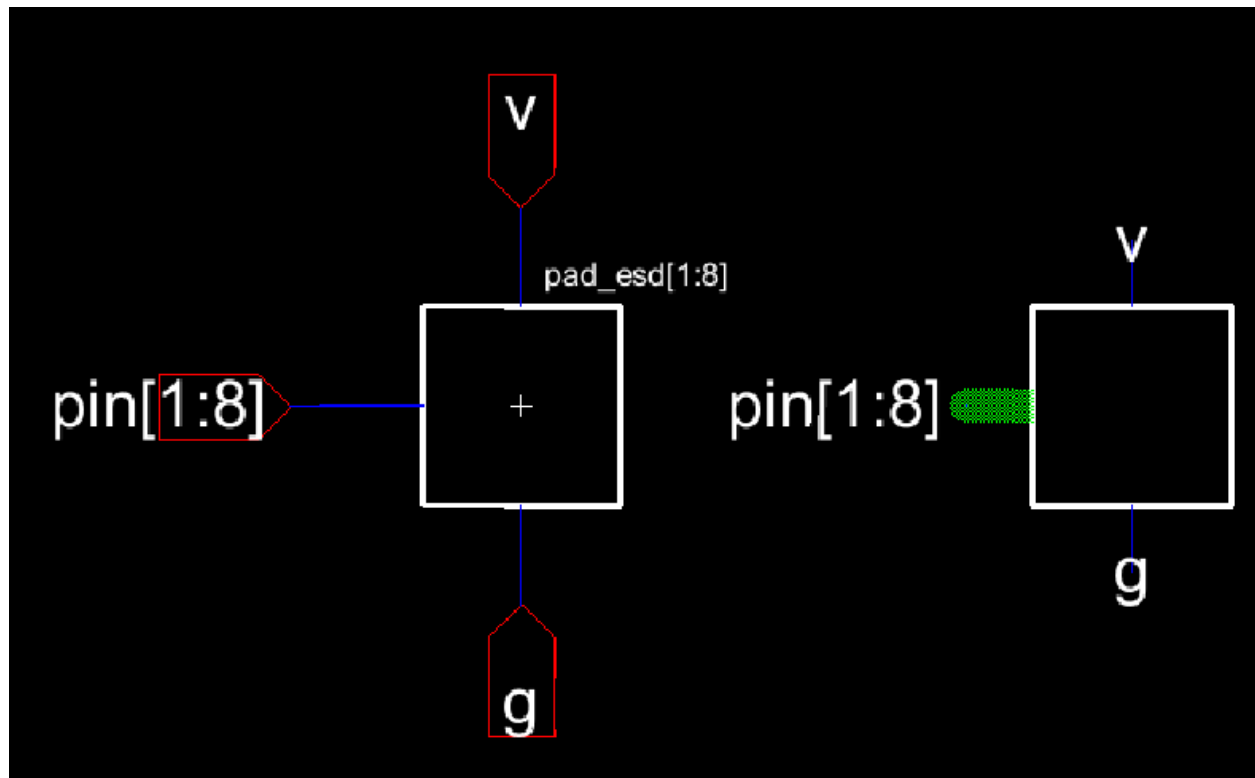Matthew Murray – 873525242

Schematic
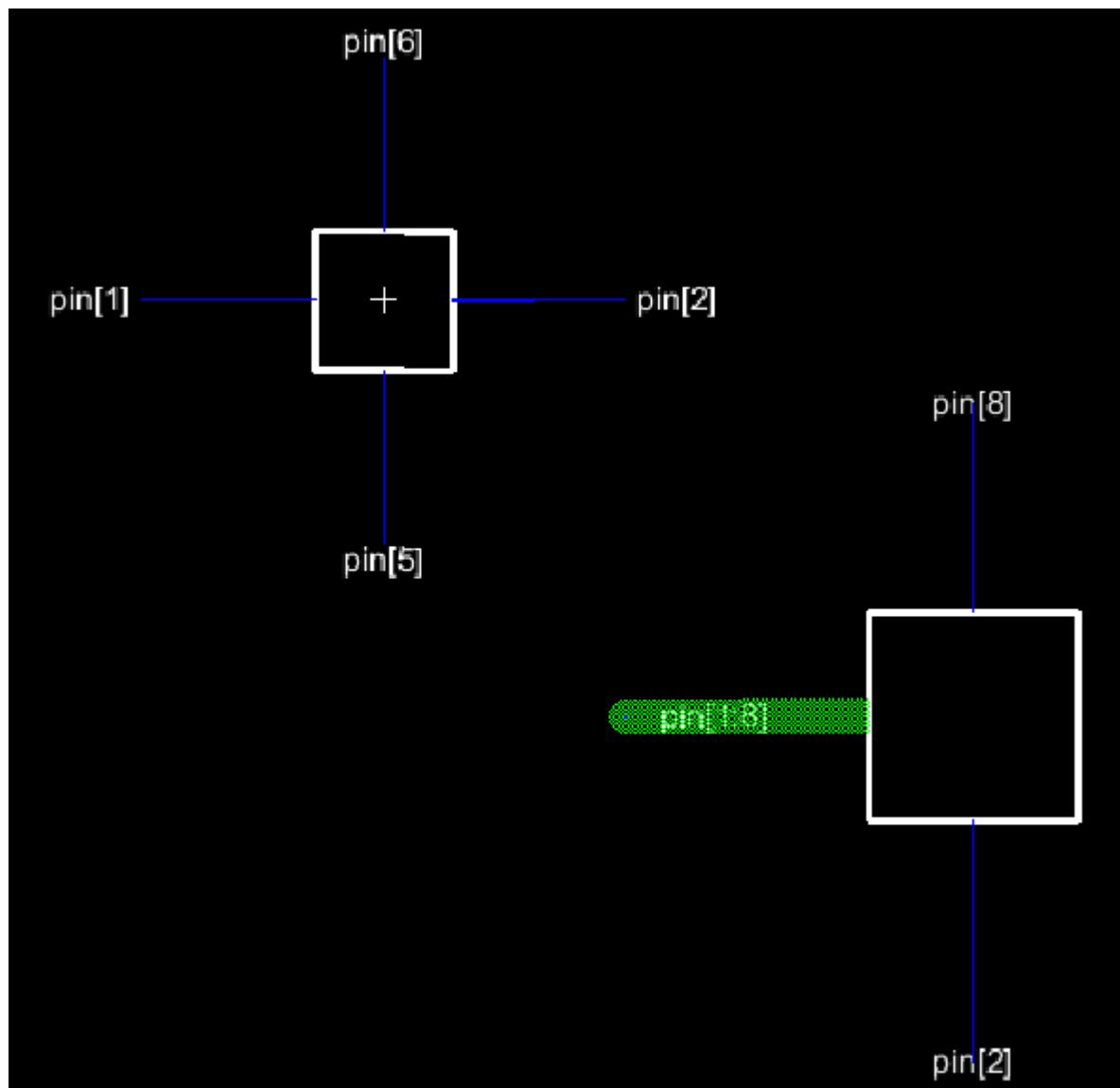
pWell-nActive / nWell-pActive
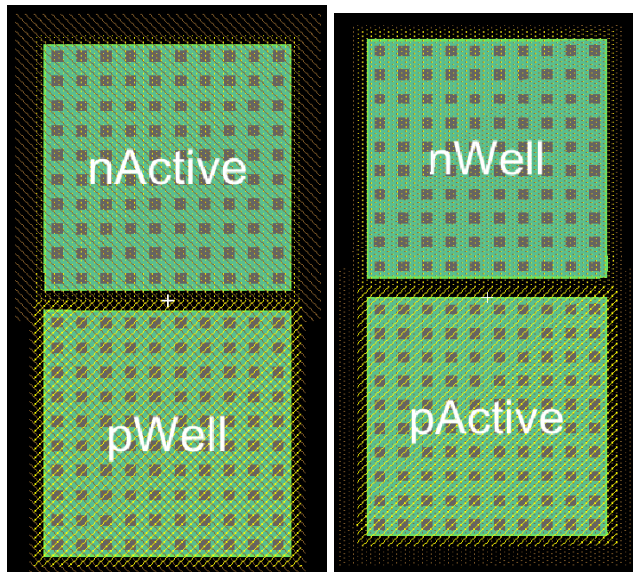
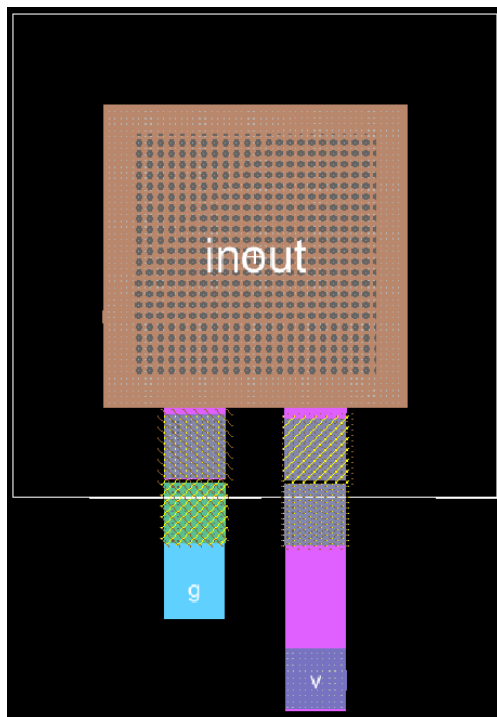Pad Cell w/ ESD

Padframe

Padframe w/ NMOS

Layout

pWell-nActive / pActive-nWell

Pad Cell w/ ESD

The horizontal busses were omitted in the individual pad cell to allow more compact placement in the padframe.

Padframe w/ NMOS