Question 1

Find NPN, PNP, SCR (NPNP) devices in the process profile from CMOS inverter cross section (next page; draw the 3 devices overtop of the CMOS process cross-section) and propose a circuit technique to avoid CMOS SCR latchup.

Question 2

Suppose you broke the loop between the PNP collector and NPN base of an SCR: describe $I_{Cpnp} = f\left(I_{Bnpn}\right)$ for this 2-BJT circuit with V_{DD} = 1.2 V, each with β = 10. Describe what happens in the closed loop.

Question 3

Create a static CMOS schematic, and sticks layout of

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x <= a NAND b; y <= b NAND c;
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Look at the two transistor schematics. Optimize and count the number of:

1. transistors
2. diffusion regions
3. metal-diffusion contacts

Question 4