Question 1

Produce a schematic and sticks layout for:

```
y <= not (a and b or a and c);
```

Minimizing and reporting the number of transistors, contacts and diffusion regions.

This question will be completed assuming that `AND` takes precedence over `OR`, resulting in the following expression.

```
y <= not ((a and b) or (a and c));
```

From here, we use a little boolean manipulation to simplify the expression further.

$$y = \overline{(ab) + (ac)}$$
$$y = \overline{a\,(b + c)}$$

We can now implement this function as a gate. The gate is available in figure 1, and the count of the component is available in table 1.

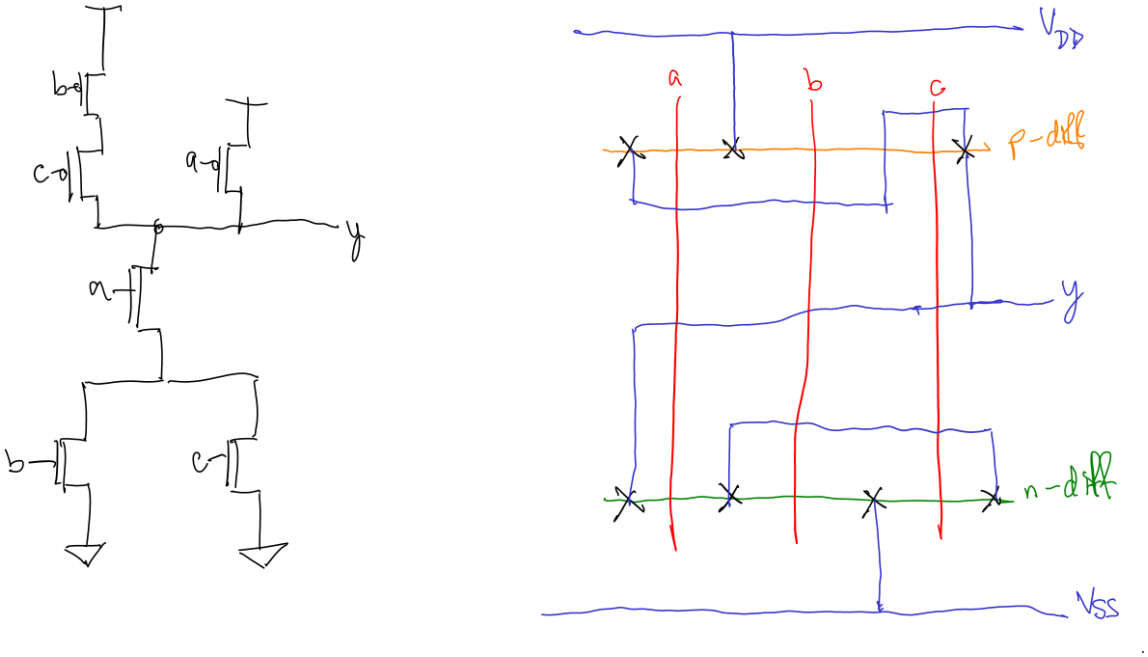

Figure 1: The transistor schematic and sticks layout for the design in question 1.

Table 1: The count of the design parameters for question 1.

Parameter	Number
Transistors	6
Contacts	7
Diffusion Region	2

Question 2

Create a static CMOS schematic and sticks layout for this function of 5 inputs (a,b,c,d,e):

```
y <= NOT(ab + ace + dcb + de);
```

Optimize and count the number of:

1. transistors (less than 20)
2. diffusion regions
3. metal-diffusion contacts

We could minimize the number of transistors in the expression a little more.

$$y = \overline{ab + ace + dcb + de}$$
$$y = \overline{a\,(b + ce) + d\,(cb + e)}$$

From here, the schematic is available in figure 2. It was found that the PUN and the PDN are Eularian, therefore, we are able to design this system using just two diffusion. With that information, the layout was construction and made available in figure 3. It was assumed that there is only one layer of poly-silicon, but multiple layers of metal, so additional contacts were added to connect poly-silicon that are too far apart.

The total count of components is available in table 2.

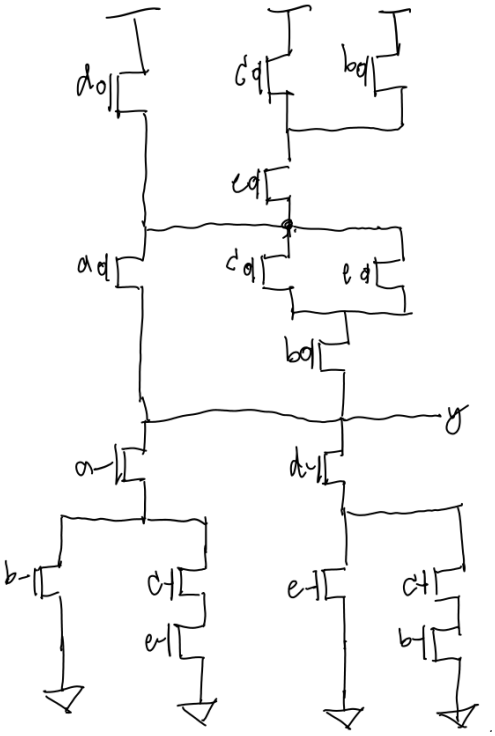

Figure 2: The schematic of the gate designed in question 2

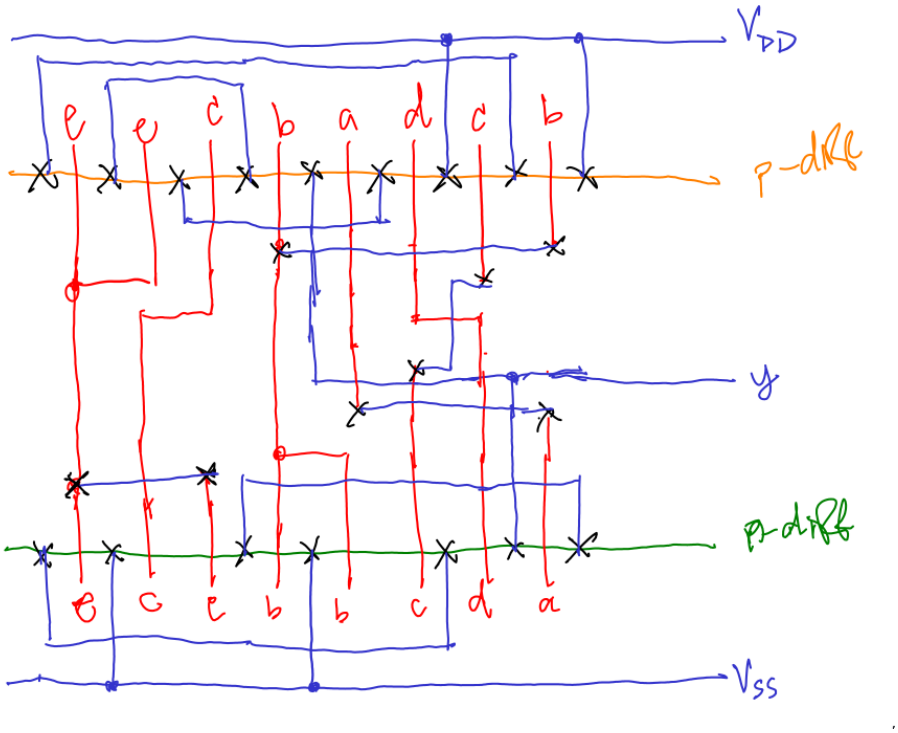

Figure 3: The layout of the gate designed in question 2. I was assumed that poly-silicon cannot cross, so additional contacts were added so that a connection between poly-silicon gates could be facilitated.

Table 2: The count of the design parameters for question 2.

Parameter	Number
Transistors	16
Diffusion Region	2
Contacts	24

Question 3

In layout, what is the difference between a common MOSFET source and drain?

In layout, a MOSFET in isolation has no difference between the source and the drain. You could start telling the difference between a source and a drain in a system by determining which active region has a path to the source (V_{DD} or V_{SS}), and which one has a path to the drain (V_{DD} or V_{SS}) or the output node.