$$y = ab + ac + cd \tag{1}$$

Question 1 a

Design a transistor schematic of a complex CMOS static gate plus inverters to implement y. Minimize transistor count. Label transistor widths (making textbook assumptions) for all stages having equivalent drive to a $W_{pmos} = 2$, $W_{nmos} = 1$ inverter.

We cannot construct y in a single stage, but we are able to implement $\overline{y}$ and then invert that value to obtain y.

Now the solution will be the implementation of $\overline{y} = ab + ac + cd$ in the first stage, then passing the output of this gate to an inverter. This design is available in figure 1. **This design uses 12 transistors**.

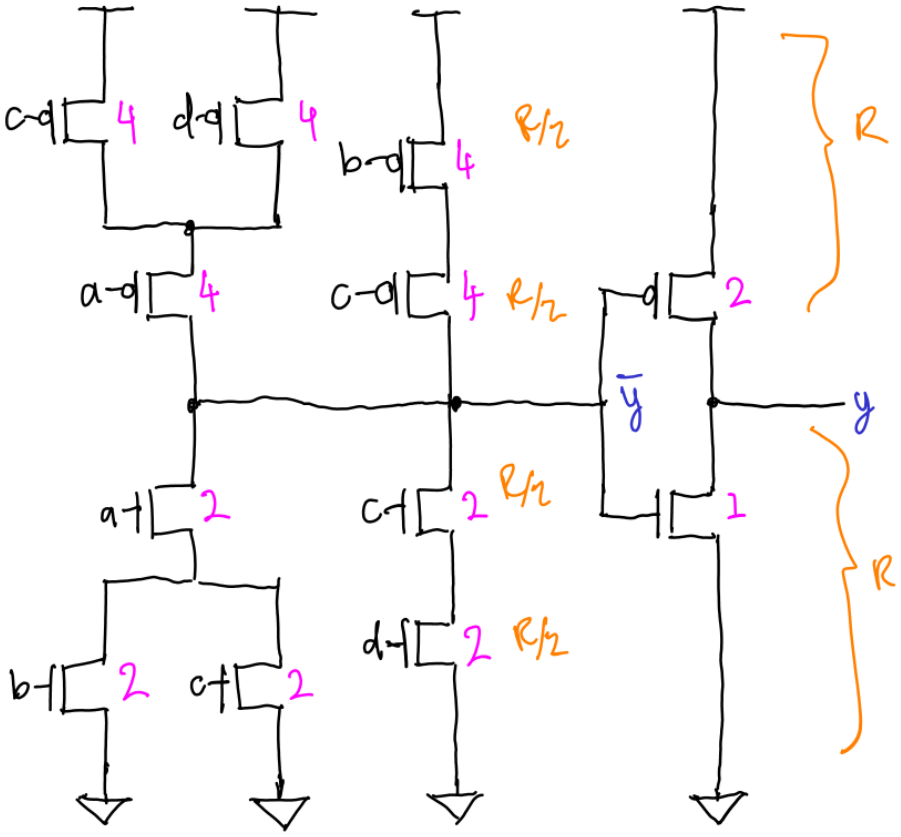

Figure 1: Schematic of the gate being implemented, with minimization of transistors applied.

Question 1 c

Design a sticks layout for your schematic (previous page). Minimize and report the number of diffusion regions and number of diffusion contacts. (Sticks diagrams are not to scale, including transistor widths.)

The required layout is available in figure 2, and the count of the components used is available in table 1.

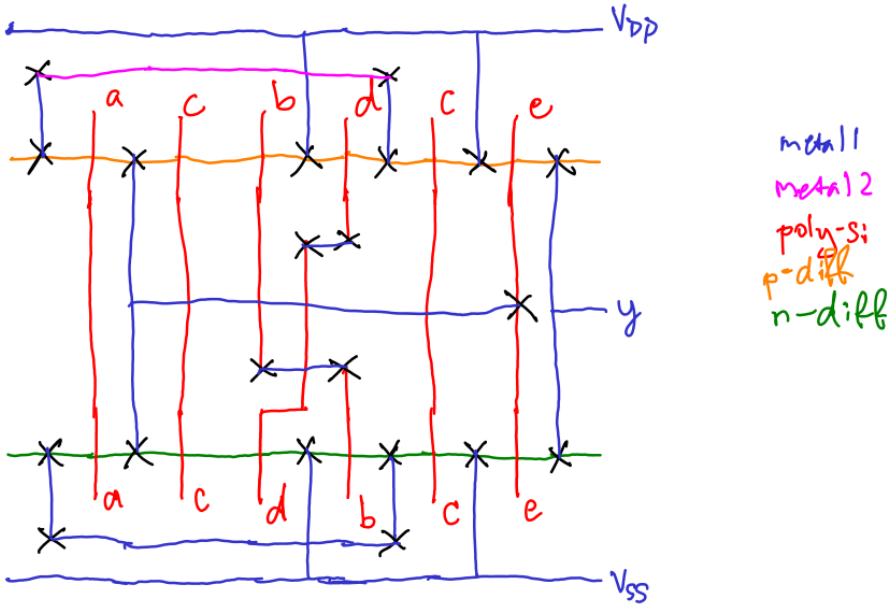

Figure 2: Layout of the implemented gate, with minimization of diffusion and contacts applied.

Table 1: The count of components used in the sticks diagram.

Parameter	Value
Diffusion Regions	2
Diffusion contacts	12

Question 1 d

Draw a gate-level schematic that implements $y = ab + ac + cd$ using nothing other than NAND gates, NOR gates and inverters. Optimize for and report the transistor count.

We could start by trying to convert the base expression into NAND/NOR/inverters. This is shown below.

$$y = ab + ac + cd$$
$$y = \overline{\overline{ab + ac + cd}}$$
$$y = \overline{\overline{(ab)} \cdot \overline{(ac)} \cdot \overline{(cd)}}$$

From here, a gate level schematic was implemented, available in figure 3. Finally, the count of the transistors in the system is available in table 2.

Table 2: Table counting the number of transistors in the gate level schematic.

Gate type	number of transistors per gate	number of gates	total number of transistors
NAND-2	4	3	12
NAND-3	6	1	6
		Sum	18

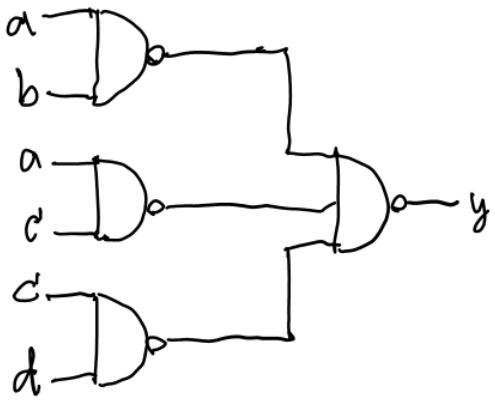

Figure 3: The gate level schematic for the NAND/NOR/inverter only implementation of (1).