Question 1

Produce a schematic design of 2-to-1 non-restoring multiplexer gate using CMOS transmission gates plus other static CMOS gates. Use inputs `{s, d0, d1}` and output `y`. Inverted signals are not provided.

Table 1: The truth table of the 2-to-1 non-restoring multiplexer.

s	d1	d0	y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

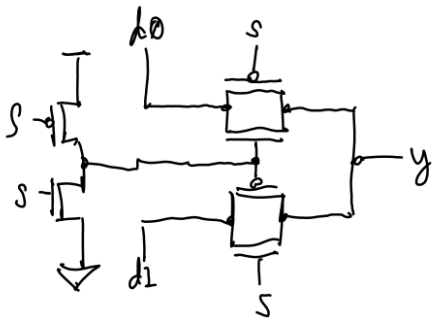

Figure 1: The schematic for the 2-to-1 nonrestoring multiplexer gate.

Question 2

Draw a sticks diagram of this mux.

Optimize and count the number of:

1. transistors
2. diffusion regions
3. metal-diffusion contacts

The layout of the 2-to-1 non-restoring multiplexer is available in figure 2. The count of the components used in the design is available in table 2.

Table 2: The number of components used in the implementation of the non-restoring 2-to-1 multiplexer.

component	number
transistors	6
diffusion regions	4
metal contacts	13

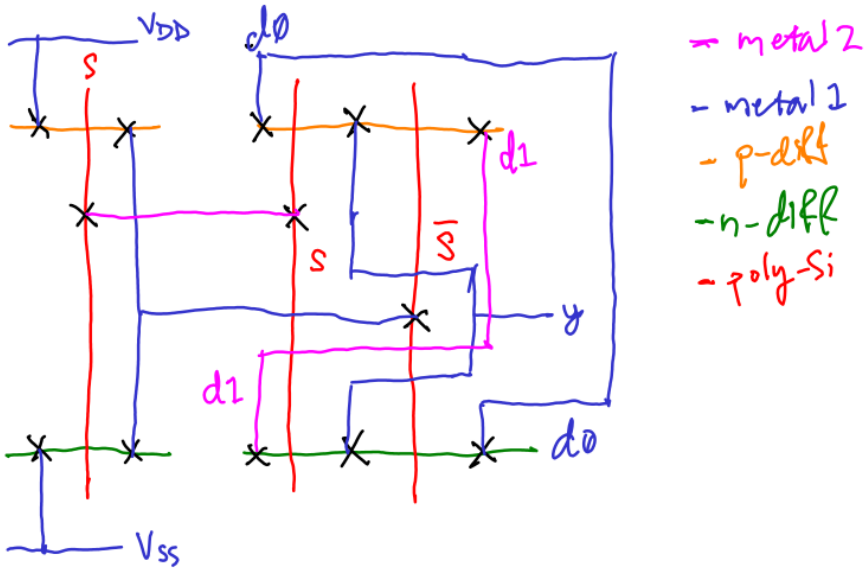

Figure 2: The layout for the 2-to-1 non-restoring multiplexer where inverted signals are not provided.

Question 3

Describe how the delay grows with the number of stages (n) of a circuit with these multiplexers connected together (one output to the next input) in a combinational path. Remember that each transistor has resistance and capacitance.

Starting with the setup of this question, we are putting the inputs and outputs of n muxes in a cascade topology, as seen in figure 3. Converting this to the schematic view, as seen in figure 4, we see that we could probably model the delay as an Elmore delay, as we would have a good view of the scaling of the delay as you add more mux into the system (no sizing here). The Elmore delay model of the system is available in figure 5.

From here, a little bit of math lets us see the scaling of the delay. In (1), we see that the delay of this system composition has a growth rate of $O\left(n^2\right)$, where n is the number of muxes in the system with it's output tied to the input of the next mux.

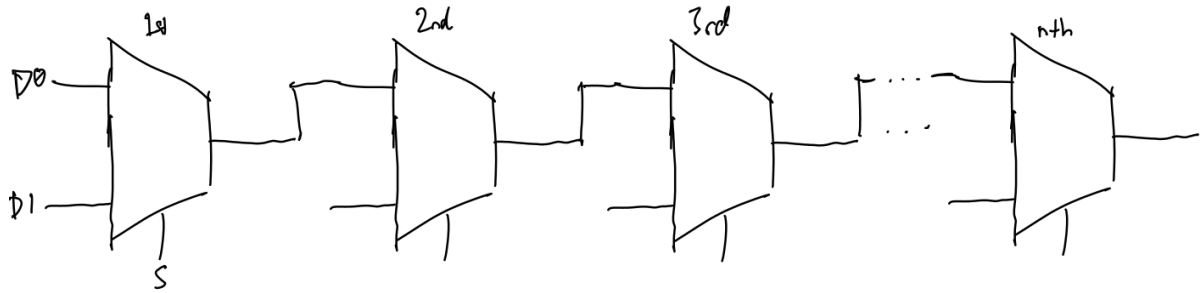

Figure 3: The architecture of the multiplexers being analyzed.

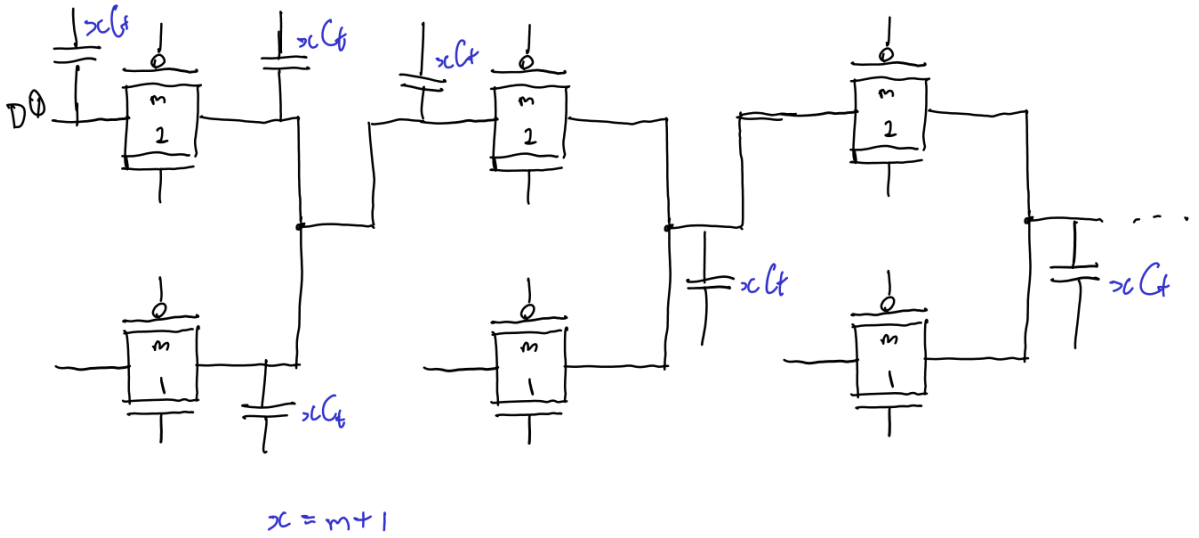

Figure 4: The schematic of the multiplexers being analyzed, where $\mu_n = m\mu_p$, and $x = m + 1$.

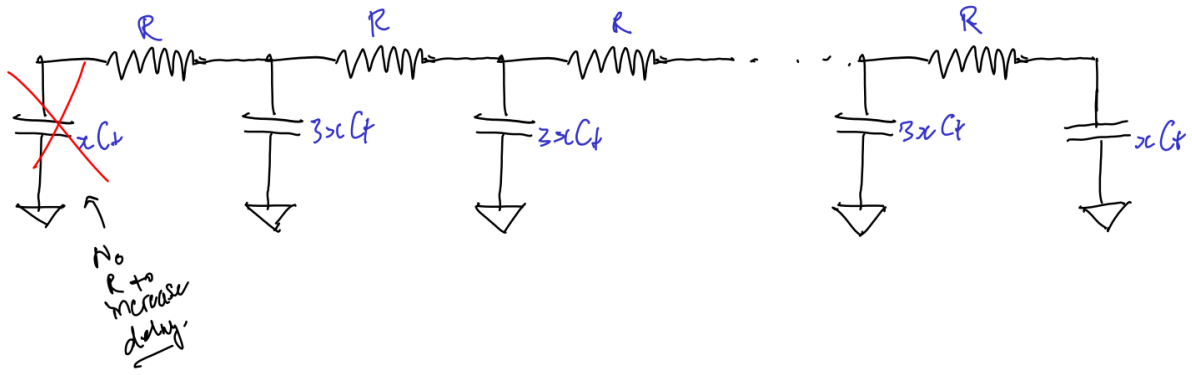

Figure 5: The Elmore model of the multiplexers being analyzed.

$$
\begin{aligned}
\text{let} \quad \mu_n = m\mu_p; \quad \text{let} \quad x = m+1 \\
t_d &= nxRC_t + \sum_{i=1}^{n-1} 3xC_t \cdot iR \\
t_d &= nxRC_t + 3xRC_t \sum_{i=1}^{n-1} i \\
t_d &= xRC_t \left(n + 3 \sum_{i=1}^{n-1} i \right) \\
t_d &= xRC_t \left(n + 3 \left(\frac{n\,(n-1)}{2} \right) \right) \\
t_d &= xRC_t \left(n + \frac{3}{2}n^2 - \frac{3}{2}n \right) \\
t_d &= xRC_t \left(\frac{3}{2}n^2 - \frac{1}{2}n \right) \\
\therefore t_d &= \frac{xRC_t}{2} \left(3n^2 - n \right) \qquad (1)
\end{aligned}
$$