Question 1

Find NPN, PNP, SCR (NPNP) devices in the process profile from CMOS inverter cross section (next page; draw the 3 devices overtop of the CMOS process cross-section) and propose a circuit technique to avoid CMOS SCR latchup.

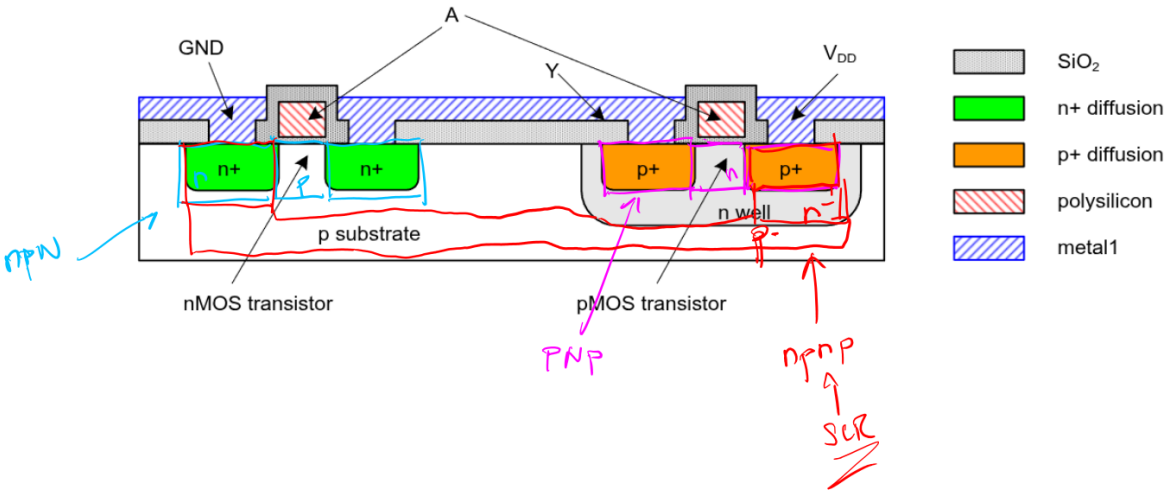

Figure 1: The NPN, PNP, and SCR devices found in the process profile of a CMOS inverter cross section.

Now, we are tasked with preventing latchup with some circuit design techniques. The first that we are going to talk about requires that the CMOS process being used supports it. The strategy here is to prevent the NPNP regions from forming using an oxide layer[1]. The big idea here is that by placing insulating regions around the nMOS and pMOS, the full NPNP junction could not form to produce a parasitic SCR. A process profile diagram for the implementation of this design is available in figure 2.

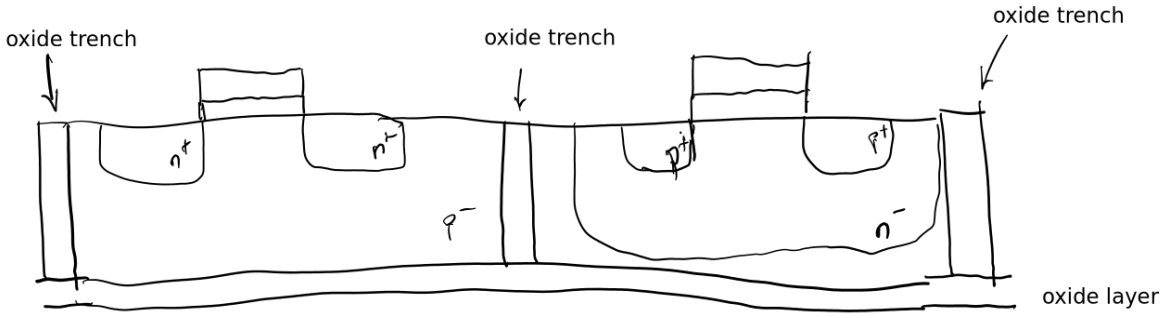

Figure 2: Circuit design that removes latch-up using oxide trenches to break the SCR.

[1] https://www.analog.com/en/resources/analog-dialogue/articles/winning-the-battle-against-latchup.html

Question 2

Suppose you broke the loop between the PNP collector and NPN base of an SCR: describe $I_{Cpnp} = f\left(I_{Bnpn}\right)$ for this 2-BJT circuit with V_{DD} = 1.2 V, each with β = 10. Describe what happens in the closed loop.

Opening up the closed loop, we see the following schematic.

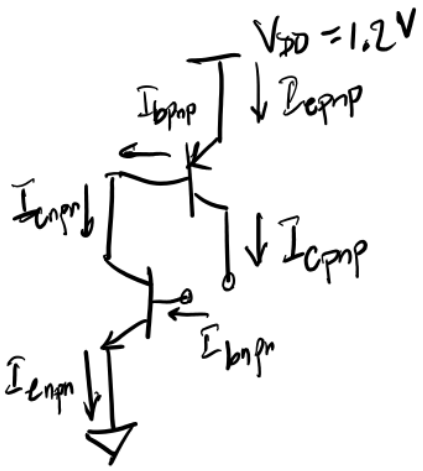

Figure 3: The schematic of the closed loop, with an artificial short at B_{npn} and C_{pnp}

Using figure 3, we could start doing some case analysis. When $I_{B_{npn}}$ is 0, the npn transistor is in cut-off, which would bring $I_{B_{pnp}}$ to 0, which would also cut-off the pnp transistor. The expression for $I_{C_{pnp}}$ in cut-off is available in (1).

$$\text{In cut off} \quad I_{C_{pnp}} = I_{B_{npn}} = 0 \tag{1}$$

In the active mode of operation, the behaviour of $I_{C_{pnp}} = f(I_{B_{npn}})$ in the system is available in (4).

$$I_C = \beta I_B \tag{2}$$

$$\beta = 10 \tag{3}$$

$$\begin{aligned}
I_{C_{pnp}} &= \beta I_{B_{pnp}} && (2)\\
I_{C_{pnp}} &= \beta I_{C_{npn}} \\
I_{C_{pnp}} &= \beta\left(\beta I_{B_{npn}}\right) && (2)\\
I_{C_{pnp}} &= 10\left(10 I_{B_{npn}}\right) && (3)\\
I_{C_{pnp}} &= 100 I_{B_{npn}} \\
\therefore f(x) &= 100 \cdot x && (4)
\end{aligned}$$

Translating this to what would happen in a closed loop, the current $I_{C_{pnp}}$ will remain at 0 until some amount of current is injected into the $I_{B_{npn}}$ node. When this occurs, the current $I_{C_{pnp}} = I_{B_{npn}}$, but since the C_{pnp} node and the B_{npn} node are the same, the amplification of the $I_{C_{pnp}}$ node will feed back into $I_{B_{npn}}$ which would further increase the collector current of the pnp BJT. This will go on until the system has reached some saturation current.

Question 3

Create a static CMOS schematic, and sticks layout of

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x <= a NAND b; y <= b NAND c;
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Look at the two transistor schematics. Optimize and count the number of:

1. transistors
2. diffusion regions
3. metal-diffusion contacts

Starting with the design, we might start with two separate NAND gates, which is available in figure 4.

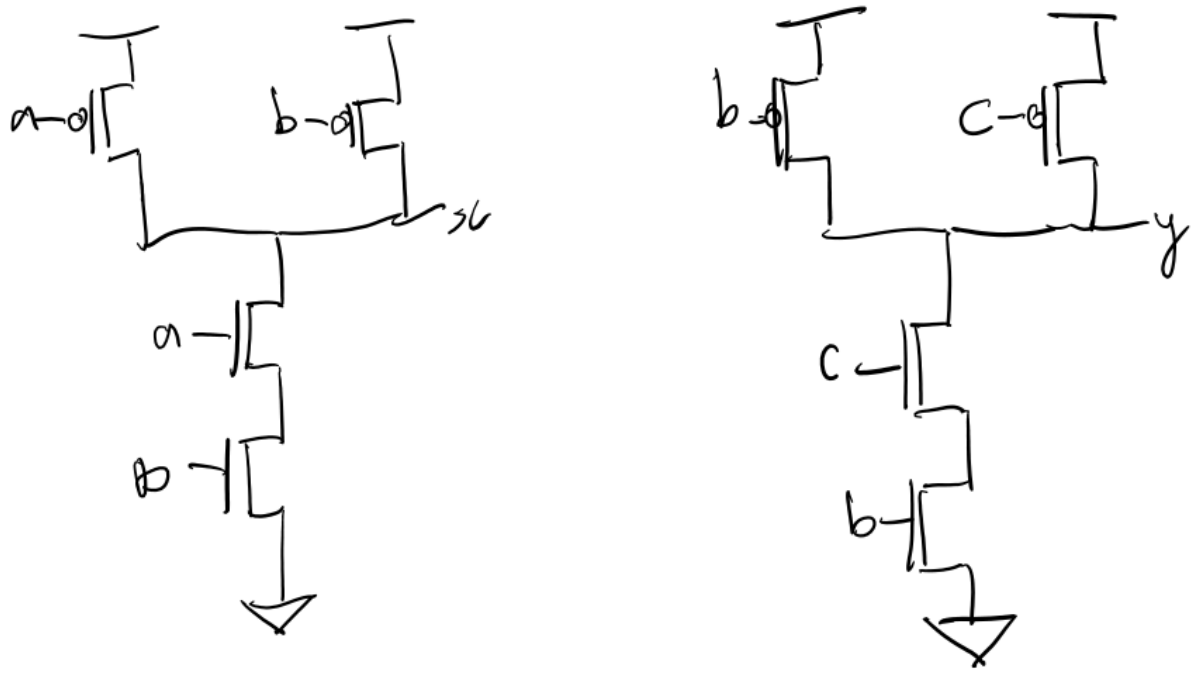

Figure 4: The basic transistor schematic of the two NAND signals.

But knowing that the b input is shared between the two gates we are defining, we could try to share some transistors, specifically, ones in series. From our schematic in figure 4, we see that the b nMOS is in series with the other input in both pull down networks. We could therefore share this transistor between the two. This new design is available in figure 5.

Following the design in figure 5, we move on to implement a stick diagram that follows this schematic in figure 6. Here, we are trying to share connections to V_{DD} and V_{SS} as much as we could, but in the pull up network, since there must be a separate b input pMOS, another region of p-diff was added.

The count for the number of components for this exercise is available in table 1.

Question 4

Create a static CMOS schematic, and sticks layout of with the same optimizations as before:

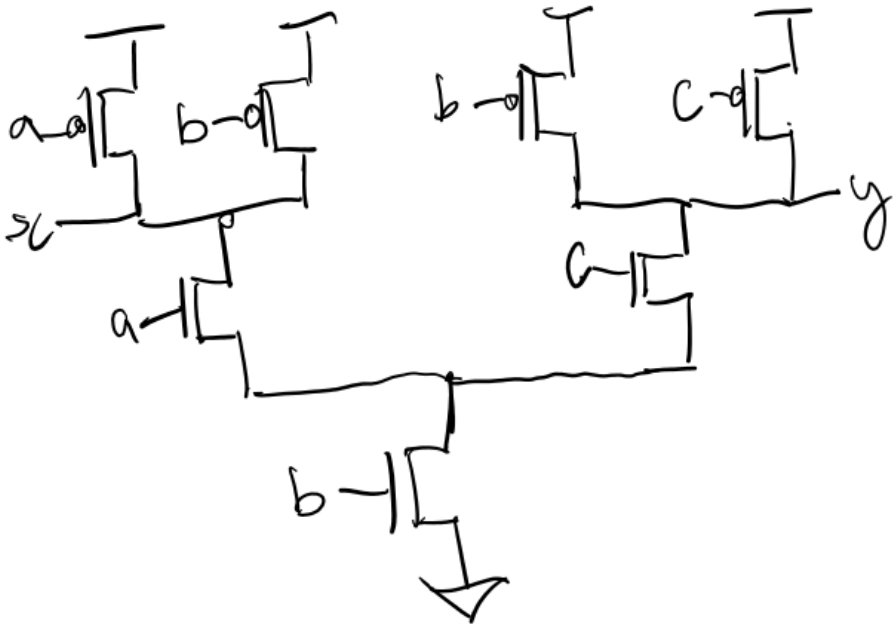

Figure 5: The transistor schematic of the two NAND sharing the b input nMOS.

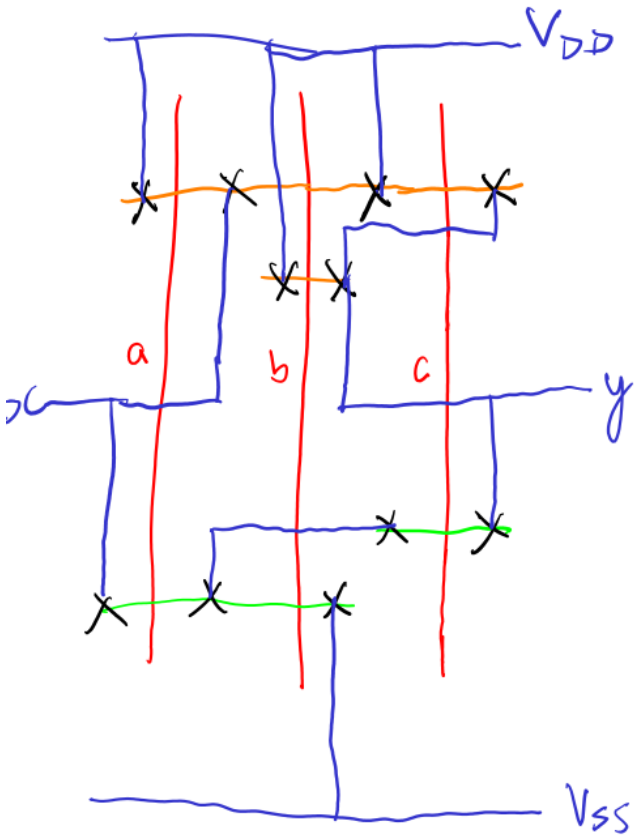

Figure 6: The stick diagram for the gate design where the b nMOS is shared.

Table 1: The number of components being optimized for in question 3.

component	number
transistors	7
diffusion regions	4
metal-diffusion contacts	11

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y <= NOT (( a OR b OR c) AND d);
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The schematic is available in figure 7, and the stick layout is available in figure 8.

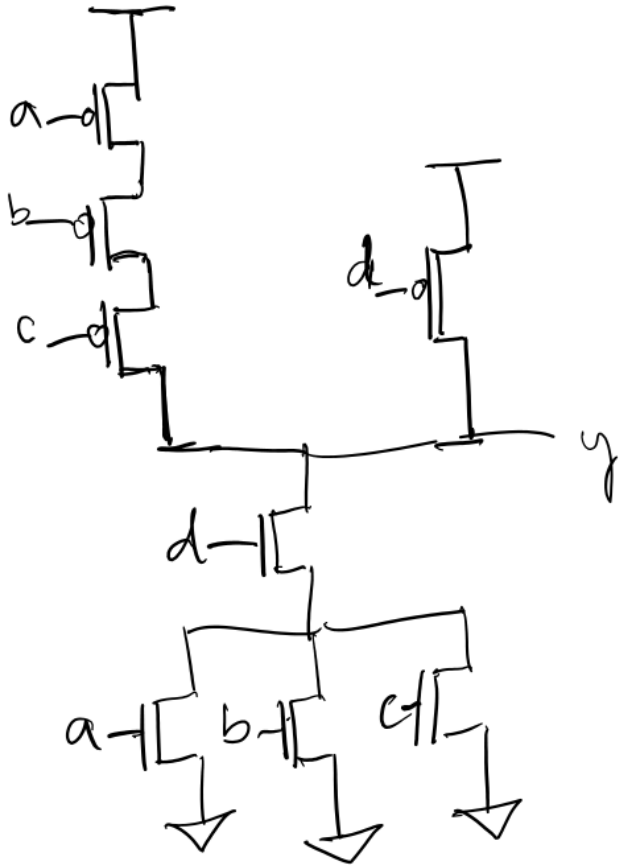

Figure 7: The transistor schematic of the defined function.

With this design we have the count for the total number of components in figure 2.

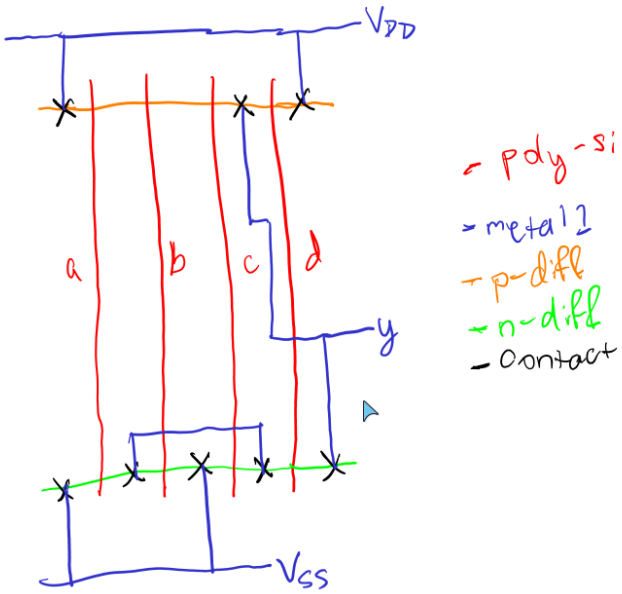

Figure 8: The stick layout of the defined gate.

Table 2: The number of components being optimized for in question 4.

component	number
transistors	8
diffusion regions	2
metal-diffusion contacts	8