$$y = ab + ac + cd \tag{1}$$

Question 1 a

Design a transistor schematic of a complex CMOS static gate plus inverters to implement y. Minimize transistor count. Label transistor widths (making textbook assumptions) for all stages having equivalent drive to a $W_{pmos} = 2$, $W_{nmos} = 1$ inverter.

Question 1 c

Design a sticks layout for your schematic (previous page). Minimize and report the number of diffusion regions and number of diffusion contacts. (Sticks diagrams are not to scale, including transistor widths.)

Table 1: The count of components used in the sticks diagram.

Parameter	Value
Diffusion Regions	
Diffusion contacts	

Question 1 d

Draw a gate-level schematic that implements $y = ab + ac + cd$ using nothing other than NAND gates, NOR gates and inverters. Optimize for and report the transistor count.