Question 1

Produce a schematic design of 2-to-1 non-restoring multiplexer gate using CMOS transmission gates plus other static CMOS gates. Use inputs `{s, d0, d1}` and output `y`. Inverted signals are not provided.

Table 1: The truth table of the 2-to-1 non-restoring multiplexer.

s	d1	d0	y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

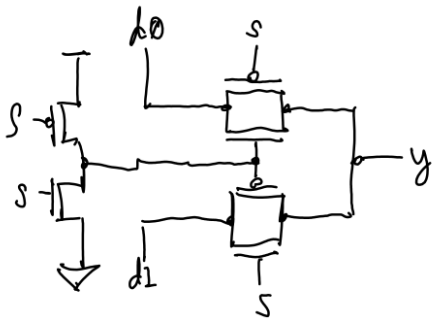

Figure 1: The schematic for the 2-to-1 nonrestoring multiplexer gate.

Question 2

Draw a sticks diagram of this mux.

Optimize and count the number of:

1. transistors
2. diffusion regions
3. metal-diffusion contacts

The layout of the 2-to-1 non-restoring multiplexer is available in figure 2. The count of the components used in the design is available in table 2.

Table 2: The number of components used in the implementation of the non-restoring 2-to-1 multiplexer.

component	number
transistors	6
diffusion regions	4
metal contacts	13

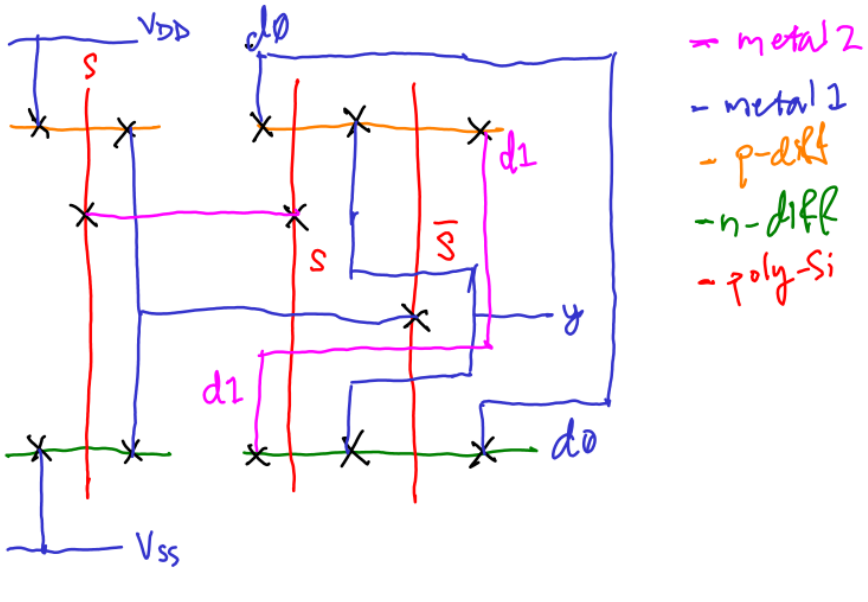

Figure 2: The layout for the 2-to-1 non-restoring multiplexer where inverted signals are not provided.

Question 3

Describe how the delay grows with the number of stages (n) of a circuit with these multiplexers connected together (one output to the next input) in a combinational path. Remember that each transistor has resistance and capacitance.