Question 1

Produce a schematic design of 2-to-1 non-restoring multiplexer gate using CMOS transmission gates plus other static CMOS gates. Use inputs `{s, d0, d1}` and output `y`. Inverted signals are not provided.

Table 1: The truth table of the 2-to-1 non-restoring multiplexer.

s	d1	d0	y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

Question 2

Draw a sticks diagram of this mux Optimize and count the number of:

1. transistors
2. diffusion regions
3. metal-diffusion contacts

Question 3

Describe how the delay grows with the number of stages (n) of a circuit with these multiplexors connected together (one output to the next input) in a combinational path. Remember that each transistor has resistance and capacitance.