Computer Organization & Architecture Laboratory

Subject Code: PCC-CS492

ASSIGNMENT – II

1. Write the VHDL programs to implement multiplexers: 2:1, 4:1, 8:1, 16:1 (using when / if-else / vector / testbench).

2. Write the VHDL programs to implement de-multiplexers: 1:2, 1:4, 1:8, 1:16 (using when / if-else / vector / testbench).

3. Write the VHDL programs to implement encoder circuits: 8:3, 4:2 and priority encoder

4. Write the VHDL programs to implement binary comparator circuit.

5. Write the VHDL programs to implement magnitude comparator circuit.

6. Write the VHDL programs to implement parity generator and parity checker.

7. Write the VHDL programs to implement flip flop units: SR, JK, D, T.

Note: Write the program in A4 page and draw the simulation result for every individual program. Submit the assignment in channel file.