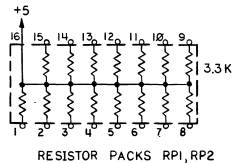
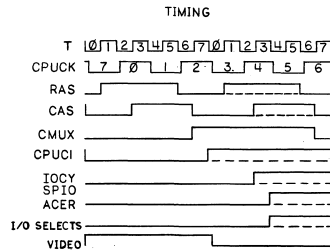
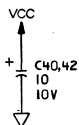
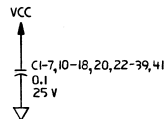
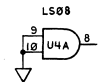
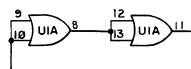


NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS VALUE ARE IN OHMS
1/4 WATT ± 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.



SPARE GATES



REFERENCE DESIGNATIONS		
DEVICE	LAST USED	NOT USED
CR	CR1	
Q	Q2	
J	J1	
R	R19	
C	CH2	
RP	RP2	
SW		
L	L1	
Y	Y1	
DS	DS1	

5-1A	SL0	5-1A	SH0
5-1A	SL1	5-1A	SH1
5-1B	SL2	5-1B	SH2
3-4C	INT0	3-2D	IAK0
3-4C	INT1	3-2D	IAK1
3-4C	INT2	3-2D	IAK2
3-4C	RSIR	3-4C	KBIR
3-1B, 3-4C	IOIR	3-2C	E
	DGND		DGND
	+5		+5
3-2D	RESET	3-2C	CPUCK
3-2D	LDMA	3-4D, 4-2B, 5-2B	BGACK
3-4C	BR	3-3C	BG
3-4A	BD0	3-4A	BD1
3-4A	BD2	3-4A	BD3
3-4A	BD4	3-4A	BD5
3-4A	BD6	3-4A	BD7
3-4B	BD8	3-4B	BD9
3-4B	BD10	3-4B	BD11
3-4B	BD12	3-4B	BD13
3-4B	BD14	3-4B	BD15
	DGND		DGND
	+5		+5
5-2D, 4-2D, 3-2C	A1	3-1C, 4-2D, 5-2D	A2
5-2D, 4-2D, 3-2C	A3	3-1C, 4-2D, 5-4D	A4
4-2D, 3-1C	A5	3-1C, 4-2D	A6
4-2D, 3-2D	A7	3-1C, 4-2D	A8
3-2D	A9	3-1C	A10
5-2B, 3-1C	A11	3-1C, 5-2B	A12
3-2C	VMA	3-4C, 3-2D	VPA
	+12		+12
3-2C, 3-4C	AS	3-4B, 3-2C, 4-4D, 4-4B, 5-4D	DTACK
3-2C	LDS	3-2C	UDS
5-2D, 3-2B	CSYNC	5-1B	INT0
5-2A	VA10B	5-2A	VA9B
2-4A	R1	2-4A	R2
5-4A, 3-4A	MD0	3-4A, 5-4A	MD1
5-4A, 3-4A	MD2	3-4A, 5-4A	MD3
5-4A, 3-4A	MD4	3-4A, 5-4A	MD5
5-4A, 3-4A	MD6	3-4A, 5-4A	MD7
5-4A, 3-4B	MD8	3-4A, 5-4A	MD9
5-4A, 3-4B	MD10	3-4A, 5-4A	MD11
5-4A, 3-4B	MD12	3-4A, 5-4A	MD13
5-4A, 3-4B	MD14	3-4A, 5-4A	MD15
	DGND		DGND
	+5		+5
4-1B	RA1	4-1B	RA2
4-1B	RA3	4-1B	RA4
4-1B	RA5	4-1B	RA6
4-1B	RA7	4-1B	RA8
3-4C	RSTSW	3-1D	A16
3-4C	A17	3-1D	A18
3-1D	A19	3-1D	A20
3-1D	MREAD	4-4B, 5-4A	CAS
5-1D	RAS	2-1C	A29
2-1D	HSYNC	3-2C, 5-1D	HOER
5-2C	VSYSN	3-2C, 5-1D	SFER
5-2D	VTD	3-1C	NW1
5-2C, 3-2B	DGND		DGND
	+5		+5

DEVICE	NAME	+5V	GND	PG#
74LS00	U7C, 6D, 15F	14	7	3, 4, 5
74LS04	U1B	14	7	2, 5
74LS08	U4A	14	7	5
74LS11	U10C	14	7	3
7417	U2E	14	7	3, 5
74LS32	U1A	14	7	2, 4
74ALS32	U2D	14	7	2, 4
74LS38	U7A	14	7	5
74S86	U4D	14	7	2, 5
74LS109	U3A, 2B, 3B, 4B, 3C, 5D, 3E	16	8	2, 4, 5
74LS132	U1E	14	7	2, 5
74LS138	U1D	16	8	2
74LS139	U13F	14	7	5
74LS138	U14F	14	7	5
74LS148	U12F	14	7	3
74LS153	U6E, 7E, 8E, 5F	14	7	4
74LS156	U4F	14	7	3
74LS166	U7F, 8F	14	7	5
74LS169	U1C	16	8	2
74LS244	U8C, 15C, 9E	20	10	3
74LS245	U11A, 11B, 14E, 15E, 9F, 11F	20	10	3, 4
74LS259	U4E	16	8	5
74LS260	U2C, U3D	14	7	2
74LS279	U5C	16	8	3
74F283	U8B, 9B, 10B	16	8	4
74LS373	U9D	20	10	4
74LS374	U6B, 11C, 7D, 11D, 11E, 13E	20	10	3, 4
74LS393	U7B, 5E, 6F	14	7	5
74ALS1002	U6A, U5B	14	7	2, 5
68000	U13A	14, 9, 16, 5, 3		3
ROM SERIAL	U6C	20	10	5
74F10	U5A	14	7	2, 3
74LS161	U8A, 9A, 10B	16	8	4
ROM, HI	U13D	28	14	3
ROM, LO	U14D	28	14	3
556	U15B	14	7	3

REV	ZONE	ECO #	REVISION	DATE	APPRO
A	B097		INITIAL RELEASE		
B	B120		SHEET 1-ADDED CH04 CH2; SHEET 1-5 MISC. CORRECTION TO SHEET-TO-SHEET DESIGNATORS & SIGNAL NAMES.	10/80	APL
C	4D	B136	SHEET 4-2-4C WAS J1-106, 2-3C WAS 2-2D, PCK WAS T5, T4 WAS T3, PIN 15(USD) WAS PIN 11, ADDED RPI-5 TO USD, ADDED PIN 11 TO USD	10/80	APL
D	2B	B142	SHEET 2- SWITCHED PIN NUMBERS 213 AND THEIR TRACES ON U2B. SHEET 3- 341-0175 WAS 374-0070, 341-0176 WAS 374-0071.	10/80	APL
E	B160		SHEET 2- U2B PIN 3 WAS CONNECTED TO U4B PIN 10, 15 NOW U1B PIN 8; REFERENCE REMOVED FROM U1B PIN 2 SHEETS 4 & 5 - MADE MINOR CLARIFICATION CORRECTIONS	10/80	APL
F	4D	B181	5H3-CB WAS 1.0	10/80	APL
H	3A	B202	SH1-R19 WAS R17, 3A ADDED DS1 SH2-ADDED R18 SH3-ADDED R19 SH4-U1C PIN 3 WAS CONNECTED TO GND, ADDED DS1	10/80	APL

METRIC

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DATE: 10/80

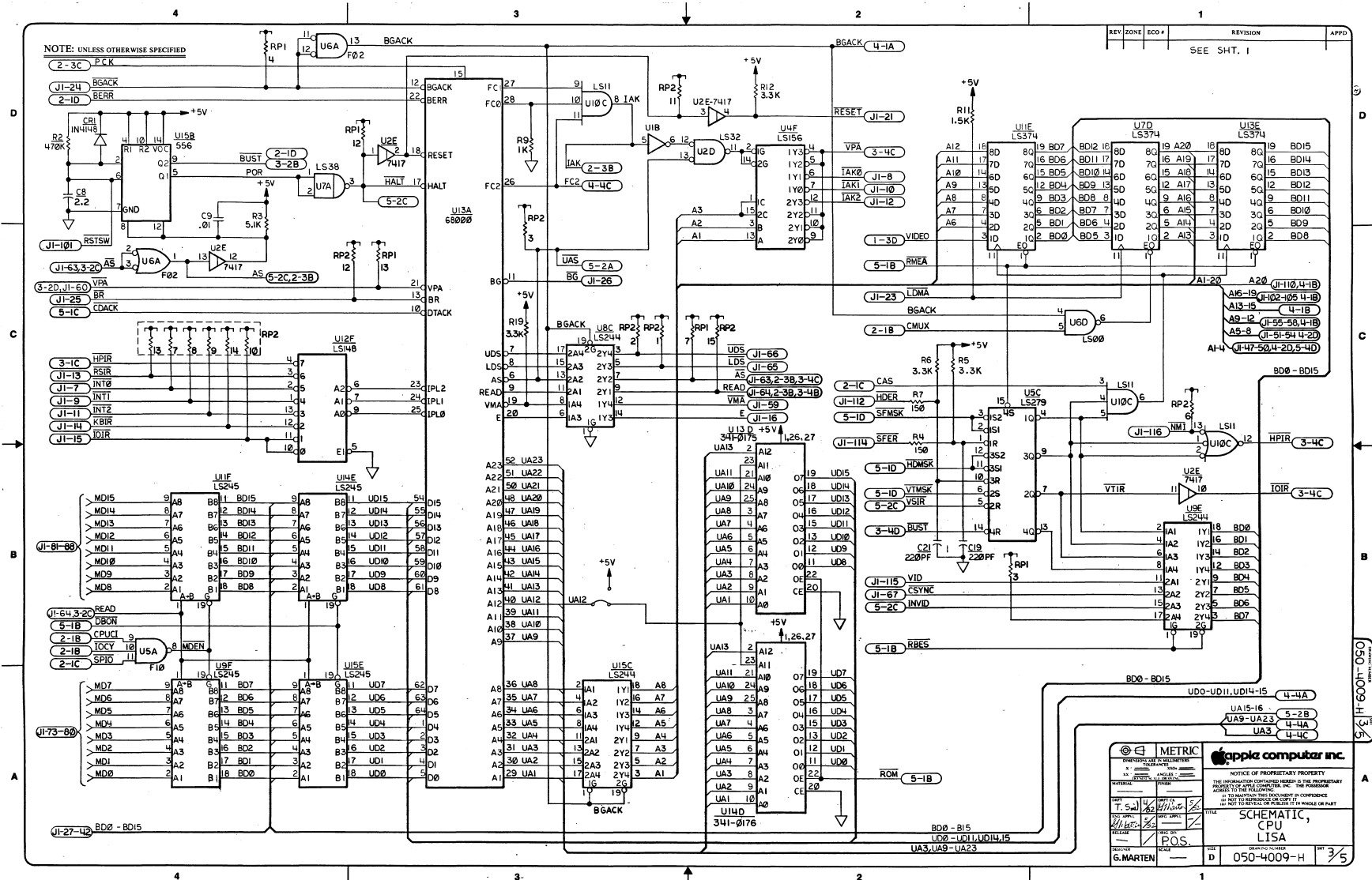
BY: G. MARTEN

FOR: CPU LISA

REV: 1

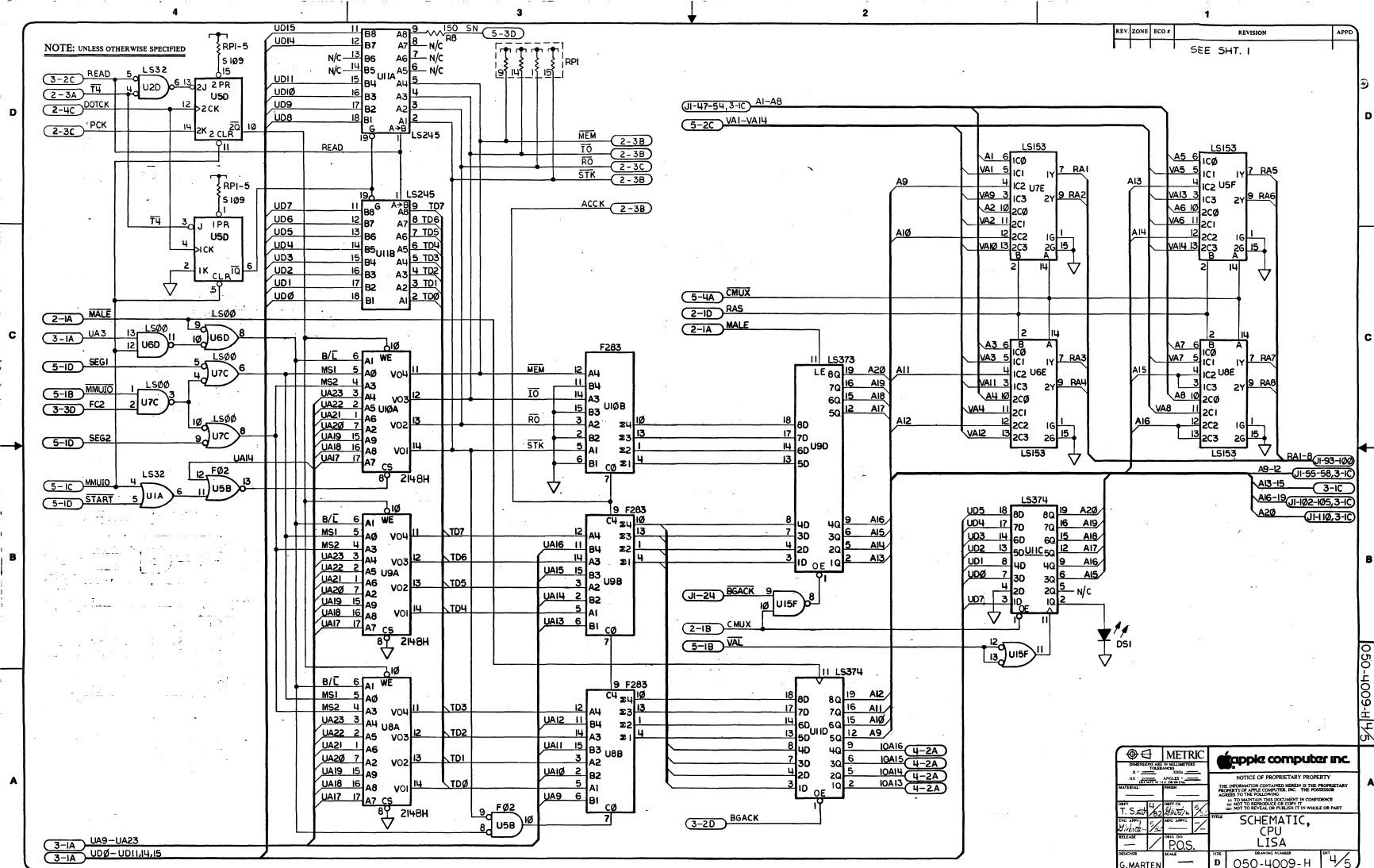
ECO: 050-4009-H

1/5



NOTE: UNLESS OTHERWISE SPECIFIED

REV ZONE ECO # REVISION APPD
SEE SHT. 1



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<p>SCHEMATIC, CPU LISA</p>			
<p>DESIGNED BY: G. MARTEN</p>		<p>DATE: 050-4009-H</p>	

