

**PRODUCT SPECIFICATION**

**PRIAM DS101**

**CONTROLLER**

**Priam Corporation  
20 West Montague Expressway  
San Jose, California 95134  
(408) 946-4600**

**February, 1984**

**300201B**

## PREFACE

### SCOPE

This specification describes the physical interconnection, electrical interconnection, and functional operation of the PRIAM Model DS101 Controller. The DS101 is one of the DELEGATE Series of advanced, intelligent storage subsystem controller products manufactured by PRIAM with a wide variety of interfaces. The Model DS101 utilizes the SMART-T interface. This document provides the technical specifications required to connect the DS101 and Winchester Disc Drives to a host system. Refer to the appropriate Auxiliary Board specification for information on other storage devices.

### APPLICABLE DOCUMENTS

One or more of the following product specifications will be applicable depending on your system configuration:

PRIAM Product Specification 3350, 6650, and 15450  
PRIAM Product Specification 3450 and 7050  
PRIAM Interface Specification  
PRIAM SMART and SMART-E Interface Product Specification  
PRIAM AUX 1 Auxiliary Controller Board Product Specification (QIC-02)

### CONTENTS

Section 1 gives an overview of the features supported by the DS101.

Section 2 describes the physical characteristics, power requirements, and environmental requirements.

Section 3 defines the host bus to DS101 interface including signal definitions and timing requirements.

Section 4 describes the functional interface to the DS101 -- that is, how a programmer would issue commands and receive results.

Section 5 presents all the commands and concepts necessary to operate the DS101 under normal conditions for most applications.

Section 6 presents commands and concepts which provide the capability to control PRIAM Winchester discs at a primitive level, and also includes commands used primarily for system maintenance and diagnostics.

Section 7 discusses error recovery techniques and operation completion status codes.

Section 8 presents device dependent information such as device capacities and transfer rates.

Section 9 presents command summary tables and quick reference information.

## NOTATION

- /// The field must be set to zeros in order to maintain compatibility with future products.
- ??? The contents of the field are undefined.
- The field should not be read or written.
- / A signal is designated active low by placing a slash character (/) after the name of the signal.
- HEX "HEX" indicates that a number is a hexadecimal value.
- MSB "MSB" indicates the most significant byte of a multi-byte value.
- LSE "LSB" indicates the least significant byte of a multi-byte value.
- Within a byte, bits are numbered 7 through 0. Bit 0 is the least significant bit, and bit 7 is the most significant bit.

## TABLE OF CONTENTS

	<b>PAGE</b>	
1.0	INTRODUCTION.....	1-1
1.1	Features.....	1-1
1.2	Compatibility.....	1-3
2.0	PRODUCT DESCRIPTION.....	2-1
2.1	Physical Characteristics.....	2-1
2.2	Power Requirements.....	2-3
2.3	Environmental Characteristics.....	2-3
2.4	Reliability.....	2-3
2.5	Controls.....	2-4
3.0	ELECTRICAL INTERFACE.....	3.1
3.1	Interface Signals - DC Characteristics.....	3-1
3.1.1	HCBUS7 thru HCBUS0.....	3-1
3.1.2	HCBUSP.....	3-1
3.1.3	HAD2, HAD1, HADO.....	3-1
3.1.4	HRD/.....	3-2
3.1.5	HWR/.....	3-2
3.1.6	HRST/.....	3-2
3.1.7	HIR/.....	3-2
3.1.8	BTDIR.....	3-2
3.1.9	DBUSENA/.....	3-3
3.1.10	BTRREQ/.....	3-3
3.1.11	BUSREQ/.....	3-3
3.1.12	BTTYP/.....	3-3
3.2	Interface Signals - AC Characteristics.....	3-9
3.2.1	HCBUS - Host Bus.....	3-10
3.2.2	HAD - Host Address.....	3-10
3.2.3	BTDIR - Block Transfer Direction.....	3-10
3.2.4	BTTYP/ - Bus Transfer Type.....	3-10
3.2.5	BTREQ/ - Block Transfer Request.....	3-11
3.2.6	BUSREQ/ - Bus Request.....	3-11
3.2.7	Timing Diagrams.....	3-11
4.0	FUNCTIONAL INTERFACE.....	4-1
4.1	Host Accessible Registers.....	4-1
4.1.1	Command Register.....	4-1
4.1.2	Block Input and Block Output Registers.....	4-1
4.1.3	Interface Status Registers.....	4-1
4.1.4	Parameter and Result Registers.....	4-1
4.2	Command Types.....	4-2
4.2.1	Register Based Commands.....	4-2
4.2.1.1	Command Initiation Phase.....	4-2

	PAGE	
4.2.1.2	Execution Phase.....	4-3
4.2.1.3	Command Completion Phase.....	4-4
4.2.2	Packet Based Command.....	4-9
4.2.2.1	Transfer Packet Command.....	4-9
4.2.2.2	Resume Packet Execution Command.....	4-12
4.2.2.3	Read Packet Status Command.....	4-13
4.2.2.4	Abort Packet Command.....	4-17
5.0	NOMINAL OPERATIONS COMMAND SET.....	5-1
5.1	Data Transfers.....	5-1
5.1.1	General.....	5-1
5.1.2	Register Based Data Transfer.....	5-2
5.1.2.1	Read Data and Write Data Command Parameters.....	5-4
5.1.2.2	Read Data and Write Data Command Results.....	5-6
5.1.3	Packet Based Data Transfers.....	5-10
5.1.3.1	General.....	5-10
5.1.3.2	Copy Data Packet Parameters.....	5-12
5.2	Formatting.....	5-17
5.2.1	General.....	5-17
5.2.1.1	Interleaving.....	5-18
5.2.1.2	Defect Mapping.....	5-20
5.2.2	Register Based Format Disc Commands.....	5-24
5.2.2.1	Format Disc With Defect Mapping.....	5-24
5.2.2.2	Format Disc Without Defect Mapping.....	5-25
5.2.2.3	Format Cylinder Without Defect Mapping.....	5-26
5.2.2.4	Format Track Without Defect Mapping.....	5-27
5.2.3	Packet Based Format Disc Command.....	5-28
6.0	EXTENDED COMMAND SET.....	6-1
6.1	Winchester Disc Functions.....	6-1
6.1.1	Defect Mapping Command.....	6-3
6.1.2	Specify Bad Sector.....	6-3
6.1.3	Specify Bad Track.....	6-4
6.1.4	Read Defect Directory.....	6-5
6.1.5	Disc Data Initialization and Verification Command.....	6-6
6.1.6	Write Track - Full Track.....	6-6
6.1.7	Write Cylinder - Full Track.....	6-7
6.1.8	Write Disk - Full Track.....	6-8
6.1.9	Verify Track.....	6-9
6.1.10	Verify Cylinder.....	6-10
6.1.11	Verify Disc.....	6-11
6.1.12	Verify Data.....	6-12
6.1.13	Verify ID.....	6-13
6.1.14	Disc Motion and Drive Control Commands.....	6-14
6.1.15	Sequence Down.....	6-14
6.1.16	Sequence Up - Return.....	6-15
6.1.17	Sequence Up - Wait.....	6-16
6.1.18	Seek.....	6-17

	PAGE	
6.1.19	Restore.....	6-18
6.1.20	Winchester Disc Primitive Read/Write Command.....	6-19
6.1.21	Write ID.....	6-19
6.1.22	Read ID.....	6-20
6.1.23	Read ID Immediate.....	6-21
6.1.24	Read Skip Defect Field.....	6-22
6.1.25	Write Skip Defect Field.....	6-23
6.1.26	Read Device Status.....	6-24
6.2	System Function.....	6-26
6.2.1	Software Reset.....	6-26
6.2.2	Specify Mode.....	6-27
6.2.3	Read Mode.....	6-27
6.2.4	Read Device Parameter.....	6-29
6.2.5	Read Device Type.....	6-30
6.2.6	Specify Parameter.....	6-31
6.2.7	Read Parameter.....	6-33
6.2.8	Completion Acknowledge.....	6-34
6.2.9	Clear BTI.....	6-35
6.3	Diagnostic Function.....	6-36
6.3.1	Registor File Wrap.....	6-38
6.3.2	ID Buffer Transfer Test.....	6-39
6.3.3	Read Buffer.....	6-40
6.3.4	Read Buffer - Extended.....	6-41
6.3.5	Write Buffer.....	6-42
6.3.6	Write Buffer - Extended.....	6-43
7.0	ERROR RECOVERY.....	7-1
7.1	Error Retry Technique.....	7-1
7.2	ECC - Error Correcting Code.....	7-2
7.3	Transaction Status Detail.....	7-3
7.4	Software Trap Supplemental Status Detail.....	7-9
7.5	Packet Related Supplemental Status Detail.....	7-11
8.0	DEVICE DEPENDENT HARDWARE REFERENCE.....	8-1
8.1	PRIAM Winchester Disc.....	8-1
8.2	Winchester - DISC Format.....	8-2
8.2.1	Sector Format.....	8-2
9.0	SUMMARY/QUICK REFERENCE.....	9-1

## LIST OF FIGURES

	<b>PAGE</b>
Figure 1-1 DS101 Peripheral Controller for Winchester Disc, Floppy Disc, and Streamer Tape.....	1-3
Figure 2-1 DS101 Outline and Mounting Dimensions.....	2-2
Figure 2-2 Connector and Switch Locations.....	2-5
Figure 3-1 HCBUS Transceiver.....	3-6
Figure 3-2 Single Line Receiver.....	3-7
Figure 3-3 Single Line Driver.....	3-8
Figure 3-4 Register File Read AC Characteristics.....	3-12
Figure 3-5 Register File Write AC Characteristics.....	3-12
Figure 3-6 Buffered Mode Data Request AC Characteristics.....	3-13
Figure 3-7 Direct Mode Data Request AC Characteristics.....	3-14
Figure 4-1 DS101 Register File General Format.....	4-5
Figure 4-2 Interface Status Register Bit Definitions.....	4-6
Figure 4-3 Command Output Sequence Flow Chart.....	4-7
Figure 4-4 Programmed I/O Buffer Transfer Flow Chart .....	4-8
Figure 4-5 Packet Status Report Structure.....	4-14
Figure 5-1 Read and Write Data Commands Structure.....	5-3
Figure 5-2 Device Select Byte Structure.....	5-8
Figure 5-3 Transaction Status Byte Structure.....	5-8
Figure 5-4 Disc Transfer Address Bytes Structure.....	5-9
Figure 5-5 Copy Data Packet Parameters Structure.....	5-14
Figure 5-6 Copy Data Step Control Bytes Structure.....	5-15
Figure 5-7 Sector Header Format.....	5-17
Figure 5-8 Format Disc Packet Parameters Structure.....	5-29
Figure 6-1 PRIAM Device Status Byte.....	6-25
Figure 6-2 Mode Byte Format.....	6-29
Figure 6-3 Option Byte 0.....	6-33
Figure 6-4 Option Byte 1.....	6-33
Figure 7-1 Command Completion Report.....	7-9
Figure 8-3 Track Format.....	8-3

## LIST OF TABLES

	PAGE
Table 2-1 Connector and Cable Types.....	2-1
Table 2-2 DS101 Switches/Controls.....	2-4
Table 3-1 Interface Connector Pin Assignment (J2).....	3-4
Table 3-2 Interface Signal Summary.....	3-5
Table 3-3 Recommended Drivers/Receivers.....	3-5
Table 3-4 HCBUS DC Characteristics.....	3-6
Table 3-5 Single Line Receiver DC Characteristics.....	3-7
Table 3-6 Single Line Drivers DC Characteristics.....	3-8
Table 5-1 ID Control Field Definitions.....	5-19
Table 5-2 Defect Directory Format.....	5-21
Table 5-3 Defect Directory Entry Format.....	5-21
Table 5-4 Recommended Alternate Areas.....	5-21
Table 5-5 Baseline Format Disc Packet Parameter Set.....	5-28
Table 6-1 Device Types.....	6-31
Table 7-1 Error Recovery Strategy.....	7-1
Table 7-2 ECC Characteristics Summary.....	7-2
Table 7-3 Completion Code (Transaction Status Bits 5-0) Definitions...	7-3
Table 7-4 Software Trap Supplemental Status Definitions.....	7-9
Table 7-5 Packet Related Supplemental Status Definitions.....	7-11
Table 8-1 PRIAM Disc Drive Characteristics.....	8-1
Table 8-2 Defect Record Format.....	8-2
Table 8-3 Track Format.....	8-3
Table 8-4 Sector Format Summary - 3350/6650/15450.....	8-5
Table 8-5 Sector Format Summary - 3450/7050.....	8-5
Table 9-1 Command Summary.....	9-1
Table 9-2 Completion Code Summary.....	9-3
Table 9-3 Packet Related Supplemental Status Codes.....	9-4
Table 9-4 Software Trap Supplemental Status Codes.....	9-5

## 1.0 INTRODUCTION

The PRIAM DS101 is an advanced intelligent subsystem whose primary function is to manage the transfer of data between a host processor and storage devices. These may consist of PRIAM fixed Winchester disc drives and a variety of removable-media devices.

### 1.1 Features

The DS101 peripheral subsystem contains an autonomous microprocessor with its own memory, I/O devices, and controllers which provide the host system with an integrated interface to Winchester discs, floppy discs, streaming tapes and start-stop tapes. The bulk of the processing required to support operations on a large variety of storage devices may be delegated to the DS101. It performs all error handling and interface protocol functions with minimal host involvement, either hardware or software.

The command set has been designed to minimize host processor intervention and host bus utilization. Groups of commands may be issued so that direct independent transfers between devices may occur without host bus or memory utilization. During the transfer operation the host may concurrently access devices controlled by the DS101 so that normal operation may continue while backup is occurring.

The DS101 peripheral subsystem is composed of one main board and a maximum of two auxiliary controller boards that mount on connectors on the main board. The DS101 main board has the following features:

- o Downward compatible with the SMART-E.
- o Supports up to four PRIAM Winchester disc drives. Any combination of PRIAM Interface models may be intermixed.
- o Variety of disc formatting capabilities including:
  - a) Logical/physical sector addressing
  - b) Sector interleave
  - c) Head and cylinder interleave
- o Complete host-transparent defect mapping with either on-track sector spares or alternate area assignment or both.
- o Supports up to two auxiliary controller boards for additional peripherals; e.g. tape and floppy operation.
- o Contains a 12K-byte multiport peripheral data buffer.
- o Provides 32-bit ECC (Error Correcting Code) on Winchester disc data.
- o Supports host bus parity.
- o Allows any sector size up to 2K bytes.
- o Automatic defect identification and mapping during normal operations.

The auxiliary controller boards implement a flexible device connection mechanism for the support of a large variety of device types and device manufacturers. Once the devices have been initialized, a common command set may be used to transfer data to and from the devices independent of the particular device type. The command set allows the development of device independent host software.

**FIGURE 1-1. DS101 PERIPHERAL CONTROLLER FOR  
WINCHESTER DISC, FLOPPY DISC, AND STREAMER TAPE**

The DS101 may be configured with auxiliary controller boards that support the following peripherals:

- o Archive Sidewinder (1/4-inch tape, 30/90 IPS, QIC Interface)
- o Cipher Quarterback (1/4-inch tape, 30/90 IPS, QIC Interface)
- o DEI Streamer (1/4-inch tape, 30/90 IPS)
- o Floppy Disc (Industry Standard 8-inch floppy, Single or Double Density)
- o Floppy Disc (Industry Standard 5 1/4-inch floppy, Single or Double Density)

## 1.2 Compatibility

While the DS101 is a PRIAM SMART type interface, there are differences between the DS101 and the earlier SMART-E interface. Some of these differences are listed below.

### a. Deleted Commands

```
05 Read Internal Status  
AE Write Defect Directory  
-- All EPI Tape Commands
```

### b. Added Commands

```
01 Clear BTI  
0B Read Parameters  
0C Specify Parameters  
E4 Read/Write Buffer (Extended)  
B0 Transfer Packet  
B1 Resume Packet Execution  
B8 Read Packet Status  
BF Abort Packet
```

### c. Added Features

- Inter-device transfers (copy)
- Advanced Interleaving Techniques
- On-Track-Sector-Sparing
- Supports Auxiliary Boards for various floppy disk and tape drives
- Expanded multi-port Buffer allows buffered data transfers of one track per disc revolution.
- Automatic Defect management which automatically identifies and reassigns sectors which have developed new defects during normal operations.

### d. Timing Changes

Buffered Mode Data Request - Time from HRD/ or HWR/ trailing edge to next DTREQ/ will occasionally be extended. See Figure 3-7. This is due to the multi-port feature of the Buffer.

e. Dimensions

DS101 is 1" longer than the SMART-E (screw mounting holes still fit the same pattern as the SMART-E).

f. Power

DS101 Draws up to 9 Amps (with two Aux Boards) vs. 5 Amps for SMART-E. DS101 has a different power connector for this reason.

g. Nomenclature

The following signals are equivalent:

<u>DS101</u>	<u>SMART-E</u>	<u>pin</u>
HRST/	RESET/	19
BTDIR	HREAD	23
BTREQ/	DTREQ/	26
HCBUSP	HCBUS8	30

n. Disc Capacity

The DS101 reserves the two inner cylinders of each Winchester disc drive for configuration information. These two cylinders are unavailable to the user. Note that the user data area remains the same as the two cylinders are taken from the alternate area.

## 2.0 PRODUCT DESCRIPTION

### 2.1 Physical Characteristics

The main DS101 assembly (Winchester disc bus control only) is on a single printed circuit board which may be mounted on either a 14-inch or 8-inch PRIAM disc drive. There are three cable connectors: one for the host interface (40 pin ribbon cable), one for the Winchester disc drive interface (50 pin ribbon cable), and one for DC power (4 pins). The host interface cable may be up to 25 feet in length. In addition to the host interface and power connectors, the DS101 contains two 36 pin auxiliary board connectors. A variety of PRIAM auxiliary controller boards are available and two may be installed on the main board to support the operations of selected peripheral devices. The interface connectors and cable types are shown below.

TABLE 2-1. CONNECTOR AND CABLE TYPES

<u>Interface</u>	<u>Connector on DS101</u>	<u>Connector on Interface Cable</u>	<u>Cable Type</u>
Host	3M 3432-13-2 or Berg 65823-085	3M 3417-7040 or Spectra Strip 802-140-002	3M 3476/40 or Spectra Strip 455-276-40
Winchester Disc Drive	3M 3433-1302 or Berg 65847-045	3M 3425-7050 or SAE RD6350-R5C	3M 3365-50
Power	AMP 641737-1	AMP 1-480424-0 with 60619-1 pins	

(TOP VIEW)

(SIDE VIEW - INCLUDING AUX BOARDS)

**FIGURE 2-1. DS101 OUTLINE AND MOUNTING DIMENSIONS**

## **2.2 Power Requirements**

DS101: +5 VDC, +5%, 6.0 AMP maximum (excluding Auxiliary Boards)

### **J-3 Pin Assignments**

<u>Pin</u>	<u>Function</u>
1	Not Used
2	Ground
3	Ground
4	+ 5V

Auxiliary Boards: The Auxiliary Boards are powered via the main PCB.

Streamer Tape Auxiliary Board: +5 VDC, +5%, 1.5 AMP maximum

Floppy Disc Auxiliary Board: +5 VDC, +5%, 1.5 AMP maximum

## **2.3 Environmental Characteristics**

### **TEMPERATURE**

Equipment Operational: 10° C to 45° C (50° F to 113° F).

Equipment Non-operational: -40° C to 60° C (-40° F to 140° F).

### **HUMIDITY**

Equipment Operational: 8% to 80% relative humidity, with a wet bulb temperature limit of 26° C (78° F) without condensation.

Equipment Non-operational: 8% to 90% without condensation.

### **ALTITUDE**

Equipment Operational: From 1,000 feet below sea level to 12,000 feet above sea level.

Equipment Non-operational: From 1,000 below sea level to 40,000 feet above sea level.

## **2.4 Reliability**

### **MTBF**

The DS101 has a mean time between failure (MTBF) of 16,000 power-on hours.

### **MTTR**

The DS101 is a field replaceable unit with a mean time to repair (MTTR) of less than 1/2 hour.

## 2.5 Controls

The DS101 controls are selected through the use of an eight position dip switch. The switches are set to define the power up or reset default configuration of the DS101. All switch selectable functions may also be specified under software control. Refer to section 6.2.6 (specify Parameters) for details. Table 2-2 identifies the switches and the assigned functions. Figure 2-2 shows the location of these switches.

---

TABLE 2-2. DS101 SWITCHES/CONTROLS

<u>SWITCH</u>	<u>Option Byte 0</u>	<u>Bit</u>	<u>FUNCTION</u>
1-4	7-4		These switches must be OFF.
5	3		Automatic Defect Management Disable — If this switch is OFF the DS101 will perform automatic surface analysis (with automatic defect mapping as required) whenever a read operation terminates with an ECC error.
6	2		Enable Initialization Complete Interrupt — If this switch is ON the HIR (Host Interrupt) line will activate when the power up/reset initialization sequence is completed.
7	1		Enable Command Complete Interrupt — If this switch is ON the HIR (Host Interrupt) line will activate when a command is complete.
8	0		Enable Parity — If this switch is ON the host bus parity option is enabled.

---

Note: Switch 1 is closest to Connector J2.

**FIGURE 2-2. CONNECTOR AND SWITCH LOCATIONS**

## **3.0 ELECTRICAL INTERFACE**

### **3.1 Interface Signals - DC Characteristics**

All host bus interface signal connections are via a single 40 pin ribbon cable connector. Table 3-1 shows the connector pin assignments. The DS101 electrical interface is downward compatible with the PRIAM SMART-E interface.

The basic host bus interface is implemented utilizing an 8 bit bidirectional bus, three address lines and two control lines. In addition to the basic bus, other control lines are supported to enable the convenient implementation of interrupt control and host Direct Memory Access (DMA) interfaces.

Table 3-2 is a quick reference for determining signal line DC characteristics.

#### **3.1.1 HCBUS7 thru HCBUS0**

The host bus (HCBUS7 - HCBUS0) is a high-active 8-bit wide bi-directional bus. The most significant bit is HCBUS7. The bus is TRISTATE bidirectional with the drivers in the DS101 enabled when the HRD/ signal is active and the receivers enabled when the HRD/ signal is inactive. These lines are terminated by a 330 ohm resistor to +5V and a 390 ohm resistor to ground on the DS101. These lines are connected directly to an 8304B bus transceiver on the DS101.

Recommended host termination for this bus is a 330 ohm resistor to +5 volts and a 390 ohm resistor to ground. Note: High current drivers (as listed in Table 3-3) are required to drive the HCBUS lines.

#### **3.1.2 HCBUSP**

If the host bus parity option is enabled, data transfers across the host bus (HCBUS7 - HCBUS0 including HCBUSP) must have even parity. The HCBUSP line is a bidirectional line that is received by a 74LS240 and driven by a 75462 on the DS101. The 75462 is enabled by the HRD/ signal. This line is terminated by a 220 ohm resistor to +5 volts and a 330 ohm resistor to ground on the DS101.

Recommended host termination for this signal is a 220 ohm resistor to +5 volts and a 330 ohm resistor to ground.

#### **3.1.3 HAD2, HAD1, HADO**

This is a high active 3-bit wide unidirectional address bus whose function is to select one of eight registers in which data is stored or from which data is read under the control of the HRD/ or HWR/ lines. These lines connect directly to a 74LS240 schmitt-triggered receiver on the DS101 and should be driven by a single line driver such as the 75462.

These signals are terminated at the DS101 with a 220 ohm resistor to +5 volts and a 330 ohm resistor to ground.

### 3.1.4 HRD/

This low active signal is used to gate the contents of the selected DS101 register (decode of HAD2, HAD1, HADO) onto the HCBUS. This line is connected directly to the 74LS240 on the DS101 and should be driven by a single line driver (75462 or equivalent).

The HRD/ line signal is terminated at the DS101 with a 220 ohm resistor to +5V and a 330 ohm resistor to ground.

### 3.1.5 HWR/

This low active signal gates the contents of the HCBUS into the selected register (decode of HAD2, HAD1, HADO) on the DS101. This line is connected directly to a 74LS240 and should be driven by a single line driver.

The HWR/ line is terminated at the DS101 with a 220 ohm resistor to +5V and a 330 ohm resistor to ground.

### 3.1.6 HRST/

This low-active signal resets the DS101 logic. The File Busy bit in the Interface Status register is set while initialization is in process. The HRST/ signal should be used by the host hardware to ensure that the Interface is disabled during the host power-up phase (minimum HRST/ pulse width is 500 ns).

The HRST/ line is received by a 74LS14 receiver and terminated on the DS101 with a 220 ohm resistor to +5 volts and a 330 ohm resistor to ground.

### 3.1.7 HIR/

This low-active signal may be used by the host adapter as an interrupt request that indicates that the DS101 requires host service. The host may specify the events that will result in the activation of the HIR/ signal under software control. Refer to Section 2.5 (Controls) or Section 6.2.6 (Specify Parameters) for details. This signal is driven by the DS101 with a 75462 driver.

Recommended host termination for this signal is a 220 ohm resistor to +5 volts and a 330 ohm resistor to ground.

### 3.1.8 BTDIR

This signal from the DS101 indicates the block transfer direction. If this signal is high, a read (data from the DS101 to the host) is the expected direction. When low, this line indicates that a write (data from the host to the DS101) is expected. This signal is driven by a 75462 driver on the DS101.

Recommended host termination for this signal is a 220 ohm resistor to +5 volts and a 330 ohm resistor to ground.

### **3.1.9 DBUSENA/**

When low, this signal from the DS101 to the host indicates that the DS101 has successfully completed the power up/reset diagnostic and initialization sequence (ready to transfer data).

Recommended host termination for this signal is a 220 ohm resistor to +5 volts and a 330 ohm resistor to ground.

### **3.1.10 BTREQ/**

This low-active signal from the DS101 to the host requests byte transfers across the host bus (HCBUS). This line is active on each byte of a block transfer.

Recommended host termination for this signal is a 220 ohm resistor to +5 volts and 330 ohm resistor to ground.

### **3.1.11 BUSREQ/**

This active low signal is the bus request line. When the DS101 is operated in direct mode (data is transferred at disc speed) this signal should be used to notify the host bus interface that a data transfer will be initiated.

Recommended host termination for this signal is a 220 ohm resistor to +5 volts and 330 ohm resistor to ground.

### **3.1.12 BTYP**

This signal is the bus transfer type indicator. Certain extended DS101 commands require that parameters be passed to the DS101 through its buffer. This line is low if a data transfer is required and high if a control/parameters transfer is required.

Recommended host termination for this signal is a 220 ohm resistor to +5 volts and 330 ohm resistor to ground.

TABLE 3-1. INTERFACE CONNECTOR PIN ASSIGNMENT (J2)

<u>PIN Number</u>	<u>Signal</u>
1	Ground
2	HCBUS0
3	HCBUS1
4	HCBUS2
5	HCBUS3
6	HCBUS4
7	HCBUS5
8	HCBUS6
9	HCBUS7
10	Ground
11	HRD/
12	Ground
13	HWR/
14	Ground
15	HAD2
16	HAD1
17	HADO
18	Ground
19	HRST/
20	Ground
21	HIR/
22	Ground
23	BTDIR
24	DBUSENA/
25	Ground
26	BTREQ/
27	Ground
28	BUSREQ/
29	Ground
30	HCBUSP
31	Ground
32	BTTYP
33	Reserved
34	Reserved
35	Reserved
36	Reserved
37	Reserved
38	Reserved
39	Reserved
40	Reserved

NOTE: The host bus interface should not make any connection to the reserved pins.

**TABLE 3-2. INTERFACE SIGNAL SUMMARY**

<u>SIGNAL NAME</u>	<u>J2-PIN(S)</u>	<u>TYPE</u>	<u>REFERENCE TABLE/FIGURE</u>	<u>DS101 TERMINATION</u>	<u>HOST TERMINATION</u>
HCBUS7-HCBUS0	9-1	I,O		330/390	330/390
HCBUSP	30	I,O		220/330	220/330
HRD/	11	I		220/330	NONE
HWR/	13	I		220/330	NONE
HAD2-HADO	15-17	I		220/330	NONE
HRST/	19	I		220/330	NONE
HIR/	21	O		NONE	220/330
BTDIR	23	O		NONE	220/330
DBUSENA/	24	O		NONE	220/330
BTREQ/	26	O		NONE	220/330
BUSREQ/	28	O		NONE	220/330
BTTYP/	32	O		NONE	220/330

NOTE: 1. Type indicates the DS101 signal type.

- a) I = DS101 Input signal, Host driven
- b) O = DS101 Output signal, Host received
- c) I,O = Bidirectional signal

**TABLE 3-3. RECOMMENDED DRIVERS/RECEIVERS**

<u>Signal</u>	<u>Driver/Receiver</u>
HCBUS7-HCBUS0	AMD, National 8304B or equivalent
All other receivers/HCBUSP	74LS244 or 74LS14 or equivalent
All other drivers/HCBUSP	75461, 75462, 75463 or equivalent

**FIGURE 3-1. HCBUS TRANSCEIVER**

**TABLE 3-4. HCBUS DC CHARACTERISTICS**

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$V_{OL}$	Output Low Level		0.5	V	$I_{OL} = 32 \text{ mA}$
$V_{OH}$	Output High Level	2.4		V	$I_{OH} = -5 \text{ mA}$
$I_{OFF}$	Output Off Current		-0.2 +0.2	mA	$V_{OFF} = 0.45 \text{ V}$ $V_{OFF} = 5.25 \text{ V}$
$V_{IL}$	Input Low Level		0.9	V	
$V_{IH}$	Input High Level	2.0		V	

**FIGURE 3-2. SINGLE LINE RECEIVER**

**TABLE 3-5. SINGLE LINE RECEIVER DC CHARACTERISTICS**

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$V_{IH}$	Input High Level	2.0		V	
$V_{IL}$	Input Low Level		0.80	V	
$I_{IH}$	Input High Level		0.02	mA	$V_I = 2.7V$
$I_{IL}$	Input Low Level		-0.20	mA	$V_I = 0.4V$

FIGURE 3-3. SINGLE LINE DRIVER

TABLE 3-6. SINGLE LINE DRIVER DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$I_{OH}$	Output High Level		0.10	mA	
$I_{OL}$	Output Low Level	300		mA	
$V_{OL}$	Output Low Level		0.8	V	$I_{OL} = 300\text{mA}$

### 3.2 Interface Signals - AC Characteristics

The DS101 supports a hardware interface hierarchy that allows the system designer to determine the level of interface required to meet the particular system environment of the design.

A minimal host bus interface design should use the following signals:

- o HCBUS7-HCRUS0 (Host Bus, bidirectional transfers between host and interface)
- o HAD2-HADO (Address Bus, selects interface registers to be read or written)
- o HRD/ (Host Read, host initiated register read strobe)
- o HWR/ (Host Write, host initiated register write strobe)
- o HRST/ (Reset signal to DS101)

All data is transferred to or from the DS101 on the HCBUS lines under the control of the host-generated HWR/ and HRD/ strobe lines. Figures 3-4 and 3-5 show the register Read and Write AC characteristics.

The minimal system may be enhanced through the use of the optional host bus parity line. If the parity option is enabled, parity is valid for all data transferred across the HCBUS except for reads of the Interface Status Register. The Interface Status Register includes hardware generated signals that change asynchronously to HRD/.

The HRST/ signal should be used by the host hardware to ensure that the DS101 is disabled during the host power-up phase. The HRST/ line is not required during normal operation of the DS101 and should never be asserted under software control.

If the host system includes interrupt processing the HIR/ (Host Interrupt) line may be used. The HIR/ line will activate the host interrupt logic at the completion of a DS101 command. The events that generate a host interrupt request may be selected either by the host under software control or by switches on the DS101.

Commands and parameters are usually transferred to the DS101 through the use of programmed I/O. Under programmed I/O the host processor is in direct control of the I/O operation. Many of the commands also require a block transfer phase which may transfer large blocks of information. Programmed I/O transfers of large blocks of information generally are very slow. In order to realize the high performance capabilities of the DS101 and Winchester disc drives, it is recommended that the host bus adapter support Direct Memory Access (DMA) for the block data transfer phase of the operation.

When the host bus interface designer implements Direct Memory Access logic the following signals will be required.

- o BTDIR (Block Transfer Direction, to or from Host)
- o BTTYP (Bus Transfer Type, data or control parameters)
- o BTREQ (Block Transfer Request)

Figure 3-6 shows the host bus timing required when the DS101 block transfers are performed by a DMA interface and the DS101 is operated in buffered mode.

In addition to buffered mode, the DS101 may also be operated in direct mode. The host software may specify that all Winchester disc transfers be performed without the use of the DS101 data buffer. Direct Mode requires a host bus interface that is capable of transmitting and receiving the data at disc speed. If direct mode is used the BUSREQ signal should function as an input to the host adapter DMA logic. Figure 3-7 shows the host bus timing required when the DS101 data transfer is performed in direct mode.

In general, host bus interfaces should use the buffered mode.

### **3.2.1 HCBUS - Host Bus**

The 8-bit HCBUS is generally an extension of the host processors' data bus.

### **3.2.2 HAD - Host Address**

The 3-bit HAD bus is usually an extension of the three least significant bits of the host processors' address bus.

### **3.2.3 BTDIR - Block Transfer Direction**

This signal is an input to the host DMA logic that indicates the direction (Read or Write) of the requested transfer. If this signal is high, the host adapter should issue a HRD/ (buffer data transfer from the DS101 to the host) to the buffer data register (Address 01). If this signal is low, the host adapter should issue a HWR/ (buffer data transfer from the host to the DS101) to the buffer data register (Address 01).

### **3.2.4 BTTYP - Bus Transfer Type**

This signal may be used to select one of two possible host DMA channels. Certain extended DS101 commands require that control parameters be passed to the DS101 through its internal buffer. The host adapter may elect to support two DMA channels; one channel would be dedicated to normal data transfer and the other channel dedicated to control parameter transfers. This signal is not required if a single DMA channel is used to support both types of buffer transfers.

### **3.2.5 BTREQ/ - Block Transfer Request**

This line is an input to the host DMA control logic that indicates that a byte of data is ready for transfer either into or out of the DS101 buffer.

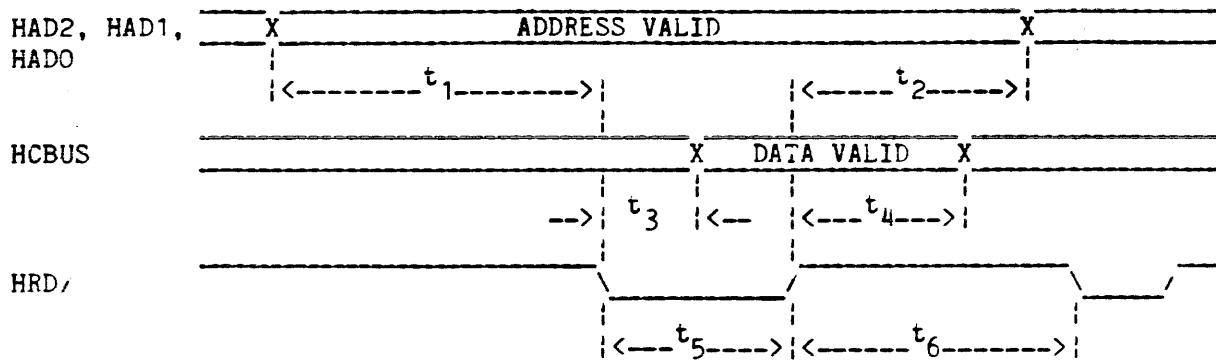
### **3.2.6 BUSREQ/ - Bus Request**

The BUSREQ signal is an early indication that a data transfer will be required. This signal should cause the host DMA logic to acquire the host processor bus so that the host DMA logic may respond quickly when the first buffer transfer request occurs. This is usually necessary for direct mode data transfers and may be used in buffered mode for performance enhancement if delays are encountered when acquiring the host bus.

### **3.2.7 Timing Diagrams**

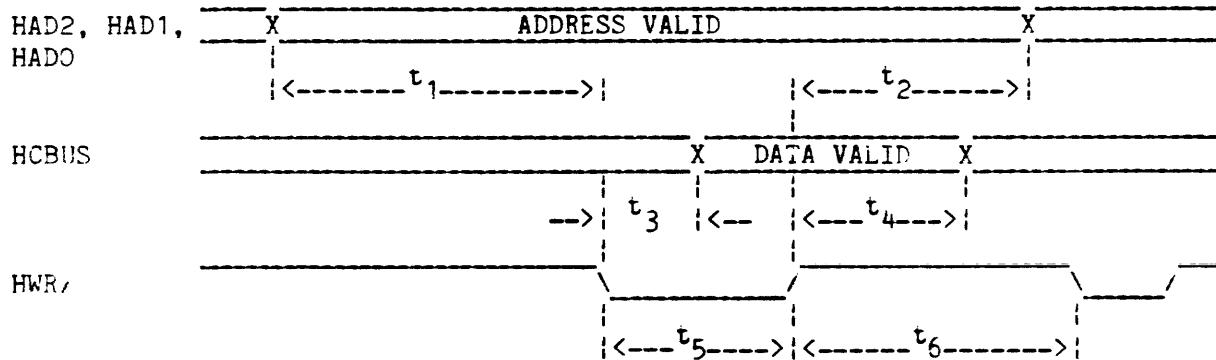
The timing relationships between the interface signals are divided into 2 categories. Figures 3-4 and 3-5 show the relationships between the register address signals, the HCBUS and the read and write strobes during a register file non-data read or write. Figures 3-6 and 3-7 depict the relationships between the read and write strobes and the BTREQ/ and BUSREQ/ during a data read or write operation (buffered and direct mode). The user should also be aware that concurrent accesses (e.g. - Reading data from a disc to the host during a disc to tape copy operation) will impact some of these timing relationships. This is due to the multi-ported buffer design which is one of the features which provide the enhanced performance of the DS101.

**FIGURE 3-4. REGISTER FILE READ AC CHARACTERISTICS**



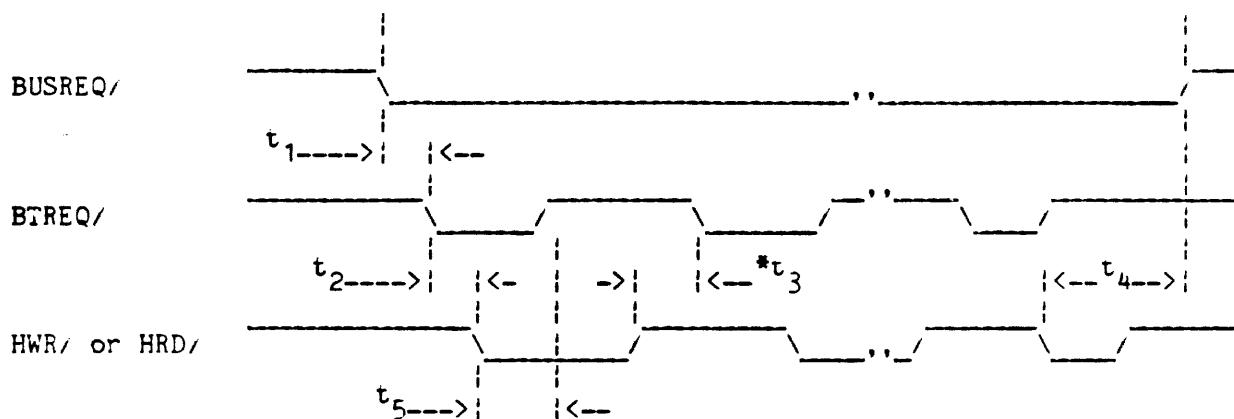
<u>Symbol</u>	<u>Parameter</u>	<u>Min</u>	<u>Max</u>	<u>Units</u>
$t_1$	Address stable before HRD	60		ns
$t_2$	Address hold time for HRD	0		ns
$t_3$	Data valid from HRD		120	ns
$t_4$	HRD to Bus Tristate condition		40	ns
$t_5$	HRD pulse width	180		ns
$t_6$	HRD recovery time	180		ns

**FIGURE 3-5. REGISTER FILE WRITE AC CHARACTERISTICS**



<u>Symbol</u>	<u>Parameter</u>	<u>Min</u>	<u>Max</u>	<u>Units</u>
$t_1$	Address stable before HWR	60		ns
$t_2$	Address hold time for HWR	0		ns
$t_3$	Write data valid from HWR		30	ns
$t_4$	Data hold time for HWR	0		ns
$t_5$	HWR pulse width	180		ns
$t_6$	Recovery time between HWR	180		ns

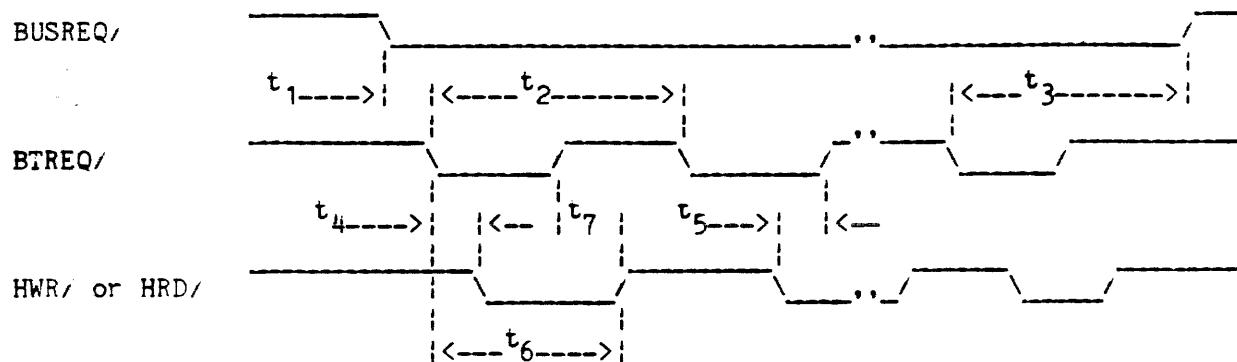
FIGURE 3-6. BUFFERED MODE DATA REQUEST AC CHARACTERISTICS



<u>Symbol</u>	<u>Parameter</u>	<u>Min</u>	<u>Max</u>	<u>Units</u>
$t_1$	Bus Request before Data Request	0		ns
$t_2$	Data Transfer Request to HWR, HRD	0		ns
$t_3$	Request Complete to next Request (mean)	300		ns
$t_4$	Bus Request Release Time		250	ns
$t_5$	Buffered Request Delay		250	ns

\* $t_3$  will occasionally be extended in order to allow a buffer access by the microprocessor. The normal value for  $t_3$  is 268 ns. The extended value is 536 ns. The mean value will not exceed the max value listed above.

**FIGURE 3-7. DIRECT MODE DATA REQUEST AC CHARACTERISTICS**



<u>Symbol</u>	<u>Parameter</u>	<u>Min</u>	<u>Max</u>	<u>Units</u>
t <sub>1</sub>	Bus Request before Data Request	12		us
t <sub>2</sub>	Byte Request to Byte Request	800	1500	ns
t <sub>3</sub>	Last Data XFER Request to Bus Rel	4		us
t <sub>4</sub>	Data Transfer Request to HWR, HRD	0		
t <sub>5</sub>	Request Release Time		250	ns
t <sub>6</sub>	Maximum Host Response Time		500	ns
t <sub>7</sub>	HWR - HRD Hold Time	0		

## **4.0 FUNCTIONAL INTERFACE**

This section describes the protocol required to issue commands, receive results, and communicate with the DS101.

### **4.1 Host Accessible Registers**

The host communicates with the DS101 across an 8-bit bidirectional bus (HCBUS) through eight addressable (via HAD2-HAD0) registers collectively known as the "Register File". Some of the registers have specific, fixed functions while the others are used on an "as needed" basis to transfer variable information. Figure 4-1 shows the locations of the registers and the following sub-sections describe the functions of the registers.

#### **4.1.1 Command Register**

This register is written by the host, read by the DS101 and contains the command code of a requested operation. Writing a value to this register causes the command and parameter registers to be copied into the DS101 internal memory and initiates the operation specified by the data written into the command register.

#### **4.1.2 Block Input and Block Output Registers**

These registers are used to transfer blocks of data between the host and the DS101. The content of these blocks may be control information (commands and parameters or status) or data read/written from peripheral devices.

Transfers occur one byte at a time via this register and may utilize DMA depending on the user's host bus adapter.

#### **4.1.3 Interface Status Register**

This register is read by the host, written by the DS101 and contains information required to control host-to-DS101 and DS101-to-host accesses. The control information is used in establishing the control/data exchange protocol as described later in this section. Figure 4-2 shows the format and defines the content of the Interface Status Register.

#### **4.1.4 Parameter and Result Registers**

These registers contain variable information dependent upon the command specified in the Command Register. Examples of the type of information which the Parameter Registers may contain are; device select, operation count, etc. Examples of the type of information that the Result Registers may contain are; completion status, residual operation count, etc.

## 4.2 Command Types

The DS101 supports two types of command: register based commands and packet based commands.

### 4.2.1 Register Based Commands

Register based commands are initiated by writing a command code into the command register. There are six other registers, called parameter registers, which may or may not be defined for each command. The parameter registers must have the appropriate data written to them prior to writing to the command register. The parameter registers may contain information such as sector, head, cylinder and drive addresses, number of blocks to be transferred, etc.

In order to describe the protocol involved in communicating with the DS101, it is convenient to consider each command as proceeding in three phases:

- o Command Initiation Phase - During this phase the host specifies the operation that is to be performed by the DS101.
- o Execution Phase - During this phase the DS101 performs the operation it was instructed to do.
- o Command Completion Phase - After completion of the operation, status and other housekeeping information are made available to the host.

Note: Any of these phases may require a block transfer, which is described below.

The following subsections describe each phase in detail.

#### 4.2.1.1 Command Initiation Phase

DS101 commands are initiated when a command is written to the Command Register in the Register File. Prior to issuing the command, the host must output the parameters associated with the command to the parameter registers in the Register File. If register addresses 2 through 7 are written by the host, parameters 0 through 5 are updated. The parameter registers are used to send information to the DS101 that will be processed when a command is issued. The content of the parameter registers depends on the type of command that is issued. The DS101 cannot modify the content of its parameter registers.

The DS101 does not normally sense the host writing to the parameter registers. When the host writes to the Command Register (Address 0) the DS101 generates an internal hardware notification that a command is ready to be processed. When a command is written to the Command Register the Register File Busy bit in the Interface Status Register will be set under hardware control. The Register File Busy bit is cleared by the DS101 after the information in the Command and Parameter registers has been copied into the DS101 local memory. The Register File Busy bit is cleared before the command is complete so that the host may use the Register File to issue overlapped commands.

The host may not write to the Command or the Parameter registers while the Register File Busy bit is active. Figure 4-3 is a flow chart that displays a typical command output sequence.

Both command types are initiated whenever the host writes to the Command Register, but packet based commands require the Transfer Packet command (see Section 6.7). When the DS101 receives this command, it allocates space in its internal memory, and prepares the hardware and Interface Status Register for a block transfer of the packet command block.

#### 4.2.1.2 Execution Phase

Depending upon the command, this phase may require a block transfer; e.g. Transfer Packet and Read Data commands.

The Block Input/Output Register (Address 1) shown in Figure 4-1 provides a means of transmitting or receiving blocks of data. Multiple writes to the Block Register cause data to be sequentially written into the DS101 buffer. Multiple reads of the Block Register cause data to be sequentially read from the DS101 buffer. Prior to requesting a block transfer the DS101 initializes the hardware required to select the correct data for the transfer.

Two types of transfers occur through multiple accesses of the Block Register; namely, data transfers and control parameter transfers. DS101 packet based commands require lists of parameters that are passed through the Block Register. Most commands require the transfer of host data to or from the DS101. Bit 0 of the status register shown in Figure 4-2 indicates the type of block transfer required.

The three low order bits of the Interface Status Register are used to control software data transfers. The block transfer bit (bit 2) becomes active when a transfer is required. Bit 1 indicates the direction of the request (transmit or receive) and bit 0 indicates the type of transfer that is required. Figure 4-4 is a flow chart of a typical data transfer software routine.

The host interface designer may elect to control the data transfers to and from the Block Register through the use of the host processor (programmed I/O) or through the use of high speed hardware logic (Direct Memory Access). Use of the programmed I/O transfer technique will result in a low performance, low cost host adapter. Because the data transfer rate will be very slow, this method of implementation is not recommended.

#### 4.2.1.3 Command Completion Phase

After the DS101 has performed the requested command the host must be provided with information that indicates the outcome of the operation. Command completion information is passed to the host through the Register File result registers under control of the Interface Status Register. After the DS101 has written to the result registers, the Command Completion Request bit is set. If register addresses 2 through 7 are read by the host, result registers 0 through 5 are accessed. The format of the result registers depends on the type of command that was issued by the host. Note that if the Transaction Status (usually posted in result register 0) indicates a good completion, the data in the remaining result registers may not be meaningful.

Once the host has copied the command completion information out of the Register File, the host must notify the DS101 that the result registers are available for the next command completion. This is done by sending a Completion Acknowledge command (command code 00 HEX). The Completion Acknowledge command is issued to the DS101 in the same manner as any other command except that this command does not have any parameters and will not generate a completion request. The Command Completion Request bit is reset by the Completion Acknowledge command.

Under software control the host may elect to initiate the command completion phase through an interrupt generated by the DS101 (HIR). See the Specify/Read Parameters commands for details.

**FIGURE 4-1. DS101 REGISTER FILE GENERAL FORMAT**

COMMAND INITIATION (HWR)							REGISTER ADDRESS (HAD2, HAD1, HADO)							COMMAND COMPLETION (HRD)						
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0					
COMMAND							0	INTERFACE STATUS												
BLOCK OUTPUT							1	BLOCK INPUT												
PARAMETER 0							2	RESULT 0												
PARAMETER 1							3	RESULT 1												
PARAMETER 2							4	RESULT 2												
PARAMETER 3							5	RESULT 3												
PARAMETER 4							6	RESULT 4												
PARAMETER 5							7	RESULT 5												

### COMMAND INITIATION

#### **COMMAND**

The Command register is used to specify the operation that should be performed. Writing to this register initiates the operation.

#### **BLOCK OUTPUT**

Data is transferred from the host to the DS101 Buffer through successive host writes to the Block Output register.

#### **PARAMETER 0 - PARAMETER 5**

The parameter registers are used to specify additional information about the command that is to be processed. This information must be written prior to writing to the command register

### COMMAND COMPLETION

#### **INTERFACE STATUS**

The Interface Status register contains information which is necessary for the control of host to Register File, Register File to host, and Block transfers.

#### **BLOCK INPUT**

Data is transferred from the DS101 Buffer to the host through successive host reads from the Block Input register.

#### **RESULT 0 - RESULT 5**

The result registers are used to supply additional information about commands that have been processed. These results are normally valid only if an error condition has occurred.

FIGURE 4-2. INTERFACE STATUS REGISTER BIT DEFINITIONS

7	6	5	4	3	2	1	0
???	CCR	SCF	BTI	RFB	BTR	BTD	BTT

**CCR — COMMAND COMPLETION REQUEST**

The CCR bit indicates that the DS101 has posted status and results to the result registers and that the host should read the result registers to determine the outcome of the requested operation. CCR will be cleared when the host issues a Completion Acknowledge Command.

**SCF — SPECIAL COMPLETION FLAG**

SCF is set along with CCR if the completion request is for a command that may be overlapped with a device command. Commands that set SCF are identified in the command descriptions.

**BTI — BLOCK TRANSFER INTERRUPT**

If the block Transfer Interrupt status bit is active the host has selected the interrupt on block transfer option and a block transfer request has occurred. The Block Transfer Interrupt may be cleared by issuing a Clear BTI command to the interface (command code = 01).

**RFB — REGISTER FILE BUSY**

The RFB bit indicates that a command has been written into the Command Register and that the DS101 has not completed the process of copying the command and parameters into local memory. RFB is a hardware generated bit that is set coincident with writing into the Command Register.

**BTR — BLOCK TRANSFER REQUIRED**

When utilizing programmed I/O block transfers, the BTR bit indicates that a read or write of the Block Register is required.

**BTD — BLOCK TRANSFER DIRECTION**

When utilizing programmed I/O block transfers, an active Block Transfer Direction (BTD) flag indicates that a host read of the Block Register is required. If this flag is inactive a host write of the Block Register is required.

**BTT — BLOCK TRANSFER TYPE**

When utilizing programmed I/O block transfers, the Block Transfer Type (BTT) flag identifies the transfer request (BTR) as either a control parameter or data transfer request. If this bit is active a data transfer is required. If this bit is inactive a control parameter transfer is required.

FIGURE 4-3. COMMAND OUTPUT SEQUENCE FLOW CHART

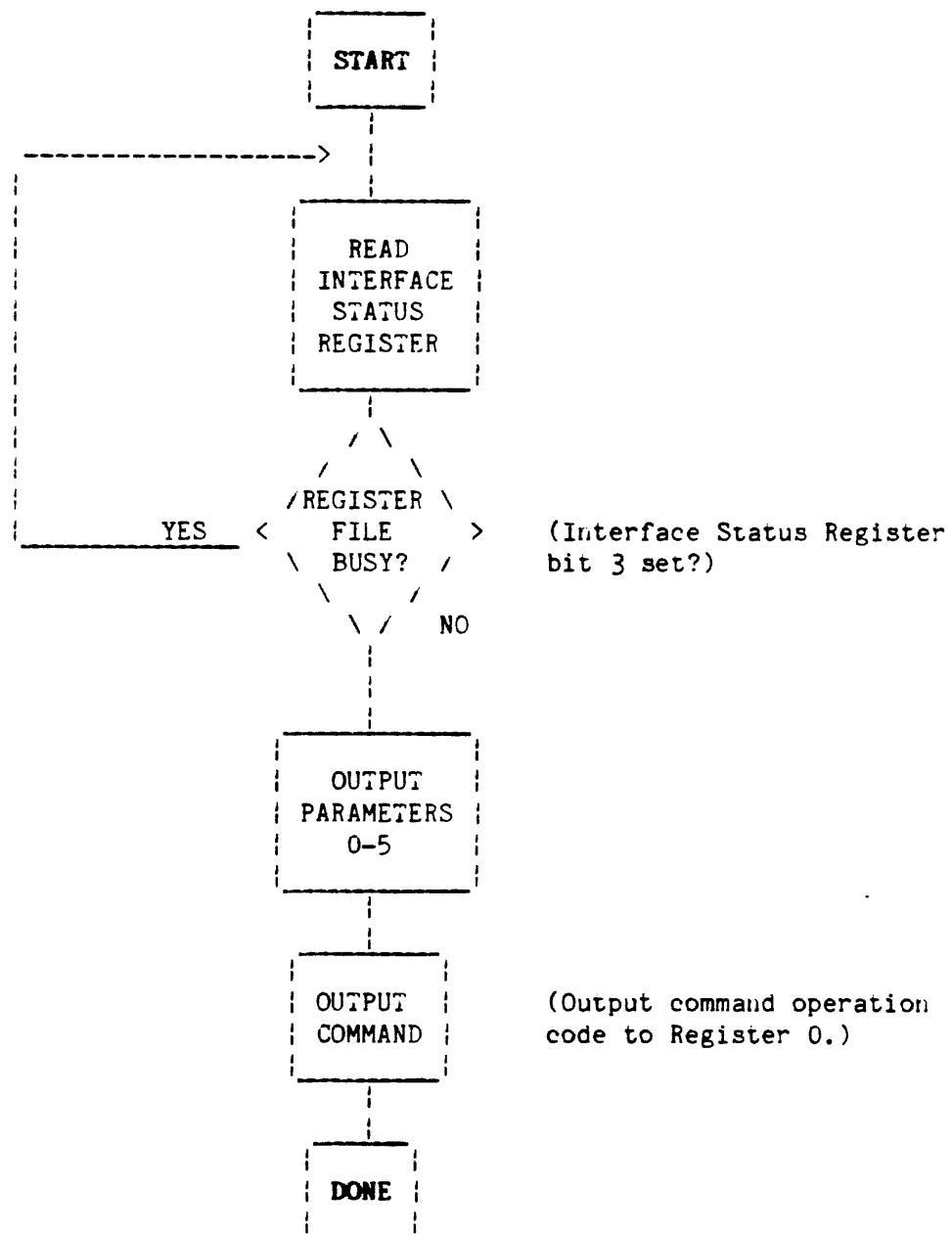
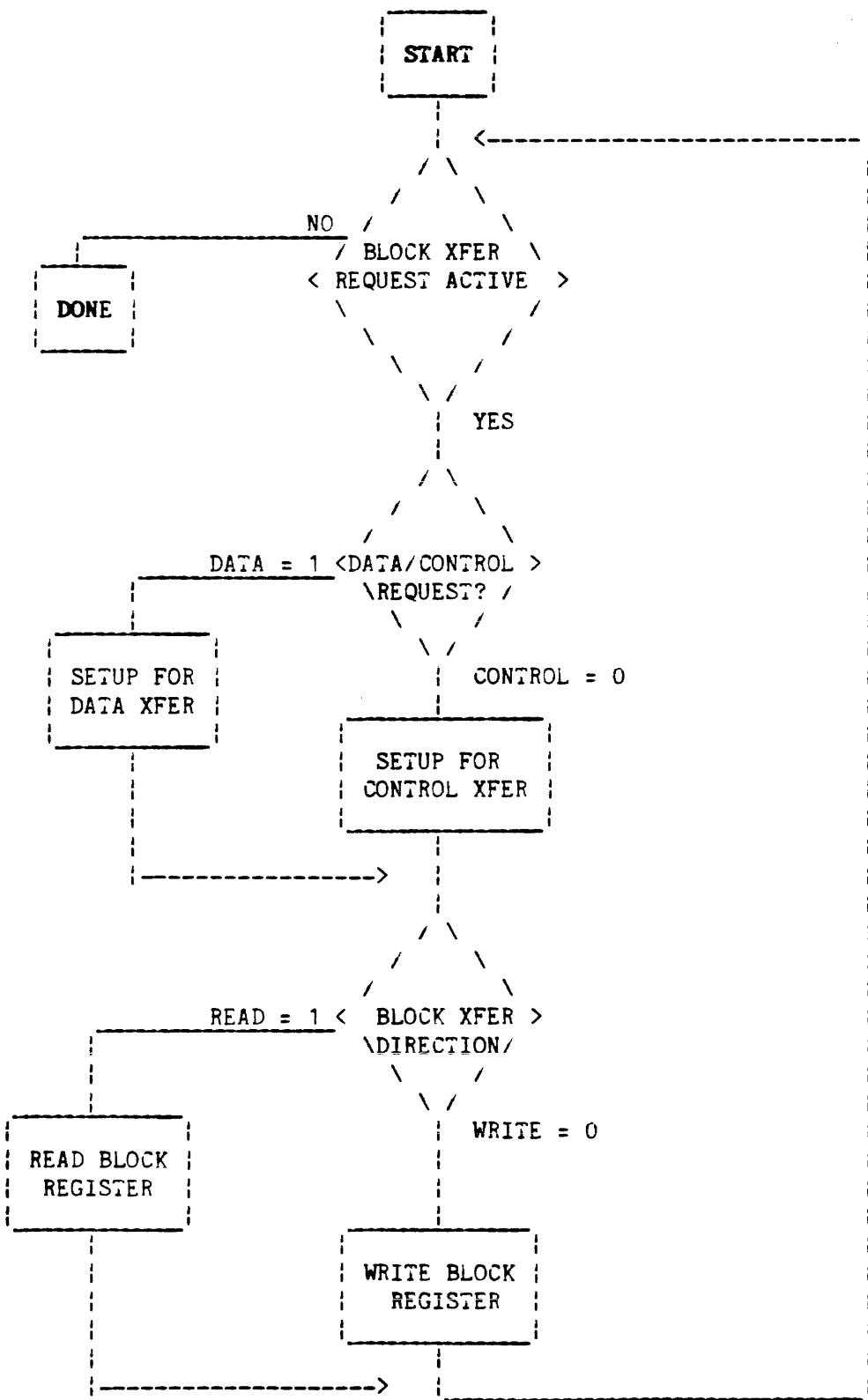


FIGURE 4-4. PROGRAMMED I/O BUFFER TRANSFER FLOW CHART



#### 4.2.2 Packet Based Commands

Packet based commands are initiated by issuing the register based Transfer Packet command. The execution phase of this command consists of a block transfer whose length (in bytes) was specified by the Transfer Packet command. The information in the block transfer is the packet based command/parameters. This section describes four register based commands which can be used to control packet based functions.

(The two packet based commands are discussed in Section 5)

##### 4.2.2.1 Transfer Packet

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = B0 HEX	0	7 0
BLOCK OUTPUT		INTERFACE STATUS
PACKET ID		---
///		* TRANSACTION STATUS
PACKET LENGTH	MSB LSB	PACKET RELATED SUPP. STATUS
///	—	???
		TDF
		TERMINATION DEVICE SELECT
		1   0   PACKET ID

\* Packet Completion Status only

##### FUNCTION

The Transfer Packet command is used to initiate all packet based commands. It notifies the DS101 to allocate memory for holding the packet and causes the DS101 to initiate a transfer of the packet data. After the packet has been transferred, the packet based commands are executed without further host intervention. There are 512 bytes available to store packets in the DS101. As many packets as desired may be transferred with one Transfer Packet command (up to 512 bytes total). Once a Transfer Packet command has been done, no more packets may be transferred until all of the current packets have been completed. Each individual set of packet parameters is referred to as a "step". Steps are performed in the order in which they were sent.

##### **PACKET ID**

Packet ID is the identification number for the packet that the host will be sending. The range is 00 - 3F HEX. This number is used (by both the host and the DS101) for all subsequent references to the packet. As of June 1983 only Packet ID = 0 is supported.

##### **PACKET LENGTH**

Packet Length is the number of bytes in the command packet to be sent by the host to the DS101. Maximum length is 512 bytes.

### **TRANSACTION STATUS (Packet Completion)**

When packet execution stops, for whatever reason, it will be indicated by a transaction status value of 08, 28, or 29, denoting the following:

- 08 This termination status arises when all commands in a packet have been executed to completion.
- 28 The packet is resumable. The host may issue a Resume Packet command to restart packet execution. This normally occurs when an end of media condition has been encountered, or if the source device is a tape and the "hold step on EOF mark" has been set. A packet that terminates in this state will not reach final completion until one of the following occurs:
  - a It is resumed and allowed to reach a terminal condition (for example, Winchester full).
  - b It is aborted via the Abort Packet command.
  - c It is replaced with another packet having the same Packet ID.
  - d It is retired due to old age (about 15 minutes after terminating in a resumable state).
- 29 The packet has been prematurely terminated due to a fatal error. Specific details can be obtained by issuing a Read Packet status command.

### **PACKET RELATED SUPPLEMENTAL STATUS**

This byte provides supplemental status information when applicable. Possible values are given in Table 9-3. A value of FF indicates that there is no supplemental status.

### **TDF — TERMINATION DEVICE FLAG**

This flag identifies the device that caused the termination. It is provided to distinguish an input versus an output operation as the cause of the termination when the same device is both source and destination (for example, when making inter-disk copies). This flag is not set and is not valid unless the same device is both source and destination.

- 0 Destination
- 2 Neither/not applicable
- 3 Source

### **TERMINATION DEVICE SELECT**

This byte contains the device select code corresponding to the device that caused the packet execution to terminate. This field is not applicable if the Termination Device Flag = 2.

### **PACKET ID**

Packet ID is the identification number for the packet that has terminated. As of June 1983 only Packet ID = 0 is supported.

#### 4.2.2.2 Resume Packet Execution

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7	0	0
COMMAND = B1 HEX		
---		
PACKET ID		
RESUME (H/C) (S) MSB	0	
ADDRESS (C) (S)	1	
(S) (S) LSB	2	
///   DF	3	NO COMPLETION IS
///	4	GENERATED FOR THIS
	5	COMMAND
	6	
	7	

#### FUNCTION

The Resume Packet Execution command is used to restart a packet that has suspended execution because of an error, or because one of the devices involved in a Copy Data operation has reached the end of its media. This command allows the operation to be restarted without sending the packet again. The resume address parameter allows the host to skip header information on floppies or to resume at a point past a sector containing an ECC error.

The Resume command normally has no command completion result registers, since termination is associated with the packet command being restarted. However, if any of its parameters are illegal then a packet completion will occur with appropriate termination status values. The packet that the host intended to resume will still be resumable/not resumable as determined by the transaction status.

#### **PACKET ID**

Packet ID is the identification number for the packet that is to be resumed. The range is 00 - 3F HEX. This number is used (by both the host and the DS101) for all subsequent references to the packet. As of June 1983 only Packet ID = 0 is supported.

#### **RESUME ADDRESS**

Contains the start address to be used for the device specified by the Device Flag when packet execution is restarted. A value of FF in each byte indicates a restart at the location given in the Packet Status Report. This normally (unless an error occurred) is the sector past the last sector accessed during packet execution. Resume addresses are ignored for streamer tapes since they are assumed to be prepositioned by the host system before the Resume command is issued.

#### **DF — DEVICE FLAG**

Specifies the device to which the Resume Address refers:

- 0 Destination device
- 3 Source device

The device flag is ignored if a Resume Address is not specified (ie., resume address = FF, FF, FF).

A Device Flag (rather than the Device Select) is used, since the same device may be both source and destination in the packet step that is being restarted.

#### 4.2.2.3 Read Packet Status

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = B8 HEX	0	0
---		
PACKET ID		7 INTERFACE STATUS
---		1 BLOCK INPUT
---		2 TRANSACTION STATUS
---		3 PACKET RELATED SUPP. STATUS
---		4
---		5 ???
---		6
---		7
		1   0   PACKET ID

#### FUNCTION

This command causes the DS101 to transfer the status of the specified packet from the DS101's internal buffer to the host. The structure of the information transferred is shown in Figure 5-9. This command will be rejected if a non-existent Packet ID is specified. The Read Packet Status command is normally sent after packet termination.

Note that packet status cannot be read during execution of steps that have the host specified as the source or destination device.

#### **PACKET ID**

Packet ID is the identification number of the packet for which a status report is desired. As of June 1983 only Packet ID = 0 is supported.

#### **PACKET RELATED SUPPLEMENTAL STATUS**

Supplemental status is set to a value in Table 9-3 if a command reject transaction status is returned. At the present time the only reason for rejecting this command is if an illegal or non-existent packet ID is specified.

FIGURE 4-5. PACKET STATUS REPORT STRUCTURE

BYTE	7	6	5	4	3	2	1	0
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								
16								
17								
18								
19								
20								
21								
22								
23								
24								
25								
26								
27								
28								
29								
30								
31								
32								
33								
34								
35								

**PACKET ID**

The packet identification number for the packet whose status is being reported.

**PACKET STATE**

A code number identifying the current packet execution state as follows:

- 01 Packet being transferred. The DS101 is still waiting to receive the number of bytes specified in the Packet Length field of the associated Transfer Packet command.
- 02 Packet being executed.
- 03 Packet waiting for a Resume Packet Execution command.
- 04 Packet in the process of resuming.
- 05 Packet preparing to wait for a Resume Packet Execution command.
- 06 Packet in the process of terminating.
- 0A Packet aborted due to Abort Packet command or 15 minute timeout.
- 0D Packet completed not resumeable (does not indicate good or bad completion).

**TDF — TERMINATION DEVICE FLAG**

A flag indicating which device caused a packet termination.

- 0 Destination
- 2 Neither/not applicable
- 3 Source

**PRIMARY TERMINATION STATUS**

The Transaction status which indicates the primary cause of Packet termination. Usually either the source or destination Transaction Status. See Table 9-2.

**SUPPLEMENTAL TERMINATION STATUS**

Supplemental Status is a function of certain Transaction Status codes which may appear as Primary Termination status. A value of FE Hex indicates that no supplemental status is given.

**PACKET OFFSET**

The number of bytes from the beginning of the DS101's internal buffer to the first byte of the packet. This value could be used in a Read Buffer command to read back the packet parameters.

**PACKET LENGTH**

The number of bytes in the packet.

**CURRENT STEP OPERATION CODE**

The operation code associated with the current step. Used for diagnosing packet errors.

**CURRENT STEP NUMBER**

Identifies the step currently being executed. Step numbers start at 1 and continue incrementing by 1 for each completed step. At packet completion this value is one greater than the number of steps in the packet. Used for diagnosing packet errors and assessing packet execution progress for multi-step packets.

**TOTAL NUMBER OF SECTORS/RECORDS COPIED**

The number of sectors/records transferred for all copy steps in the packet. This number is incremented based on the number that have been output to the destination device. It is updated only at the completion of each output operation, and does not include any sectors/records that may be in the process of being output.

**SOURCE DEVICE SELECT**

Identifies the device selected as the source of the data to be copied. Conforms to the standard device select format.

**SOURCE TRANSACTION STATUS**

Contains the transaction status for the source device. (See Table 9-2)

**SOURCE SUPPLEMENTAL STATUS**

Contains supplemental source device status. A value of FE HEX indicates no supplemental status is given.

**SOURCE TRANSFER ADDRESS**

Contains the current transfer address associated with the source device. At the termination of the packet this address is one sector/record past the last sector input. This address will be used if the packet is resumed unless overridden by the Resume parameters. This address is formatted in the mode (logical or physical) specified in the step control field (ELM).

**NUMBER OF SOURCE DEVICE SECTORS/RECORDS INPUT FOR CURRENT COPY STEP**

A four byte value giving the number of sectors/records read from the source device during execution of the current step. This value is updated at the completion of each input operation, and consequently does not include any sectors/records currently in transit from the source device to the DS101's buffer.

Since the DS101 does large multi-sector reads from the source device during step execution, this value may lag the actual number transferred by a value up to the number of sectors per cylinder. However, the Source Transfer Address is updated for each sector and will be much closer to the actual "in transit" address.

**DESTINATION DEVICE DATA**

Items associated with the destination device have descriptions analogous to the corresponding items for the source device.

#### 4.2.2.4 Abort Packet

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = FF HEX	0	0
---	0	0
PACKET ID	1	0
---	2	0
---	3	0
---	4	0
---	5	0
---	6	0
---	7	0
///	---	---

#### FUNCTION

The Abort Packet command forces the termination of a packet operation that is either currently executing or waiting to be resumed. Command completion will not occur until all devices involved in the currently executing packet step (in the specified packet) have been stopped.

Aborting a packet that has already reached completion or is non-existent will cause a command reject.

Packet execution may not be restarted with the Resume Packet Execution command after an Abort Packet command. The Read Packet Status command may be executed after an Abort Packet command to determine how much data was transferred up to the time of the abort.

Command completion format conforms to the standard packet termination format.

#### **PACKET ID**

Packet ID is the identification number of the packet that is to be aborted. As of June 1983 only Packet ID = 0 is supported.

## 5.0 NOMINAL OPERATIONS COMMAND SET

This section discusses the DS101 commands that provide the capability for accessing data. These include both register based and packet based commands for transferring data and formatting.

The host system may direct the DS101 to perform the following two types of transfers:

- o Transfers between the host memory and a selected storage drive.
- o Transfers between two selected storage devices without host intervention.

Transfers of the first type are usually done with register based Read and Write commands, although a packet based Copy command could also be used. Transfers between devices are only requested with the packet based Copy command.

Many formatting variations are also available. Formatting may be done with or without defect mapping, with or without several levels of interleaving, and with or without on-track-sector-sparing. These various formatting variations are selected through either a register based Format command or, for the more advanced/optimized formats, a packet based Format command.

### 5.1 Data Transfers

#### 5.1.1 General

There are several important parameters which must be defined in order to transfer data. Among these are the following:

- a. The two devices between which data will flow.
- b. The direction of the data transfer.
- c. The location on the devices at which the transfer will begin.
- d. The amount of data to transfer.

For all register based Read and Write commands, the host memory is defined as one of the ends of the transfer path. Also, the DS101 is not informed of the location in host memory at which the transfer begins (although a DMA host adapter would be given this information).

This reduces the number of parameters required to transfer data between the host and a storage device to the following:

- o The device with which the host will interact (one byte)
- o The direction of the data transfer (one byte)
- o The location on the selected device at which the transfer will begin (3 bytes)
- o The number of data blocks to transfer (one byte)

Since a register based command has seven registers available (6 parameter registers and one command register), a Read data or Write data command will fit.

If a data transfer between two storage devices is desired, four more bytes of data are required at the minimum, in order to specify both the second device (one byte), and the location on the second device where the transfer will begin (3 bytes).

This much information cannot be contained in a register based command. To implement a Copy command, a register based Transfer Packet command is sent. This command initiates a data transfer which can contain as much information as required. See Section 4.2.2 for details on this command. This also allows more options to be available with a Copy command.

Many of these options have to do with controlling the copy process when a backup device (such as a floppy disk or streaming tape) is full (end of media condition) and needs to have another tape or diskette inserted.

### 5.1.2 Register Based Data Transfer

The Read Data and Write Data commands are register based commands used to transfer data between the host and devices connected to the DS101. The data is transferred in accordance with the parameters specified in the Register File at the time the command is issued (see Figure 5-1). The command is initiated by writing the command into the command register.

Upon command initiation the DS101 verifies parameters and performs any operations required to prepare the selected device for data transfer (e.g. sequence up, seek, fault reset on a disc).

The DS101 will position the device to the specified transfer start address; i.e. an implied seek is performed. If a Write Data command was issued and the buffered mode is enabled then the DS101 will begin transferring data from the host to its internal buffer while the seek is taking place. As soon as the seek is complete and at least one sector of data has been transferred the write operation will be initiated. For a multi-sector Read Data command in the buffered mode the data will begin to be transferred to the host as soon as the first sector has been successfully input to the DS101's internal buffer. Subsequent sectors will be transferred as they arrive so data may be simultaneously entering and exiting the DS101.

The DS101 will handle multi-sector operations that cross track boundaries. The required processing such as incrementing to the next sector, head switches, seeking to the next cylinder when necessary, and restarting the read/write operation, is handled in a manner that is transparent to the host (except for the possible delays in the data flow).

The basic operation of the Read or Write Data commands may be modified through the use of the mode byte. A complete definition of the mode byte is presented in the System Functions section of this specification (Section 6.2). The mode byte format is shown in Figure 6.2. After a reset, the mode byte is cleared to zero by the DS101. If the host system software utilizes logical sector addressing, mode byte bit 6 should be set.

**FIGURE 5-1. READ AND WRITE DATA COMMANDS STRUCTURE**

**READ DATA**

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 53/43 HEX*	0	7 0 INTERFACE STATUS
—	1	1 BLOCK INPUT
DEVICE SELECT	2	2 TRANSACTION STATUS
—	3	— MSB
TRANSFER START ADDRESS	4	4 — TRANSFER END ADDRESS
—	5	5 — LSB
OPERATION COUNT	6	6 RESIDUAL OPERATION COUNT
///	7	7 DEVICE SELECT RESULT

**WRITE DATA**

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 52/42 HEX	0	7 0 INTERFACE STATUS
BLOCK OUTPUT	1	1 —
DEVICE SELECT	2	2 TRANSACTION STATUS
—	3	— MSB
TRANSFER START ADDRESS	4	4 — TRANSFER END ADDRESS
—	5	5 — LSB
OPERATION COUNT	6	6 RESIDUAL OPERATION COUNT
///	7	7 DEVICE SELECT RESULT

\* When two hex values for a command are given, the first will usually be for enabled retries and the second for the same command with retries disabled.

It is recommended that retries be enabled during normal operation.

### **5.1.2.1 Read Data and Write Data Command Parameters**

The parameters associated with the Read Data and Write Data commands conform to the nominal descriptions presented in this section. These parameters are used in many (though not all) register based commands.

The common fields are shown in Figures 5-2 through 5-4.

Common fields usually associated with the issuance of a command are:

- o The destination or source device.
- o The number of operations required.
- o The location on the device where the transfer is to begin (if a data transfer is involved).

#### **DEVICE SELECT**

The format of the device select field is displayed in Figure 5-2. Devices may be attached to the PRIAM Interface channel, Auxiliary Channel 0 or Auxiliary Channel 1. Within a channel, the specific device is selected by the unit number. The PRIAM Interface channel may be configured with any combination of PRIAM 8-inch or 14-inch Winchester discs. The devices that attach to the PRIAM bus contain switches that determine the unit number of the device. Each device on the bus must have a unique unit number between 0 and 15. The Auxiliary channels support a variety of auxiliary controller boards that may be configured according to the host system requirements. The units attached to the auxiliary controller boards must also have a unique unit number between 0 and 15. The DS101 command set includes commands that may be used by the host system software to conveniently determine the physical and logical configuration of the units attached to the peripheral subsystem (see Section 6).

## TRANSFER START ADDRESS

The transfer start address defines the location on the disc at which the specified operation will begin. While not all operations require the same level of addressing (sector, head, cylinder), all commands which require a transfer start address specify three bytes of addressing. It is recommended that non-required fields within the transfer start address be filled with zeroes.

All read and write transfer operations utilize physical or logical addressing mode (absolute addressing is required when issuing certain extended Winchester disc commands discussed in Section 6). The DS101 interprets a transfer address as physical or logical depending on the current mode established for the selected device.

There are three types of addressing used to identify a location on the disc(s):

- o Absolute Addressing
- o Physical Addressing (See Figure 5-4)
- o Logical Addressing (See Figure 5-4)

Absolute addressing identifies a location by specifying a head address, cylinder address, and sector address. The head addresses run from 0 to N-1, where N is the number of read/write heads on the drive; each possible value represents a particular head. The cylinder addresses run from 0 to T-1, where T is the number of tracks per disc surface; each possible value represents a particular cylinder, with 0 at the outer edge of the usable disc surface. The sector addresses run from 0 to S-1, where S is the number of sectors per track; each possible value represents a definite sector, and the sectors are numbered consecutively. The sector addresses increase as the disc rotates; sector 0 is the first sector after the Skip Defect Record.

Physical addressing uses the same format (head, cylinder, sector) as absolute addressing, but the physical address of a given sector may be different from that sector's absolute address. There are two factors leading to such differences -- defect mapping, and interleaving (see Section 5.2).

Logical addressing allows the host system to view the disc storage space as a sequential list of sectors numbered from 0 to the total number of usable sectors minus one on the drive.

Logical sectors are ordered such that logical sector 0 corresponds to sector 0 of cylinder 0 under head 0. The next logical sector is found by incrementing the sector number by one. If the new sector number is equal to the number of available sectors on a track then the head number is incremented and the sector number is reset to 0. If the new head number is equal to the number of heads on the drive then the cylinder number is incremented and the head number is reset to zero.

For example, if the drive has three heads and has been formatted with 18 user accessible sectors per track (spare sectors are not user accessible) then logical sectors correspond to physical sectors as follows:

<u>logical sectors</u>	<u>sectors</u>	<u>head</u>	<u>cylinder</u>
0-17	0-17	0	0
18-35	0-17	1	0
36-53	0-17	2	0
54-71	0-17	0	1
72-89	0-17	1	1
:	:	:	:
.	.	.	.

When the DS101 reports results to the host system, it translates the physical address back into a logical address if required by the current mode byte for the particular device.

#### OPERATION COUNT

This one byte field specifies the number of consecutive operations that are requested. The interpretation of the number in this field is dependent upon selected device type and the specified command.

Examples are:

- a) Sectors, cylinders, or tracks for disc devices.
- b) Blocks, records, or files for tape devices.

If the command specified involves data transfer, each successful operation will cause the device operation count to be decremented. The command will continue until either the operation count goes to zero, an unrecoverable error occurs or the end of media is encountered on the device. Remember that the value in the parameter register itself is never modified. The operation count is stored and decremented internally on the DS101.

An initial operation count of zero is illegal.

#### 5.1.2.2 Read Data and Write Data Command Results

Common fields usually associated with a command completion are:

- o The completion status (Transaction Status).
- o The residual count.
- o The destination or source device.
- o The location on the device where the transfer ended (if a data transfer was involved).

## **TRANSACTION STATUS**

The Transaction Status indicates the result of the requested command. During the command completion phase the Transaction Status should be read and tested by the host processor. The Transaction Status is composed of the unit number, the completion type, and the completion code. If the completion type (see Figure 5-3) is zero the command was successfully completed (a good completion is an exception to this rule).

The DS101 automatically performs error retry and recovery, therefore the software designer should assume that a non-zero completion type indicates a fatal error. The completion code may be utilized to obtain information required for diagnosing errors. Table 5-1 defines the various completion codes and Section 7.3 gives a more complete description of each completion code.

## **TRANSFER END ADDRESS**

The transfer end address will contain the address of the sector in error if the transfer was unsuccessful. This result should only be used by host disc diagnostics and logic required for fatal error recovery. The format of the transfer end address is the same as for the transfer start address (see Figure 5-4).

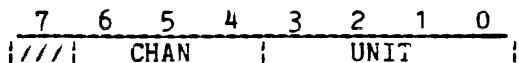
## **RESIDUAL OPERATION COUNT**

This field is zero if a command was successfully completed. Otherwise it contains the number of operations remaining to be performed.

## **DEVICE SELECT RESULT**

The device select result is returned so that host software may associate the reported status with the command issued in cases when multiple commands are outstanding at one time. This field has the same format as the Device Select field.

**FIGURE 5-2. DEVICE SELECT BYTE STRUCTURE**



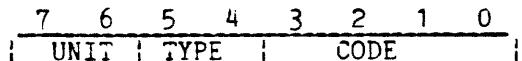
**CHAN** — Devices connected to the DS101 are attached to a channel. Channel assignments are as follows:

Channel	
0	PRIAM Interface Bus
1	Auxiliary Bus 0
2	Auxiliary Bus 1
3	Host Memory
4	Special Function
5-7	Rewind

**UNIT** — ID number corresponding to the number set by switches on the device. This number must be unique for each device on a given channel. Up to sixteen units may be selected within a channel.

---

**FIGURE 5-3. TRANSACTION STATUS BYTE STRUCTURE**



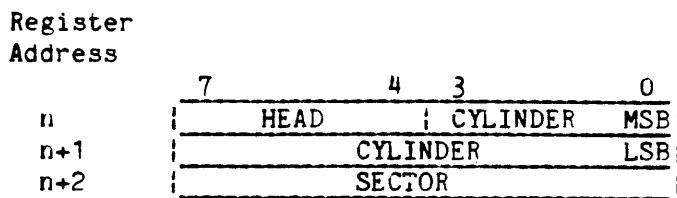
**UNIT** — The unit field is a copy of the least significant two bits of the specified Device Select parameter and is included for SMART-E compatibility. The full Device Select parameter is returned in register 7.

**TYPE** — The completion type field indicates the major class of the completion status.

Type	Class
0	Good Completion
1	System Error or Initialization Complete
2	Operator Intervention
3	Command or Device Error

**CODE** — The completion codes provide a detailed definition of the command completion. A summary of completion codes is given in Table 9-2.

**FIGURE 5-4. DISC TRANSFER ADDRESS BYTES STRUCTURE**



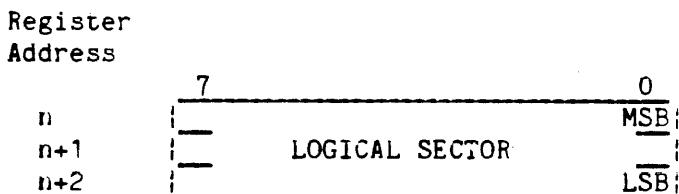
PHYSICAL/ABSOLUTE ADDRESS FORMAT

**HEAD** — Heads are numbered consecutively, starting with zero.

**CYLINDER (MSB)** — This field contains the upper 4 bits of the cylinder address (bits 11, 10, 9, 8). Cylinders are numbered consecutively, starting with zero.

**CYLINDER (LSB)** — This field contains the eight least significant bits of the cylinder address.

**SECTOR** — This field is the sector address. Within a given track, logical sectors are numbered consecutively, starting with sector zero.



LOGICAL ADDRESS FORMAT

**LOGICAL SECTOR** — The Logical Sector address is a three byte value where register n specifies the most significant byte (bits 23-16), register n + 1 specifies the middle byte (bits 15-8) and register n + 2 specifies the least significant byte (bits 7-0).

### 5.1.3 Packet Based Data Transfer (Copy Command)

#### 5.1.3.1 General

The packet based Copy Data command allows the transfer of data between devices connected to the DS101. A key aspect of this command is that it does not utilize the host processor, the host memory, or the host data bus once the Copy Data command has been initiated. This allows the host to continue to access the disc during copy operations.

The Copy Data command is a packet based command that is primarily used for backup and restore operations. However, since disc to disc transfers are allowed, it may also be used to copy files within a single drive or from one drive to another. Copy Data operations, once started, take place without host processor intervention so the host may continue to access the drives while the backup/restore/copy operation is occurring.

Each set of Copy Data parameters (see Figure 5-5) is assumed to refer to a logically contiguous segment on the source and destination devices. (A "contiguous segment" on a PRIAM drive is equivalent to a span of logical sectors, see Section 5.1.2.1). Copy Data parameters may be concatenated so that multiple segments may be transferred via a single command packet. This allows files consisting of multiple non-contiguous extents to be backed up or restored with little host overhead. Each 16 byte packet is referred to as a "step".

If, for example, a file is to be restored from a backup tape (which can be treated as one large logically contiguous segment) then the host system must know the available storage areas on the destination drive and their lengths (in sectors). One 16 byte set of Copy Data parameters is generated for each logically contiguous area on the destination disc. These sets of Copy Data parameters, or steps, are concatenated to form the command packet to be sent to the DS101. Only one command packet may be issued at a time.

The Copy Data operation is initiated by sending a Transfer Packet command to the DS101 via the Register File. The DS101 will then request a control parameters transfer for the number of bytes specified in the Transfer Packet command. This control data must contain a series of Copy Data command(s) and parameters that define the source device, destination device, source start transfer address, destination start transfer address, the number of sectors to be transferred and step control parameters. These fields are described in Section 5.1.3.2.

Normally there will be one Copy Data command for each logically contiguous segment on the source or destination device. If any segment contains more than 65535 contiguous sectors then multiple Copy Data commands will be required for that segment. Note that an entire device may be transferred with a single Copy Data command by setting the transfer length parameter to zero. However, unless the two devices involved in the Copy Data operation have the same capacity, the transfer will be terminated whenever the lower capacity device reaches its limit. In this case the host will be sent an appropriate special completion status message (see Section 4.2.2.1) defining which device caused the termination. It is then the hosts' responsibility to initiate another Copy Data command packet or to resume the operation from the

point of termination with a Resume Packet Execution command (see Section 4.2.2.2). This mechanism allows the host to prompt the operator for another tape cassette or floppy disc before the operation is continued.

Transfer of data between devices connected to the DS101 is handled without host processor intervention. The DS101 automatically steps to the next set of parameters in the packet as it completes each set. This process continues until one of the following conditions is encountered:

- a) The specified number of sectors have been transferred for all sets of Copy Data parameters in the packet (nominal termination).
- b) The specified number of consecutive file marks have been read from a source tape.
- c) The end of tape is found.
- d) The source disc is empty; i.e. last sector of the source disc has been read and transferred to the destination device.
- e) The destination disc is full; i.e. last sector of the destination disc has been written.
- f) An error has occurred on either the source or destination device and the host specified a "terminate on error" condition in the Copy Data parameters.

Any termination of a Copy Data operation, since it can happen asynchronously to normal host operations, causes the special completion bit to be set (as well as the completion request bit) in the DS101 status word. The Register File can then be accessed to determine the termination status for the packet operation. The structure of the status returned is shown in Section 4.2.2.1. Status of the entire packet may be obtained by issuing a Read Packet Status command (see Section 5.2.2.3).

If the Copy Data operation has terminated prematurely (i.e. before all specified data has been transferred) then it may be resumed from the point of termination with the Resume command, provided that the Resume command is issued within 15 minutes of the premature termination and the packet terminated in a resumable state. Using this command allows the host to continue Copy Data operations without reference to the termination address and facilitates the backup/restore operation when multiple backup media are required. The Resume command is interpreted as being applicable to the current Copy Data packet so the host must not send another command packet before the current one has completed execution unless the host does not intend to resume the existing packet.

A packet that has terminated in a resumable state (ie., transaction status = 28 HEX) will hold on to certain DS101 internal resources (eg., a portion of the data buffer) and will consequently slow system response. It is advisable to abort any packets that have terminated in this state when it is known that they will not be resumed.

### **5.1.3.2 Copy Data Packet Parameters**

The following sections define the parameters that form a Copy Data packet command. These parameters are graphically shown in Figure 5-5.

#### **COPY DATA OPERATION CODE**

This parameter is a code number equal to 01 HEX that identifies the following 15 bytes as Copy Data parameters.

#### **STEP CONTROL**

The bit fields in these parameters provide control information for the Copy Data operation, and also determine the actions to be taken when errors are detected in either the source device or the destination device, or when an end of file (EOF) mark is encountered on the source device. Figure 5-6 describes the fields within these parameter bytes.

#### **TRANSFER LENGTH**

The transfer length is the number of blocks that are to be counted from the device specified by the OCD bit in Step Control Byte 0. If one of the devices is a streamer tape or the host, and the other device is a disc, the transfer length indicates the number of blocks that should be copied to/from the disc. If a disc is not involved in the transfer, then this field must be set to 0.

If this field is 0 then the transfer will terminate when any one of the following conditions occur:

- a) End of tape is encountered.
- b) A tape file mark is encountered.
- c) The last track on the source disc has been transferred.
- d) The last track on the destination disc has been written.

Note that a transfer length value of 0 will cause the Copy Data operation to continue until a device is full/empty. That is, a transfer length of 0 would be the normal value if an entire disc is to be backed up or restored.

#### **SOURCE DEVICE SELECT**

This parameter selects the device from which the data to be transferred will be read. The format of this byte conforms to the standard Device Select format. Additionally, a value of 30 HEX may be used to specify the host as the source device (i.e., an extended Write Data command).

#### **SOURCE TRANSFER ADDRESS**

This parameter specifies the starting address on the source device for the transfer operation.

The address format depends on the device addressing mode specified in Step Control Byte 1. These formats conform to the standard Transfer Start Address formats.

<u>Mode</u>	<u>Byte</u>	<u>Format</u>
Physical	7	Head/Cylinder MSB
	8	Cylinder LSB
	9	Sector
Logical	7	Logical Sector MSB
	8	Logical Sector
	9	Logical Sector LSB

A tape (and the host) is assumed to be positioned to the specified start address before the Copy Data commands are executed. Consequently, this address is ignored for tapes (and the host).

#### **DESTINATION DEVICE SELECT**

Selects the device to which the data will be written. The format of this byte conforms to the standard Device Select format. Additionally, a value of 30 HEX may be used to specify the host as the destination device (i.e., an extended Read Data command).

#### **DESTINATION TRANSFER ADDRESS**

This group of three bytes specifies the starting address on the destination device for the transfer operation. See "Source Start Address" above for applicable formats.

**FIGURE 5-5. COPY DATA PACKET PARAMETERS STRUCTURE (one step)**

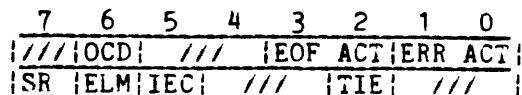
BYTE	7	6	5	4	3	2	1	0	
0					01	HEX			
1					///				
2	/// OCD	/// EOF	ACT ERR	ACT					STEP CONTROL 0
3	SR ELM IEC	/// TIE	///						STEP CONTROL 1
4	NUMBER OF SECTORS/RECORDS								TRANSFER LENGTH
5									
6	TO TRANSFER							LSB	
7	///  SRC CH#   SRC UNIT #								SOURCE DEVICE SELECT
8	SOURCE (H/C)	(S)						MSB	SOURCE TRANSFER ADDRESS
9	TRANSFER (C)	(S)							
10	ADDRESS (S)	(S)						LSB	
11					///				
12	///  DST CH#   DST UNIT #								DESTINATION DEVICE SELECT
13	DESTIN (H/C)	(S)						MSB	DESTINATION TRANSFER ADDRESS
14	TRANSFER (C)	(S)							
15	ADDRESS (S)	(S)						LSB	

One Copy Data Command Packet may contain as many as 32 sixteen-byte steps of Copy Data Packet Parameters (see Section 4.2.2.1).

#### FUNCTION

The Copy Data packet command allows data to be copied between various devices connected to the DS101. The specified number of sectors will be read from consecutive sectors on the source device starting at the specified transfer address and written to consecutive sectors on the destination device starting at its specified transfer address. The source and destination device may be the same device provided that the device is a disc. If the host is the source or destination device then overlapped reads/writes via the normal register based commands are not possible.

**FIGURE 5-6. COPY DATA STEP CONTROL BYTES STRUCTURE**



**OCD — OPERATIONS COUNTING DEVICE**

The device (source or destination) specified by this bit determines when the step is complete, according to the number of sectors transferred. The operation counter in the specified device is added to the TOTAL NUMBER OF SECTORS COPIED counter in the Packet Status Report.

- 0 Source device
- 1 Destination device

**EOF ACT — END OF FILE ACTION**

Determines the action taken when an end of file (EOF) mark is encountered on the source device.

- 0 Terminate step and execute next step.
- 1 Hold step. Terminate, but allow the host to resume with the tape positioned after the EOF mark. This must be the EOF ACT value when inputting more than one streamer tape.
- 2 Terminate step after the second consecutive EOF mark.
- 3 Hold step after the second consecutive EOF mark.

**ERR ACT — ERROR ACTION**

Determines the action taken when an error is encountered.

- 0 Terminate step and execute next step.
- 1 Hold step. Terminate, but allow the host to resume from the point of error or at a specified address.
- 2 Terminate packet. Terminate the current step and bypass all remaining steps.
- 3 Ignore ECC errors on the source device and continue execution. Works in conjunction with TIE bit as follows:

<u>MODE</u>	<u>error action</u>
TIE ERR ACT	
0 not 3	Terminate, hold, etc. based on other error action value. Action taken as soon as error is detected.
0 3	Deletes/skips sectors with ECC errors on the source device. Sectors with ECC errors are not copied to the destination device. Source sector count is incremented (see Read Packet Status command) but destination sector count is not incremented.

- 1 not 3 Terminate hold, etc. based on other error action value. Transfers data until the end of the current input operation then takes error action. Source sector count is incremented. It is indeterminate whether the sector containing the ECC error was transferred to the destination device. If ERR ACT = 1 (ie, hold on error) then a Resume command will cause the bad sector to be transferred to the destination device.
- 1 3 Transfers sector containing the ECC error to the destination device. Both source and destination counters are incremented.

#### **SR — SUPPRESS RETRIES**

If set to 1 then retries will not be attempted during the Copy Data operation - that is, the ERROR ACTION field will take effect as soon as an error is detected. If set to 0 then 3 retries will be attempted before the ERROR ACTION field takes effect and an error status is reported.

#### **ELM — ENABLE LOGICAL ADDRESSING MODE**

See Mode Byte Format (Figure 6-2).

#### **IEC — INHIBIT ECC CORRECTION**

See Mode Byte Format (Figure 6-2).

#### **TIE — TRANSFER IF ERROR**

See Mode Byte Format (Figure 6-2).

## 5.2 Formatting

### 5.2.1 General

Formatting a disc drive is the process which writes all of the sector headers, or ID fields, on the disc. With the DS101 this process includes automatic defect mapping and interleaving. It does not necessarily include writing the data fields (a packet based Format command may write data fields). After formatting a disc, the disc must have its data field written to before any Read Data or Verify commands are sent. The ID field is shown in Figure 5-7. Any size sector up to 2K bytes is legal with a DS101. If a sector size less than 256 bytes is desired, contact the factory for performance information with respect to small sector sizes.

FIGURE 5-7. SECTOR HEADER FORMAT

ID	SECT.	HDA	CYL.	ID	ECC (4 BYTES)	FILL
SYNC	ADD.		CYL.	ADD.	CONTROL	(ZEROES)
BYTE	*	ADD.	LSB	FIELD		
(F9)		MSB		**		

\* Interleaving is controlled by assigning appropriate sector addresses

\*\* Defect Mapping is controlled by the ID Control Byte (see Table 5-1)

TABLE 5-1. ID CONTROL FIELD DEFINITIONS

FIELD VALUE (HEX)	DEFINITION
FF	User Data
FD	User Alternate
FA	Unused on-track spare
FB	Bad Sector
F5	Bad Track
F0	Defect Directory
F3	Interleave Factor Table
F7	System Configuration (The only sector with this control field is always written within the two innermost cylinders. These two cylinders are not accessible by the user.)

### 5.2.1.1 Interleaving

Interleaving is the capability of the DS101 to format a disc such that consecutive physical sectors are not consecutive absolute sectors. This provides host processing time between the accesses to consecutive sectors without suffering an entire rotational latency delay, and a means of limiting the average disk data transfer rate during multisector operations.

Interleaving may be performed within tracks, from track to track, and from cylinder to cylinder. The user controls the interleaving function by specifying three interleave factors when the floppy or Winchester disc is formatted. Only interleaving within a track can be implemented with both a packet based and a register based Format command. The other two types of interleaving and On-Track-Sector Sparing can only be implemented by issuing a packet based Format command.

In the absence of interleaving the sectors are accessed sequentially; successive physical or logical sectors are also successive absolute sectors. If no interleaving between the sectors within a track is desired, a sector interleave factor of 0 should be specified. A value of F2H is used to suppress head (track-to-track) and cylinder (last track to first track) interleaving.

The values specified as the interleave factors are the number of absolute sectors that lie between successive physical sectors. For example, if the user specifies a sector interleave factor of 3, then physical sectors 0, 1, 2, ... will correspond to absolute sectors 0, 4, 8, ...

If On-Track-Sector Sparing has been implemented, the last sector on each track is usually an unused spare sector. If head or cylinder interleaving has also been enabled (Interleave Factor other than F2 for these two parameters), this will affect that interleaving. The DS101 bases its interleaving on the position of the last used sector of the track with respect to the position of the first sector of the next track. For instance, if a head interleave factor of zero is specified, then sector zero of each track is aligned with the sector immediately following the last used sector of the previous track (i.e. there are zero sectors between the last used sector of one track and the first sector, sector zero, of the next). If On-Track-Sector Sparing has not been enabled, then sector zero on each track will be the first sector after the index pulse. This occurs because the last used sector of each track is the one which immediately precedes the index pulse. If On-Track-Sector Sparing had been enabled with one spare sector per track, sector zero of the second track on the disc would appear as the last sector before the index pulse. This is because the last sector of the first track is an unused spared sector, and the DS101 therefore references the second-to-the-last sector of the first track for the head interleave. (Note that if there were one defective sector on the first track, that the first sector of the second track would then follow the index mark.) This is why an Interleave Factor of zero for head and cylinder interleaving does not mean that head and cylinder interleaving have been suppressed.

During the formatting process, the DS101 establishes the absolute position of physical sector zero, then skips k absolute sectors (where k is the sector interleave factor), then assigns physical address 1 into the ID field of the next absolute sector, and so on. The process continues until physical addresses have been assigned to all absolute sectors on the track to be formatted.

It is also important to note that some interleave factors will not allow an assignment that results in k absolute sectors between all physical sectors. Thus if during the setup of the ID fields the DS101 detects that the next sector is already used then the next available sector will be assigned instead (see example 2). This situation can be further aggravated by the presence of defects.

---

EXAMPLES: Sector interleave factor/sector assignment

1. Sectors per track = 5  
Sector interleave factor = 1

Absolute Sector Number: 0 1 2 3 4  
Physical Sector Number: 0 3 1 4 2

2. Sectors per track = 6  
Sector interleave factor = 1

Absolute Sector Number: 0 1 2 3 4 5  
Physical Sector Number: 0 3 1 4 2 5

This example demonstrates a case where the sectors per track/interleave factor combination does not result in the specified spacing for all sectors. Physical sector 3 is actually two sectors from physical sector 2.

---

If the host system must implement custom sector interleave formats not supported by the standard algorithm, the user may specify a sector interleave table directly.

If the interleave factor is set to F0 HEX the Interface will request that N bytes of data be transferred from the host, where N is the number of sectors per track. These N bytes of data are the Sector Interleave Table and will be used in the order sent to assign sector numbers to the respective absolute sectors on each track. This feature is most often used to interleave the disk in units of Interface buffer size rather than in single sector units.

Interleave factors are specified at the time of formatting, and cannot be changed dynamically during normal operation.

In choosing an interleave factor the user should consider the following:

- o Data transfer time across the host interface.
- o Host processing time for this data.
- o Number of sectors to be transferred on a single command.
- o Time taken to send commands to the DS101.
- o Time taken by the DS101 to initiate command execution.

Track to track interleaving can only be implemented with a packet based format command. This interleaving establishes the absolute position of physical sector zero based on the absolute position of the last user sector on the previous track. This provides a predictable track-to-track access time even when the sector interleave factor is changed. The technique is helpful when multisector operations are performed that cross track boundaries; eg. a read of two sectors where the first sector to be input is the last physical sector on any track. Disc read and write operations performed by the DS101 are momentarily interrupted at track boundaries, and it subsequently takes processing time to restart the read or write operation. The drive is still rotating and ideally the next sector to be accessed (i.e. sector zero) would then be passing under the drive read/write head when the operation is restarted. Track to track interleaving can take these delays into account when the drive is formatted, and order the sectors on successive tracks so that physical sector zero on each track is a short rotational delay away from the last physical sector on the previous track. All subsequent sectors on the track are established based on the sector interleave factor.

Two different track crossing situations occur; (1) where only a head switch is required as in accessing sectors on successive tracks on the same cylinder and (2) where the switch is from the last sector on the last track of cylinder n to the first sector on the first track of cylinder n+1. In case (1) the rotational delay can be as short as one sector. In case (2) a single-cylinder seek will be required. The cylinder interleave factor specified by the host should account for this additional delay (typically this value is about 1/2 of a revolution of the disk).

### **5.2.1.2 Defect Mapping**

During operation of the Format Disc command the DS101 may encounter a defective sector on a track. Defective sectors are identified by entries in the Skip Defect Record, which is written on each track of each drive at the factory. The defect mapping capabilities of the DS101 allow it to assign alternates for defective sectors and tracks. The DS101 creates a Defect Directory during the format operation. Each drive then has an area reserved for alternate sectors and tracks.

- o Defect Map Format

The Defect Directory is created on the first sector of the first flawless track of the alternate area. (See Tables 5-2 through 5-5.)

The Defect Map is a linked list of 128-byte records. Locations 1 and 2 of each record contain the address of the track that contains the next directory record. The last record in the directory has a link address of zero.

TABLE 5-2. DEFECT DIRECTORY FORMAT

<u>Location (HEX)</u>	<u>Description</u>
0	Configuration Level
01,02	Next entry link address
03	Interleave Factor (SMART-E/T Only)
04,05	Interleave Factor Table Address
06-0F	Configuration Data (to be defined)
10-7B	Defect Directory Entries (see Table 5-3)
7C-7F	Fill (FF HEX)

TABLE 5-3. DEFECT DIRECTORY ENTRY FORMAT

<u>Location</u>	<u>Description</u>
0	Defect Cylinder Address LSB
1	Defect Head/Cylinder Address MSB
2	Defect Physical Sector Address (If FF HEX = End of directory, if FE HEX = defective track.)
3	Alternate Cylinder Address LSB
4	Alternate Head/Cylinder Address MSB
5	Alternate Physical Sector Address

TABLE 5-4. RECOMMENDED ALTERNATE AREAS

<u>Drive Type</u>	<u>User Cylinders</u>	<u>Alternate Area*</u> <u>(Cylinders)</u>
3350	0-554	555-558
6650/15450	0-1107	1108-1118
3450	0-514	515-522
7050	0-1038	1039-1046
803	0-834	835-847
804	0-1033	1034-1047
806	0-834	835-847
807	0-1463	1464-1486

\* The DS101 reserves the last two cylinders of the drive for configuration data.

A defect directory entry is created for each bad track and each bad sector that must be assigned an alternate off-track.

The Format Disc command proceeds as follows:

- a. The alternate area is formatted and the first defect directory is established on the first flawless track of the alternate area.
- b. The user area is formatted. As each bad track or sector is encountered, it is assigned an alternate and the assignment is recorded in the defect directory. New defect directory records are initialized and linked as each preceding record is filled and written to disk. Defective sectors are written with an 8-byte record that contains the address of its alternate. This is known as a forwarding address.
- c. After the user area is formatted, the last defect directory record is written to the disk.
- d. The last two cylinders, reserved for PRIAM use, are formatted, and two copies of the disk configuration record are written to the last cylinder.

o Read/Write Data Operations - Defect Handling

Read or Write requests that are performed on sectors that are not defective do not encounter any overhead due to the defect mapping feature. Defect mapping is only performed when the Interface cannot locate the specified sector. The major steps in the defect mapping logic are outlined below.

- a. Attempt to perform the operation on the sector as specified.
- b. If the specified sector is not found, read the 8-byte forwarding address record (ID control field = FB).
- c. If the forwarding address is found, perform the specified operation on the alternate. Otherwise, search the defect directory for the requested sector or track. To improve the performance of bad-track processing, the defect mapping logic keeps the read/write head on the alternate to a bad-track until the host requests an operation on a different cylinder and head.
- d. If the required forwarding address is found, operate on the alternate sector specified. If not found then search the Defect Directory.

o Adding Defect Directory Entries Under Host Control

New entries may be added to the Defect Directory by using the Specify Bad Sector command or the Specify Bad Track command. The user may give a physical address (if the DS101 is in physical mode) or a logical address (if the DS101 is in logical mode).

It should be noted that adding a Defect Directory entry does not of itself amend the Skip Defect Record on the corresponding track. This can be accomplished by using the Write Skip Defect Field command. These commands also do not write to the new data fields. These areas must be written to before they can be read.

On-track sector sparing allocates a user specified number of sectors on each track to be used when other sectors contain defects. The other form of defect mapping assigns alternate sectors from the alternate cylinders area of the disc. When formatting with on-track sector sparing, each sector that contains one or more defects will be identified and marked with an ID control field indicating a bad sector. The user sectors are then assigned from the remaining available sectors. If the number of bad sectors on a track is no greater than the number of on-track sector spares, all user sectors can be assigned, making the access of off-track spares unnecessary.

When all on-track spares have been used and another defect is encountered on that track then the DS101 will locate the closest available spare sector on another track to be used as the alternate sector. The closest available spare is first chosen from spare sectors on the same cylinder but under a different head. In the unlikely event that all tracks on the same cylinder have used all their spare sectors then the DS101 will check the lower cylinders (cylinder -1, cylinder -2, etc.), expanding downward from the current cylinder until an available spare is found. The defective sector will then be written with redundant information pointing to this alternate sector, and thus when the defect event occurs the seek time to the alternate sector will be minimized.

Of the tracks that contain defects, the vast majority of these contain only one defect and hence only one on-track sector spare would be needed. A small access time penalty is paid when a defect event occurs for those few tracks containing two or more defects. This time penalty can be eliminated by increasing the number of on-track sector spares. However, a time penalty will still occur when the entire track is defective.

The cost of on-track sector sparing is a decrease in the usable storage capacity of the drive. This must be balanced against the time penalty paid when a seek to the alternate cylinders area of the drive is required. When on-track sector sparing is selected, fewer alternate cylinders need to be allocated.

#### **AUTOMATIC DEFECT MANAGEMENT**

The Automatic Defect Management feature will invoke a single sector digital surface analysis routine whenever a read operation completes with an ECC error (Completion Code = 03 HEX or 11 HEX). If this surface analysis of the sector in question then indicates a hard error or a marginal area on the disc, the DS101 will automatically reassign that sector. The sector will be reassigned to the alternate area or to an on-track spare sector, depending on the type of defect mapping that is in effect. It will also transfer the user data from the original location to the new location. It will not update the Skip Defect Record. The data in the reassigned sector will then be in one of two states:

1. Valid corrected data (ECC correction was successfully performed)
2. Original data with data error. Note that the data still contains an uncorrectable ECC error and the DS101 will report that error whenever the sector is read. The user must now rewrite the sector in order to correct the error.

The DS101 performs Automatic Defect Management as required whenever the disc is formatted with defect mapping. The feature can be disabled by setting the ADM bit in Option Byte 0 (See Figure 6-3) or by setting the ADM switch (See Section 2.6).

## 5.2.2 Register Based Format Disc Commands

### 5.2.2.1 Format Disc With Defect Mapping

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = A8 HEX	0	7 INTERFACE STATUS
BLOCK OUTPUT	1	---
DEVICE SELECT	2	TRANSACTION STATUS
///	3	---
INTERLEAVE FACTOR	4	---
///	5	???
	6	---
	7	DEVICE SELECT RESULT

#### FUNCTION

This command causes the following operations to occur:

1. Sector ID (identifier) fields are written for all sectors on the disc.
2. The Skip Defect Records are used to locate disc defects and flag the bad sectors/tracks.
3. An alternate area is defined and a defect directory is created.
4. Alternates are assigned for each bad sector and track and entries are made in the defect directory. When a defect event occurs, the directory is searched for the alternate to the bad sector or track.

This command does not write any data fields. Before data may be read from the disc, the user must issue a command that writes the data fields.

### 5.2.2.2 Format Disc Without Defect Mapping

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = A0 HEX	0	7 INTERFACE STATUS
BLOCK OUTPUT		---
DEVICE SELECT		TRANSACTION STATUS
---		---
///		???
INTERLEAVE FACTOR		---
---		---
///		DEVICE SELECT RESULT
		0

#### FUNCTION

This command causes Sector ID (identifier) fields to be written for all sectors on the disc.

This command does not write any data fields. Before data may be read from the disc, the user must issue a command that writes the data fields.

This command is intended to be used for diagnostic purposes only.

### 5.2.2.3 Format Cylinder Without Defect Mapping

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7	0	7
COMMAND = A1 HEX	0	INTERFACE STATUS
BLOCK OUTPUT	1	---
DEVICE SELECT	2	TRANSACTION STATUS
CYLINDER	MSB LSB	3
INTERLEAVE FACTOR		4
///		5
		6
		7
		DEVICE SELECT RESULT

#### FUNCTION

This command causes Sector ID (identifier) fields to be written for all sectors on a particular cylinder.

This command does not write any data fields. Before data may be read from the disc, the user must issue a command that writes the data fields.

This command is intended to be used for diagnostic purposes only.

#### 5.2.2.4 Format Track Without Defect Mapping

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7	0	0
COMMAND = A2 HEX		INTERFACE STATUS
BLOCK OUTPUT		---
DEVICE SELECT		TRANSACTION STATUS
HEAD/CYLINDER	MSB	---
CYLINDER	LSB	---
INTERLEAVE FACTOR		???
///	—	—
	7	DEVICE SELECT RESULT

#### FUNCTION

This command causes Sector ID (identifier) fields to be written for all sectors on a particular track.

This command does not write any data fields. Before data may be read from the disc, the user must issue a command that writes the data fields.

This command is intended to be used for diagnostic purposes only.

### 5.2.3 Packet Based Format Disc Command

This section describes the Format Disc Packet Parameters. A thorough understanding of interleaving, defect mapping, and the specific application in which the DS101 is to be used is necessary in order to optimize a disc format. It should also be noted that, once a set of Format Disc packet parameters have been calculated, tests should be run on the storage system in order to select the optimum parameter values for the application. Table 5-5 provides values for a baseline set of Format Disc Packet Parameters.

TABLE 5-5. BASELINE FORMAT DISC PACKET PARAMETER SET

<u>BYTE</u>	<u>VALUE HEX</u>
0	02
1	Device Select
2	80
3	00
4	Sector Size
5	Sector Size
6	00
7-3350	04
7-6650/15450	0B
7-3450/7050	08
8	F2
9	F2
10	0
11	0

These values represent the same basic format as the register based Format Disc command (without interleaving). This provides the user with a controlled transition from register based formats to packet based formats. Once the user is successful with this set of values and has established a baseline set of performance statistics, evaluation of more complex packet based formats is simplified. Note that these are only intended to be used as a starting point in determining an optimum set of Format Disc packet parameter values for a given system.

**FIGURE 5-8. FORMAT DISC PACKET PARAMETERS STRUCTURE**

HARD DISC FORMAT							
BYTE	7	6	5	4	3	2	1    0
0					02 HEX		
1	///	CH #			UNIT #		
2	FBD	///			MEDIA TYPE = 0		
3					FILL BYTE		
4					SECTOR		
5					SIZE		
6	DMD	///			# SPARE SCT		
7					# ALTERNATE CYLINDERS		
8					CYLINDER INTERLEAVE FACTOR		
9					HEAD INTERLEAVE FACTOR		
10					SECTOR INTERLEAVE FACTOR		
11					SECTOR INTERLEAVE TABLE LENGTH		
12	:				SECTOR INTERLEAVE TABLE		
					(OPTIONAL)		
14	:				:		

OPERATION CODE  
DEVICE SELECT  
SECTOR CONTROL  
  
DEFECT CONTROL  
INTERLEAVE CONTROL

#### FUNCTION

The Format Disc command initializes the selected disc. The structure of the parameters in this command will be interpreted in one of two possible forms based on the type of disc to be formatted (as determined by the DS101 from the Device Select field). The format operation creates sectors on each track and may optionally preset the data bytes in each sector to a specified value (optional for hard discs only - floppy disc sectors are always preset). Defect mapping is performed for hard discs only. The order in which physical sector numbers are assigned on each track is specified by the Interleave Control fields.

The Format Disc command packet parameters (see Figure 5-8) are interpreted in two slightly different manners depending on the type of disc to be formatted; hard or floppy. The following sections discuss the hard disc format parameters. Floppy Disc formatting details are discussed in the Auxiliary Controller Board Specification. The basic difference between the floppy disc and hard disc parameter structures are related to the fact that defect mapping is not performed for floppies. Secondly, the structure of a floppy track is controllable by the user.

#### **OPERATION CODE**

This parameter is a code number equal to 02 HEX that identifies the following 11 bytes (at least) as format parameters. Note that the command may be longer than 12 bytes if an Interleave Table is specified (total length must always be an even number of bytes).

#### **DEVICE SELECT**

This parameter selects the device to be formatted and consequently determines how the remaining parameters are interpreted. The host, as well as the

DS101, must know that the device is a hard or floppy disc and structure the format command parameters accordingly.

#### **FILL BYTE DISABLE (FBD)**

0 = initialize all data fields with the Fill Byte  
1 = Do not initialize the data fields

The fill byte disable flag, when set, indicates that the fill phase, setting every byte of each sector to the fill byte, should be bypassed. This option is not available for floppy discs, i.e. the fill byte parameter is always used for floppies. The Fill Byte is not used if FBD = 1

#### **FILL BYTE**

The fill byte parameter is used to preset the value in every byte of a sector data record.

#### **SECTOR SIZE**

This two byte parameter specifies the number of data bytes in each sector. For all floppies, and those PRIAM drives that allow the sector size to be specified under software control, this value will be used. For those drives whose sector size is controlled by switches on the drive this value will be compared against the switch settings. A sector size invalid transaction status will be generated if the values are not compatible, and the format operation will be aborted. Note that any sector size up to 2K bytes is legal with a DS101. Sector sizes below 256 bytes may adversely effect throughput. It is recommended that all Winchester disc drives on a system be formatted with the same sector size.

#### **DEFECT MAPPING DISABLE (DMD)**

0 = Defect Mapping Enabled: 1 = Defect Mapping Disabled  
This bit flag, when set, disables the defect mapping logic of the Format command. This bit is normally zero. Setting this bit to one is not recommended.

#### **NUMBER OF SPARE SECTORS**

This parameter controls the on-track sector sparing option in the DS101. If its value is zero then the option will be disabled and all sectors on each track will be available to the host. Alternate sectors will then be assigned from the alternate area.

If non-zero then the specified number of sectors will be reserved on each track for assigning alternate sectors for those sectors that contain defects. Using on-track sector spares decreases the final capacity of the drive but also significantly decreases the access time penalty associated with defective sectors. Up to three defects per track are identified by the Skip Defect Record on each track (more than three defects generates a defective track indication). A value of one is recommended for this parameter unless speed is an absolute premium commodity (in which case 3 would be the recommended number).

## **NUMBER OF ALTERNATE CYLINDERS**

This parameter specifies the number of cylinders to be taken for use in allocating alternate tracks (and alternate sectors if on-track sector sparing is disabled). The DS101 always allocates the last two cylinders on PRIAM drives for its own use in internal disc diagnostics and maintaining system configuration data.

## **CYLINDER INTERLEAVE FACTOR**

This parameter specifies the number of sectors delay required between the last sector of the last track in cylinder n and the first sector on the first track in cylinder n+1. This delay biases the absolute location of physical sector 0 to compensate for the rotation of the disc during a single cylinder seek.

A value of F2 hex will disable cylinder interleaving and cause physical sector 0 to be assigned to absolute sector 0 on the first track of every cylinder.

## **HEAD INTERLEAVE FACTOR**

This parameter is the number of sectors delay required between the last sector of a track and the first sector of the next track when both tracks are in the same cylinder. It is used to adjust the absolute location of physical sector 0 to compensate for the rotation of the disc when a head switch is required.

A value of F2 will disable head and cylinder interleaving and cause physical sector 0 to be assigned to absolute sector 0 on every track.

## **SECTOR INTERLEAVE FACTOR**

The Sector Interleave Factor specifies the number of absolute sectors to be skipped before the next physical sector is generated. See section 5.3.1.1 for a full discussion of interleaving. Sector interleaving will be suppressed if this factor is 0. Specifying a non-zero sector interleave factor as well as a non-zero interleave table length will cause a command reject Transaction Status to be returned, and the format operation will not take place. The DS101 can generate interleaved sectors while also accommodating head and cylinder interleaving.

## **SECTOR INTERLEAVE TABLE LENGTH**

The Sector Interleave Table length parameter is the number of bytes in the Sector Interleave Table. If there is no Sector Interleave Table following the required parameters then this value must be 0. If not 0 then the DS101 will interleave sectors as specified by the Sector Interleave Table. This value, when non-zero, must be equal to the number of available sectors on a track - that is, it should not include spare sectors.

## **SECTOR INTERLEAVE TABLE**

The Sector Interleave Table is an optional set of parameters that permit the host to specify a custom sector interleave structure. The table must contain a one byte physical sector number corresponding to each absolute sector. That is, the first entry in the table specifies the physical sector number to be given to absolute sector 0 on each track; the second entry gives the physical sector number to be assigned to absolute sector 1; etc.

The total length of the Sector Interleave Table must be an even number of bytes even though a track may contain an odd number of sectors (the last byte of the table will be ignored). The Sector Interleave Table Length parameter must be the number of valid entries in the Sector Interleave Table (i.e. may be even or odd depending on the number of user accessible sectors on each track).

## 6.0 EXTENDED COMMAND SET

The host may perform the following operations through the use of various extended commands:

- o Specify/Interrogate System Level Parameters

The system level commands generally will be used by the host initialization logic to specify the basic operating mode of the Peripheral Subsystem. The system level commands are also used so the host processor may determine the configuration of the Peripheral Subsystem.

- o Specify/Interrogate Device Level Parameters

The device level commands are used by the host to specify software selectable parameters of a device (such as floppy disc single/double density select).

- o Device Control

The device commands are supported for host diagnostics and special application functions which cannot be implemented with the normal command set presented in the previous section. These commands are usually not required for normal system operation.

- o Diagnostic Functions

### 6.1 Winchester Disc Functions

This section describes basic commands required for the host to operate the disc drives directly. Included in this section are:

- o Defect Mapping Commands

1. Specify Bad Sector
2. Specify Bad Track
3. Read Defect Directory

- o Disc Data Initialization/Verification Commands

1. Write Track - Full Track
2. Write Cylinder - Full Track
3. Write Disc - Full Track
4. Verify Track
5. Verify Data
6. Verify ID
7. Verify Cylinder
8. Verify Disc

- o Disc Motion and Drive Control Commands

1. Sequence Down
2. Sequence Up - Return
3. Sequence Up - Wait
4. Seek
5. Seek-Return Immediate
6. Restore
7. Read Device Status

- o Winchester Disc Primitive Read/Write Commands

1. Write ID
2. Read ID
3. Read ID Immediate
4. Read Skip Defect Field
5. Write Skip Defect Field
6. Read Device Status

### 6.1.1 Defect Mapping Commands

The defect mapping commands can be used if the disc has been previously formatted with defect mapping enabled. If the disc was formatted without defect mapping these commands are disabled.

### 6.1.2 Specify Bad Sector

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = AA HEX	0	0 INTERFACE STATUS
---		1 ---
DEVICE SELECT		2 TRANSACTION STATUS
---	MSB	3 ---
TRANSFER ADDRESS	MSB	4 ???
---	LSB	5 ---
///	---	6 ---
		7 DEVICE SELECT RESULT

#### FUNCTION

If during operation of the disc the host software determines that a sector on the disc is defective, the host may use this command to flag the bad sector and assign an alternate.

When this command is issued the following operations are performed:

- o The bad sector is flagged.
- o An alternate sector is located.
- o The Defect Directory is updated to show the location of the alternate.

This command does not update the Skip Defect Record. Therefore if the disc is reformatted again the bad sector must also be re-specified or the Skip Defect Record may be updated by the host.

This command may only be executed, on a disc that has previously been reformatted with defect mapping enabled.

The user data field is not copied to the alternate location. The data field must have data written to it prior to attempting to read or verify the alternate sector.

#### **TRANSFER ADDRESS**

Used to specify the defective sector.

### 6.1.3 Specify Bad Track

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = A9 HEX	0	7 0
---	1	INTERFACE STATUS
DEVICE SELECT	2	---
TRANSFER ADDRESS	3 MSB	TRANSACTION STATUS
---	4 LSB	---
---	5	???
---	6	---
---	7	DEVICE SELECT RESULT

#### FUNCTION

This command is used by a host routine to request that the DS101 flag a bad track and assign an alternate.

The operation of this command is the same as the Specify Bad Sector command except an entire track is flagged and mapped to an alternate. The Skip Defect Record is not updated nor is any data written to the newly assigned alternate track. These areas must have data written to them prior to attempting to read or verify these new fields.

This command may only be executed, for a disc that has previously been formatted with defect mapping enabled.

#### 6.1.4 Read Defect Directory

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = A6 HEX	0	7 INTERFACE STATUS
---		1 BLOCK INPUT
DEVICE SELECT	2	TRANSACTION STATUS
---	3	---
///	4	??? ---
DIRECTORY ENTRY	5	---
---	6	---
///	7	DEVICE SELECT RESULT

#### FUNCTION

This command may be used to read the Defect Directory if the disc has been formatted with defect mapping enabled (see Defect Mapping discussion). The Defect Directory is a linked list of 128 byte records. The directory records are numbered from zero to the number of entries minus one. When reading the directory the host should read successive records from zero until an End of Directory status code is received.

#### **DIRECTORY RECORD**

128 bytes of data are transferred from the DS101 to the host for each defect directory record.

#### **DIRECTORY ENTRY**

This parameter specifies the directory record that should be transferred (Range = 0 to the number of directory entries -1).

### 6.1.5 Disc Data Initialization and Verification Commands

The following set of commands are normally used by disc formatting routines and diagnostics.

### 6.1.6 Write Track - Full Track

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7	0	7
COMMAND = AD HEX	0	INTERFACE STATUS
BLOCK OUTPUT	1	---
DEVICE SELECT	2	TRANSACTION STATUS
TRANSFER START ADDRESS	3 MSB 4 LSB	5 MSB 6 LSB 7 ???
///	—	DEVICE SELECT RESULT

#### FUNCTION

This command is used to initialize the disc data fields on one track. The data pattern specified is written to all sectors on the track selected by the Transfer Start Address.

If an error occurs the result registers indicate the sector that was being transferred when the error occurred.

The DS101 transfers one sector of data from the host.

### 6.1.7 Write Cylinder - Full Track

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7	0	7
COMMAND = AC HEX	0	INTERFACE STATUS
BLOCK OUTPUT	1	---
DEVICE SELECT	2	TRANSACTION STATUS
	3	MSB
TRANSFER START ADDRESS	4	---
	5	TRANSFER END ADDRESS
---	6	LSB
---	7	???
---		DEVICE SELECT RESULT

#### FUNCTION

This command is used to initialize the data fields on a cylinder of the disc. The data pattern transferred is written to all sectors on the cylinder selected by the Transfer Start Address.

If an error occurs, the result registers indicate the sector that was being written when the error occurred.

The DS101 transfers one sector of data from the host.

### 6.1.8 Write Disc - Full Track

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = AB HEX	0	7 INTERFACE STATUS
BLOCK OUTPUT	1	---
DEVICE SELECT	2	TRANSACTION STATUS
---	3	MSB
---	4	TRANSFER END ADDRESS
---	5	LSB
---	6	???
---	7	DEVICE SELECT RESULT

#### FUNCTION

This command is used to initialize the data fields for an entire disc.

If an error occurs, the result registers indicate the sector that was being written when the error occurred.

The DS101 transfers one sector of data from the host, and this data pattern is written to each sector on the disc.

### 6.1.9 Verify Track

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = A5 HEX	0	7 0
---		INTERFACE STATUS
DEVICE SELECT	1	---
TRANSFER START ADDRESS	2 MSB	TRANSACTION STATUS
	3	
---	4	TRANSFER END ADDRESS
TRANSFER START ADDRESS	5 LSB	MSB
---	6	LSB
///	7	???
		DEVICE SELECT RESULT

#### FUNCTION

This command is used to verify that a single track of the disc is formatted properly. Every ID and data field on the specified track is read and the ECC is checked. If an error is detected, the operation is terminated and the result registers indicate which sector contains the error.

### 6.1.10 Verify Cylinder

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = A4 HEX	0	7 0 INTERFACE STATUS
---	1	---
DEVICE SELECT	2	2 TRANSACTION STATUS
	3	3 MSB
TRANSFER START ADDRESS	4	4 TRANSFER END ADDRESS
	5	5 LSB
///	6	6 ???
	7	7 DEVICE SELECT RESULT

#### FUNCTION

This command is used to verify that a single cylinder of the disc is formatted properly. Every ID and data field on the specified cylinder is read and the ECC is checked. If an error occurs, the operation is terminated and the result registers indicate which sector contains the error.

### 6.1.11 Verify Disc

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = A3 HEX	0	7 0 INTERFACE STATUS
---		1 ---
DEVICE SELECT	2 ---	2 TRANSACTION STATUS
---	3 ---	3 MSB
---	4 ---	4 TRANSFER END ADDRESS
---	5 ---	5 LSB
---	6 ---	6 ???
---	7 ---	7 DEVICE SELECT RESULT

#### FUNCTION

This command is used to verify that a disc is formatted properly. Every ID and data field on the disc is read and the ECC is checked. If an error is detected, the operation is terminated and the result registers indicate which sector contains the error.

### 6.1.12 Verify Data

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 44 HEX	0	7 INTERFACE STATUS
---	1	---
DEVICE SELECT	2	TRANSACTION STATUS
TRANSFER START ADDRESS	3 MSB	4 MSB
OPERATION COUNT	5 LSB	6 MSB
///	7	RESIDUAL OPERATION COUNT DEVICE SELECT RESULT

#### FUNCTION

This command is used to verify that the sectors indicated by the parameter registers are formatted properly. Every ID and data field specified is read and the ECC check is performed. If an error occurs, the operation is terminated and the result registers indicate which sector contains the error.

### 6.1.13 Verify ID

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 48 HEX	0	7 0
---		INTERFACE STATUS
DEVICE SELECT	1	---
	2	TRANSACTION STATUS
TRANSFER START ADDRESS	3 MSB	3 MSB
	4 LSB	4 LSB
OPERATION COUNT	5	5
///	6	RESIDUAL OPERATION COUNT
	7	DEVICE SELECT RESULT

#### FUNCTION

This command is used to verify that the ID fields on a track are readable. Every ID field specified by the parameter registers is read and the ECC is checked. If an error is detected, the operation is terminated and the result registers indicate which ID field contains the error.

#### 6.1.14 Disc Motion and Drive Control Commands

The following commands are supported so that the host may have complete use of the disc drive motion control capability. The commands are implied by any other DS101 command if required. During normal operation (with the exception of Sequence Down) the host should not need these commands to operate the DS101.

#### 6.1.15 Sequence Down

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 81 HEX	0	7 INTERFACE STATUS
---	1	---
DEVICE SELECT	2	TRANSACTION STATUS
---	3	DEVICE STATUS
---	4	---
---	5	???
---	6	---
---	7	DEVICE SELECT RESULT

#### FUNCTION

The Sequence Down command causes the PRIAM disc drive defined by Device Select to position the heads over the landing zone. The spindle motor's dynamic braking is initiated. The drive will set the Write Protect status bit and clear the Ready bit. When dynamic braking is initiated the Command Completion bit will be set with the device status in Register 3 (see Figure 6-1 in Section 6.1.26).

While not strictly necessary, since the same actions occur when power is removed from the drive, the Sequence Down command does provide a controlled termination.

The drive takes about 40 seconds to stop the platters from spinning. Power may then be removed or the drive may be kept in a sequenced down state until the next time it is to be accessed. The DS101 will automatically sequence up a PRIAM drive before any read/write operation if it finds the drive in a sequenced down state. Thus, the host may issue commands without reference to the sequence up/down state of the drive being accessed. Commands issued to a sequenced down drive will take about 30-60 seconds longer since the command may not be executed until the sequence up has been completed.

### 6.1.16 Sequence Up - Return

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 83 HEX	0	7 0
---		INTERFACE STATUS
DEVICE SELECT	1	---
---	2	TRANSACTION STATUS
---	3	DEVICE STATUS
---	4	---
---	5	???
---	6	---
---	7	DEVICE SELECT RESULT

#### FUNCTION

The Sequence Up - Return command causes the disc drive defined by the Device Select to power up its spindle motor. The operation is similar to that in Sequence Up - Wait command, but the DS101 does not wait until the drive is up to speed and the heads are positioned over Cylinder 0 before posting the command completion.

### 6.1.17 Sequence Up - Wait

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 82 HEX	0	7 INTERFACE STATUS
---	1	---
DEVICE SELECT	2	TRANSACTION STATUS
---	3	DEVICE STATUS
---	4	---
---	5	???
---	6	---
---	7	DEVICE SELECT RESULT

#### FUNCTION

The Sequence Up - Wait command causes the disc drive defined by Device Select to power up its spindle motor. The disc drive will monitor the rotational speed of the disc and when it is at speed and stable, the drive will position the heads at cylinder zero.

The Sequence Up - Wait command is similar to the Sequence Up - Return command, except that the Sequence Up-Wait command will not complete until the drive is ready for data transfer.

### 6.1.18 Seek

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 51/41 HEX	0	7 INTERFACE STATUS
---		---
DEVICE SELECT	1	TRANSACTION STATUS
	2	
	3	MSB
TRANSFER START ADDRESS	4	TRANSFER END ADDRESS
	5	LSB
	6	???
///	7	DEVICE SELECT RESULT

#### FUNCTION

When a Seek command is used the DS101 will position the head(s) (access arm) of the selected device over the target cylinder defined by the Transfer Start Address.

The seek command is automatically issued by the DS101 as required.

#### COMMAND

- 51 HEX - Retry Enabled
- 41 HEX - Retry Disabled

### 6.1.19 Restore

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 40 HEX	0	0
---		
DEVICE SELECT		7 INTERFACE STATUS
---		1
---		2 TRANSACTION STATUS
---		3
---		4 ???
---		5
---		6
---		7 DEVICE SELECT RESULT

#### FUNCTION

The Restore command causes the access arm on the device specified by the Device Select parameter to be positioned over cylinder zero.

This command is not normally issued by the user because the Restore command is automatically issued by the DS101 when required; e.g. after a seek fault.

A Restore is different from a seek to cylinder 0 in that the drive withdraws the heads until a particular servo track is found that provides a positive position indication; whereas a seek to cylinder 0 causes the drive to count track crossings to determine when it has reached cylinder 0. A restore operation is slower than a seek but it returns the drive to an absolute location.

### 6.1.20 Winchester Disc Primitive Read/Write Commands

#### 6.1.21 Write ID

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 55/45 HEX	0	7 INTERFACE STATUS
BLOCK OUTPUT	1	---
DEVICE SELECT	2	TRANSACTION STATUS
TRANSFER START ADDRESS	3 MSB	4
	4	TRANSFER END ADDRESS
OPERATION COUNT	5 LSB	6
///	7	RESIDUAL OPERATION COUNT
		DEVICE SELECT RESULT

#### FUNCTION

This command causes the 4 byte ID field to be written at the absolute sector location specified. The logical sector number is recorded from the buffer data. The command execution sequence is similar to the Write Data command with the following exception. The writing is enabled when the absolute sector count (number of sector marks past index) matches the Absolute Sector Address. The operation count shall not be greater than the number of sectors on a track.

If an error occurs, the result registers specify which sector contains the error.

The 4 byte ID field data is transferred from the host to the DS101.

Byte 0 - Logical Sector Address  
Byte 1 - Head/Cylinder Address MSB  
Byte 2 - Cylinder Address LSB  
Byte 3 - ID Control Value = FF HEX (See Defect Mapping discussion)

A 4 byte ID field will be transferred for each ID field written. This command is intended to be used for diagnostic purposes only.

#### COMMAND

55 HEX - Retry Enabled  
45 HEX - Retry Disabled

### 6.1.22 Read ID

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 56/46 HEX	0	7 INTERFACE STATUS
---		1 BLOCK INPUT
DEVICE SELECT	2 TRANSFER START ADDRESS	2 TRANSACTION STATUS
	MSB	3 TRANSFER END ADDRESS
	LSB	4 RESIDUAL OPERATION COUNT
OPERATION COUNT	5 ///	5 DEVICE SELECT RESULT
		6 MSB
		7 LSB

#### FUNCTION

This command causes the 4 byte ID field to be Read from the absolute sector location specified. The operation count shall not be greater than the number of sectors on a track. If an error occurs, the result registers specify which sector contains the error.

The 4 byte ID field data is transferred from the DS101 to the host.

- Byte 0 - Logical Sector Address
- Byte 1 - Head/Cylinder Address MSB
- Byte 2 - Cylinder Address LSB
- Byte 3 - ID Control Value (See Defect Mapping discussion)

A 4 byte ID field will be transferred for each ID field read.

#### **COMMAND**

- 56 HEX - Retry Enabled
- 46 HEX - Retry Disabled

### 6.1.23 Read ID Immediate

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 57/47 HEX	0	7 0 INTERFACE STATUS
---		1 BLOCK INPUT
DEVICE SELECT	2	2 TRANSACTION STATUS
TRANSFER START ADDRESS	3 MSB	3
	4 LSB	4 TRANSFER END ADDRESS
///	5	5 ???
	6	6 DEVICE SELECT RESULT
	7	7

#### FUNCTION

This command causes the ID field at the next physical sector encountered to be read.

The 4 byte ID field data is transferred from the DS101 to the host.

- Byte 0 - Logical Sector Address
- Byte 1 - Head/Cylinder Address MSB
- Byte 2 - Cylinder Address LSB
- Byte 3 - ID Control Value (See Defect Mapping discussion)

#### COMMAND

- 57 HEX - Retry Enabled
- 47 HEX - Retry Disabled

#### 6.1.24 Read Skip Defect Field

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 59/49 HEX	0	0
---	0	7
DEVICE SELECT	1	INTERFACE STATUS
---	2	BLOCK INPUT
TRANSFER START ADDRESS	2	TRANSACTION STATUS
---	3	MSB
TRANSFER START ADDRESS	3	---
---	4	TRANSFER END ADDRESS
---	5	LSB
---	6	???
---	7	DEVICE SELECT RESULT

#### FUNCTION

This command causes the 8 byte Skip Defect Field to be read from the location specified. If the record checksum is incorrect, an Uncorrectable ECC Error (Transaction Status 11) is reported.

The 8 byte Skip Defect Record is transferred from the DS101 to the host. See Section 5.2.1.2 for the Skip Defect Field format.

#### **COMMAND**

- 59 HEX - Retry Enabled
- 49 HEX - Retry Disabled

### 6.1.25 Write Skip Defect Field

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 5A/4A HEX	0	7 INTERFACE STATUS
BLOCK OUTPUT	0	---
DEVICE SELECT	1	TRANSACTION STATUS
TRANSFER START ADDRESS	2	TRANSFER END ADDRESS
MSB	3	---
LSB	4	---
///	5	///
	6	///
	7	DEVICE SELECT RESULT

#### FUNCTION

This command causes the 8 byte Skip Defect Field to be written to the location specified. The record checksum is automatically computed and appended to the record.

A Write Fault will occur if this command is attempted without disabling the drive's Skip Defect Field protection feature.

The 8 byte Skip Defect Record is transferred from the host to the DS101. See Section 5.2.1.2 for the Skip Defect Field format.

#### COMMAND

- 5A HEX - Retry Enabled
- 4A HEX - Retry Disabled

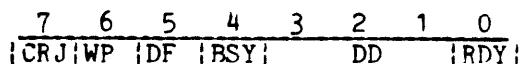
### 6.1.26 Read Device Status

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 06 HEX	0	0
---	1	---
DEVICE SELECT	2	TRANSACTION STATUS
---	3	DEVICE STATUS
---	4	---
---	5	???
---	6	---
---	7	DEVICE SELECT RESULT

#### FUNCTION

The Read Device Status command reads the device status byte, which is returned in register 3. Details of the PRIAM device status byte are given in Figure 6-1.

**FIGURE 6-1. PRIAM DEVICE STATUS BYTE**



**CRJ — COMMAND REJECT**

The CR bit indicates that the device has received an undefined or improper command.

**WP — WRITE PROTECT**

The WP bit indicates that the device hardware write disable logic is enabled.

**DF — DEVICE FAULT**

The errors that will generate DF are device dependent

The fault conditions detected by PRIAM Winchester drives are:

1. WRITE GATE without write current at the head.
2. Write current at the head without WRITE GATE.
3. WRITE GATE without READY.
4. More than one head selected.
5. No transitions during write (MFM format).
6. WRITE GATE with WRITE PROTECT.
7. WRITE GATE between INDEX and the first SECTOR MARK (when the Skip Defect Record is write protected).

**BSY — BUSY**

The device is in the process of executing a command.

**DD — DEVICE DEPENDENT**

<u>BIT</u>	<u>NAME</u>	<u>DEFINITION</u>
3	Cylinder Zero	The access arm is set to Cylinder 0.
2	Seek Fault	A fault was detected during a seek operation
1	Seek Complete	This bit is set when a seek operation is completed

**RDY — READY**

The drive is up to speed, servo system is locked onto a servo track, and the unit is in a state to read, write, or seek.

## 6.2 System Functions

The commands in this section provide the capability for the host to specify/interrogate system and device level parameters.

### 6.2.1 Software Reset

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 07 HEX	0	7 INTERFACE STATUS
---		1
		2 TRANSACTION STATUS
		3
		4 TRANSACTION STATUS
///	---	5 DEPENDENT
	---	6
	---	7

#### FUNCTION

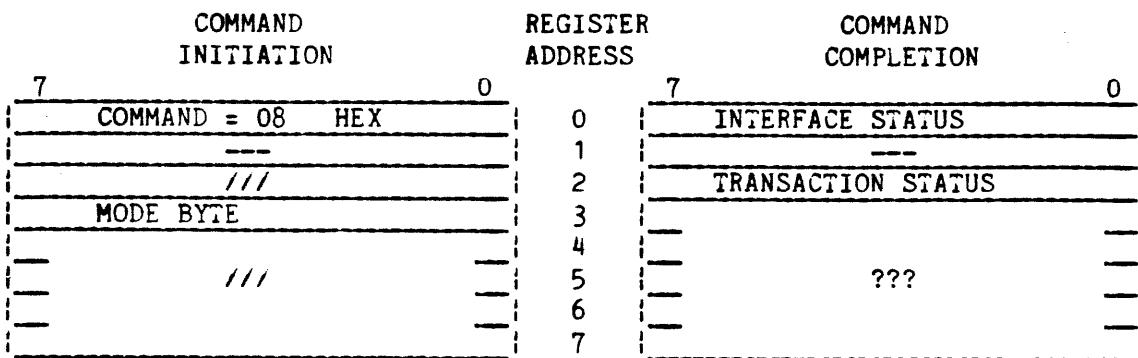
This command causes the DS101 to abort all in-progress commands and run the microdiagnostics.

The information received when Register File addresses 3-7 are read depends on the outcome of the microdiagnostics. If the Transaction Status code indicates initialization complete, the five bytes are initialized as follows:

Register Read	Value (HEX)
3	AA
4	55
5	F0
6	0F
7	00

Section 7.3 defines the value of this field when various error conditions are reported.

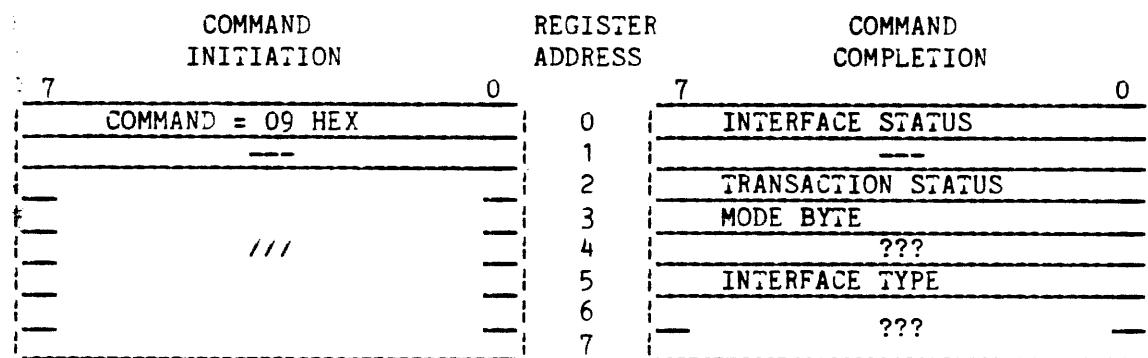
### 6.2.2 Specify Mode



#### FUNCTION

This command is used to modify the DS101 Mode Byte. Figure 6-2 defines the Mode Byte format.

### 6.2.3 Read Mode



#### FUNCTION

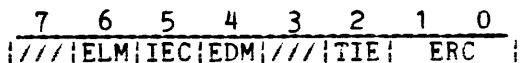
This command is used to determine the current mode of the DS101. Figure 6-2 defines the Mode Byte format.

#### INTERFACE TYPE

This register returns a byte value that identifies the type of Interface.

<u>Interface Type Code</u>	<u>Interface</u>
01	SMART
02	SMART-E
03	DS101

**FIGURE 6-2. MODE BYTE FORMAT**



**ELM — ENABLE LOGICAL ADDRESSING MODE**

ELM = 0: Use Transfer Address with Physical Address Format  
ELM = 1: Use Transfer Address with Logical Address Format

**IEC — INHIBIT ECC CORRECTION**

IEC = 0: Attempt normal error recovery (re-read) and if the retry is unsuccessful, attempt ECC recovery  
IEC = 1: Attempt normal error recovery (re-read) but do not attempt ECC correction

**EDM — ENABLE DIRECT MODE**

EDM = 0: Perform buffered mode transfers  
EDM = 1: Perform direct mode transfers (data is transferred to/from the device without passing through the buffer). ECC correction is disabled by selecting this feature

**TIE — TRANSFER IF ERROR**

TIE = 0: Do not initiate a data transfer if the requested sector cannot be read without error  
TIE = 1: Transfer data to the host even if a fatal data error is encountered

**ERC — ERROR CORRECTION CONTROL**

Through the use of the ERC field, host diagnostics may assume control of the ECC logic.

<u>ERC1</u>	<u>ERC0</u>	<u>FUNCTION</u>
0	0	Normal write and read functions.
0	1	Read operations, calculate syndrome and return syndrome bits to user. This combination is used by diagnostic routines which test the ECC functions. ECC correction is disabled.
1	0	Not used.
1	1	Write data with user-supplied ECC check bits. On read operations, return these same check bits to the host. This combination is used by diagnostic routines which test the ECC functions. ECC correction is disabled.

NOTE: If Mode Byte Bit 5, 4, 1, or 0 is set, ECC correction is disabled.

#### 6.2.4 Read Device Parameters

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 85 HEX	0	7 INTERFACE STATUS
---		---
DEVICE SELECT	1	TRANSACTION STATUS
---	2	HEADS CYLINDERS MSB
---	3	CYLINDERS LSB
---	4	SECTORS PER TRACK
---	5	# ON TRK SPARES MSB
---	6	LOGICAL SECTOR SIZE LSB
---	7	

#### FUNCTION

This command may be used by a software driver that is set up to handle multiple disc types. Through the use of this command, the driver can determine the parameters required to use the attached device.

#### HEADS/CYLINDERS

This field defines the number of user accessable cylinders on a disc (physical number of cylinders - reserved alternate cylinders).

MSB BITS 7-4: Number of heads  
 MSB BITS 3-0: Number of cylinders bits 11-8  
 LSB BITS 7-0: Number of cylinders bits 7-0

#### SECTORS PER TRACK

This field defines the number of user accessable sectors on a track (physical sectors per track - on track sector spares).

#### NUMBER ON TRK SPARES

This nibble contains the number of on-track sector spares specified when the drive was formatted.

#### LOGICAL SECTOR SIZE

The logical sector size is expressed as the number of usable data bytes within a physical sector (physical sector size - overhead).

### 6.2.5 Read Device Type

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 86 HEX	0	7 INTERFACE STATUS
---	1	---
DEVICE SELECT	2	TRANSACTION STATUS
---	3	DEVICE TYPE
---	4	PHYSICAL SECTOR SIZE MSB
---	5	---
---	6	PHYSICAL SECTOR SIZE LSB
---	7	???
		DEVICE SELECT RESULT

#### FUNCTION

This command may be used by a software driver that is setup to handle multiple device types.

**DEVICE TYPE** — Table 6-1.

#### **PHYSICAL SECTOR SIZE**

The physical sector size is expressed as the number of bytes between sector marks.

---

TABLE 6-1. DEVICE TYPES

Type Code (HEX)	Device Type
00	Invalid
01	Model 3350-10 or -01 (20,160 bytes/track)
02-03	Reserved
04	Model 3450 (13,440 bytes/track)
05	Model 7050 (13,440 bytes/track)
06	Model 6650 (20,160 bytes/track)
07	Model 15450 (20,160 bytes/track)
08	Model 804
09	Model 803
0A	Reserved
0B	Model 806
0C	Model 807
0D-FF	Reserved

### 6.2.6 Specify Parameters

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 0C HEX	0	7 INTERFACE STATUS
---		1 ---
DEVICE SELECT	2	TRANSACTION STATUS
PARAMETER SELECT	3	
PARAMETER BYTE	4	
---	5	???
---	6	
---	7	DEVICE SELECT RESULT

#### FUNCTION

This command allows the host to specify parameters associated with the DS101's operational characteristics. Default characteristics can be overridden using this command.

#### DEVICE SELECT

Device Select must be 40 HEX.

+

#### PARAMETER SELECT

- 0 Option Byte 0 (See Figure 6-3)
- 1 Option Byte 1 (See Figure 6-4)

+

#### PARAMETER BYTE

The parameter byte selected to be specified should be written to this register.

**FIGURE 6-3. OPTION BYTE 0**

7	6	5	4	3	2	1	0
///  ADM ICE CCE  EP							

**ADM — AUTOMATIC DEFECT MANAGEMENT DISABLE**

If ADM = 1 the Automatic Defect Management feature will be disabled.

**ICE — INITIALIZATION COMPLETE INTERRUPT ENABLE**

If ICE = 1 an interrupt (HIR) will be generated after the DS101 has completed the power up/reset diagnostics.

**CCE — COMMAND COMPLETION INTERRUPT ENABLE**

If CCE = 1 an interrupt (HIR) will be generated when the CCR (Command Completion Request) bit is set in the Interface Status Register. HIR due to a CCR is cleared by issuing a Completion Acknowledge (00 HEX) command.

**EP — ENABLE PARITY**

If EP = 1 the DS101 will check for even parity on the host bus interface.

When the DS101 is initialized, Option Byte 0 is set to the values selected by the DIP switches (see Table 2-2). Switches 1 thru 8 affect bits 7 thru 0, respectively, of Option Byte 0.

**FIGURE 6-4. OPTION BYTE 1**

7	6	5	4	3	2	1	0
///  HPD BTE WTD							

**BTE — BLOCK TRANSFER INTERRUPT ENABLE**

If BTE = 1, an interrupt (HIR) will be generated and the BTI bit in the Interface status register will be set whenever the DS101 requires a block transfer. HIR and BTI are cleared by issuing a Clear BTI (01 HEX) command.

**WTD — WATCHDOG TIMER DISABLE**

If WTD = 1, all software Watchdog timing functions are disabled. These functions are related to data transfers, commands to disc drives, commands via Aux boards, device motion, and Resume Packet Execution.

**HPD — HIGH PERFORMANCE DISABLE**

If HPD = 1, the DS101 high performance mode is disabled.  
HPD is normally set to 0.

When the DS101 is initialized, Option Byte 1 is set to zero.

### 6.2.7 Read Parameters

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = OB HEX	0	7 INTERFACE STATUS
---		---
DEVICE SELECT	1	TRANSACTION STATUS
PARAMETER SELECT	2	PARAMETER BYTE
---	3	---
---	4	---
---	5	???
---	6	---
---	7	DEVICE SELECT RESULT

#### FUNCTION

This command allows the host to interrogate parameters associated with the DS101's operational characteristics.

#### DEVICE SELECT

Device Select must be 40 HEX.

#### PARAMETER SELECT

- 0 Option Byte 0 (See Figure 6-3).
- 1 Option Byte 1 (See Figure 6-4).

#### PARAMETER BYTE

The parameter byte selected to be read is reported in this register.

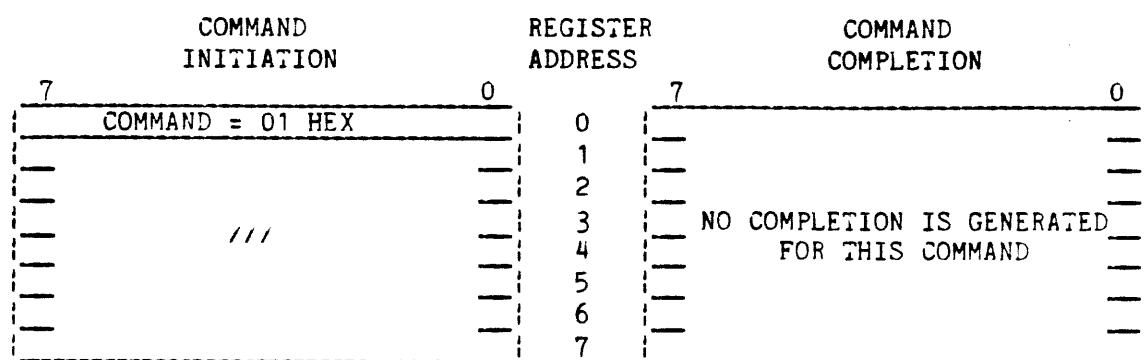
### 6.2.8 Completion Acknowledge

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 00 HEX	0	7
—	0	—
—	1	—
—	2	—
—	3	NO COMPLETION IS GENERATED
—	4	FOR THIS COMMAND
—	5	—
—	6	—
—	7	—

#### FUNCTION

This command is used to clear the Command Completion Request bit after the host has completed aquiring the command completion results. This command will also clear the special Completion Request (if set) and HIR (if CCI in option Byte 0 is set -- see Figure 6-3).

### 6.2.9 Clear BTI



#### FUNCTION

This command will clear the Block Transfer Interrupt status bit and HIR (if BTE in option Byte 1 is set see Figure 6-4).

### 6.3 Diagnostic Functions

The DS101 performs three distinct types of diagnostic procedures:

- o Power Up Diagnostics -- Those performed automatically upon power up or software reset.
- o User-invoked Diagnostics -- Those which are performed in response to a diagnostic command sent by the host to the DS101.
- o In-process Diagnostics -- Those which are inherent in the execution of individual commands.

#### 1. Power Up Diagnostics

Upon power up (or software reset) the DS101 performs an initialization routine. The initialization sequence includes a RAM test, an ID buffer test and a PROM test. If the initialization is complete and normal, the value 16 HEX is returned for the transaction status, and the following values are placed in the remaining registers:

<u>Register Read</u>	<u>Value (HEX)</u>
3	AA
4	55
5	F0
6	0F
7	00

The RAM test is performed on the microprocessor scratch pad RAM and the data buffer. The RAM test is performed by writing each memory location with a data value equal to its own address (LSB), then reading the RAM and comparing the values read with those written. The entire process is then repeated, using data values equal to the complement of the respective addresses. If an error occurs the value 1A is returned for the Transaction Status, and Register File locations 3-7 are loaded with the following information:

<u>Register Read</u>	<u>Description</u>
3	Expected Data
4	Received Data
5	Memory Address MSB
6	Memory Address LSB
7	Type - 00 = Buffer 01 = Scratch Pad

The ID buffer test consists of a series of paired write/read operations to/from the four byte locations of the ID buffer:

	<u>ID Buffer Location</u>			
	<u>0</u>	<u>1</u>	<u>2</u>	<u>3</u>
First write/read:	00	01	02	03
Second write/read:	01	02	03	04
Third write/read:	02	03	04	05
	.	.	.	.
Last write/read:	FF	01	02	03

If a discrepancy is found, the value 1B is returned for the transaction status, and Register File locations 3-5 are loaded with the following information:

<u>Register Read</u>	<u>Description</u>
3	Expected Data
4	Received Data
5	Buffer Location

The PROM test is performed on the microprocessor program area. Each PROM contains a 16-bit checksum in the last two locations. Each PROM contains a 16-bit checksum in the last two locations. At power-up the checksum is computed and compared with the stored value. If a PROM failure is detected the PROM number is reported in Register 3 as follows:

<u>Register File Location 3</u>	<u>Description</u>
=0	PROM Location 9L
=1	PROM Location 8L
=2	PROM Location 6L

## 2. User-invoked Diagnostics

The user-invoked diagnostics include the following commands:

- 04 Write Buffer
- 03 Read Buffer
- E0 Transfer Parameter to Result
- E1 ID Buffer Transfer Test

The Write Buffer command is used in conjunction with the Read Buffer command to test the data buffer RAM. Refer to the individual command descriptions for details.

### 6.3.1 Register File Wrap

COMMAND INITIATION		REGISTER ADDRESS	COMMAND COMPLETION	
7	0	7	0	
COMMAND = E0 HEX		0	INTERFACE STATUS	
---		1	---	
TEST BYTE 0		2	TEST BYTE 0	
TEST BYTE 1		3	TEST BYTE 1	
TEST BYTE 2		4	TEST BYTE 2	
TEST BYTE 3		5	TEST BYTE 3	
TEST BYTE 4		6	TEST BYTE 4	
TEST BYTE 5		7	TEST BYTE 5	

#### FUNCTION

The Register File Wrap command may be used to test the operation of Registers 2 thru 7. The host writes any six bytes to registers 2 thru 7, and then reads these six bytes (after the DS101 has transferred the test bytes) and compares the values received with the values written.

### 6.3.2 ID Buffer Transfer Test

COMMAND INITIATION		REGISTER ADDRESS	COMMAND COMPLETION	
7	0	7	0	
COMMAND = E1 HEX		0	INTERFACE STATUS	
---		1	---	
///		2	TRANSACTION STATUS	
TEST BYTE 0		3	TEST BYTE 0	
TEST BYTE 1		4	TEST BYTE 1	
TEST BYTE 2		5	TEST BYTE 2	
TEST BYTE 3		6	TEST BYTE 3	
///		7	???	

#### FUNCTION

The ID Buffer Transfer Test command may be used to test the operation of the ID buffer. The host writes any four bytes to registers 3 thru 6 and issues command E1. The four bytes are transferred via the 4 byte ID buffer to the corresponding result registers. The host then reads the result registers and compares each byte with its respective original input.

### 6.3.3 Read Buffer

#### Read Buffer (SMART/-E Compatible)

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 03 HEX	0	7 0
---	1	INTERFACE STATUS
	2	BLOCK INPUT
	3	TRANSACTION STATUS
///	4	
	5	???
	6	
	7	

#### FUNCTION

The Read Buffer command may be used in conjunction with the Write Buffer command to test the DS101 data buffer. Starting at buffer address zero, the DS101 will transfer 2048 bytes from its internal buffer to the host.

#### 6.3.4 Read Buffer (Extended)

COMMAND INITIATION		REGISTER ADDRESS	COMMAND COMPLETION	
7	0	7	0	
COMMAND = E4 HEX		0	INTERFACE STATUS	
---		1	BLOCK INPUT	
03 HEX		2	TRANSACTION STATUS	
///		3		
OFFSET	MSB	4		
	LSB	5	???	
COUNT	MSB	6		
	LSB	7		

#### FUNCTION

The Read Buffer command may be used in conjunction with the Write Buffer command to test the DS101 data buffer. The DS101 will transfer the specified number of bytes from its internal buffer to the host. The initial location from which the data will be sent is specified as an offset from the start of the DS101's buffer.

#### **OFFSET**

This field is a 16 bit offset (from zero) into the DS101 buffer for the start of the transfer. The DS101 buffer contains 16K bytes (0-3FFF HEX).

#### **COUNT**

The count field specifies the number of bytes that are to be transferred to the host.

### 6.3.5 Write Buffer

#### Write Buffer (SMART/-E Compatible)

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7 COMMAND = 04 HEX	0	7 INTERFACE STATUS
BLOCK OUTPUT	1	---
---	2	TRANSACTION STATUS
---	3	---
---	4	---
---	5	---
---	6	---
---	7	???

#### FUNCTION

The Write Buffer command may be used in conjunction with the Read Buffer command to test the DS101 data buffer.

Starting at buffer address zero, the DS101 will transfer 2048 bytes from the host to its internal buffer.

### 6.3.6 Write Buffer (Extended)

COMMAND INITIATION	REGISTER ADDRESS	COMMAND COMPLETION
7	0	0
COMMAND = E4 HEX		INTERFACE STATUS
BLOCK OUTPUT		---
04 HEX		TRANSACTION STATUS
OFFSET	MSB	---
	LSB	---
COUNT	MSB	???
	LSB	---
///		---
	7	

#### FUNCTION

The Write Buffer command may be used in conjunction with the Read Buffer command to test the DS101 data buffer.

The DS101 will transfer the specified number of bytes from the host to its internal buffer. The initial location to which the data will be sent is specified as an offset from the start of the DS101's buffer.

#### **OFFSET**

This field is a 16 byte offset (from zero) into the DS101 buffer to the start of the transfer. The DS101 buffer contains 16K bytes (0-3FFF HEX).

#### **COUNT**

The count field specifies the number of bytes that are to be transferred to the DS101 buffer.

## 7.0 ERROR RECOVERY

### 7.1 Error Retry Technique

If an error occurs during the execution of the command and the retry feature is selected (i.e., retries are enabled), the DS101 will automatically retry the command. If retries are not enabled, the command is aborted and the appropriate transaction status is immediately returned to the host. Table 7-1 outlines the retry strategies employed. All the commands that require accessing data are preceded by a seek to the correct cylinder before the data transfer is begun. If the command is a logical or physical data access, the disc cylinder is verified by reading the ID field information.

TABLE 7-1. ERROR RECOVERY STRATEGY

<u>Error Type</u>	<u>Retry Procedure</u>
CRC Error	b
ECC Error	f
Motion Fault	c
Data Fault	d
Device Not Ready	d
Write Protect	None
Sector Not Found	e
Device Command Reject	None
Device Command Timeout	d
Host Data Transfer Timeout	a
Illegal Transfer Address	None

#### Retry Procedures

- a. The command must be reissued by the host.
- b. The DS101 automatically performs four retries for any operation that results in a CRC error.
- c. If a motion fault occurs, the motion fault is reset and the operation is retried four times.
- d. A reset is issued to the drive and the command is retried four times.
- e. The defect mapping logic is initiated when a sector is not found.
- f. The DS101 automatically performs four retries for any operation that results in an ECC error. If the error persists, four additional retries are performed, and the syndrome pattern is checked for recurrence. If a given pattern appears two times, error correction is attempted, using the ECC.

## 7.2 ECC - Error Correcting Code

The DS101 supports 32-bit computer generated code that is selected for insensitivity to short double bursts with good detection span. The ECC check characters and error syndromes are generated by hardware. ECC correction is performed under software control. It should be noted that there is no performance penalty resulting from the use of the ECC error detection capability if error correction is not attempted. When error correction is invoked, the DS101 returns a 03 completion code in the Transaction Status register. Note that when an ECC error is encountered, either correctable or uncorrectable, the Automatic Defect Management feature will be invoked if it has not been disabled. The operation of the error recovery logic is impacted by the Mode byte specified by the host (see Section 6.2.2). If the DS101 is operating in direct mode, the data has been transferred to the host memory before an ECC error is detected. The recommended error recovery is as follows:

1. Direct mode unrecoverable ECC error reported.
  2. Change Mode byte to buffered operation.
  3. Reissue read command.
  4. If read successful, rewrite sector.
  5. If re-read error free, restore direct mode.
  6. If re-read in error, specify bad sector and rewrite.
  7. Restore direct mode.
- 

TABLE 7-2. ECC CHARACTERISTICS SUMMARY

- o 32-bit computer-generated code.
  - o Maximum correction span of 5 bits.
  - o Single burst detection span of 32 bits.
  - o Optimized for double burst detection.
  - o No performance penalty unless ECC correction required.
  - o Read retry recovery from soft errors.
  - o ECC correction attempted only on hard errors with a repeatable syndrome.
-

### 7.3 Transaction Status Detail

This section provides a summary of the completion codes and a detailed description of each code.

**TABLE 7-3. COMPLETION CODE DEFINITIONS (Transaction Status Bits 5-0)**

<u>Completion Code (Transaction Status Bits 5-0)</u>	<u>Description</u>
00	No Retries Required This status code indicates that the command completed successfully without any retries.
01	Motion Retries Performed This status code indicates that an automatic retry was used to recover from an error and then the command completed successfully.
02	Data Retries Performed This status code indicates that a data error occurred but an automatic retry recovered from the error and completed the command successfully.
03	ECC Correction Performed This status code indicates that a hard read error occurred but the ECC logic was able to correct the bits in error.
08	Packet Termination - Not Resumable - Good Completion This status code indicates that a packet command has terminated, and is not resumable. This arises when all commands in a packet have been executed to completion. See Table 9-3 for Supplemental Status Codes.
0A	Packet Aborted This status code indicates that a packet operation was aborted by an Abort Packet command.
10	Late Data Transfer This error may occur when operating the DS101 in direct mode. A late data transfer will occur if the host interface does not read/write data fast enough to match the disc transfer rate.
11	Uncorrectable ECC Error This status code indicates that a CRC error was detected on a read operation, or that an uncorrectable ECC error was detected.
12	Motion Fault - Drive Reported This status code indicates that a seek was attempted and the seek failed.

Completion Code  
(Transaction Status  
Bits 5-0)

		<u>Description</u>
13	Data Fault	<p>This status code indicates that the operation was terminated due to an error detected by the device. The fault conditions detected by PRIAM Winchester drives are:</p> <ol style="list-style-type: none"><li>1. WRITE GATE without write current at the head.</li><li>2. Write current at the head without WRITE GATE.</li><li>3. WRITE GATE without READY.</li><li>4. More than one head selected.</li><li>5. No transitions during write (MFM format).</li><li>6. WRITE GATE with WRITE PROTECT.</li><li>7. WRITE GATE between INDEX and the first SECTOR MARK (when the Skip Defect Record is write protected).</li></ol>
14	Auxiliary Trap (Supplemental Status)	<p>This status code indicates that an error has been detected by an Auxiliary Controller Board. Supplemental status is reported in Register 3, as detailed in the Auxiliary Controller Boards Product Specification.</p>
15	Motion Fault - DS101 Reported	<p>This status code indicates that a seek was performed and completed by the drive, but a comparison of the drive current cylinder registers with the intended address indicated that the wrong cylinder was accessed.</p>
16	Initialization Complete	<p>This status code indicates that the DS101 has successfully completed a restart operation (power up or interface line reset). This completion provides the following File Register values:</p> <p>Register 3 = AA Register 4 = 55 Register 5 = F0 Register 6 = 0F Register 7 = 00</p>

<u>Completion Code (Transaction Status Bits 5-0)</u>	<u>Description</u>												
17	<p>Hardware Trap (No Supplemental Status yet defined)  This status code indicates that a hardware system failure has been detected. Supplemental status will be reported in Register 3. The user should note the value found in Register 3 for use in communications with PRIAM technical support.</p>												
18	<p>Software Trap (Supplemental Status see Table 9-4)  This status code indicates that an error has been detected by the DS101 software system.  Supplemental status is reported in Register 3, as detailed in Section 7.4.</p>												
19	<p>Device Data Transfer Timeout  This status code indicates that read operation was terminated before the expected number of data bytes were read from the disc.</p>												
1A	<p>RAM Failure  This status code indicates that the microdiagnostics have detected a bad RAM location.</p>												
	<p>The File Registers have the following meanings:</p> <table> <tr><td>Register 3</td><td>=</td><td>Expected Data</td></tr> <tr><td>Register 4</td><td>=</td><td>Received Data</td></tr> <tr><td>Register 5</td><td>=</td><td>Memory Address MSB</td></tr> <tr><td>Register 6</td><td>=</td><td>Memory Address LSB</td></tr> </table>	Register 3	=	Expected Data	Register 4	=	Received Data	Register 5	=	Memory Address MSB	Register 6	=	Memory Address LSB
Register 3	=	Expected Data											
Register 4	=	Received Data											
Register 5	=	Memory Address MSB											
Register 6	=	Memory Address LSB											
1B	<p>ID Buffer Failure  This status code indicates that the microdiagnostics have detected an error in the ID buffer.</p>												
	<p>The File Registers have the following meanings:</p> <table> <tr><td>Register 3</td><td>=</td><td>Expected Data</td></tr> <tr><td>Register 4</td><td>=</td><td>Received Data</td></tr> <tr><td>Register 5</td><td>=</td><td>Buffer Location</td></tr> </table>	Register 3	=	Expected Data	Register 4	=	Received Data	Register 5	=	Buffer Location			
Register 3	=	Expected Data											
Register 4	=	Received Data											
Register 5	=	Buffer Location											
1C	<p>Bus Parity Error  This status code indicates that the DS101 Interface has detected a parity error (the HCBUS7-HCBUS0 and HCBUSP should have even parity) on the host interface. This applies to both commands and data.</p>												

Completion Code  
(Transaction Status  
Bits 5-0)

Description

1D	PROM Cnecksum Error This status code indicates that the diagnostics have detected a program ROM failure.  Register 3 contains the PROM number in error:  = 0      PROM Location 9L = 1      PROM Location 8L = 2      PROM Location 6L
20	Device Not Ready This status code indicates that the DS101 attempted to access a device, and the device did not indicate that it was ready within the expected period of time, as for example when a Winchester drive has failed to sequence up within the allowable time limit.
21	Write Protect This status code indicates that a write operation was attempted on a write-protected drive.
22	Device Not Present The device specified is not connected or not powered up.
23	Sector Size Invalid The sector switches on the drive are set incorrectly.
24	Alternate Area Overflow This status code indicates that there are more defective sectors or tracks than there are spare sectors or tracks on the disc.
25	Defect Directory Full The defect mapping logic was unable to expand the size of the defect directory because all available space was in use.
26	End of Defect Directory If the disc has been formatted with defect mapping enabled, there will be a Defect Directory located in the user alternate area. The directory is a linked list of 128 byte records that are numbered through N-1 where N is the number of 128 byte records in the directory. This error code will be received if a Read or Write Defect Directory command is issued that has specified a record number greater than N.

Completion Code  
 (Transaction Status  
Bits 5-0)

	<u>Description</u>
27	Defect Directory Not Present This status code indicates that a Read Defect Directory command was issued to a drive that was formatted without defect mapping.
28	Packet Termination - Resumable (Supplemental Status - See Table 9-3) This status code indicates that a packet command has terminated, but is resumable. The host may issue a Resume Packet command to restart packet execution. This normally occurs when an end of media condition has been encountered, or if the source device is a tape and the "hold step on EOF mark" has been set.
29	Packet Termination - Not Resumable - Fatal Error Occurred (Supplemental Status - See Table 9-3)
30	Sector Not Found This code indicates that the specified logical sector could not be located.
31	SMART Command Reject This status code indicates that the received command is not supported by the DS101.
32	Device Command Time-out This status code indicates that the DS101 issued a command to the drive and the drive did not properly complete the command.
33	Host Data Transfer Timeout This status code indicates that the DS101 Interface requested a data transfer to the host and the transfer was not completed within 3 seconds.
34	Illegal Transfer Address This code indicates that a head number or cylinder number greater than the maximum supported was specified as a parameter.
35	Invalid Device Select This code indicates that a drive number greater than three was specified as a parameter.
36	Sector Number Invalid This code indicates that a physical operation (as distinguished from a logical operation) failed to find the specified sector.

Completion Code  
(Transaction Status  
Bits 5-0)

Description

- |    |   |
|----|---|
| 37 | <b>Command Already In Progress</b><br>This code indicates that the specified device already had a command in progress.  |
| 38 | <b>Command Double Write</b><br>This error occurs if the host writes to the command or parameter registers when the Register File Busy bit is set.   |
| 39 | <b>Device Command Reject</b><br>This error code indicates that the received command is not supported by the device.   |
| 3A | <b>Multisector Operation Error</b><br>This error code indicates that a read or write data command was issued with a multisector count equal to zero.  |
| 3B | <b>Invalid Interleave Factor</b><br>This error code indicates that a command requiring an interleave factor was issued and that the interleave factor was incorrect. The discussion on interleaving describes the use of the interleave factor. |

#### 7.4 Software Trap Supplemental Status Detail

This section defines the supplemental status information for the Software Trap (18 HEX) transaction status condition. This supplemental information is reported in Register 3, as shown in Figure 7.1.

FIGURE 7-1. COMMAND COMPLETION REPORT

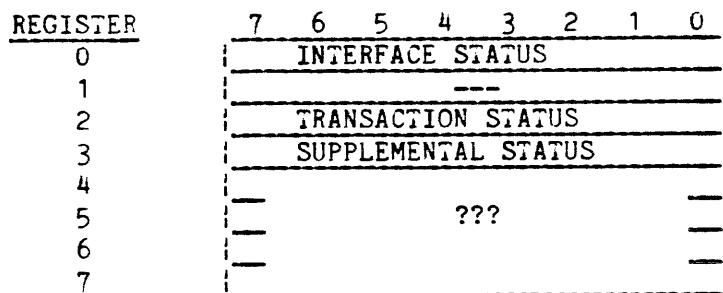


TABLE 7-4. SOFTWARE TRAP SUPPLEMENTAL STATUS DEFINITIONS

CODE	DEFINITION
00	No Configuration Record This status code is returned by the Format process for a Winchester disc when, at the end of the format procedure, no good tracks can be found on the last cylinder, and the DS101 is unable to write a copy of the configuration record.
01	Format SDR Limit During formatting, if an I/O error occurs when the Skip Defect Record (SDR) is read, or if its checksum is incorrect, the corresponding track is formatted as a bad track. The DS101 permits 25 such errors to occur during the entire formatting process. Format aborts and returns this status code as soon as the 26th SDR error occurs.
02	System Full This status code indicates that the system contains 12 devices. No further devices may be accessed without replacing an existing device and issuing a Read Device Parameters command for the new device.
03	Invalid Device Type This status code is returned when the host issues an incompatible command to a device (for example, Rewind Disc).
04	Aux Board Not Present This code indicates that a command was issued to an Aux channel that did not have an Aux board attached.
05	Aux Fault This code is issued when the controller is having difficulty communicating with the Aux board.

TABLE 7-4 CONTINUED

<u>CODE</u>	<u>DEFINITIONS</u>
06	Invalid Mode The current Mode Byte specifies a mode which is incompatible with the selected device (i.e. - a tape related command being sent when the Mode Byte specifies direct mode).
07	Incorrect Power-up PROM The DS101 detected an incorrect ID on the first PROM it accessed during a Power-Up or Reset.
08	Version and/or PROM number mismatch The DS101 detected an incorrect ID on the second or third PROM it accessed during a Power-Up or Reset.
09	Invalid AUX type The Aux Board ID does not match the device type referenced in a command for a given Aux channel.

## 7.5 Packet Related Supplemental Status

This section defines the supplemental status information for the three Packet Completion Codes, 08H (Good Completion - Not Resumable), 28H (Good Completion - Resumable), and 29H (Error - Not Resumable). These codes are reported in the Supplemental Status register.

**TABLE 7-5. PACKET RELATED SUPPLEMENTAL STATUS DEFINITIONS**

<u>Code</u>	<u>Related Completion Code</u>	<u>Definition</u>
01	28	<u>End of Destination Media</u> - Resumable completion if new media is installed in removable media device within 15 minutes. Not a resumable completion if the device is a fixed media device.
02	28	<u>End of Source Media</u> - (see code 01 of this table)
20	29	<u>Unrecognized Step Operation Code</u> - Same as Command Reject for register based commands. With multi-step packets, the operation codes are checked when the individual steps begin execution.
21	29	<u>Illegal Device in Step Parameters</u> - A device was specified which is not valid for the operation selected. The device vs. operation check is performed when the individual steps begin execution.
2F	29	<u>Resume Not Sent Within 15 Minutes</u> - Fifteen minute timeout after posting a resumable Completion Code (28 HEX). The Completion Code would now be 29 HEX.
30	29	<u>All Available Packet Space Used or Illegal Packet ID</u> - Host attempted to send more than 512 bytes in a packet, or an illegal packet ID was sent (packet ID other than zero).
31	29	<u>Packet ID Already In Use</u> . - As of June 1983 the only valid packet ID is zero and only one packet may be loaded on the DS101 at one time.
32	29	<u>Illegal Packet Step Length</u> - The DS101 has determined that, considering the packet operation code and all other pertinent information, a step within a packet is not the proper length. Step lengths are checked when the individual steps begin execution.

TABLE 7-5. PACKET RELATED SUPPLEMENTAL STATUS DEFINITIONS CON'T

- |    |    |   |
|----|----|---|
| 33 | 29 | <u>Non-Existant Packet ID Specified</u> - A register based, packet related command has been sent which references a packet ID which no current packet has (see also code 31 of this table). |
| 34 | 29 | <u>Packet Not Resumable</u> - This code is returned when a Resume Packet Execution command is issued for a non-resumable packet.  |
| 38 | 29 | <u>Illegal Device Flag Specified</u> - The DF bit in the register based Resume Packet Execution command is not correct for the situation.   |

## 8.0 DEVICE DEPENDENT HARDWARE REFERENCE

### 8.1 PRIAM Winchester Discs

TABLE 8-1. PRIAM DISC DRIVE CHARACTERISTICS

Model	Disc Size	No. of Data Heads	No. of Servo Heads	Data Transfer Rate MB/Sec	Usable Bytes per Track	Bytes per Cyl.	Bytes per Drive	Cyl. per Drive
3350-10	14"	3	1	1.04	20,124	60,372	33,868,692	561
6650-10	14"	3	1	1.04	20,124	60,372	67,677,012	1121
15450-10	14"	7	1	1.04	20,124	140,868	157,913,028	1121
3450-10	8"	5	1	0.8	13,404	67,020	35,185,500	525
7050-10	8"	5	1	0.8	13,404	67,020	70,303,980	1049
803	8"	5	1	1.21	20,124	100,800	85.68M	850
804	8"	5	1	1.21	20,124	100,800	105.74M	1049
806	8"	11	1	1.21	20,124	221,760	188.5M	850
807	8"	11	1	1.21	20,124	221,760	330.2M	1489

Data capacities specified are based upon the number of eight bit bytes that may be recorded on a track. This unsectored capacity does not include any allowance for gaps or any format overhead. However, allowance is made for the 36 byte defect record.

## 8.2 Winchester - Disc Format

### 8.2.1 Sector Format

The track format used by the Interface is shown in Figure 9-1.

Each track starts with an INDEX pulse, which corresponds to a certain position on the servo track. The servo track also provides rotational position information for the generation of SECTOR pulses. A sector pulse precedes each record, and successive records are separated by gaps within which the sector pulses occur. The sector size is selected by setting the sector switches on the drive according to the decimal physical sector size. Table 8-4 defines the sector switch settings required to select 256, 512, or 1024 byte logical sector sizes on each of the PRIAM drive types. It is recommended that all Winchester disc drives in a system be set to the same sector size.

#### PRE-RECORD GAP (GAP 1)

The Pre-Record Gap, or Gap 1, appears at the beginning of every record. It consists of 23 bytes of zeros. The length of Gap 1 never varies. The first Gap 1, after INDEX, is followed by the Skip Defect Record. All other Gap 1's, after SECTOR pulses, are followed by ID records.

#### SKIP DEFECT RECORD

The Skip Defect Record (Table 9-2) consists of 11 bytes: a Data Sync using the hexadecimal pattern FB, the address of the first defect using 2 bytes, the address of the second defect using 2 bytes, the address of the third defect using 2 bytes, a checksum across the previous 3 words (2 bytes) using 2 bytes, and fill characters of zeros using 2 bytes. If an address is 0000, then there are not any additional defects on the track. If the address of the first defect is FFFF HEX, the whole track is defective.

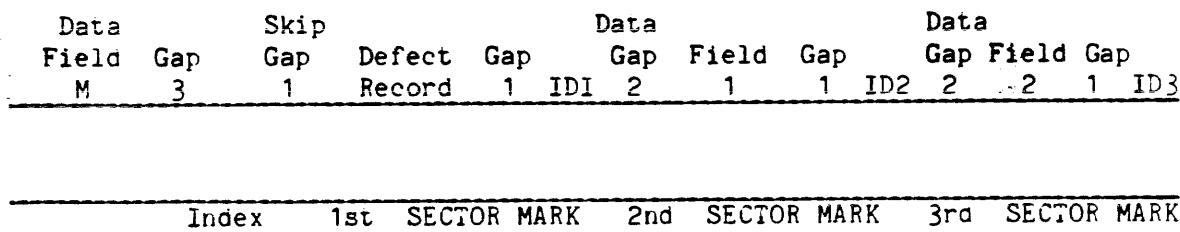
---

TABLE 8-2. DEFECT RECORD FORMAT

<u>Decimal Location</u>	<u>Data</u>
000-022	Gap 1 - 23 Zeros
023	Defect Record Sync (FB Hex)
024	1st Address MSB
025	1st Address LSB
026	2nd Address MSB
027	2nd Address LSB
028	3rd Address MSB
029	3rd Address LSB
030	Checksum MSB
031	Checksum LSB
032-035	Fill (Zero)

---

**FIGURE 8-3. TRACK FORMAT**



**TABLE 8-3. TRACK FORMAT**

Index:	Derived from servo track	
Gap 1:	Zeros	23 Bytes
Skip Defect Record:	Data Sync, FB Hex 1st defect address 2nd defect address 3rd defect address Checksum Fill characters - zeros	1 Byte 2 Bytes 2 Bytes 2 Bytes 2 Bytes 2 Bytes
Gap 1:	Zeros	23 Bytes
Sector Mark:	Derived from INDEX and servo clock	
ID Field:	ID Sync, F9 Hex Sector address Head and cylinder address MSB Cylinder address LSB ID Control ECC Fill characters (zeros)	1 Byte 1 Byte 1 Byte 1 Byte 1 Byte 4 Bytes 2 Bytes
Gap 2:	Zeros	11 Bytes
Data Field:	Data Sync, FD Hex Data ECC Fill characters (zeros)	1 Byte 128, 256, 512, or 1024 Bytes 4 Bytes 2 Bytes
Gap 3:	Zeros (size depends on data field size)	

### **ID FIELD**

The Identification Field contains 11 bytes: an ID sync using the hexadecimal pattern F9, the sector number of 1 byte, the head address and high order cylinder address of 1 byte, the low order cylinder address of 1 byte, an ID control field of 1 byte, 4 ECC (Error Correction Code) bytes, and 2 bytes of zeros for filling. The cylinder and head address, along with the sector number, verify that the drive has addressed the correct track and sector. The ID control field is discussed in the Section 5.2.1.

### **ID GAP (GAP 2)**

The ID Gap, or Gap 2, separates each successive Identification Field (ID) from its Data Field. It contains 11 bytes of zeros.

### **DATA FIELD**

Following Gap 2, the Data Field consists of 135, 263, 519, or 1031 bytes depending on the selected data length. The first byte is the data sync (hexadecimal pattern FD), while the last bytes consist of 4 bytes of ECC and 2 bytes of zeros.

### **PRE-INDEX GAP (GAP 3)**

The Pre-Index Gap, or Gap 3, is used only once on a track. It appears at the end of the last data field and persists until INDEX. This gap contains zeros.

---

**TABLE 8-4. SECTOR FORMAT SUMMARY - 3350/6650/15450/80X**  
(20,160 bytes/track)

<u>Logical Size*</u>	<u>Physical Size</u>	<u>Sectors Per Track</u>	<u>Switch Setting</u>
256	309	65	7, 1
512	574	35	6, 2, 1
1024	1118	18	5, 2

NOTE: Switch 8 should be off.

---

**TABLE 8-5. SECTOR FORMAT SUMMARY - 3450/7050**  
(13,440 bytes/track)

<u>Logical Size*</u>	<u>Physical Size</u>	<u>Sectors Per Track</u>	<u>Switch Setting</u>
256	311	43	6, 4, 2, 1
512	582	23	5, 3, 2, 1
1024	1117	12	4, 3

NOTE: Once a Sector Switch is set the disc must be sequenced down, then sequenced back up in order to initialize the Sector Mark generator to the newly selected value.

---

\* These tables list common sector sizes. The DS101 will accept any sector size up to 2K bytes. Performance may be reduced if sector size is less than 256 bytes. It is recommended that all Winchester disc drives attached to a common DS101 be set to the same sector size.

## 9.0 SUMMARY/QUICK REFERENCE

Table 9-1 is a summary of the register based commands that are supported by the DS101. These commands are discussed in Sections 5 and 6 of this specification.

TABLE 9-1. COMMAND SUMMARY

<u>COMMAND CODE (HEX)</u>	<u>COMMAND NAME</u>
00	Completion Acknowledge
01	Clear BTI (Block Transfer Interrupt)
03	Read Buffer (SMART/-E compatible)
04	Write Buffer (SMART/-E compatible)
+ 06	Read Device Status
+ 07	Software Reset
+ 08	Specify Mode
+ 09	Read Mode
+ 0B	Read Parameters
+ 0C	Specify Parameters
40	Restore
# 44	Verify Data
# 48	Verify ID
# 51	Seek - Wait - Retry Enabled
# 41	Seek - Wait - Retry Disabled
# 52	Write Data - Retry Enabled
# 42	Write Data - Retry Disabled
# 53	Read Data - Retry Enabled
# 43	Read Data - Retry Disabled
# 55	Write ID - Retry Enabled
# 45	Write ID - Retry Disabled
# 56	Read ID - Retry Enabled
# 46	Read ID - Retry Disabled
# 57	Read ID Immediate - Retry Enabled
# 47	Read ID Immediate - Retry Disabled
# 59	Read Skip Defect Field - Retry Enabled
# 49	Read Skip Defect Field - Retry Disabled
# 5A	Write Skip Defect Field - Retry Enabled
# 4A	Write Skip Defect Field - Retry Disabled

<u>COMMAND CODE (HEX)</u>	<u>COMMAND NAME</u>
81	Sequence Down
82	Sequence Up - Wait
83	Sequence Up - Return
+ 85	Read Device Parameters
+ 86	Read Device Type
A0	Format Disc Without Defect Mapping
A1	Format Cylinder Without Defect Mapping
A2	Format Track Without Defect Mapping
A3	Verify Disc
A4	Verify Cylinder
A5	Verify Track
+ A6	Read Defect Directory
A8	Format Disc With Defect Mapping
#+ A9	Specify Bad Track
#+ AA	Specify Bad Sector
AB	Write Disc - Full Track
AC	Write Cylinder - Full Track
AD	Write Track - Full Track
+ B0	Transfer Packet
+ B1	Resume Packet Execution
B8	Read Packet Status
+ BF	Abort Packet
+ EO	Register File Wrap
+ E1	ID Buffer Transfer Test
E4	Read/Write Buffer (Extended)

- # In the DS101, commands marked with '#' will accept a logical address if the Interface is in Logical Sector Mode.
- + In the DS101, command marked with '+' will cause the Special Completion Request bit to be set in the Interface Status Register.

**TABLE 9-2. COMPLETION CODE SUMMARY**  
 (See Table 7-3)

<u>TYPE/CODE</u>	<u>DEFINITION</u>
00	No Retries Performed
01	Motion Retry Performed
02	Data Retry Performed
03	ECC Correction Performed
05	End of Media
08	Packet Termination - Good (Supplemental Status - Table 9-3)
0A	Packet Aborted
10	Late Data Transfer
11	Uncorrectable ECC Error
12	Motion Fault - Drive Reported
13	Data Fault
14	Auxiliary Trap (Supplemental Status) - See Appropriate Aux Board Specification
15	Motion Fault - DS101 Reported
16	Initialization Complete
17	Hardware Trap (Supplemental Status - no applicable table)
18	Software Trap (Supplemental Status - Table 9-4)
19	Device Data Transfer Timeout
1A	RAM Failure
1B	ID Buffer Failure
1C	Bus Parity Error
1D	PROM Checksum Error
20	Device Not Ready
21	Write Protect
22	Device Not Present
23	Sector Size Invalid
24	Alternate Area Overflow
25	Defect Directory Full
26	End of Defect Directory
27	Defect Directory Not Present
28	Packet Termination - Resumable (Supplemental Status - Table 9-3)
29	Packet Termination Not Resumable (Supplemental Status - Table 9-3)
30	Sector Not Found
31	SMART Command Reject
32	Device Command Time-Out
33	Host Data Transfer Time-Out
34	Illegal Transfer Address
35	Invalid Device Select
36	Sector Number Invalid
37	Command Already In Progress
38	Command Double Write
39	Device Command Reject
3A	Multisector Operation Error
3B	Invalid Interleave Factor

TABLE 9-3. PACKET RELATED SUPPLEMENTAL (29H, 28H & 08) STATUS CODES  
(See Table 7-5)

<u>CODE (HEX)</u>	<u>DEFINITION (Related Code)</u>
01	End of destination media (28)
02	End of source media (28)
20	Unrecognized step operation code (29)
21	Illegal device in step parameters (29)
2F	Resume not sent within 15 minutes (29)
30	All available packet space used/illegal packet ID (29)
31	Packet ID already in use (29)
32	Illegal packet step length (29)
33	Non-existent packet ID specified (29)
34	Packet not resumable (29)
38	Illegal Device Flag specified (29)
FE	No supplemental status available (08)

Note: Codes 10 - 2F are codes which may be outputted during packet execution. Codes 30 - 3F are codes which explain why a packet may not be executed.

**TABLE 9-4. SOFTWARE TRAP SUPPLEMENTAL STATUS CODES  
(See Table 7-4)**

<u>CODE (HEX)</u>	<u>DEFINITION</u>
00	No Configuration Record
01	Format SDR Limit
02	System Full
03	Invalid Device Type
04	Aux Board Not Present
05	Aux Fault
06	Invalid Mode
07	Incorrect Power up PROM
08	Version and/or PROM # mismatch
09	Invalid AUX type