MICROPROCESSOR – EXPT 2

WARREN FERNANDES 8940

CODE: data segment num1 dw 4444h num2 dw 0002h result dw? quo dw? rem dw? msg db 'Enter option: \$' msg1 db '1)ADD \$' msg2 db '2)SUB \$' msg3 db '3)MUL \$' msg4 db '4)DIV \$' code segment assume ds:data, cs:code start: mov ax,data mov ds,ax lea dx,msg mov ah,09h int 21h lea dx,msg1 mov ah,09h int 21h lea dx,msg2 mov ah,09h int 21h

lea dx,msg3 mov ah,09h int 21h lea dx,msg4 mov ah,09h int 21h mov ah,08h int 21h cmp al,31h jnz next1 mov ax,num1 add ax,num2 mov result,ax next1: cmp al,32h jnz next2 mov ax,num1 sub ax,num2 mov result,ax next2: cmp al,33h jnz next3 mov ax,num1 mov bx,num2 mul bx mov result,ax next3: cmp al,34h jnz next4

mov ax,0000h

mov dx,0000h

mov ax,num1

div num2

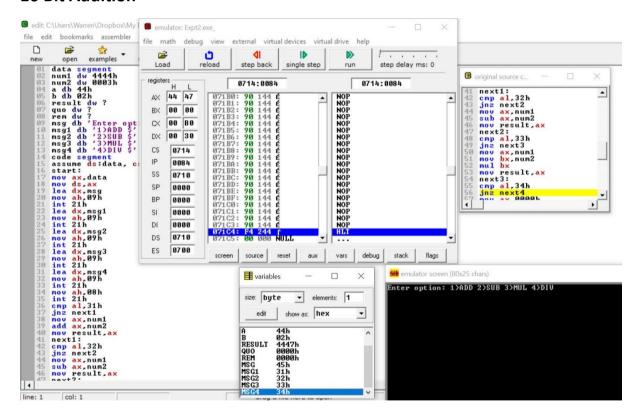
mov quo,ax

mov rem,dx

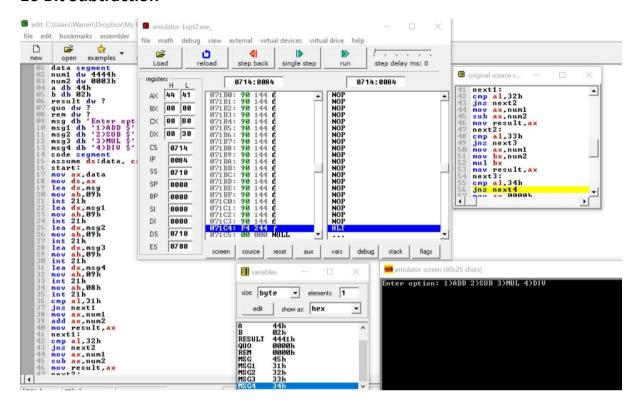
next4:

end start

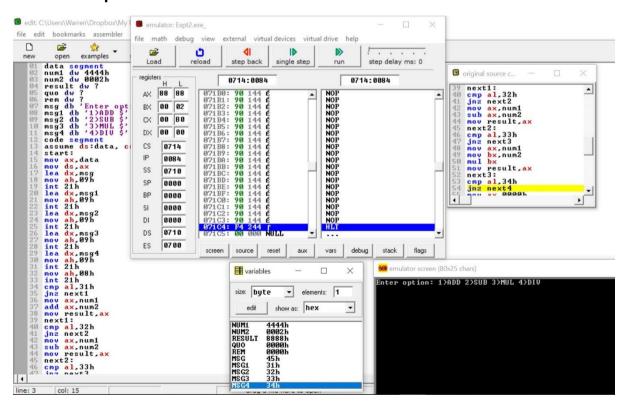
16 Bit Addition



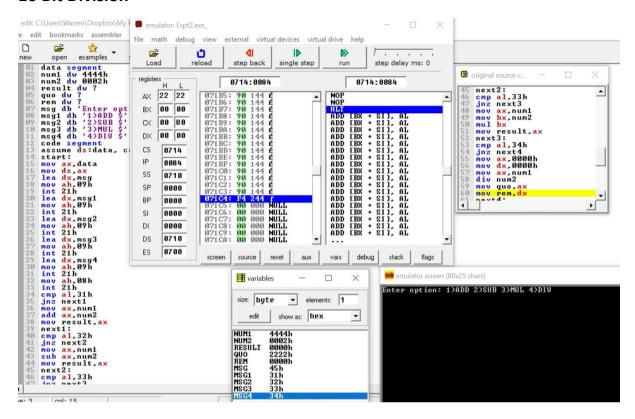
16 Bit Subtraction



16 Bit Multiplication



16 Bit Division



POSTLAB:

Q1.	Registers of 8086.
30	ALGISTON
	in 8086 Microprocessor the registors are
	categorized into mainly four types
	categorized into mainly four types. 1) General Purpose Registers.
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	The Children of the Control of the C
100	
	work others may wrong on our
30.5	value or some operands. 1) AX 2) BX 3) CX 4) DX
	1) AX 2) BX 3) CA . T)
	and sound and had accommodate to the
dos	a) Segment Registers.
0.0008	Deade Hegment.
19	users cannot modify the context
	2) Vata segment
	User can modify the content
	3) Stack degment
	SS is used to store the information
	about the memory segment 1
	a) Extra segment
	If there is less space in DS segment
	then Es is used
	a) Right & la 1000 Peniote-s
	3) Point & Index Registers.
	2) Base Pointer
	3) Stack Pointer
	A) source Index
	5) perhination Index 1
) beathmons 1.100 x

4) flag or Status registers.

The flag or Status register which contains of flags and the remaining of bits are idle in this register. These flags tell about the status of the process after any anotheretic or logical operation. 2 logical Address It is generated to by CPV while a program is running. The logical address is victural address as it does not exist physically therefore It is also known as Virtual Address . This address is used as a reference to accuss the physical memory location by CPU. The term degical advesses space. is used for the st of all bogical addresses The hardware device called Memory Management Unit is used for mapping logical address. Physical Address It identifies a physical location of required data in a memory the user never directly deals with the physical address but can access by it corresponding logical address must be mapped up to the physical address by MMV before they are used.