(a) If our processor has no forwarding and/or branch prediction (i.e., branches are resolved at the MEM stage, and we should stall the processor until it is resolved), fill in the following table. Write (f,d,e,m,w) for each column. If the processor has been stalled, show it by "-"(the first two instructions are filled already).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
addi	f	d	e	m	w															
ori		f	d	e	m	w														
sub			f	d	e	m	w													
add				f	d	-	e	m	w											
or					f	-	d	-	-	e	m	w								
lw							f	-	-	d	-	-	e	m	w					
beq										f	-	-	d	e	m	w				
and													-	-	-	f	d	e	m	w

(b) *Now assume that we have forwarding but the branch is still resolved at the MEM stage. Complete the table again. Show stalls with "-". If there is a forwarding, show it with ∗ (for BOTH the forwarding stage and EX).*

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
addi	f	d	e	m	w										
ori		f	d	e	m	w∗									
sub			f	d	e	m	w∗								
add				f	d	e∗	m	w							
or					f	d	e∗	m∗	w∗						
lw						f	d	e∗	m	w					
beq							f	d	e∗	m	w				
and								-	-	-	f	d	e	m	w

(c) *Now assume that we have forwarding and the branch is resolved at the DE stage. Complete the table again. Use "-" for stalls and ∗ for forwarding.*

	1	2	3	4	5	6	7	8	9	10	11	12	13
addi	f	d	e	m	w								
ori		f	d	e	m	w∗							
sub			f	d	e	m	w∗						
add				f	d	e∗	m	w					
or					f	d	e∗	m∗	w∗				
lw						f	d	e∗	m	w			
beq							f	d	e∗	m	w		
and								-	f	d	e	m	w

(d) *What is the speed up in case b compared to a?*

There is a 5 cycle speed up in case b comared to case a.

(e) *What is the speed up in case c compared to a?*

There is a 7 cycle speed up in case c comared to case a.