Lecture 12.01
6809 Assembly Process

CPS310
Computer Organization II
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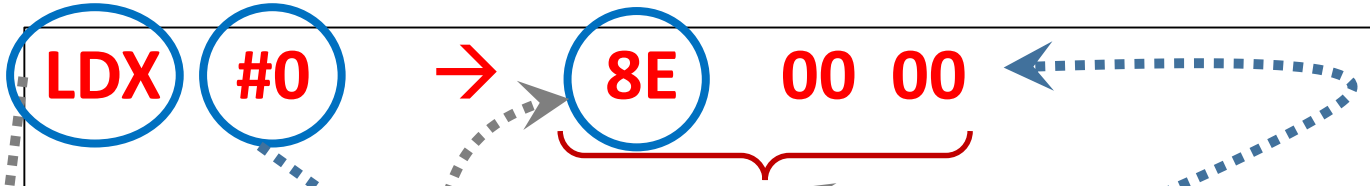
ASSEMBLY PROGRAMS TO MACHINE CODE - EXAMPLE #1

Note: 6809's assembler is not case sensitive

Instruction			Addresses	Opcode
	ORG	$100		
	LDX	#0	100	8E 00 00
MORE:	LDB	,X+	103	E6 80
	STB	$00FF, X	105	E7 88 FF
	CMPX	#$40	108	8C 00 40
	BNE	MORE	10B	26 F6
	END		10D	

LDX #0 in Location (address) $100



Address	Memory Content
$100	8E
	00
	00
$103	

The next instruction will start at address **$103**

FROM C5

Op-Codes for 6809

Instruction		ADDRESSING MODE																				
		Immediate			Direct			Indexed			Extended			Inherent or Register			M <= EA (memory addr.)					
Oper	Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C	
	LDX	8E	3	3	9E	5	2	AE	5+	2+	BE	6	3				X <-- [M : M+1]	1	1	0		

LDB ,X+ in Location $103

POSTBYTE

LDB ,X+ → E6 80

Register field : RR = 00 --> X
01 --> Y
10 --> U
11 --> S

Indexed → requires post-byte

In indexed addressing, the referenced data is specified by a **post-byte**

FROM C1

7	6	5	4	3	2	1	0	Indexed Addressing Mode
1	R	R	0	0	0	0	0	, R +

FROM C3

80	,X+

Post-byte: **1000 0000**

The following instruction in **$105**

FROM C5

Op-Codes for 6809

Instruction Oper	Mnem	Immediate Op	c	b	Direct Op	c	b	Indexed Op	c	b	Extended Op	c	b	Inherent or Register Op	c	b	M <= EA (memory addr.) RTL Description	N	Z	V	C
LDB		C6	2	2	D6	4	2	E6	4+	2+	F6	5	3				B <-- [M]	1	1	0	

STB $00FF, X in location $105

POSTBYTE

STB $00FF, X → E7 88 FF

Register field : RR = 00 --> X
01 --> Y
10 --> U
11 --> S

FROM C1

7	6	5	4	3	2	1	0	Indexed Addressing Mode
1	R	R	i	1	0	0	0	EA = , R + 8-bit offset

FROM C3

Post-byte: 1000 1000

88 nn,X

FROM C5

The next instruction in location $108

Op-Codes for 6809

Instruction Oper	Mnem	Immediate Op	c	b	Direct Op	c	b	Indexed Op	c	b	Extended Op	c	b	Inherent or Register Op	c	b	M <= EA (memory addr.) RTL Description	N	Z	V	C
	STB				D7	4	2	E7	4+	2+	F7	5	3				M <-- [B]	1	1	0	

CMPX #$40 in Location $108

CMPX #$40 → 8C 00 40

FROM C5

Op-Codes for 6809

Instruction		ADDRESSING MODE												Inherent or Register			M <= EA (memory addr.)	See Legend below			
		Immediate			Direct			Indexed			Extended										
Oper	Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C
	CMPX	8C	4	3	9C	6	2	AC	6+	2+	BC	7	3				[X] - [M]	1	1	1	1

The next instruction starts in location **$10B**

BNE MORE in Location $10B

Need to calculate the displacement

BNE MORE → 26 F6

PC at this point refers to the next instruction, $10D

MORE is the address of the 2nd line of code, $103

The displacement is the distance between where PC is and where the lable MORE points to:
(103 – 10D) = -10 →

(+ 10) 0000 1010
(- 10) 1111 0110 → F6

FROM C4

µ6809 Instruction	Mnemonic	e	b	c	Branch test
Branch if not equal to zero	BNE	26	2	3	Z = 0
	LBNE	10 26	4	5+	.

The next instruction is in location **$10D**

ASSEMBLY PROGRAM TO MACHINE CODE CONVERSION

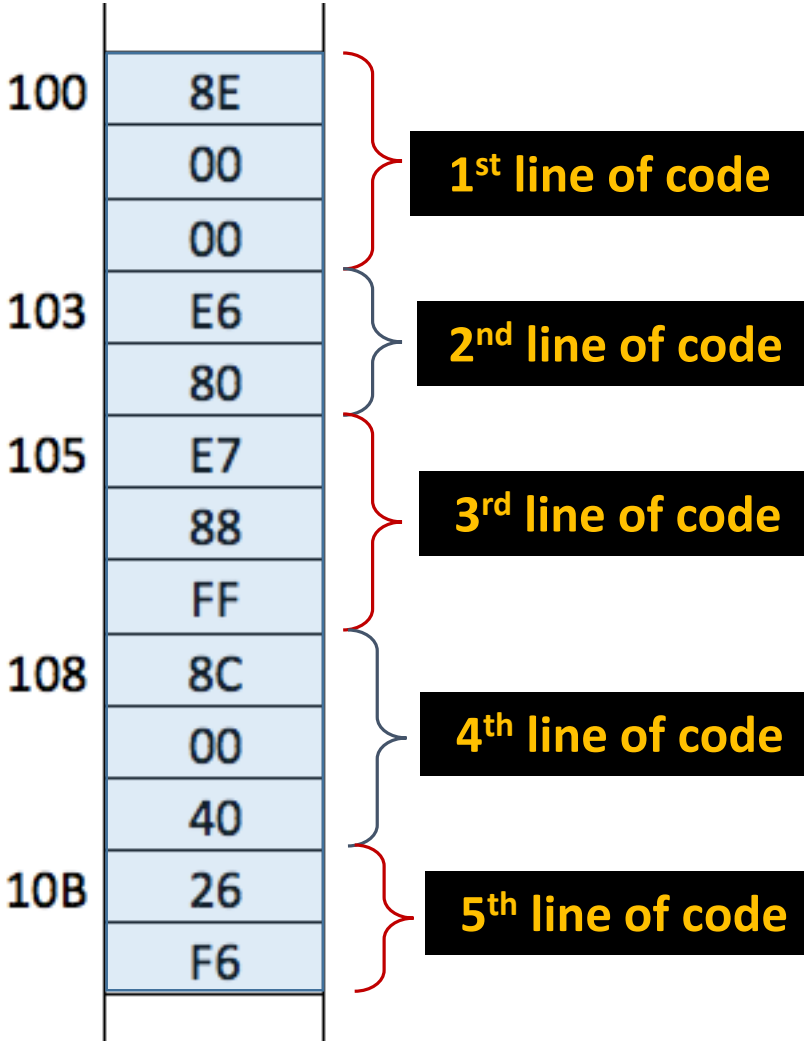
We just finished converting the given assembly program to the machine code:

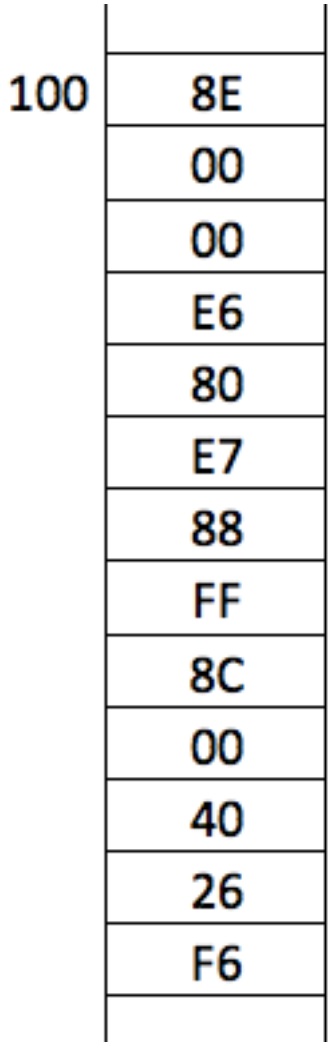
LDX	#0	→	8E	00	00
LDB	,X+	→	E6	80	
STB	$00FF, X	→	E7	88	FF
CMPX	#$40	→	8C	00	40
BNE	MORE	→	26	F6	

How does the memory map look like?

Memory Map for the given Example

Your program inside the memory after conversion to machine code





Actual look of the memory map where the instructions are not clearly identified

Second Example

Instructions		
	ORG	$100
	CLRB	
	LDU	#$68
FRED:	PSHU	B
	LEAU	-1,U
	CMPU	#$5F
	BNE	FRED

CLRB in Location 100

CLRB → 5F

The next instruction is in location **101**

FROM C5

Op-Codes for 6809		ADDRESSING MODE												Inherent or					See Legend below		
Instruction		Immediate			Direct			Indexed			Extended			Register			M <= EA (memory addr.)				
Oper	Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C
	CLRB													5F	2	1	B <-- 0	0	1	0	0

LDU #$68 in Location $101

LDU #$68 → CE 0068

FROM C5

Op-Codes for 6809

Instruction		ADDRESSING MODE																	
		Immediate			Direct			Indexed			Extended			Inherent or Register			M <= EA (memory addr.)				
Oper	Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C
	LDU	CE	3	3	DE	5	2	EE	5+	2+	FE	6	3				U <-- [M : M+1]	1	1	0	

The next instruction is in location **$104**

Post-Byte for Push and Pull

- The post-byte for push and pull are straight forward

- For example, the post-byte for pulling or pushing register B on a stack (U or S) would be 00000100_2 or 04_{16}. Every bit is cleared except bit-1

Bit-7 (MSB)	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
PC	S/U	Y	X	DP	B	A	CC

PSHU B in Location $104

PSHU B → 36 04

The next instruction is in location **$106**

Post-byte as explained in the previous slide is **4**

FROM C5

Op-Codes for 6809

Instruction		ADDRESSING MODE												Inherent or			M <= EA (memory addr.)					
		Immediate			Direct			Indexed			Extended			Register								
Oper	Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C
	PSHU	36	5+	2													push to U stack					

LEAU -1,U in Location $106

LEAU -1,U → 33 5F

Register field : RR = 00 --> X
01 --> Y
10 --> U
11 --> S

The next instruction is in location **$108**

Post-byte: **5F**

7	6	5	4	3	2	1	0	Indexed Addressing Mode
0	R	R	d	d	d	d	d	EA = , R + 5 bit offset

Post-byte: 0101 1111

5F -1,U

FROM C5

Op-Codes for 6809		ADDRESSING MODE				Inherent or									
Instruction		Immediate			Direct			Indexed			Extended			Register			M <= EA (memory addr.)					
Oper	Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C
	LEAU							33	4+	2+							U <– EA				

CMPU #$5F in Location $108

CMPU #$5F → 1183 005F

The next instruction is in location **$10C**

FROM C5

Op-Codes for 6809	ADDRESSING MODE												Inherent or				M <= EA (memory addr.)	See Legend below			
Instruction	Immediate			Direct			Indexed			Extended			Register								
Oper Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C
CMPU	1183	5	4	1193	7	3	11A3	7+	3+	11B3	8	4				[U] - [M]	1	1	1	1

BNE FRED in Location $10C

BNE FRED → 26 F6

The next instruction is in location **$10E**

Need to calculate the displacement

PC in 6809 always refer to the next instruction, ie, **$10E**

FRED is **$104**

The displacement is (104 – 10E) = -10 → 0000 1010

1111 0110 → F6

FROM C4

µ6809 Instruction	Mnemonic	e	b	c	Branch test
Branch if not equal to zero	BNE	26	2	3	Z = 0
	LBNE	10 26	4	5+	.

Second Example & memory map

Instructions		
	ORG	$100
	CLRB	
	LDU	#$68
FRED:	PSHU	B
	LEAU	-1,U
	CMPU	#$5F
	BNE	FRED

Addresses	Opcode
100	5F
101	CE 0068
104	36 04
106	33 5F
108	1183 005F
10C	26 F6
10E	

3rd Example

```
        ORG     $200
LIST1   FCB     1,2,3,4,5
        ORG     $300
LIST2   FCB     2,3,4,5,6
        ORG     $400
LIST3   RMB     5
        ORG     $100
        LDB     #5
        LDX     #LIST1
        LDY     #LIST3
LOOP    LDA     ,X
        ADDA    $100,X
        LEAX    1,X
        STA     ,Y+
        DECB
        BNE     LOOP
        END
```

3rd Example

	ORG	$200				
LIST1	FCB	1,2,3,4,5				
	ORG	$300				
LIST2	FCB	2,3,4,5,6				
	ORG	$400				
LIST3	RMB	5				
	ORG	$100				
	LDB	#5		$100	C6	05
	LDX	#LIST1		$102	8E	0200
	LDY	#LIST3		$105	108E	0400
LOOP	LDA	,X	❶	$109	A6	84
	ADDA	$100,X	❷	$10B	AB	89 0100
	LEAX	1,X	❸	$10F	30	01
	STA	,Y+	❹	$111	A7	A0
	DECB			$113	5A	
	BNE	LOOP	❺	$114	26	F3
	END					

Machine codes

LDB #5

FROM C5

Instruction		Immediate			Direct			Indexed			Extended			Register			M <= EA (memory addr.)					
Oper	Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C
	LDB	C6	2	2	D6	4	2	E6	4+	2+	F6	5	3				B <-- [M]	1	1	0	

$100 C6 05

Machine codes

LDX #LIST1

Instruction		Immediate			Direct			Indexed			Extended			Register			M <= EA (memory addr.)					
Oper	Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C	
	LDX	8E	3	3	9E	5	2	AE	5+	2+	BE	6	3				X <-- [M : M+1]	1	1	0		

FROM C5

$102 8E 0200

Machine codes

LDY #LIST3

Instruction Oper Mnem	Immediate Op c b	Direct Op c b	Indexed Op c b	Extended Op c b	Register Op c b	M <= EA (memory addr.) RTL Description	N	Z	V	C
LDY	108E 4 4	109E 6 3	10AE 6+ 3+	10BE 7 4		Y <-- [M : M+1]	1	1	0	

FROM C5

$105 108E 0400

Machine codes ❶

LDA ,X

Instruction Oper	Mnem	Immediate Op	c	b	Direct Op	c	b	Indexed Op	c	b	Extended Op	c	b	Register Op	c	b	M <= EA (memory addr.) RTL Description	N	Z	V	C
	LDA	86	2	2	96	4	2	A6	4+	2+	B6	5	3				A <-- [M]	1	1	0	

FROM C5

Register field : RR = 00 --> X
01 --> Y
10 --> U
11 --> S

Post-byte 84 ,X

7	6	5	4	3	2	1	0	Indexed Addressing Mode
1	R	R	i	0	1	0	0	EA = , R + 0 offset

Post-byte: 1000 0100

$109 A6 84

Machine codes ❷

ADDA $100,X

Op-Codes for 6809		ADDRESSING MODE																Inherent or			See Legend below				
Instruction		Immediate			Direct			Indexed			Extended			Register			M <= EA (memory addr.)							
Oper	Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C			
	ADDA	8B	2	2	9B	4	2	AB	4+	2+	BB	5	3				A <-- [A] + [M]		1	1	1			

FROM C5

mmnn,
89 X

Register field : RR = 00 --> X
01 --> Y
10 --> U
11 --> S

7	6	5	4	3	2	1	0	Indexed Addressing Mode
1	R	R	i	1	0	0	1	EA = , R + 16-bit offset

Post-byte: 1000 1001

$10B AB 89 0100

Machine codes ❸

LEAX 1,X

Op-Codes for 6809

Instruction		ADDRESSING MODE										Inherent or						M <= EA (memory addr.)				
Oper	Mnem	Immediate			Direct			Indexed			Extended			Register			RTL Description	N	Z	V	C
	LEAX							30	4+	2+							X <-- EA		1			

FROM C5

Post-byte 01 1.X

Register field : RR = 00 --> X
01 --> Y
10 --> U
11 --> S

7	6	5	4	3	2	1	0	Indexed Addressing Mode
0	R	R	d	d	d	d	d	EA = , R + 5 bit offset

Post-byte: 0000 0001

$10F 30 01

Machine codes ❹

STA ,Y+

Op-Codes for 6809	ADDRESSING MODE																Inherent or					
Instruction	Immediate			Direct			Indexed			Extended			Register			M <= EA (memory addr.)					
Oper Mnem	Op	c	b	Op	c	b	Op	c	b	Op	c	b	Op	c	b	RTL Description	N	Z	V	C	
STA				97	4	2	A7	4+	2+	B7	5	3				M <-- [A]	1	1	0		

FROM C5

Post-byte

A0 ,Y+

Register field : RR = 00 --> X
01 --> Y
10 --> U
11 --> S

7	6	5	4	3	2	1	0	Indexed Addressing Mode
1	R	R	0	0	0	0	0	, R +

Post-byte: 1010 0000

$111 A7 A0

Machine codes

DECB

Op-Codes for 6809		ADDRESSING MODE				Inherent or				See Legend below				
Instruction	Immediate	Direct	Indexed	Extended	Register	M <= EA (memory addr.)								
Oper Mnem	Op c b	Op c b	Op c b	Op c b	Op c b	RTL Description				N	Z	V	C	
DECB					5A 2 1	B <-- [B] - 1				1	1	1		

FROM C5

$113 5A

Machine codes ❺

BNE LOOP

µ6809 Instruction	Mnemonic	Opcode	b	c	Branch test
Branch if not equal to zero	BNE	26	2	3	Z = 0

FROM C4

Displacement: **PC is $116, LOOP is $109**

$109 - $116 = -$13

0000 1101

1111 0011

$114 26 F3