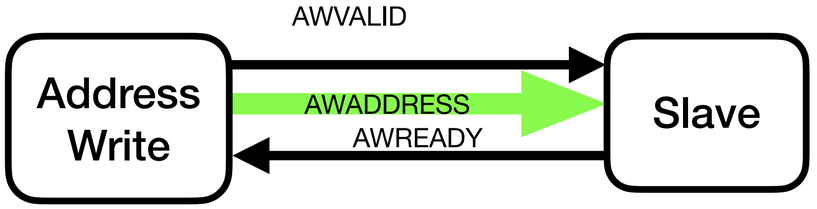
AXI4 vs. AXI4 Lite

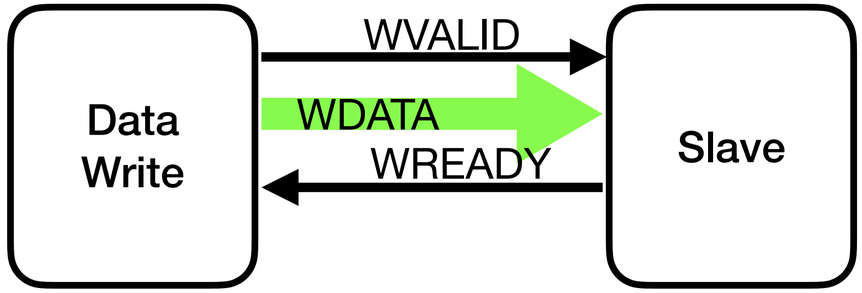
AXI4	AXI4 Lite
Burst Lengths up to 256 words	All transactions are of burst length 1
Access to a portion of the bus width in 2**n increments	All data accesses use the full width of the data bus
Up to 128 bytes bus width	AXI4-Lite supports a data bus width of 32-bit or 64-bit
Can carry ID, QOS, User info	Limited transfer information



AXI4 Address Write Bus Signals

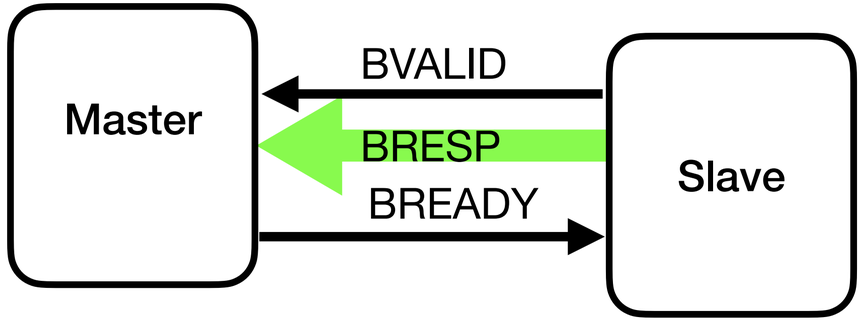
Signal Name	Source	Description
AWID	Master	Transaction ID , Allows for non-ordered transactions
AWVALID	Master	Write **Address from Master is valid.**
AWREADY	Slave	**Slave is ready to accept write Address from Master**
AWADDRESS	Master	**The write address. This is the base address for the burst.**
AWSIZE	Master	Bus subset in bytes, 2**AWSIZE, 0 = 1 byte , 7=128 bytes
AWBURST	Master	Burst type, 0 = fixed , 1 = Increment, 2 = Wrap, 3 = reserved
AWLEN	Master	Burst Length , 0=1 , up to 255=256
AWLOCK	Master	Atomic Access , 0 = Normal access , 1 = Exclusive Access
AWCACHE	Master	Memory type, bufferable, non-bufferable, cacheable, non-cacheable, etc. Refer to the AXI4 Spec
AWQOS	Master	User defined QOS value, usually an indication of priority
AWUSER	Master	User defined value, label for transaction
AWPROT	Master	**Access Protections. 3 Bits. Bit 0 = 1-privaeledged 0-privaeledged , Bit 1 = 1 Secure 0 Nonsecure, Bit 2 = 1 Instruction 0 Data**

AXI4 Data Write Bus Signals



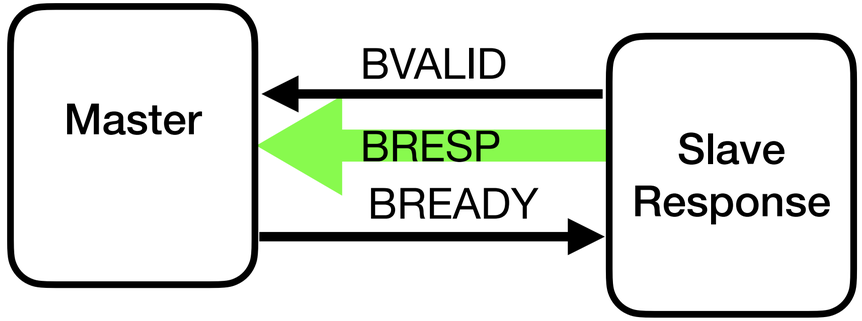
Signal Name	Source	Description
WVALID	Master	Write Data from Master is valid.
WREADY	Slave	Slave is ready to accept write Data from Master
WDATA	Master	The write Data. This is the data bus up to 128 bytes
WSTROBE	Master	Identifies which bytes of the data are valid, one bit for each byte
WLAST	Master	Last Word of the transaction
WID	Master	Transaction ID

AXI4 Write Response Bus Signals



Signal Name	Source	Description
BID	Slave	Transaction ID
BVALID	Slave	Write Response is Valid from Slave
BREADY	Master	Master is ready to accept response
BRESP	Slave	Response information from Slave

AXI4 Write Responses

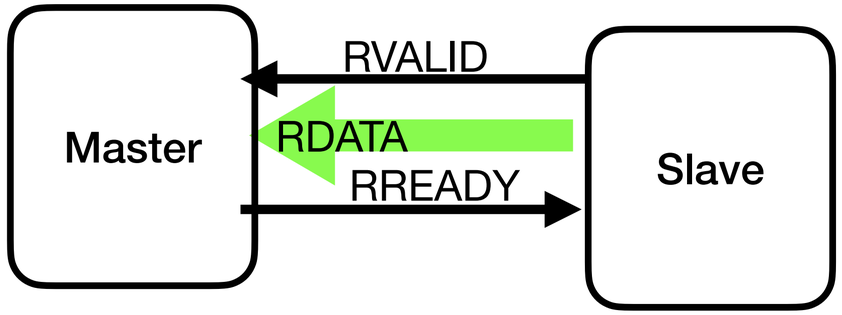


Response	Resp[1:0]	Description
OKAY	00	The write operation was a success
EXOKAY	01	Exclusive Access is OK.
SLVERR	10	The Slave reports an error , but address is in range
DECERR	11	The Address was not in range of the slave

AXI4 Address Read Bus Signals

Signal Name	Source	Description
ARVALID	Master	Read Address from Master is valid.
ARREADY	Slave	Slave is ready to accept Read Address from Master
ARADDRESS	Master	The Read address. This is the base address of the read burst operation.
ARLEN	Master	Burst Length , 0=1 , up to 255=256
ARSIZE	Master	Bus subset in bytes, 2**AWSIZE, 0 = 1 byte , 7=128 bytes
ARBURST	Master	Burst type, 0 = fixed , 1 = Increment, 2 = Wrap, 3 = reserved
ARLOCK	Master	Atomic Access , 0 = Normal access , 1 = Exclusive Access
ARCACHE	Master	Memory type, bufferable, non-bufferable, cacheable, non-cacheable, etc. Refer to the AXI4 Spec
ARPROT	Master	**Access Protections. 3 Bits. Bit 0 = 1-privaeledged 0-privaeledged , Bit 1 = 1 Secure 0 Nonsecure, Bit 2 = 1 Instruction 0 Data**
ARQOS	Master	User defined QOS value, usually an indication of priority
ARUSER	Master	User defined value, label for transaction
ARID	Master	Transaction ID , Allows for non-ordered transactions

AXI4 Read Data Bus Signals



Signal Name	Source	Description
RVALID	Slave	Read Data from Slave is Valid
RREADY	Master	Master is Ready to Accept Read Data
RDATA	Slave	Read Data from Slave
RRESP	Slave	Read response from Slave
RID	Slave	Transaction ID
RLAST	Slave	Last word of the burst

AXI4 Read Responses

Response	Resp[1:0]	Description
OKAY	00	The read operation was a success
EXOKAY	01	Exclusive Access is OK.
SLVERR	10	The Slave reports an error , but address is in range
DECERR	11	The Address was not in range of the slave