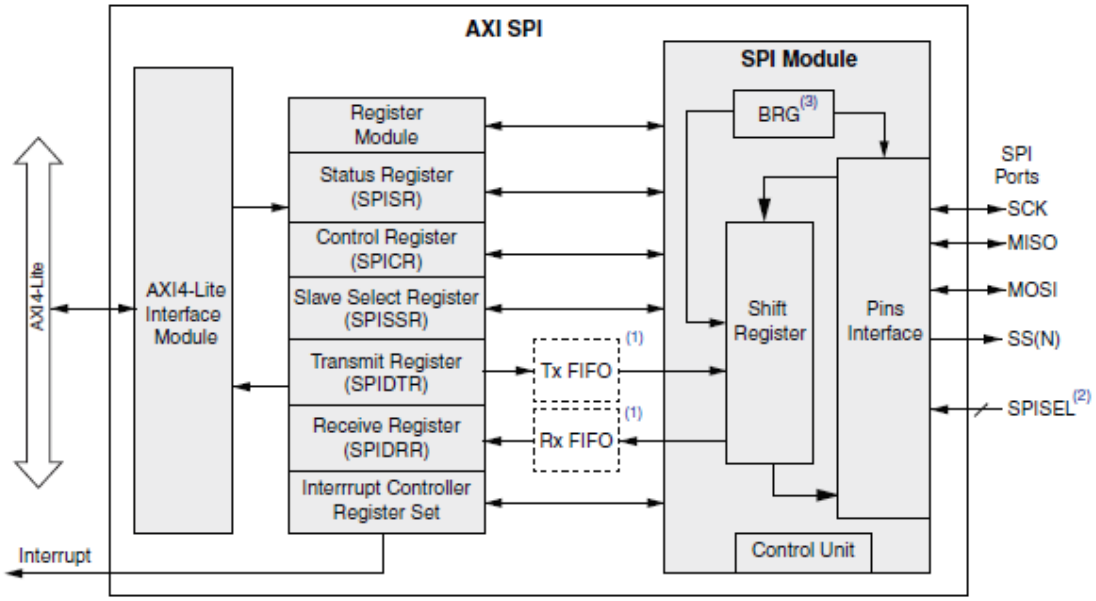
LogiCORE IP AXI Serial Peripheral Interface (AXI SPI)

1. Design Description

- The AXI Serial Peripheral Interface (SPI) connects to the Advanced eXtensible Interface (AXI4).
- This core provides a serial interface to SPI devices such as SPI Electrically Erasable Programmable Read-Only Memories (EEPROMs) and SPI serial flash devices.



i. **AXI4-Lite IP IPIF Interface (IPIF):** The AXI4-Lite IP Interface (IPIF) provides the interface to the AXI4-Lite to IP Interconnect (IPIC). The read and write transactions done at AXI4-Lite interface.

ii. **SPI Register Module:** The SPI Register Module includes all memory mapped registers.

iii. **Interrupt Controller Register set Module:** The Interrupt Controller Register set Module consists of interrupt related registers.

iv. **SPI Module:** The SPI Module consists of a shift register, a parameterized baud rate generator (BRG) and a control unit.

v. **Optional FIFOs:** The Tx FIFO and Rx FIFO are implemented on both transmit and receive paths when enabled by the parameter C_FIFO_EXIST. The width of Tx FIFO and Rx FIFO are the same and depend on the generic C_NUM_TRANSFER_BITS. When the FIFOs are enabled, their depth is fixed at 16.

- AXI4-Lite interface is based on the AXI4 specification
- Connects as a 32-bit AXI4-Lite slave
- Supports four signal interface SPI:
    - Master Out Slave In (MOSI)
    - Master In Slave Out (MISO)
    - Serial Clock (SC)
    - SS

- Slave select (SS) bit for each slave on the SPI bus
- Full-duplex operation
- Master and slave SPI modes
- Programmable clock phase and polarity
- Back-to-back transactions
- Automatic or manual slave select modes
- MSB/LSB first transactions
- Transfer length of 8-bits, 16-bits or 32-bits
- Local loopback capability for testing
- Multiple master and multiple slave environment
- Optional 16 element deep (an element is a byte, a half-word or a word) Transmit and Receive First In First Out (FIFO)

Manual Slave Select mode:

- This mode allows the user to manually control the slave select line using the data written to the slave select register.
- This allows transfers of an arbitrary number of elements without toggling the slave select line between elements.
- However, the user must toggle the slave select line before starting a new transfer.

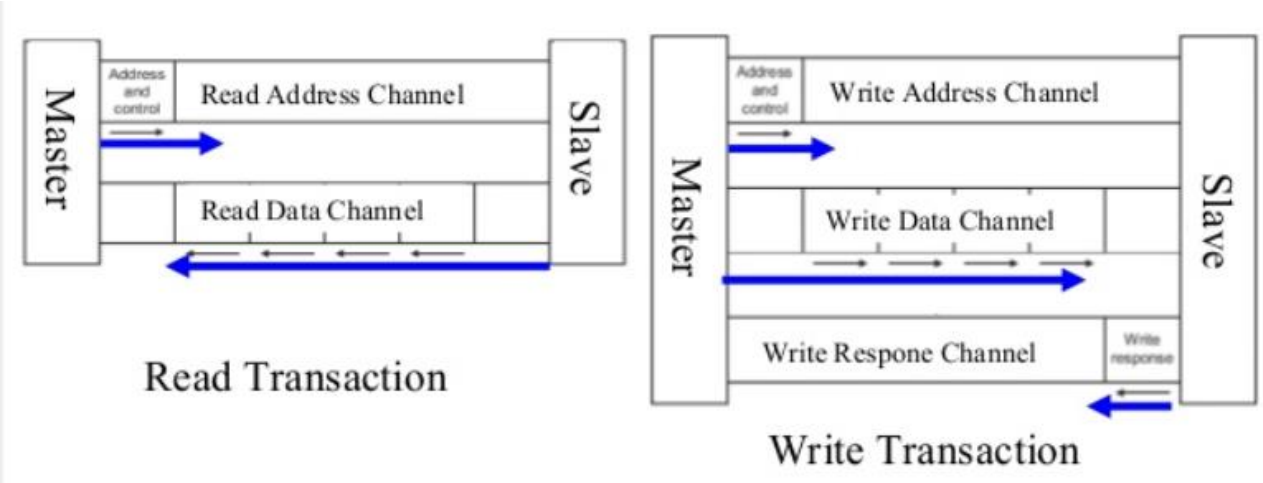
Automatic Slave Select Mode:

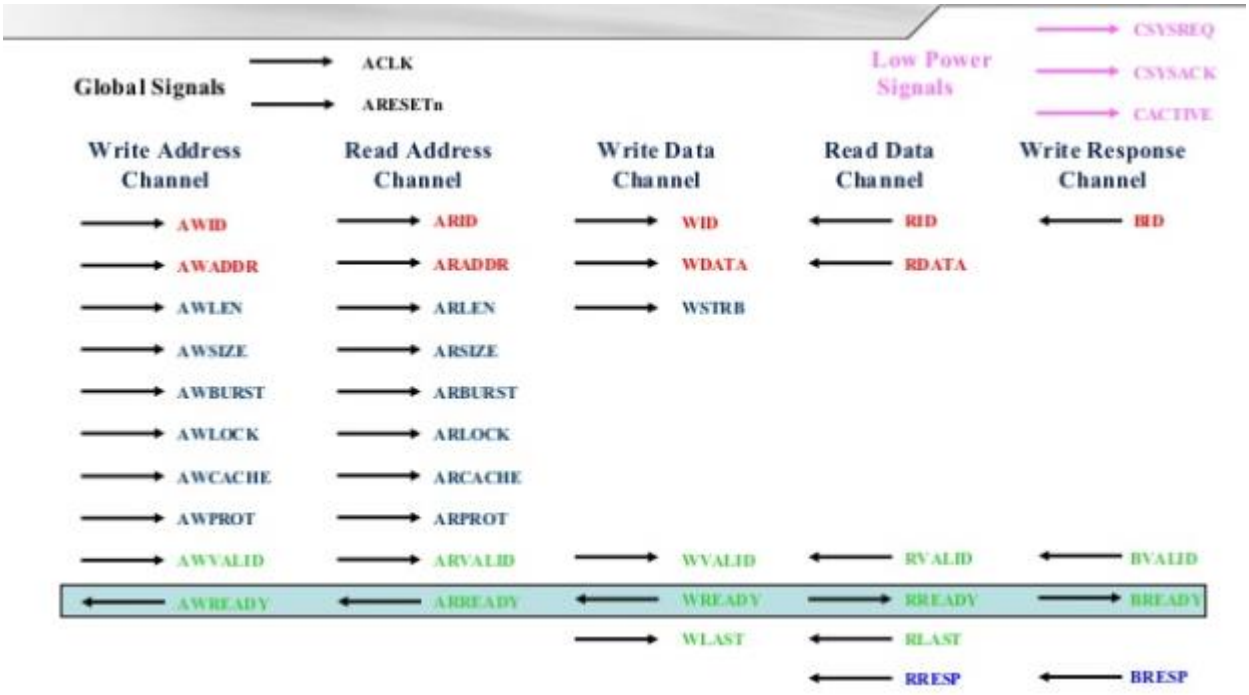
In this mode the slave select line is toggled automatically after each element transfer.

- When the core is configured as a slave and if inadvertently its slave select line (SPISEL) goes high (inactive state) in between the data element transfer, then the current transfer is aborted.
- Again if the slave select line goes low then the aborted data element is transmitted again.
- The number of slaves is limited to 32 by the size of the Slave Select Register
- The core supports only 32-bit word access to all SPI and INTR register modules.

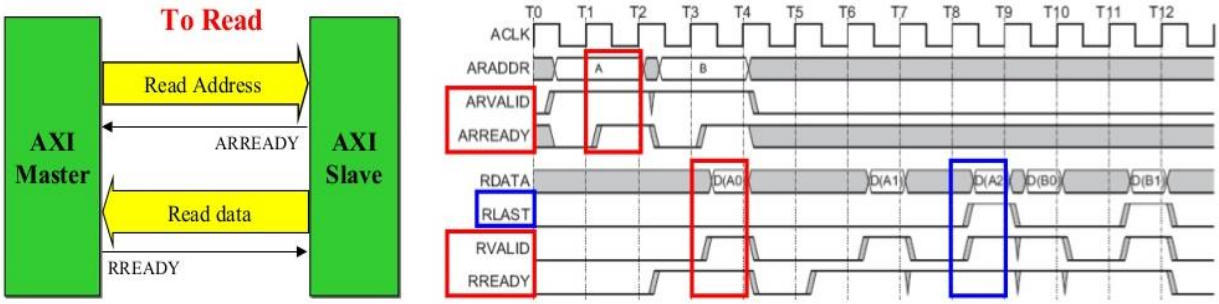
2. AXI Interface

Channels :

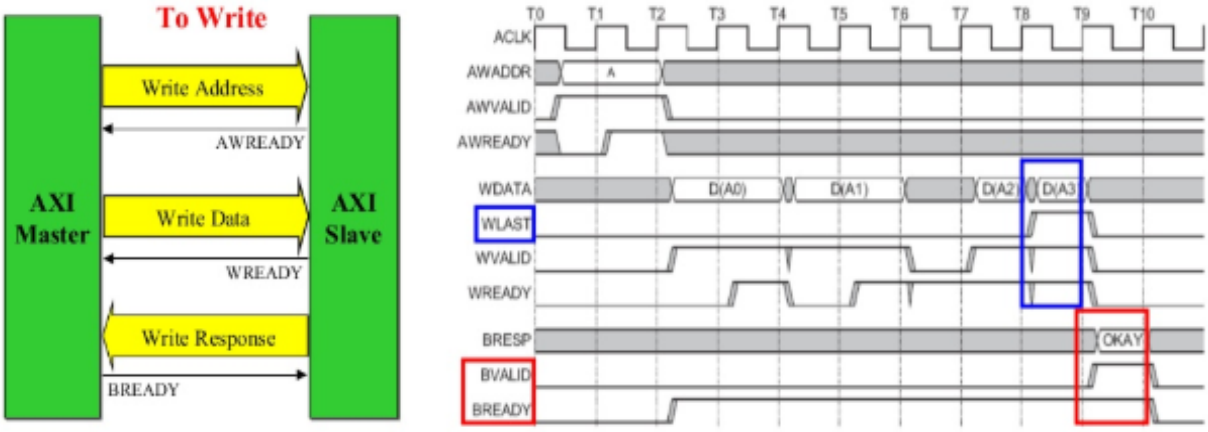




Read Transaction :

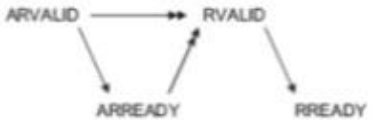


Write Transaction :



Valid and Ready Handshake during transactons :

Read



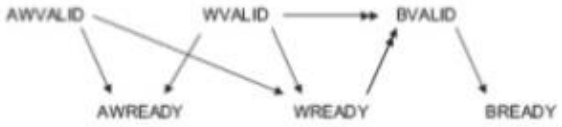
Write data can appear before Write address

Write data appear in the same cycle as the address

Read data always come after Read address

Write response always come after write data

Write



Signal Name	Interface	I/O	Initial State	Description
AXI Global System Signals				
S_AXI_ACLK	AXI	I	-	AXI Clock
S_AXI_ARESETN	AXI	I	-	AXI Reset, active Low
AXI Write Address Channel Signals				
S_AXI_AWADDR[(C_S_AXI_ ADDR_WIDTH - 1) : 0]	AXI	I	-	AXI Write address. The write address bus gives the address of the write transaction.
S_AXI_AWVALID	AXI	I	-	Write address valid. This signal indicates that a valid write address and control information are available.
S_AXI_AWREADY	AXI	O	0	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
AXI Write Channel Signals				
S_AXI_WDATA[(C_S_AXI_ DATA_WIDTH - 1) : 0]	AXI	I	-	Write data
S_AXI_WSTB[((C_S_AXI_ DATA_WIDTH/8) - 1) : 0]	AXI	I	-	Write strobes. This signal indicates which byte lanes to update in memory.
S_AXI_WVALID	AXI	I	-	Write valid. This signal indicates that valid write data and strobes are available.
S_AXI_WREADY	AXI	O	0	Write ready. This signal indicates that the slave can accept the write data.
AXI Write Response Channel Signals				
S_AXI_BRESP[1 : 0]	AXI	O	0	Write response. This signal indicates the status of the write transaction 00 - OKAY (normal response) 10 - SLVERR (error response) 11 - DECERR (not issued by core)

Signal Name	Interface	I/O	Initial State	Description
S_AXI_BVALID	AXI	O	0	Write response valid. This signal indicates that a valid write response is available.
S_AXI_BREADY	AXI	I	-	Response ready. This signal indicates that the master can accept the response information.
AXI Read Address Channel Signals				
S_AXI_ARADDR[(C_S_AXI_ ADDR_WIDTH - 1) : 0]	AXI	I	-	Read address. The read address bus gives the address of a read transaction.
S_AXI_ARVALID	AXI	I	-	Read address valid. When HIGH, this signal indicates that the read address and control information is valid and remains stable until the address acknowledgement signal, S_AXI_ARREADY, is high.
S_AXI_ARREADY	AXI	O	1	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
AXI Read Data Channel Signals				
S_AXI_RDATA[(C_S_AXI_ DATA_WIDTH - 1) : 0]	AXI	O	0	Read data
S_AXI_RRESP[1 : 0]	AXI	O	0	Read response. This signal indicates the status of the read transfer. 00 - OKAY (normal response) 10 - SLVERR (error condition) 11 - DECERR (not issued by core)
S_AXI_RVALID	AXI	O	0	Read valid. This signal indicates that the required read data is available and the read transfer can complete.
S_AXI_RREADY	AXI	I	-	Read ready. This signal indicates that the master can accept the read data and response information.

3. SPI Interface

SPI Interface Signals				
IP2INTC_Irpt	SPI	O	0	Interrupt control signal from SPI
SCK_I	SPI	I	-	SPI bus clock input
SCK_O	SPI	O	0	SPI bus clock output
SCK_T	SPI	O	1	3-state enable for SPI bus clock.Active Low
MOSI_I	SPI	I	-	Master output slave input
MOSI_O	SPI	O	1	Master output slave input
MOSI_T	SPI	O	1	3-state enable master output slave input. Active Low.
MISO_I	SPI	I	-	Master input slave output
MISO_O	SPI	O	1	Master input slave output
MISO_T	SPI	O	1	3-state enable master input slave output. Active Low.
SPISEL(1)	SPI	I	1	Local SPI slave select active Low input Must be set to 1 in idle state
SS_I[(C_NUM_SS_BITS - 1):0]	SPI	I	-	Input one-hot encoded. This signal is a dummy signal and is used in the design as chip-select input.
SS_O[(C_NUM_SS_BITS - 1):0]	SPI	O	1	Output one-hot encoded, active Low slave select vector of length n.
SS_T	SPI	O	1	3-state enable for slave select. Active Low.

4. Registers

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
Core Grouping				
C_BASEADDR + 40	SRR	Write	N/A	Software Reset Register
C_BASEADDR + 60	SPICR	R/W	0x180	SPI Control Register
C_BASEADDR + 64	SPISR	Read	0x25	SPI Status Register
C_BASEADDR + 68	SPIDTR	Write	0x0	SPI Data Transmit Register A single register or a FIFO
C_BASEADDR + 6C	SPIDRR	Read	NA	SPI Data Receive Register A single register or a FIFO
C_BASEADDR + 70	SPISSR	R/W	No slave is selected	SPI Slave Select Register
C_BASEADDR + 74	SPI Transmit FIFO Occupancy Register (1)	Read	0x0	Transmit FIFO Occupancy Register
C_BASEADDR + 78	SPI Receive FIFO Occupancy Register(1)	Read	0x0	Receive FIFO Occupancy Register
Interrupt Controller Grouping				
C_BASEADDR + 1C	DGIER	R/W	0x0	Device Global Interrupt Enable Register
Base Address + Offset (hex)	**Register Name**	**Access Type**	**Default Value (hex)**	**Description**
C_BASEADDR + 20	IPISR	R/TOW(2)	0x0	IP Interrupt Status Register
C_BASEADDR + 28	IPIER	R/W	0x0	IP Interrupt Enable Register

1. Exists only when C_FIFO_EXIST = 1.
2. TOW = Toggle On Write. Writing a 1 to a bit position within the register causes the corresponding bit position in the register to toggle.