Lab 1 - Seven Segment Display
Section 01 ECE 491
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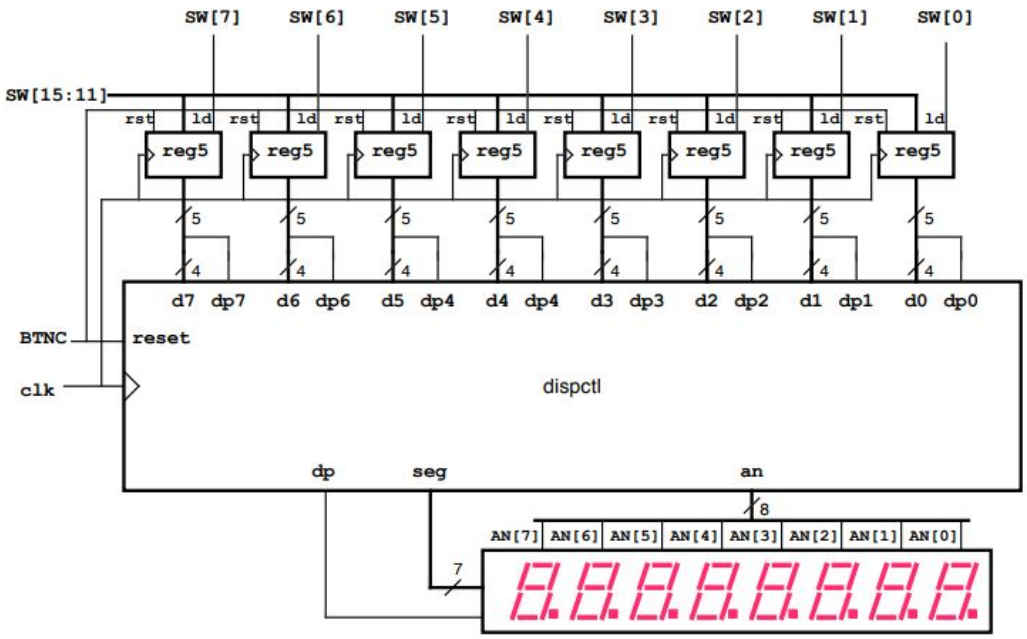
Design Approach:

For our design approach, we followed the suggested design approach explained by the lab handout. In this approach, we began by instantiating a clock divider to send an enable pulse once every 1000 clock pulses (decided by the DIVFREQ parameter of the module). This enable signal that comes out of the clock divider goes into a 3-bit counter that increments on the enable pulse, at a specific rate. The output of the 3-bit counter is then connected to one 8-1 multiplexer that selects one of the eight digits that goes into a seven segment decoder, one 8-1 multiplexer that selects one of the eight decimal points, and a 3-8 decoder which generates the anode enable for the specific selected digit (which are active low).

Note: Hexadecimal letter symbols are not all in the same case. This was a design decision to make it easier to read the displayed results. This is because all the symbols are unique. (e.g. conflict between ‘8’ and ‘B’ , ‘0’ and ‘D’ etc.)

The figure below (taken from the ECE 491 Lab01 handout) displays the top level design for the system.



Requirements CheckList

Description	**Test Method**	**Detailed Results**
1. Module Interface	Code Inspection	Code is neat, orderly and follows the Coding Guidelines
2. Module function: accepts four 4-bit inputs and four 1-bit “decimal point” inputs and displays 4 7-segment outputs without noticeable flicker.	Demonstration in hardware using Nexys 4 DDR board: Proper display of all 8 digits and 16 digit symbols. Proper display of 4 decimal points Free of noticeable flicker	-All 8 digits are able to display all 16 hex numbers. -All decimal points are displayed and can be configured on/off individually or as groups -No Flicker noticed by instructor or by students
3. Uses Nexys4 board 100Mhz clock; all flip-flop clock inputs tied directly to this signal	- Check every flip-flop and verify that it is driven by the board 100Mhz clock	PASS
4. Contains no latches	Inspection of Synthesis Report	The synthesis report had no warnings relative to latching
5. Test circuit – show test that test circuit functions properly to exercises circuit.	-Test if all 16 digits display correctly on all 8 segments -Test if the decimal point displays correctly on all 8 segments -Test that if any switch is on and a hex digit is changed, all the corresponding segment displays the correct digit -Test that the reset button sets all digits to 0	Circuit passed all of the mentioned tests
In submitting this checklist as part of our report, I/We certify that the tests described above were conducted and that the results of these tests are accurately described and represented. I/We understand that any misrepresentation of the tests or the results constitutes a violation of the College policy on academic dishonesty.		
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