SSD1675

Product Preview

160 Source x 296 Gate Red/Black/White
Active Matrix EPD Display Driver with Controller

This document contains information on a product under development. Solomon Systech reserves the right to change or discontinue this product without notice.

Appendix: IC Revision history of SSD1675 Specification

Version	Change Items	Effective Date
0.10	1st Release	04-May-16

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TABLES

FIGURES

1 General Description

The SSD1675 is an Active Matrix EPD Display Driver with Controller which can support Red/Black/White.

It consists of 160 source outputs, 296 gate outputs, 1 VCOM and 1 VBD for border that can support a maximum display resolution 160x296. In addition, the SSD1675 has a cascade mode that can support higher display resolution.

The SSD1675 embeds booster, regulators and oscillator. Data/Commands are sent from general MCU through the hardware selectable Serial peripheral or I2C interface.

2 Features

- Design for dot matrix type active matrix EPD display
- Support Red/Black/White mono color
- Resolution: 160 source outputs; 296 gate outputs; 1 VCOM; 1VBD for border
- Power supply:
  - VCI: 2.2 to 3.7V
  - VDDIO: Connect to VCI
  - VDD: 1.8V, regulate from VCI supply
- On chip display RAM
  - Mono B/W: 160x296 bits
  - Mono Red: 160x296 bits
- On-chip booster and regulator for generating VCOM, Gate and Source driving voltage
- Gate driving output voltage:
  - 2 levels output (VGH, VGL)
  - Max 42Vp-p
  - VGH: 10V to 21V; VGL: -VGH
  - Voltage adjustment step: 500mV
- Source / VBD driving output voltage:
  - 4 levels output (VSH1, VSS, VSL, and VSH2)
    - VSH1/VSH2: 2.4V to 18V (Voltage step: 100mV for 2.4V to 8.8V, 200mV for 8.8V to 18V.)
    - VSL: -9V to -18V (Voltage step: 500mV)
- VCOM output voltage

DCVCOM	ACVCOM
-3V to -0.2V in 100mV resolution	• 3 levels output ➢ VSH1+DCVCOM ➢ DCVCOM ➢ VSL+DCVCOM

- Built in VCOM sensing
- On-chip oscillator
- Programmable output waveform for different types of EPD display:
  - 28 phases (4 phases/group, 7 groups with repeat function)
  - 1 to 256 times for repeat count
  - Max. 255 frame/phase
- On-chip OTP can store LUT (max. 25 sets), including (LUT, gate/source voltage, frame rate and Temperature Range), VCOM value and waveform version ID
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Read OTP function
- Auto write RAM command for regular pattern
- I2C Single Master Interface to read external temperature sensor reading.
- Cascade mode to support higher display resolution.
- MCU interface: Serial peripheral and I2C interface available
- Maximum SPI write speed 20MHz
- Available in COG package

3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SSD1675Z	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 12um

4 Block Diagram

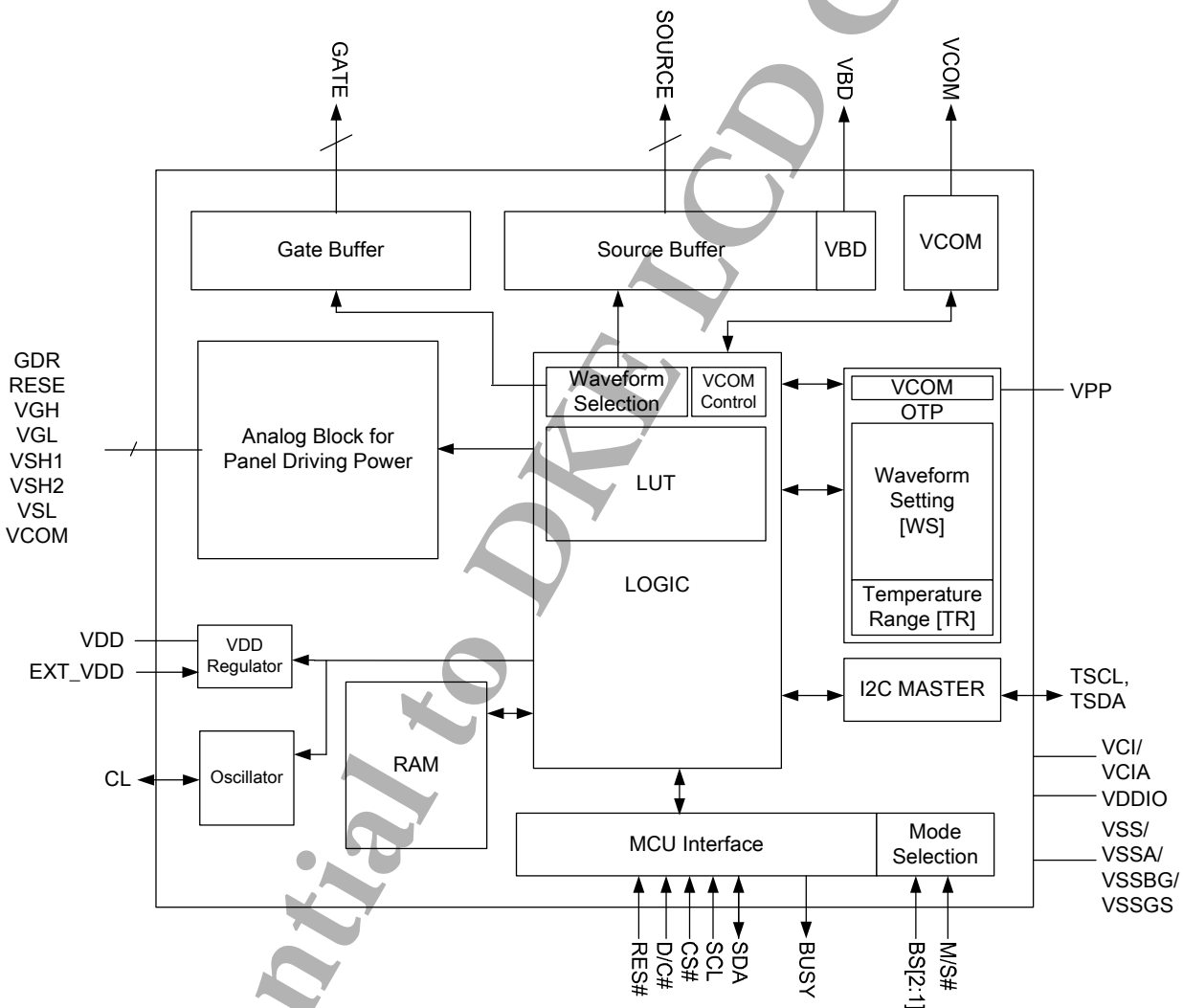


Figure 4-1 : SSD1675 Block Diagram

5 PIN DESCRIPTION

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to V_{SS}, Pull H = connect to V_{DDIO}

Pin name	Type	Connect to	Function	Description	When not in use
Input power					
VCI	P	Power Supply	Power Supply	Power input pin for the chip.	-
VCIA	P	Power Supply	Power Supply	Power input pin for the chip. - Connect to VCI in the application circuit.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the Interface. - Connect to VCI in the application circuit.	-
VDD	P	Capacitor	Regulator output	Core logic power pin VDD can be regulated internally from VCI. - For the single chip application, a capacitor should be connected between VDD and VSS under all circumstances. - For the cascade mode application, a capacitor should be connected between VDD and VSS in the master chip under all circumstances. For the slave chip, the capacitor is not necessary as VDD will be supplied from the cascade master chip externally.	-
EXTVDD	I	VDDIO/ VSS	Regulator bypass	This pin is VDD regulator bypass pin. For the single chip application, EXTVDD should be connected to VSS in the application circuit. - For the cascade mode application, EXTVDD of the master chip should be connected to VSS while EXTVDD of the slave chip should be connected to VDDIO in the application circuit.	-
VSS	P	VSS	GND	Ground (Digital).	-
VSSA	P	VSS	GND	Ground (Analog) - Connect to VSS in the application circuit.	-
VSSBG	P	VSS	GND	Ground (Reference) pin. - Connect to VSS in the application circuit.	-
VSSGS	P	VSS	GND	Ground (Output) pin. - Connect to VSS in the application circuit.	-
VPP	P	Power Supply	OTP power	Power Supply for OTP Programming.	Open
Digital I/O					
SCL	I	MPU	Data Bus	Serial clock pin for interface: Refer to Session 6.1 - MCU Interface.	-
SDA	I/O	MPU	Data Bus	Serial data pin for interface: Refer to Session 6.1 - MCU Interface.	
CS#	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU. Refer to Session 6.1 - MCU Interface.	VDDIO or VSS
D/C#	I	MPU	Logic Control	This pin is Data/Command control pin connecting to the MCU. Refer to Session 6.1- MCU Interface.	VDDIO or VSS

<table>
<tr><th>Pin name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>RES#</td><td>I</td><td>MPU</td><td>System Reset</td><td>This pin is reset signal input.
Active Low.</td><td>-</td></tr>
<tr><td>BUSY</td><td>O</td><td>MPU</td><td>Device Busy Signal</td><td>This pin is Busy state output pin
When Busy is High, the operation of the chip should not be interrupted, and command should not be sent.
For example., The chip would put Busy pin High when
- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

In the cascade mode, the BUSY pin of the slave chip should be left open.</td><td>Open</td></tr>
<tr><td>M/S#</td><td>I</td><td>VDDIO/VSS</td><td>Cascade Mode Selection</td><td>This pin is Master and Slave selection pin.
- For the single chip application, the M/S# pin should be connected to VDDIO.
- In the cascade mode:
For Master Chip, the M/S# pin should be connected to VDDIO.
For Slave Chip, the M/S# pin should be connected to VSS. The oscillator, booster and regulator circuits of the slave chip will be disabled. The corresponding pins including CL, VDD, VDDIO, VGH, VGL, VSH1, VSH2, VSL and VCOM must be connected to the master chip.</td><td>-</td></tr>
<tr><td>CL</td><td>I/O</td><td>NC</td><td>Clock signal</td><td>This is the clock signal pin.
- For the single chip application, the CL pin should be left open.
- In the cascade mode, the CL pin of the slave chip should be connected to the CL pin of the master chip.</td><td>Open</td></tr>
<tr><td>BS [2:1]</td><td>I</td><td>VDDIO/VSS</td><td>MCU Interface Mode Selection</td><td>These pins are for selecting different bus interface.
Table 5-1 : MCU interface selection
<table>
<tr><td>BS2</td><td>BS1</td><td>MCU Interface</td></tr>
<tr><td>NC / L</td><td>L</td><td>4-wire serial peripheral interface (SPI)</td></tr>
<tr><td>NC / L</td><td>H</td><td>3-wire serial peripheral interface (SPI) – 9 bits SPI</td></tr>
<tr><td>H</td><td>L</td><td>I2C Interface</td></tr>
</table></td><td>-</td></tr>
<tr><td>TSDA</td><td>I/O</td><td>Temperature sensor SDA</td><td>Interface to Digital Temp. Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Data pin.
External pull up resistor is required when connecting to I^2C slave.</td><td>Open</td></tr>
<tr><td>TSCL</td><td>O</td><td>Temperature sensor SCL</td><td>Interface to Digital Temp. Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Clock pin.
External pull up resistor is required when connecting to I^2C slave.</td><td>Open</td></tr>
</table>

Pin name	Type	Connect to	Function	Description	When not in use
Analog Pin					
GDR	O	POWER MOSFET Driver Control	VGH, VGL Generation	N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		Current sense input pin for the control Loop.	-
VGH	C	Stabilizing capacitor		Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and VSS in the application circuit.	-
VGL	C	Stabilizing capacitor		This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and VSS in the application circuit.	-
VSH1	C	Stabilizing capacitor	VSH1, VSH2, VSL Generation	This pin is Positive Source driving voltage, VSH1 Connect a stabilizing capacitor between VSH1 and VSS in the application circuit.	-
VSH2	C	Stabilizing capacitor		This pin is Positive Source driving voltage, VSH2 Connect a stabilizing capacitor between VSH2 and VSS in the application circuit.	
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage. Connect a stabilizing capacitor between VSL and VSS in the application circuit.	-
VCOM	C	Panel/ Stabilizing capacitor	VCOM Generation	These pins are VCOM driving voltage Connect a stabilizing capacitor between VCOM and VSS in the application circuit.	-
Panel Driving					
S [159:0]	O	Panel	Source driving signal	Source output pin.	Open
G [295:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD	O	Panel	Border driving signal	Border output pin.	Open
Others					
NC	NC	NC	Not Connected	Keep open. Don't connect with other NC pins.	Open
TPA, TPB, TPC, TPD, TPF, FB	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Don't connect to other NC pins and test pins including TPA, TPB, TPC, TPD, TPE, TPF and FB.	Open
TIN	I	NC	Reserved for Testing	Reserved pins. - Keep open.	Open
TPE	O	NC			Open

6 Functional Block Description

6.1 MCU Interface

6.1.1 MCU Interface selection

The SSD1675 can support 3-wire/4-wire serial peripheral and I2C interface. In the SSD1675, the MCU interface is pin selectable by BS [2:1] shown in Table 6-1.

Note
(1) L is connected to V_{SS}
(2) H is connected to V_{DDIO}

Table 6-1 : Interface pins assignment under different MCU interface

	Pin Name						
MCU Interface	**BS2**	**BS1**	**RES#**	**CS#**	**D/C#**	**SCL**	**SDA**
4-wire serial peripheral interface (SPI)	Not Connect / Connect to VSS	Connect to VSS	Required	Required	Required	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	Not Connect / Connect to VSS	Connect to VDDIO	Required	Required	Connect to VSS	SCL	SDA
I2C Interface	Connect to VDDIO	Connect to VSS	Required	Connect to VSS	SA0	SCL	SDA

6.1.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure 4-wire SPI is shown in Table 6-2

Table 6-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:
(1) L is connected to V_{SS} and H is connected to V_{DDIO}
(2) ↑ stands for rising edge of signal
(3) SDA(Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

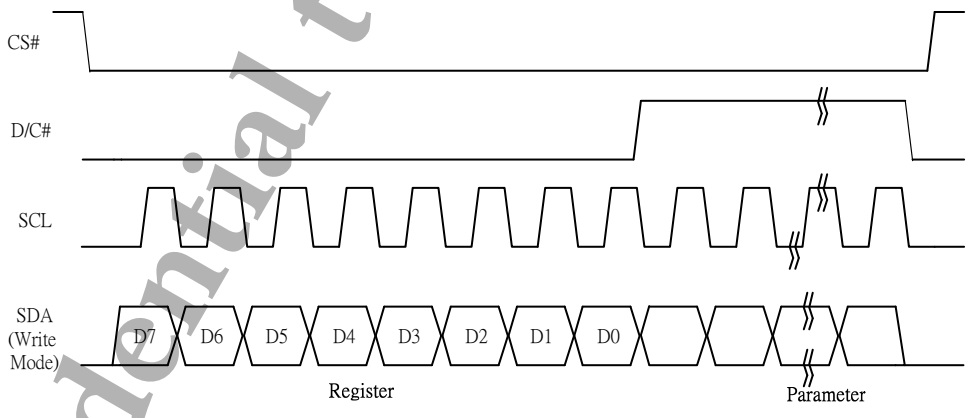


Figure 6-1 : Write procedure in 4-wire SPI mode

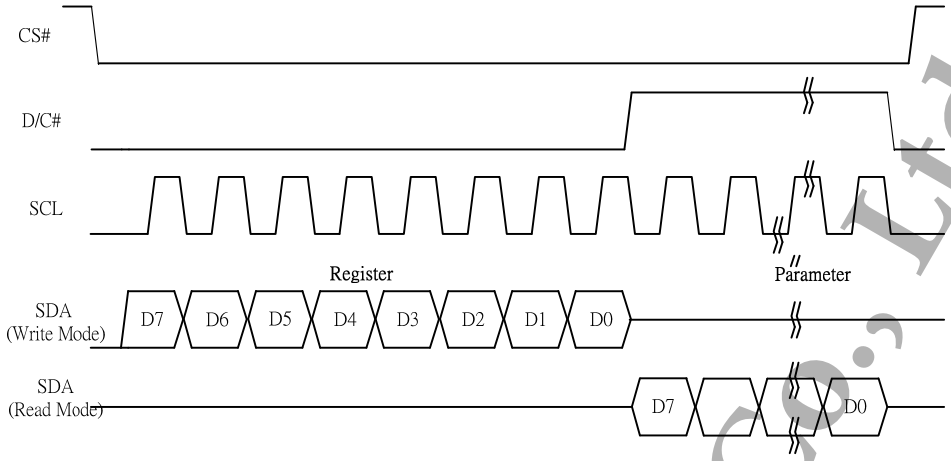


Figure 6-2 : Read procedure in 4-wire SPI mode

6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

Table 6-3 : Control pins status of 3-wire SPI

Function	SCLK pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

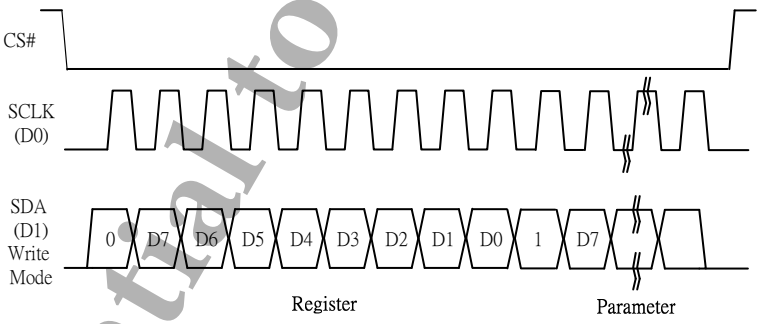


Figure 6-3 : Write procedure in 3-wire SPI

6.1.4 MCU I2C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA and I²C-bus clock signal SCL. Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1675 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	1	1	1	1	0	SA0	R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1675. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.
It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

6.1.4.1 I2C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to **Error! Reference source not found.** for the write mode of I²C-bus in chronological order.

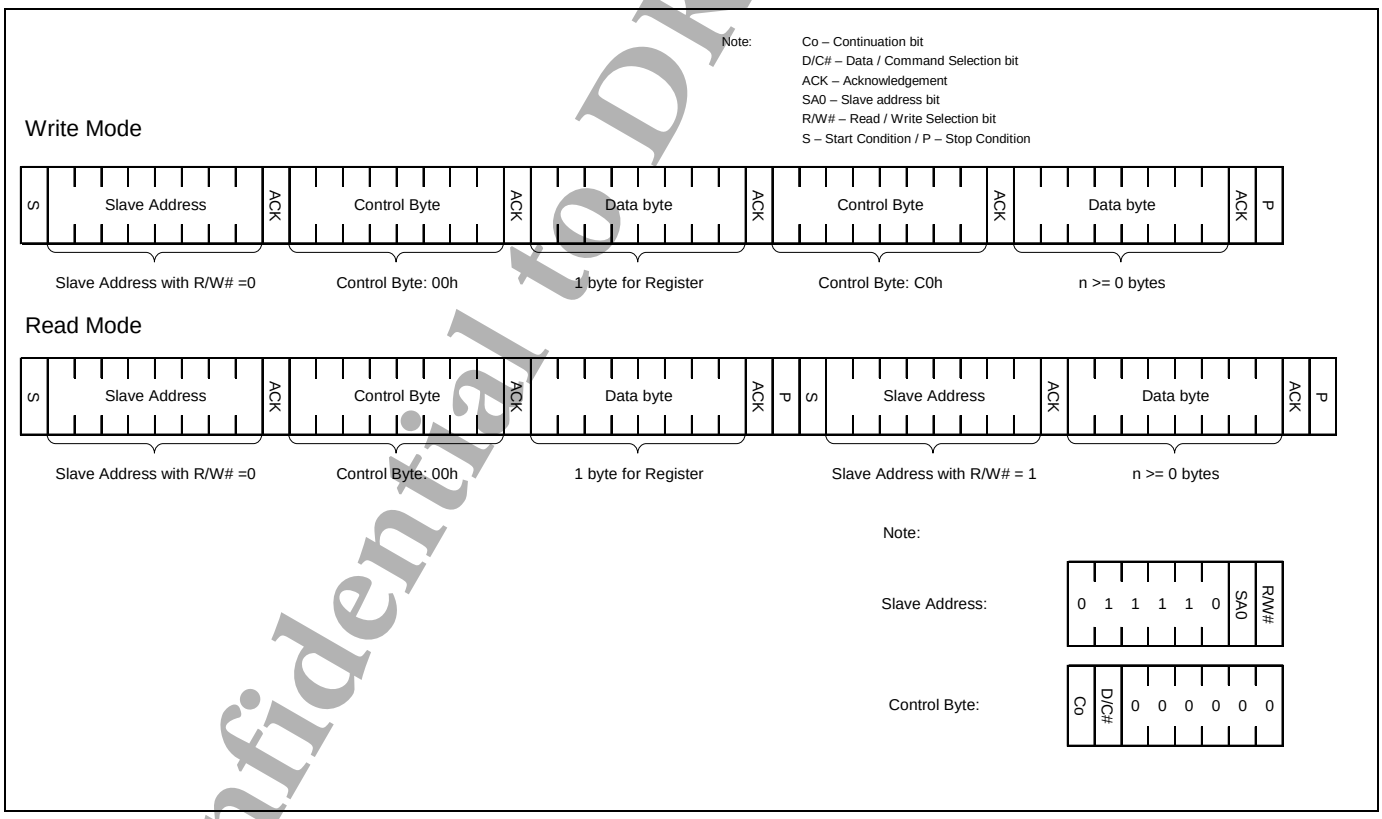


Figure 6-4 : I²C-bus data format

6.1.4.2 Write mode for I2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6-5. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1675, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 6-6 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
    a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6-5. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

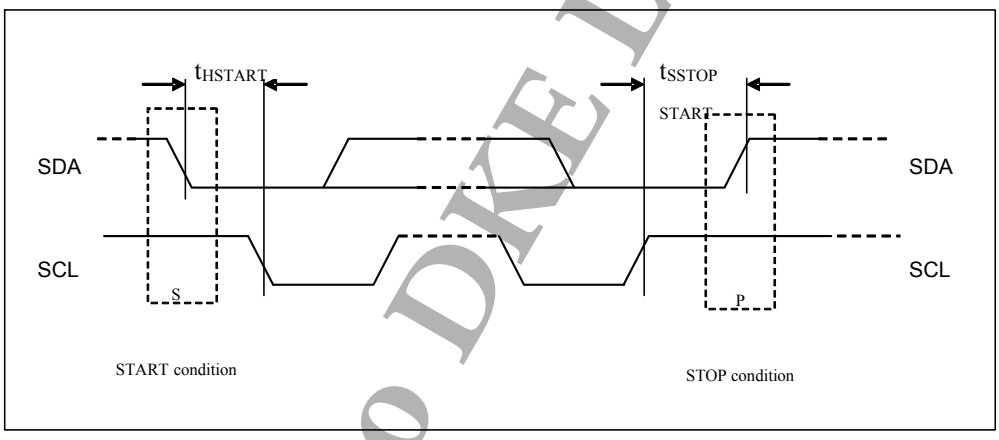


Figure 6-5 : Definition of the Start and Stop Condition

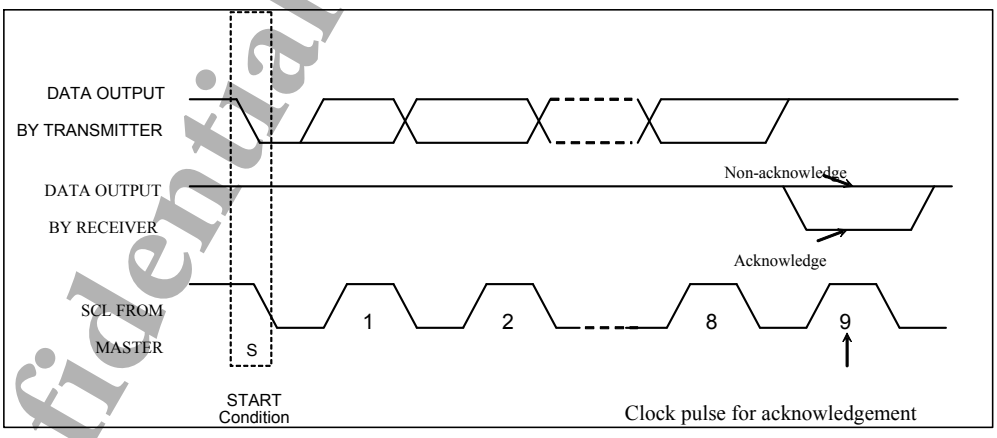


Figure 6-6 : Definition of the acknowledgement condition

Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the “HIGH” period of the clock pulse. Please refer to the Figure 6-7 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

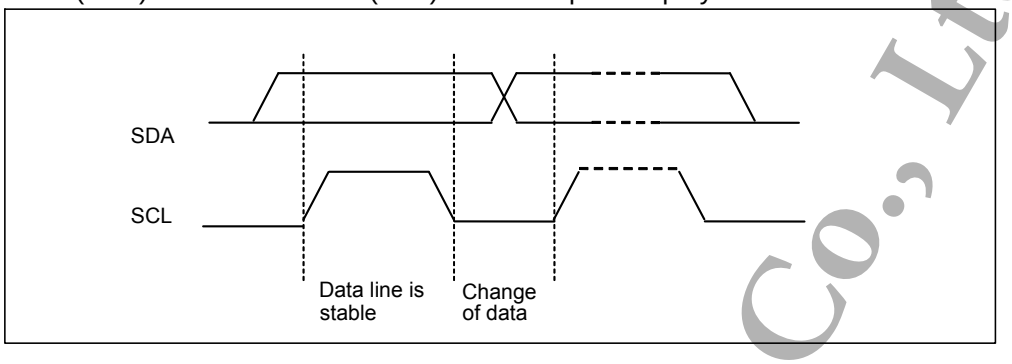


Figure 6-7 : Definition of the data transfer condition

6.2 RAM

The On chip display RAM is holding the image data.
1 set of RAM is built for Mono B/W. The RAM size is 160x296 bits.
1 set of RAM is built for Mono Red. The RAM size is 160x296 bits.

Table 6-4 : LUT mapping to RAM content for Mono Black White and Mono Red

R	B/W	LUT
0	0	LUT 0
0	1	LUT 1
1	0	LUT 2
1	1	LUT 3

.

In order to write the image data into the display RAM, it is necessary to define the Data Entry Mode Setting (Command 0x11h), the Driver Output Control (Command 0x01h) and the Gate Scan Start Position (Command 0x0Fh). The following is an example to show how to set these commands. And, Table 6-5 is the corresponding RAM address mapping of these command settings.

- Command “Data Entry Mode Setting” R11h is set to:

Address Counter update in X direction	AM=0
X: Increment Y: Increment	ID[1:0] =11

- Command “Driver Output Control” R01h is set to:

296 Mux		MUX = 127h
Select G0 as 1st gate		GD = 0
Left and Right gate Interlaced		SM = 0
Scan From G0 to G295		TB = 0

- Command “Gate Scan Start Position” R0Fh is set to:

Set the Start Position of Gate = G0	SCN=0

- Then the data byte sequence: DB0, DB1, DB2 … DB18 … DB19, DB20 … DB5919

Table 6-5 : RAM address map according to above condition

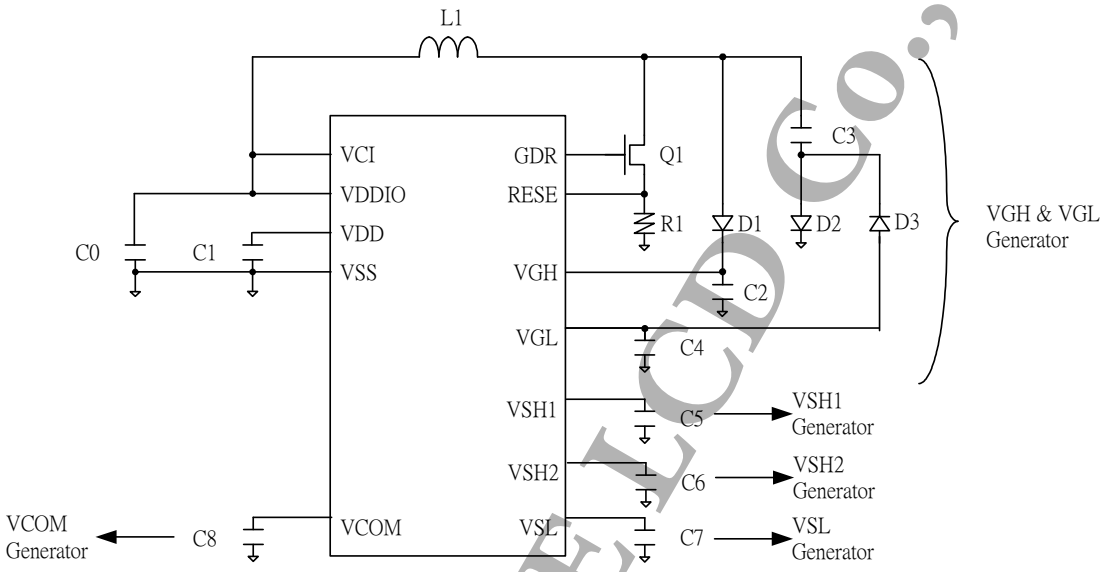
		S0	S1	S2	S3	S4	S5	S6	S7	…	…	S152	S153	S154	S155	S156	S157	S158	S159	Source X-ADDR
		00h								…		13h								
G0	00h	DB0 [7]	DB0 [6]	DB0 [5]	DB0 [4]	DB0 [3]	DB0 [2]	DB0 [1]	DB0 [0]	…	…	DB19 [7]	DB19 [6]	DB19 [5]	DB19 [4]	DB19 [3]	DB19 [2]	DB19 [1]	DB19 [0]	
G1	01h	DB20 [7]	DB20 [6]	DB20 [5]	DB20 [4]	DB20 [3]	DB20 [2]	DB20 [1]	DB20 [0]	…	…	DB39 [7]	DB39 [6]	DB39 [5]	DB39 [4]	DB39 [3]	DB39 [2]	DB39 [1]	DB39 [0]	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
G294	126h	DB5880 [7]	DB5880 [6]	DB5880 [5]	DB5880 [4]	DB5880 [3]	DB5880 [2]	DB5880 [1]	DB5880 [0]	…	…	DB5899 [7]	DB5899 [6]	DB5899 [5]	DB5899 [4]	DB5899 [3]	DB5899 [2]	DB5899 [1]	DB5899 [0]	
G295	127h	DB5900 [7]	DB5900 [6]	DB5900 [5]	DB5900 [4]	DB5900 [3]	DB5900 [2]	DB5900 [1]	DB5900 [0]	…	…	DB5919 [7]	DB5919 [6]	DB5919 [5]	DB5919 [4]	DB5919 [3]	DB5919 [2]	DB5919 [1]	DB5919 [0]	
GATE	Y-ADDR																			

6.3 Oscillator

The oscillator module generates the clock reference for waveform timing and analog operations.

6.4 Booster & Regulator

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH1, VSH2, VSL and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.



6.5 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level. The sensed value can be programmed into OTP.

The flow of VCOM sensing:

- Active Gate is scanning during the VCOM sense Period.
- Source are VSS.
- VCOM pin used for sensing.
- During Sensing period, BUSY is high.
- After Sensing, Active Gate return to non-select stage.

6.6 Gate waveform, Programmable Source and VCOM waveform

- There are 7 groups, each group contains 4 phases, totally 28 phases for programmable Source waveform with different phase length.
- The phase length of LUT0~LUT4 is defined as TP[nX]
  - The range of TP[nX] is from 0 to 255.
  - n represents the Group number from 0 to 6; X represents the sub-group number from A to D.
  - TP[nX] = 0 indicates phase skipped.
- The repeat count of group is defined as RP[n], which is used for the count of repeating TP[nA] , TP[nB], TP[nC] and TP[nD];
  - The range of RP[n] is from 0 to 255.
  - n represents the Group number from 0 to 6;
  - RP[n] = 0 indicates run time =1,
- Source/VCOM Voltage Level: VS [nX-LUT] is constant in each phase.
- VS [nX-LUTn] indicates the voltage in phase n for transition LUT.
  - 00 – VSS
  - 01 – VSH1
  - 10 – VSL
  - 11 – VSH2

Table 6-6 : VS [nX-LUTn] value mapping table

LUT0	B	00 – VSS, 01 – VSH1, 10 – VSL, 11-VSH2
LUT1	W	00 – VSS, 01 – VSH1, 10 – VSL, 11-VSH2
LUT2	R	00 – VSS, 01 – VSH1, 10 – VSL, 11-VSH2
LUT3	R	Assign as the same as LUT2
LUT4	VCOM	00 –DCVCOM, 01 – VSH1+DCVCOM, 10 – VSL+ DCVCOM

- VS [nX-LUT], TP[nX], RP[n], VSH , VSL are stored in waveform lookup table register [LUT].

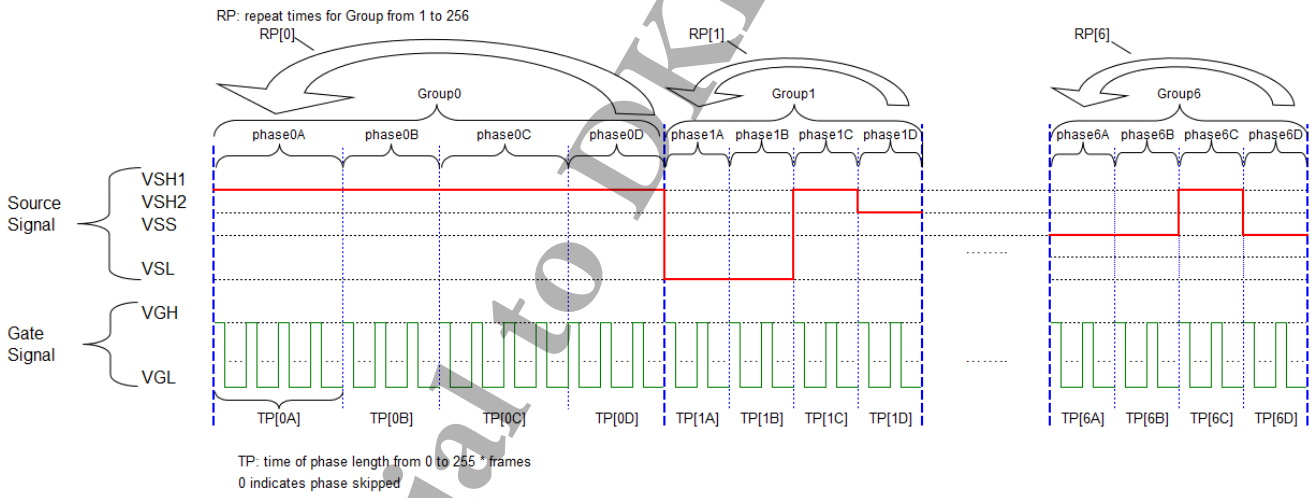


Figure 6-8 : Gate waveform and Programmable Source and VCOM waveform illustration

6.7 Waveform Setting

WAVEFORM SETTING (WS) contains 70bytes, which define the display driving waveform settings. They are arranged in following format figure shown

	D7	D6	D5	D4	D3	D2	D1	D0
0	VS[0A-L0]		VS[0B-L0]		VS[0C-L0]		VS[0D-L0]	
1	VS[1A-L0]		VS[1B-L0]		VS[1C-L0]		VS[1D-L0]	
2	VS[2A-L0]		VS[2B-L0]		VS[2C-L0]		VS[2D-L0]	
3	VS[3A-L0]		VS[3B-L0]		VS[3C-L0]		VS[3D-L0]	
4	VS[4A-L0]		VS[4B-L0]		VS[4C-L0]		VS[4D-L0]	
5	VS[5A-L0]		VS[5B-L0]		VS[5C-L0]		VS[5D-L0]	
6	VS[6A-L0]		VS[6B-L0]		VS[6C-L0]		VS[6D-L0]	
7	VS[0A-L1]		VS[0B-L1]		VS[0C-L1]		VS[0D-L1]	
…								
…								
31	VS[3A-L4]		VS[3B-L4]		VS[3C-L4]		VS[3D-L4]	
32	VS[4A-L4]		VS[4B-L4]		VS[4C-L4]		VS[4D-L4]	
33	VS[5A-L4]		VS[5B-L4]		VS[5C-L4]		VS[5D-L4]	
34	VS[6A-L4]		VS[6B-L4]		VS[6C-L4]		VS[6D-L4]	
35	TP[0A]							
36	TP[0B]							
37	TP[0C]							
38	TP[0D]							
39	RP[0]							
40	TP[1A]							
41	TP[1B]							
42	TP[1C]							
43	TP[1D]							
44	RP[1]							
…	…							
…	…							
65	TP[6A]							
66	TP[6B]							
67	TP[6C]							
68	TP[6D]							
69	RP[6]							
70	VGH							
71	VSH1							
72	VSH2							
73	VSL							
74	Frame 1							
75	Frame 2							

Figure 6-9 : VS[nX-LUT] and TP[n] mapping in LUT

WS can be accessed by MCU interface or loaded from OTP.
5 registers are involved to set WS from MCU interface

- WS byte 0~69, the content of VS [n-XY], TP [n#], RP[n], are the parameter belonging to Register 0x32
- WS byte 70, the content of gate level, is the parameter belonging to Register 0x03.
- WS byte 71~73, the content of source level, is the parameter belonging to Register 0x04.
- WS byte 74, the content of dummy line, is the parameter belonging to Register 0x3A.
- WS byte 75, the content of gate line width, is the parameter belonging to Register 0x3B.

6.8 OTP

6.8.1 The OTP information

The OTP is the non-volatile memory and stored the information of:

- 25 set of WAVEFORM SETTING (WS).
- 25 set of TEMPERATURE RANGE (TR). which consist of
  - Low limit (TEMP [m-L]) and High limit (TEMP [m-H]) for each set of WS#.
- VCOM value
- Waveform version ID

Remark:

- WS [m] means the waveform setting of temperature set m, the configuration are same as the definition in LUT. The corresponding low temperature range of WS[m] defined as TEMP [m-L] and high range defined as TEMP [m-H]
- Load WS [m] from OTP for LUT if Temp [m-L] < Temperature Register <= Temp [m-H]

6.8.2 The OTP content and address mapping

The mapping table of OTP for waveform setting and temperature range is shown in Figure 6-10 :

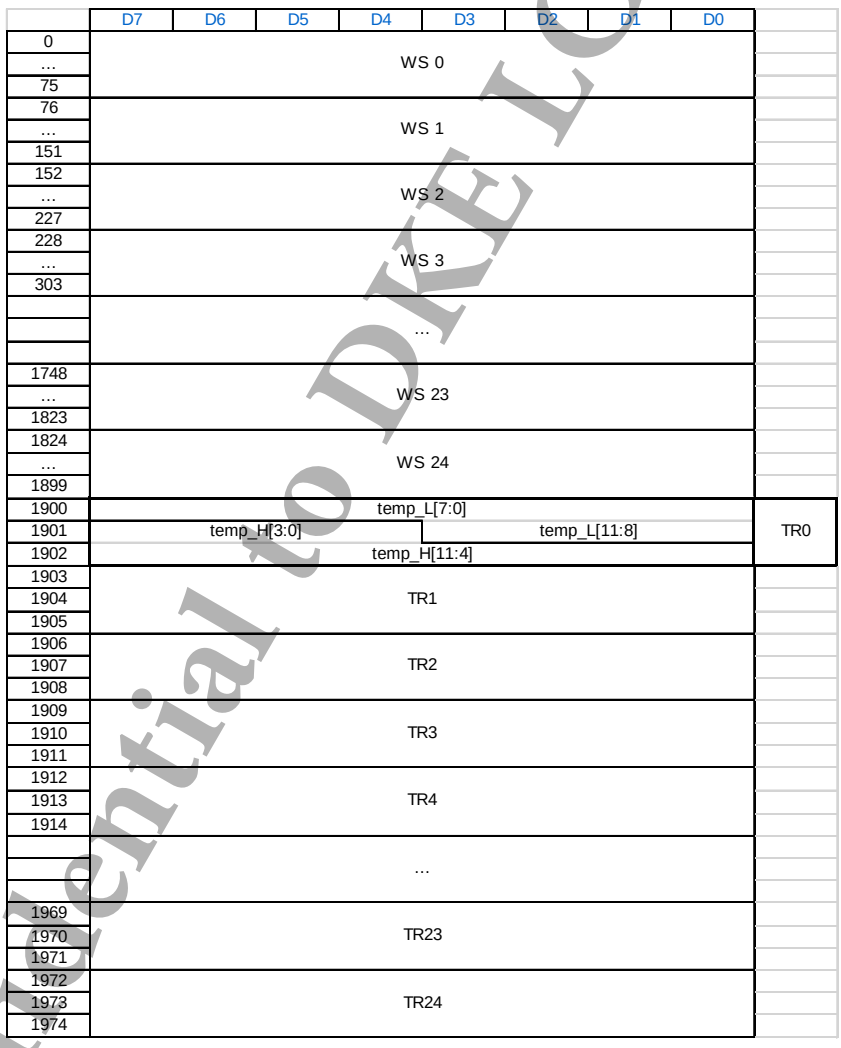


Figure 6-10 : The Waveform setting mapping in OTP for waveform setting and temperature range

6.9 Temperature Searching Mechanism

Legend:

WS#	Waveform Setting no. #
TR#	Temperature Range no. #
LUT	560 bit register storing the waveform setting (volatile)
Temperature register	12bit Register storing reading from temperature sensor (volatile)
OTP	A non-volatile storing 25 sets of waveform setting and 25 set of temperature range
WS_sel_ address	an address pointer indicating the selected WS#

OTP (non-volatile)	
WS0	TR0
WS1	TR1
WS2	TR2
WS3	TR3
…	…
WS23	TR23
WS24	TR24

Figure 6-11 : Waveform Setting and Temperature Range # mapping

IC implementation requirement

1 Compare temperature register from **TR0 to TR24**, in sequence. **The last match will be recorded**

i.e. If the temperature register fall in both TR3 and TR5. WS5 will be selected

2 There is no restriction on the sequence of TR0, TR2…. TR24

Example Temperature Range assignment

Waveform setting	**Temperature range**	**Lower Limit [Hex]**	**Upper Limit[Hex]**
WS0	-128 DegC < Temperature <= 5 DegC	800	050
WS1	5 DegC < Temperature <= 10DegC	050	0A0
WS2	10 DegC < Temperature <= 15DegC	0A0	0F0
WS3	15 DegC < Temperature <= 20DegC	0F0	140
WS4	20 DegC < Temperature <= 25DegC	140	190
WS5	25 DegC < Temperature <= 30DegC	190	1E0
WS6	30 DegC < Temperature <= 35DegC	1E0	230
WS7	35 DegC < Temperature <= 127.9DegC	230	7FF
Others		000	000

Figure 6-12 : Example Temperature Range

User application

1 If temperature is 5 DegC, WS0 is selected

2 If temperature is 23 DegC, WS4 is selected

3 If temperature > 35 DegC, WS7 is selected

6.10 External Temperature Sensor I2C Single Master Interface

The chip provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing.
TSDA will treat as SDA line and TSCL will treat as SCL line. They are required connecting with external pull-up resistor.

1. If the Temperature value MSByte bit D11 = 0, then
   the temperature is positive and value (DegC) = + (Temperature value) / 16
2. If the Temperature value MSByte bit D11 = 1, then
   the temperature is negative and value (DegC) = - (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

6.11 Cascade Mode

The SSD1675 has a cascade mode that can cascade 2 chips to achieve the display resolution up to 160 (sources) x 296 (gates). The pin M/S# is used to configure the chip. When M/S# is connected to VDDIO, the chip is configured as a master chip. When M/S# is connected to VSS, the chip is configured as a slave chip.

When the chip is configured as a master chip, it will be the same as a single chip application, ie, all circuit blocks will be worked as usual. When the chip is configured as a slave chip, its oscillator and booster & regulator circuit will be disabled. The oscillator clock and all booster voltages will be come from the master chip. Therefore, the corresponding pins including CL, VDD, VGH, VGL, VSH1, VSH2, VSL, VGL and VCOM must be connected to the master chip.

6.12 VCI Detection

The VCI detection function is used to detect the VCI level when it is lower than Vlow, threshold voltage set by register.

In the SSD1675, there is a command to execute the VCI detection function. When the VCI detection command is issued, the VCI detection will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of VCI, which 0 is normal, 1 is VCI<Vlow.

6.13 HV Ready Detection

The HV Ready detection function is used to detect whether the analog block is ready.

In the SSD16, there is a command to execute the HV Ready detection function. When the HV Ready detection command is issued, the HV Ready will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of HV Ready, which 0 is normal, 1 indicate HV is not ready.

7 COMMAND TABLE

Table 7-1: Command Table

<table>
<tr><th colspan="12">Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output control</td><td rowspan="4">Gate setting
A[8:0]= 127h [POR], 296 MUX
MUX Gate lines setting as (A[8:0] + 1).

B[2:0] = 000 [POR].
Gate scanning sequence and direction

B[2]: GD
Selects the 1st output Gate
GD=0 [POR],
G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, …
GD=1,
G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, …

B[1]: SM
Change scanning order of gate driver.
SM=0 [POR],
G0, G1, G2, G3…295 (left and right gate interlaced)
SM=1,
G0, G2, G4 …G294, G1, G3, …G295

B[0]: TB
TB = 0 [POR], scan from G0 to G295
TB = 1, scan from G295 to G0.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate Driving voltage Control</td><td rowspan="2">Set Gate driving voltage
A[4:0] = 19h [POR] , VGH at 21V [POR]
VGH setting from 10V to 21V
<table><tr><th>A[4:0]</th><th>VGH</th><th>A[4:0]</th><th>VGH</th></tr><tr><td>03h</td><td>10</td><td>0Fh</td><td>16</td></tr><tr><td>04h</td><td>10.5</td><td>10h</td><td>16.5</td></tr><tr><td>05h</td><td>11</td><td>11h</td><td>17</td></tr><tr><td>06h</td><td>11.5</td><td>12h</td><td>17.5</td></tr><tr><td>07h</td><td>12</td><td>13h</td><td>18</td></tr><tr><td>08h</td><td>12.5</td><td>14h</td><td>18.5</td></tr><tr><td>09h</td><td>13</td><td>15h</td><td>19</td></tr><tr><td>0Ah</td><td>13.5</td><td>16h</td><td>19.5</td></tr><tr><td>0Bh</td><td>14</td><td>17h</td><td>20</td></tr><tr><td>0Ch</td><td>14.5</td><td>18h</td><td>20.5</td></tr><tr><td>0Dh</td><td>15</td><td>19h</td><td>21</td></tr><tr><td>0Eh</td><td>15.5</td><td>Other</td><td>NA</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

A[7]/B[7] = 1,
VSH1/VSH2 voltage setting from 2.4V to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 18V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	4Ch	17.2
34h	12.4	4Dh	17.4
35h	12.6	4Eh	17.6
36h	12.8	4Fh	17.8
37h	13	50h	18
38h	13.2	Other	NA
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7] = 0,
VSL setting from -9V to -18V

C[7:0]	VSL
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
3Ch	-17.5
3Eh	-18
Other	NA

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting.
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:0] -> Soft start setting for Phase1 = 8Bh [POR]
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		B[7:0] -> Soft start setting for Phase2 = 9Ch [POR]
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		C[7:0] -> Soft start setting for Phase3 = 96h [POR]
0	1		0	0	D_5	D_4	D_3	D_2	D_1	D_0		D[7:0] -> Duration setting = 0Fh [POR]

Bit Description of each byte:
A[6:0] / B[6:0] / C[6:0]:

Bit[6:4]	Driving Strength Selection
000	1(Weakest)
001	2
010	3
011	4
100	5
101	6
110	7
111	8(Strongest)

Bit[3:0]	Min Off Time Setting of GDR [Time unit]
0000 ~ 0011	NA
0100	2.6
0101	3.2
0110	3.9
0111	4.6
1000	5.4
1001	6.3
1010	7.3
1011	8.4
1100	9.8
1101	11.5
1110	13.8
1111	16.5

D[5:0]: duration setting of phase
D[5:4]: duration setting of phase 3
D[3:2]: duration setting of phase 2
D[1:0]: duration setting of phase 1

Bit[1:0]	Duration of Phase [Approximation]
00	10ms
01	20ms
10	30ms
11	40ms

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 295. A[8:0] = 000h [POR] When TB=0: SCN [8:0] = A[8:0] When TB=1: SCN [8:0] = 295 - A[8:0]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: A[0] : Description 0 Normal Mode [POR] 1 Enter Deep Sleep Mode After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	1		0	0	0	0	0	0	0	A_0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect A[2:0] VCI level A[2:0] VCI level A[2:0] VCI level 011 2.2V 101 2.4V 111 2.6V 100 2.3V 110 2.5V Other NA The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh [POR]
0	1		A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
0	1		A_3	A_2	A_1	A_0	0	0	0	0		
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.
1	1		A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
1	1		A_3	A_2	A_1	A_0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] A[7:4] Red RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content A[3:0] BW RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

	Parameter (in Hex)
Enable Clock Signal, Then Enable ANALOG Then DISPLAY Then Disable ANALOG Then Disable OSC	C7
Enable Clock Signal, Then Load LUT	90
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT	B0
Enable ANALOG Then DISPLAY Then Disable ANALOG Then Disable OSC	47
To Enable Clock Signal (CLKEN=1)	80
To Enable Clock Signal, then Enable ANALOG (CLKEN=1, ANALOGEN=1)	C0
To DISPLAY	04
To Disable ANALOG, then Disable Clock Signal (CLKEN=0, ANALOGEN=0)	03
To Disable Clock Signal (CLKEN=0)	01

0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM [According to parameter of Register 41h to select reading RAM(BW) / RAM(RED)], until another command is written. Address pointers will advance accordingly.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[6]=1, Normal Mode A[6]=0, Reserve A[3:0] = 09h, duration = 10s. VCOM sense duration = Setting + 1 Seconds
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	44h	-1.7
0Bh	-0.3	48h	-1.8
10h	-0.4	4Bh	-1.9
14h	-0.5	50h	-2
17h	-0.6	54h	-2.1
1Bh	-0.7	58h	-2.2
20h	-0.8	5Bh	-2.3
24h	-0.9	5Fh	-2.4
28h	-1	64h	-2.5
2Ch	-1.1	68h	-2.6
2Fh	-1.2	6Ch	-2.7
34h	-1.3	6Fh	-2.8
37h	-1.4	73h	-2.9
3Ch	-1.5	78h	-3
40h	-1.6	Other	NA

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read	Read Register stored in OTP: 1. A[7:0]: VCOM OTP Selection (R37, Byte A) 2. B[7:0]: VCOM Register (R2C) 3. C[7:0]~F[7:0]: Reserved 4. G[7:0]~H[7:0]: Module ID / Waveform Version (R37, Byte F and Byte G) [2 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x21] A[5]: HV Ready Detection flag [POR=1] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	0	A_4	0	0	A_1	A_0		
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [70 bytes], which contains the content of VS [nX-LUT], TP #[nX], RP#[n]). Refer to Session 6.7 Waveform Setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write OTP selection	Write the OTP Selection: A[7]=1 spare VCOM OTP selection B[7:0]~E[7:0] reserved F[7:0]~G[7:0] module ID /waveform version.
0	1		A_7	0	0	0	0	0	0	0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set number of dummy line period A[6:0] = 30h [POR] A[6:0]: Number of dummy line period in term of TGate Available setting 0 to 127.
0	1		0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set Gate line width (TGate) A[3:0] = 1010 [POR] Remark: Default value will give 50Hz Frame frequency under 48 dummy line pulse setting.
0	1		0	0	0	0	A_3	A_2	A_1	A_0		

The reference parameter of register 0x3A and 0x3B for 296 MUX

Frame input [Hz]	0x3B	0x3A
15	0x0E	0x7E
20	0x0E	0x14
25	0x0D	0x2A
30	0x0C	0x52
40	0x0B	0x47
50	0x0A	0x30
60	0x09	0x25
70	0x08	0x2C
80	0x08	0x01
90	0x07	0x0C
100	0x06	0x25
110	0x06	0x07
120	0x05	0x18
130	0x04	0x35
140	0x04	0x1C
150	0x04	0x07
160	0x03	0x20
170	0x03	0x0D
180	0x02	0x33
190	0x02	0x20
200	0x02	0x10

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option A[7:6] — Select VBD as 00 — GS Transition, Defined in A[1:0] 01 — Fix Level, Defined in A[5:4] 10 — VCOM 11[POR] — HiZ A [5:4] Fix Level Setting for VBD A[5:4] — VBD level 00[POR] — VSS 01 — VSH1 10 — VSL 11 — VSH2 A [1:0] GS Transition setting for VBD A[1:0] — VBD Transition 00[POR] — LUT0 01 — LUT1 10 — LUT2 11 — LUT3
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to 24h 1 : Read RAM corresponding to 26h
0	1		0	0	0	0	0	0	0	A_0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 13h
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Hieght, POR= 000 Step of alter RAM in Y-direction according to Gate
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[6:4]	Height	A[6:4]	Height
000	8	100	128
001	16	101	256
010	32	110	296
011	64	111	NA

A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	160
010	32	110	NA
011	64	111	NA

BUSY pad will output high during operation.

0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Hieght, POR= 000 Step of alter RAM in Y-direction according to Gate
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[6:4]	Height	A[6:4]	Height
000	8	100	128
001	16	101	256
010	32	110	296
011	64	111	NA

A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	160
010	32	110	NA
011	64	111	NA

During operation, BUSY pad will output high.

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1	74	0	1	1	1	0	1	0	0	Set Analog Block Control	A[7:0]: 54h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1	7E	0	1	1	1	1	1	1	0	Set Digital Block Control	A[7:0]: 3Bh
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

8 COMMAND DESCRIPTION

8.1 Driver Output Control (01h)

This triple byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		0	0	1	1	1	1	1	1
W	1								MUX8
POR									1
W	1						GD	SM	TB
POR							0	0	0

MUX[8:0]: Specify number of lines for the driver: MUX[8:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 296MUX.

GD: Selects the 1st output Gate
This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

SM: Change scanning order of gate driver.
When SM is set to 0, left and right interlaced is performed.
When SM is set to 1, no splitting odd / even of the GATE signal is performed,
Output pin assignment sequence is shown as below (for 296 MUX ratio):

	SM=0	SM=0	SM=1	SM=1
Driver	**GD=0**	**GD=1**	**GD=0**	**GD=1**
G0	ROW0	ROW1	ROW0	ROW148
G1	ROW1	ROW0	ROW148	ROW0
G2	ROW2	ROW3	ROW1	ROW149
G3	ROW3	ROW2	ROW149	ROW1
:	:	:	:	:
G146	ROW146	ROW147	ROW73	ROW222
G147	ROW147	ROW146	ROW222	ROW73
G148	ROW148	ROW149	ROW74	ROW223
G149	ROW149	ROW148	ROW223	ROW74
:	:	:	:	:
G292	ROW292	ROW293	ROW146	ROW294
G293	ROW293	ROW292	ROW294	ROW146
G294	ROW294	ROW295	ROW147	ROW295
G295	ROW295	ROW294	ROW295	ROW147

See “Scan Mode Setting” on next page.

TB: Change scanning direction of gate driver.
This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB = 0) or from bottom to up (TB = 1).

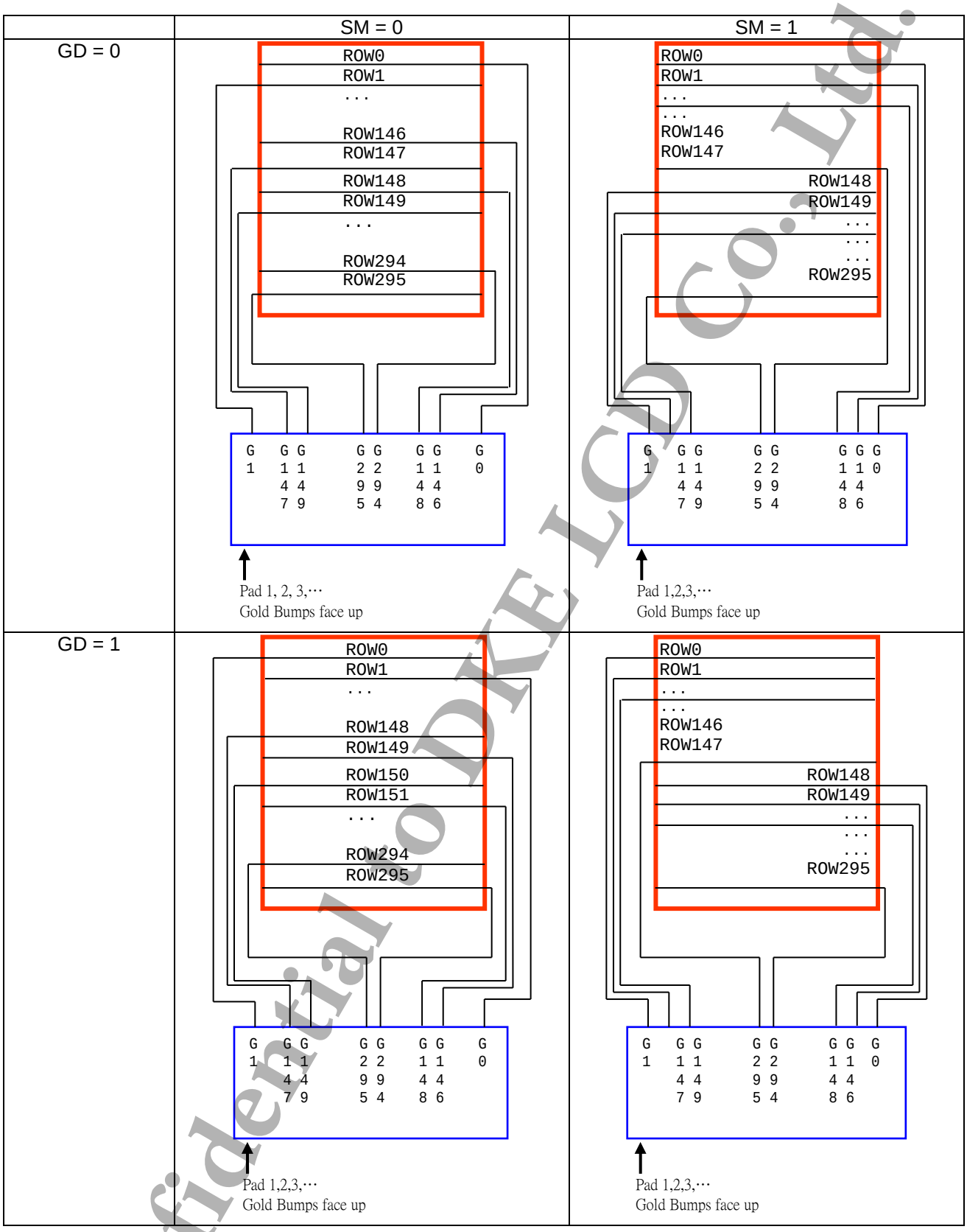


Figure 8-1: Output pin assignment on different Scan Mode Setting

8.2 Gate Scan Start Position (0Fh)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	SCN8
POR		0	0	0	0	0	0	0	0

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to 295. Figure 8-2 shows an example using this command of this command when MUX ratio= 295 and MUX ratio= 148 “ROW” means the graphic display data RAM row.

Figure 8-2: Example of Set Display Start Line with no Remapping

	MUX ratio (01h) = 127h	MUX ratio (01h) = 093h	MUX ratio (01h) = 095h
GATE Pin	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 04Ah
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
:	:	:	:
:	:	:	:
G72	:	:	-
G73	:	:	-
G74	:	:	ROW74
G75	:	:	ROW75
:	:	:	:
:	:	:	:
G146	ROW146	ROW146	:
G147	ROW147	ROW147	:
G148	ROW148	-	:
G149	ROW149	-	:
:	:	:	:
	:	:	:
G220	:	:	:
G221	:	:	:
G222	:	:	ROW222
G223	:	:	ROW223
	:	:	:
:	:	:	:
G292	ROW292	-	-
G293	ROW293	-	-
G294	ROW294	-	-
G295	ROW295	-	-
Display Example			

Figure 8-3: Example of Set Display Start Line with no Remapping

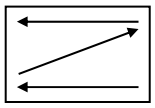
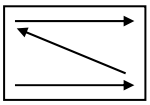
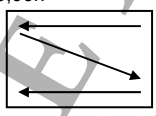
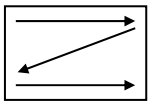
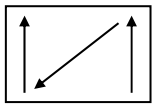
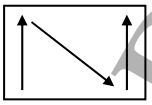
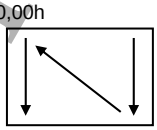
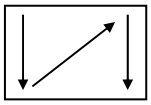
8.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

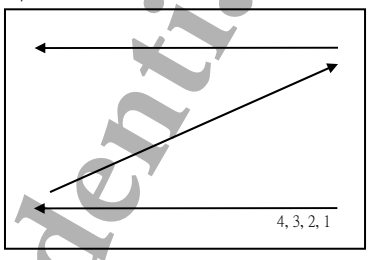
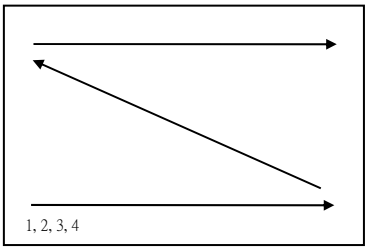
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	1	1

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = “01”. The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = “00”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = “0”, the address counter is updated in the X direction. When AM = “1”, the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00” X: decrement Y: decrement	ID [1:0]="01” X: increment Y: decrement	ID [1:0]="10” X: decrement Y: increment	ID [1:0]="11” X: increment Y: increment
AM="0” X-mode	00,00h  13,127h	00,00h  13, 127h	00,00h  13, 127h	00,00h  13, 127h
AM="1” Y-mode	00,00h  13, 127h	00,00h  13, 127h	00,00h  13, 127h	00,00h  13, 127h

The pixel sequence is defined by the ID [0],

	ID[1:0]="00” X: decrement Y: decrement	ID[1:0]="01” X: increment Y: decrement
AM="0” X-mode	00,00h  4, 3, 2, 1 13,127h	00,00h  1, 2, 3, 4 13,127h

8.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1				XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1				XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	0	1	0	0	1	1

XSA[4:0]/XEA[4:0]: Specify the start/end positions of the window address in the X direction by 8 times address unit. Data is written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write.
It allows on XEA [4:0] ≤ XSA [4:0]. The settings follow the condition on 00h ≤ XSA [4:0], XEA [4:0] ≤ 13h. The windows is followed by the control setting of Data Entry Setting (R11h)

8.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	YSA8
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		0	0	1	0	0	1	1	1
W	1	0	0	0	0	0	0	0	YEA8
POR		0	0	0	0	0	0	0	1

YSA[8:0]/YEA[8:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by YSA [8:0] and YEA [8:0]. These addresses must be set before the RAM write.
It allows YEA [8:0] ≤ YSA [8:0]. The settings follow the condition on 00h ≤ YSA [8:0], YEA [8:0] ≤ 127h. The windows is followed by the control setting of Data Entry Setting (R11h)

8.6 Set RAM Address Counter (4Eh-4Fh)

Reg#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1				XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0
	W	1								YAD8
	POR									0

XAD[4:0]: Make initial settings for the RAM X address in the address counter (AC).
YAD[8:0]: Make initial settings for the RAM Y address in the address counter (AC).

After RAM data is written, the address counter is automatically updated according to the settings with AM, ID bits and setting for a new RAM address is not required in the address counter. Therefore, data is written consecutively without setting an address. The address counter is not automatically updated when data is read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AM, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

9 Typical Operating Sequence

9.1 Normal Display

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply);	
2	User	-	HW Reset	
	IC		After HW reset, the IC will be ready for command input	
	User	C 12	Command: SW Reset	
	IC		After SW reset, the IC will have Registers load with POR value VCOM register loaded with OTP value IC enter idle mode	BUSY = H
	User	-	Wait until BUSY = L	
3		-	Send initial code to driver including setting of	
	User	C 74 D 54	Command: Set Analog Block Control	
	User	C 7E D 3B	Command: Set Digital Block Control	
	User	C 01	Command: Driver Output Control (MUX, Source gate scanning direction)	
	User	C 3A	Command: Set dummy line period	
	User	C 3B	Command: Set Gate line width	
	User	C 3C	Command: Border waveform control	
4		-	Data operations for Black White	
	User	C 11	Command: Data Entry mode setting	
	User	C 44	Command: RAM X address start /end position	
	User	C 45	Command: RAM Y address start /end position	
	User	C 4E	Command: RAM X address counter	
	User	C 4F	Command: RAM Y address counter	
	User	C 24	Command: write BW RAM	
			Ram Content for Display	
5		-	Data operations for RED	
	User	C 11	Command: Data Entry mode setting	
	User	C 44	Command: RAM X address start /end position	
	User	C 45	Command: RAM Y address start /end position	
	User	C 4E	Command: RAM X address counter	
	User	C 4F	Command: RAM Y address counter	
	User	C 26	Command: write RED RAM	
			Ram Content for Display	
6	User	C 22	Command: Display Update Control 2	BUSY = H
	User	C 20	Command: Master Activation	
	IC	-	Booster and regulators turn on	
	IC	-	Load LUT register with corresponding waveform setting stored in OTP)	
	IC	-	Send output waveform according RAM content and LUT.	
	IC	-	Booster and Regulators turn off	
	IC	-	Back to idle mode	
	User	-	Wait until BUSY = L	
7	User	-	IC power off	

9.2 VCOM OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI and VPP supply)	
2	User	-	HW Reset	
	User	C 12	Command: SW Reset	BUSY = H
	User	-	Wait until BUSY = L	
3	User	C 74 D 54	Command: Set Analog Block Control	
	User	C 7E D 3B	Command: Set Digital Block Control	
	User	C 22 D 80 C 20	Command: Master Activation (assigned by R22h) (Enable clock signal)	BUSY = H
	User	-	Wait until BUSY = L	
4	User	C 37	Proceed OTP sequence. Command: OTP selection Control (default or spare)	OTP selection register
5	User	C 36	Command: Program OTP selection	BUSY = H
	User	-	Wait until BUSY = L	
	User	-	Power OFF (VPP supply)	
6		-	Send initial code to driver including setting of (or leave as POR)	VCOM sensing should have same setting during application
	User	C 01	Command: Driver Output Control (MUX, Source gate scanning direction)	
	User	C 03	Command: Gate Driving voltage Control	
	User	C 04	Command: Source Driving voltage Control	
	User	C 3A	Command: Set dummy line period	
	User	C 3B	Command: Set Gate line width	
	User	C 32	Command: Write LUT register VCOM sense required full set of LUT for operation, USER required writing LUT in register 32h	
		-	LUT parameter	
	User	C 22 D 40 C 20	Command: Master Activation (assigned by R22h) [Enable Analog blocks]	BUSY = H
	User	-	Wait until BUSY = L	
7	User	C 29 D 49	Command: VCOM Sense Duration for 10 seconds	
8	User	C 28	Command: VCOM sense	BUSY = H
	IC	-	VCOM pin in sensing mode	
	IC	-	All Source cell have VSS output	
			All Gate scanning continuously	
	IC	-	According to R29h	
	IC	-	Detect VCOM voltage and store in register	
	IC	-	All Gate Stop Scanning.	
	User	-	Wait until BUSY = L	
9	User	C 22 D 02 C 20	Command: Master Activation (assigned by R22h) [Disable Analog blocks]	BUSY = H
	User	-	Wait until BUSY = L	
	User	-	Power On (VPP supply)	
10	User	C 2A	Command: Program VCOM OTP	BUSY = H
	User	-	Wait until BUSY = L	
11	User	C 22 D 01 C 20	Command: Display Update Control 2 and Master Activation (Disable clock signal)	BUSY = H
	User	-	Wait until BUSY = L	
12	User	-	IC power off (VCI and VPP Supply)	

9.3 WS OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply)	
2	User	-	Power on (VPP supply)	
3	User	-	HW Reset	
	User	C 12	Command: SW Reset	BUSY = H
	User	-	Wait until BUSY = L	
4	User	C 74 D 54	Command: Set Analog Block Control	
	User	C 7E D 3B	Command: Set Digital Block Control	
	User	C 22 D 80 C 20	Command: Master Activation (assigned by R22h) (Enable clock signal)	BUSY = H
	User	-	Wait BUSY = L	
5	User	C 11 D 03	Command: Data Entry mode setting Set Address automatic increment setting = X increment and Y increment Set Address counter update in X direction	
6	User	C 44 D 00 D 13	Command: RAM X address start /end position Set RAM X address start /end from S0 to S159	
7	User	C 45 D 00 D 00 D 27 D 01	Command: RAM Y address start /end position Set RAM Y address start /end from G0 to G295	
8	User	C 4E D 00	Command: RAM X address counter Set RAM X address counter as 0	
9	User	C 4F D 00 D 00	Command: RAM Y address counter Set RAM Y address counter as 0	
12	User	C 24	Write corresponding data into RAM	
			Following specific format	
			Write into RAM	
			Full LUT	
13	User	C 4E D 00 C 4F D 00 D 00	Command: RAM address start /end position (Initial Ram address counter)	
14	User	C 30	Command: Program WS OTP Waveform Setting OTP programming	BUSY = H
	User	-	Wait BUSY = L	
15	User	C 22 D 01 C 20	Command: Master Activation (assigned by R22h) [Disable clock signal]	BUSY = H
	User	-	Wait BUSY = L	
16	User	-	Power off VPP and VCI	

10 Absolute Maximum Rating

Table 10-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} be constrained to the range $V_{SS} < V_{CI}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 Electrical Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 11-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{CI}	VCI operation voltage	VCI		2.2	3.0	3.7	V
V_{DD}	VDD operation voltage	VDD		1.7	1.8	1.9	V
V_{COM_DC}	VCOM_DC output voltage	VCOM		-3.0		-0.2	V
dV_{COM_DC}	VCOM_DC output voltage deviation	VCOM		-200		200	mV
V_{COM_AC}	VCOM_AC output voltage	VCOM		V_{SL} + V_{COM_DC}	V_{COM_DC}	V_{SH1}+ V_{COM_DC}	V
V_{GATE}	Gate output voltage	G0~G295		-21		+21	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage	G0~G295				42	V
V_{SH1}	Positive Source output voltage	VSH1		+2.4	+15	+18	V
dV_{SH1}	VSH1 output voltage deviation	VSH1	From 2.4V to 8.8V	-100		100	mV
			From 8.8V to 18V	-200		200	mV
V_{SH2}	Positive Source output voltage	VSH2		+2.4	+5	+18	V
dV_{SH2}	VSH2 output voltage deviation	VSH2	From 2.4V to 8.8V	-100		100	mV
			From 8.8V to 18V	-200		200	mV
V_{SL}	Negative Source output voltage	VSL		-18	-15	-9	V
dV_{SL}	VSL output voltage deviation	VSL		-200		200	mV
V_{IH}	High level input voltage	SDA, SCL, CS#, D/C#, RES#, BS[2:1], M/S#, EXTVDD, CL		0.8V_{DDIO}			V
V_{IL}	Low level input voltage					0.2V_{DDIO}	V
V_{OH}	High level output voltage	SDA, BUSY, CL	IOH = -100uA	0.9V_{DDIO}			V
V_{OL}	Low level output voltage		IOL = 100uA			0.1V_{DDIO}	V
V_{PP}	OTP Program voltage	VPP		7.25	7.5	7.75	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
Idslp_VCI	Deep Sleep mode current	VCI	VCI=3.7V DC/DC OFF No clock No output load No MCU interface access Ram data retain only and cannot access the RAM.		1		uA
Islp_VCI	Sleep mode current	VCI	VCI=3.7V DC/DC OFF No clock No output load MCU interface access Ram data retain		20		uA
Iopr_VCI	Operating Mode current	VCI	VCI=3.0V		1000		uA
V_{GH}	Operating Mode Output Voltage	VGH	Enable Clock and Analog by Master Activation Command VGH=21V VGL=-VGH VSH1=15V VSH2=5V VSL=-15V VCOM = -2V No waveform transitions. No loading. No RAM read/write No OTP read /write	20.5	21	21.5	V
V_{SH1}		VSH1		14.8	15	15.2	V
V_{SH2}		VSH2		4.9	5	5.1	V
V_{SL}		VSL		-15.2	-15	-14.8	V
V_{COM}		VCOM		-2.2	-2	-1.8	V

Table 11-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVGH	VGH current	VGH = 21V	VGH			200	uA
IVGL	VGL current	VGL = -VGH	VGL			300	uA
IVSH	VSH1 current	VSH1 = +15V	VSH1			800	uA
IVSH1	VSH2 current	VSH2 = +5V	VSH2			800	uA
IVSL	VSL current	VSL = -15V	VSL			800	uA
IVCOM	VCOM current	VCOM = -2V	VCOM			100	uA

12 AC Characteristics

12.1 Oscillator frequency

The following specifications apply for: VSS=0V, VDD=1.8V, T_{OPR}=25ºC.

Table 12-1: Oscillator Frequency

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.2 to 3.7V	CL	0.95	1	1.05	MHz

12.2 Serial Peripheral Interface

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, $\mathbf{T_{OPR}}$ = 25°C, CL=20pF

Table 12-2 : Serial Peripheral Interface Timing Characteristics

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Write Mode)			20	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	20			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	20			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	25			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
t_{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t_{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Read Mode)			2.5	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	180			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
t_{SOSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t_{SOHLD}	Time SO (SDA Read Mode) will remain stable after the rising edge of SCL		70		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

Figure 12-1: SPI timing diagram

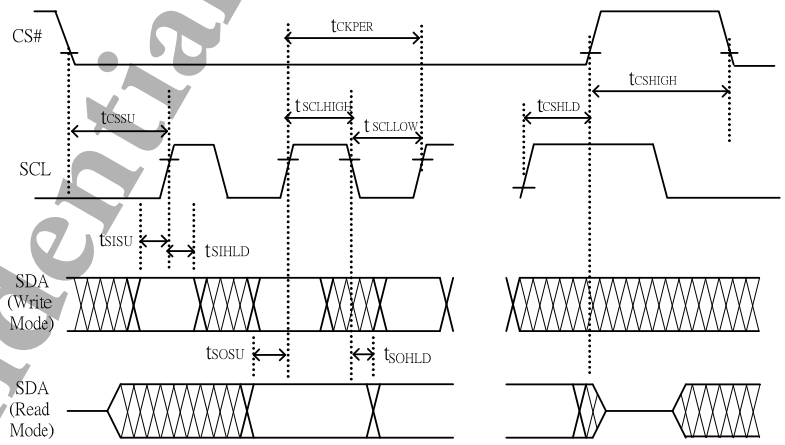


Figure 12-2 : Serial peripheral interface characteristics

12.3 I2C Interface Timing Characteristic

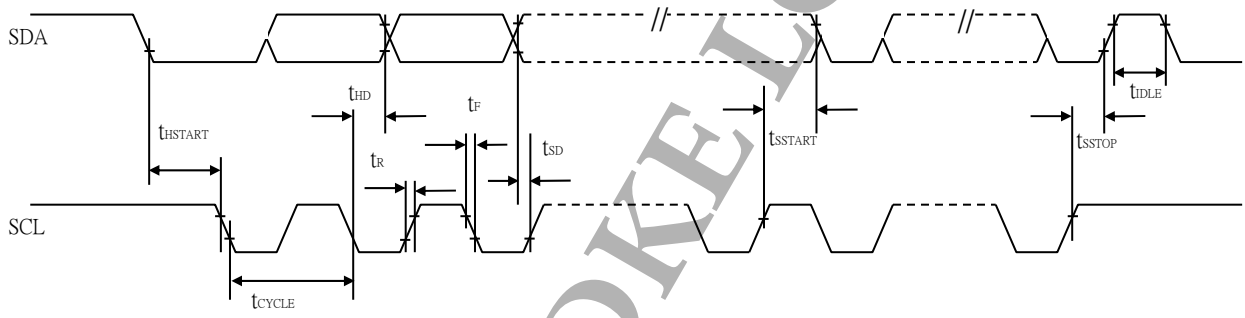
The following specifications apply for:V_{DDIO} - V_{SS} = 2.2V to 3.7V, T_{OPR} = 25°C, C_L=20pF

Table 12-3 : I²C Interface timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.8	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{SD}	Data Setup Time	400	-	-	ns
t_{HD}	Data Hold Time	300	-	-	ns
t_{SSTOP}	Stop condition Setup Time	0.8	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Note: All timings are based on 20% to 80% of VDDIO-VSS

Figure 12-3 : I²C interface timing diagram



The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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