EPD Module User Manual

DEPG0154BNS75AF0

Specification for 1.54 inch EPD

Model NO. : DEPG0154BNS75AF0

DKE's Confirmation:

Prepared by	Checked by	Approved by

Customer approval:

Customer	Approved by	Date

Revision History

Version	Content	Date	Producer
1.0	New release	2017/03/08	
2.0	Part number change from DEPG0154B06 to DEPG0154BNS75AF0	2017/06/07	

CONTENTS

1. Over View

DEPG0154BNS75AF0 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The 1.54inch active area contains 152×152 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

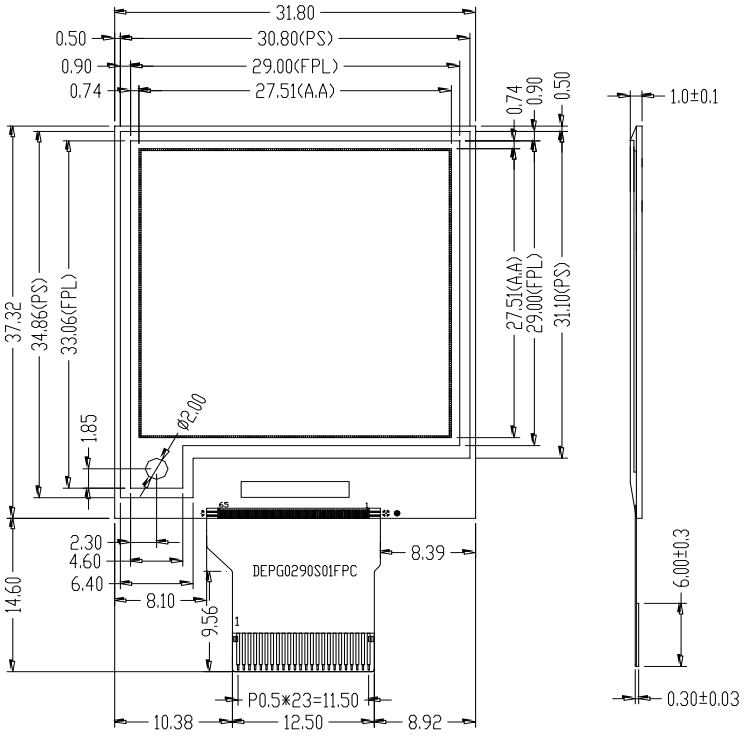
- ◆152×152 pixels display
- ◆High contrast High reflectance
- ◆Ultra wide viewing angle Ultra low power consumption
- ◆Pure reflective mode
- ◆Bi-stable display
- ◆Commercial temperature range
- ◆Landscape portrait modes
- ◆Hard-coat antiglare display surface
- ◆Ultra Low current deep sleep mode
- ◆On chip display RAM
- ◆Waveform can stored in On-chip OTP or written by MCU
- ◆Serial peripheral interface available
- ◆On-chip oscillator
- ◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆I^2C signal master interface to read external temperature sensor
- ◆Support partial update mode
- ◆Built-in temperature sensor

3. Mechanical Specification

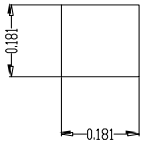
Parameter	Specifications	Unit	Remark
Screen Size	1.54	Inch	
Display Resolution	152(H)×152(V)	Pixel	DPI:140
Active Area	27.512×27.512	mm	
Pixel Pitch	0.181×0.181	mm	
Pixel Configuration	Square		
Outline Dimension	31.8(H)×37.3 (V) ×1.05(D)	mm	
Weight	2.18±0.5	g	

4.Mechanical Drawing of EPD Module

DATE	REV.	MODIFICATION
2017-06-14	A	FIRST ISSUE



PIN	SIGNAL
1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	TSCL
7	TDA
8	BS1
9	BUSY
10	RES#
11	D/C#
12	CS#
13	SCL
14	SDA
15	VDDIO
16	VCI
17	VSS
18	VDD
19	VPP
20	VSH1
21	VGH
22	VSL
23	VGL
24	VCOM



Pixel Pitch

NOTE

1 DISPLAY MODE 1.54″ ARREY FOR EPD
2 RESOLUTION:152gate*152source
3 PIXEL SIZE: 0.181mm* 0.181 mm
4 Unspecified Tolerance:±0.2mm

DESIGN MODEL		DEPG0154	
VAR.	A	DATE	2017.06.14
CUSTOMER MODEL		APPROVED BY	SY ZHAO
		CHECKED BY	BZ HOU
PAGE 1/1		DRAWN BY	PP SUN

5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	NC	Positive Source driving voltage	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, /O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +50	℃.
Storage Temp range	TSTG	-25 to+70	℃.

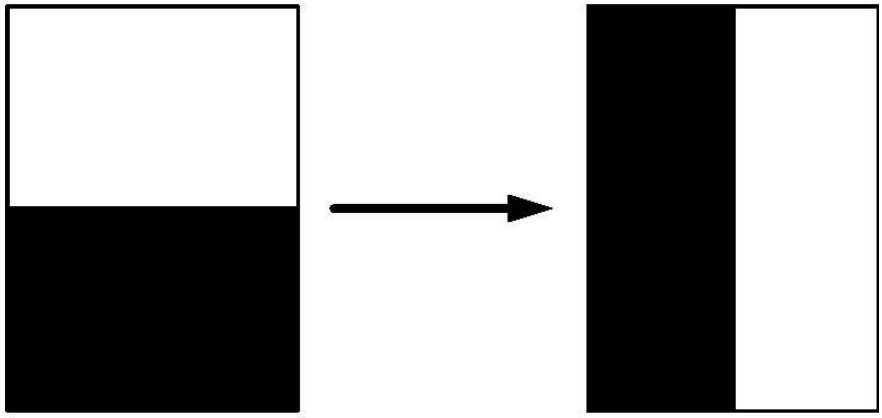
Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25℃.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.2	3.0	3.7	V
Core logic voltage	V_{DD}		VDD	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{CI}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{CI}	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	5.1	6	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_V_{CI}	V_{CI} =3.0V	-	-	1.7	2	mA
Image update time	-	25 ℃	-	-	3	5	sec
Sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by DKE.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25℃.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-2.5	-2	-1.5	V
Positive Source output voltage	V_{SH}	-	S_0~S_{151}	+14.5	+15	+15.5	V
Negative Source output voltage	V_{SL}	-	S_0~S_{151}	-15.5	-15	-14.5	V
Positive gate output voltage	Vgh	-	G_0~G_{151}	+21	+22	+23	V
Negative gate output voltage	Vgl	-	G_0~G_{151}	-21	-20	-19	V

6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

6.4.2 MCU Serial Interface (4-wire SPI)

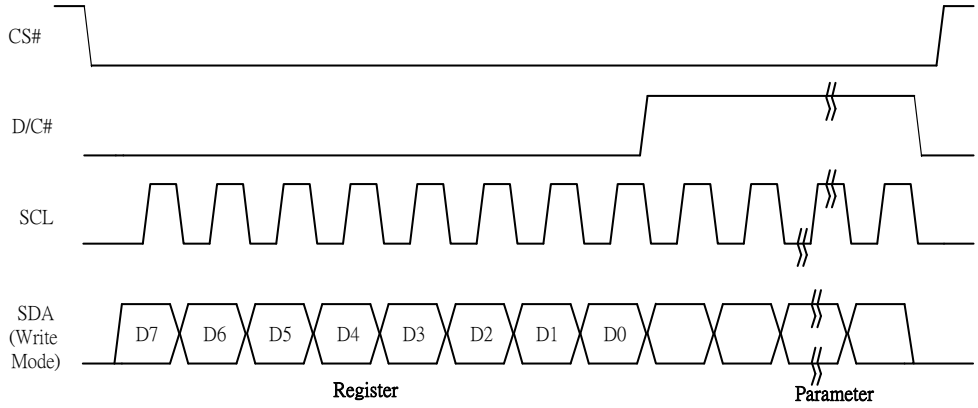
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte . The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

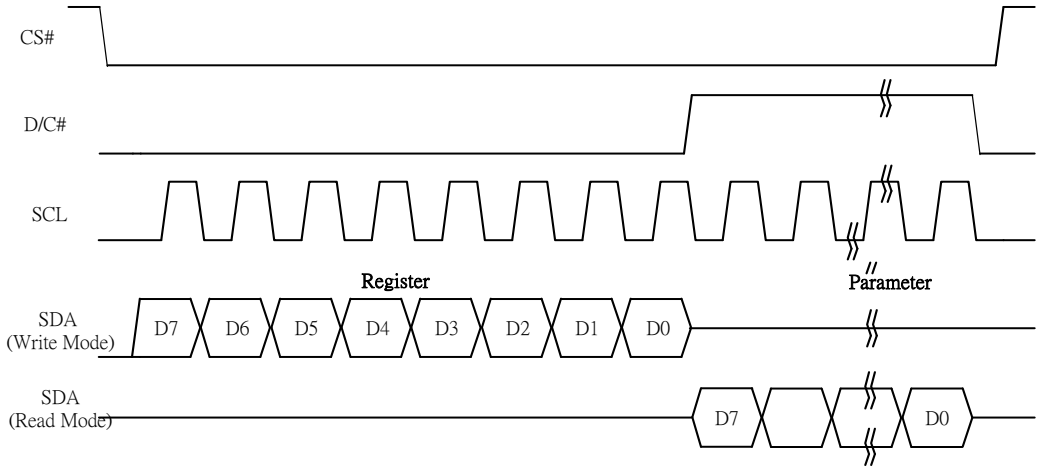
Figure 6-1: Write procedure in 4-wire SPI mode



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode



6.4.3 MCU Serial Interface (3-wire SPI)

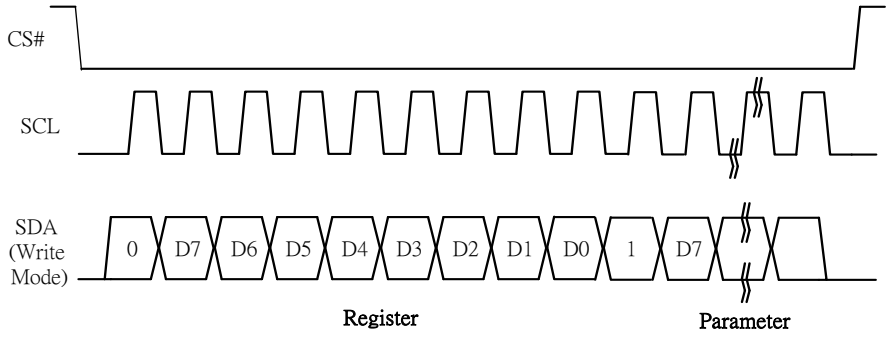
The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

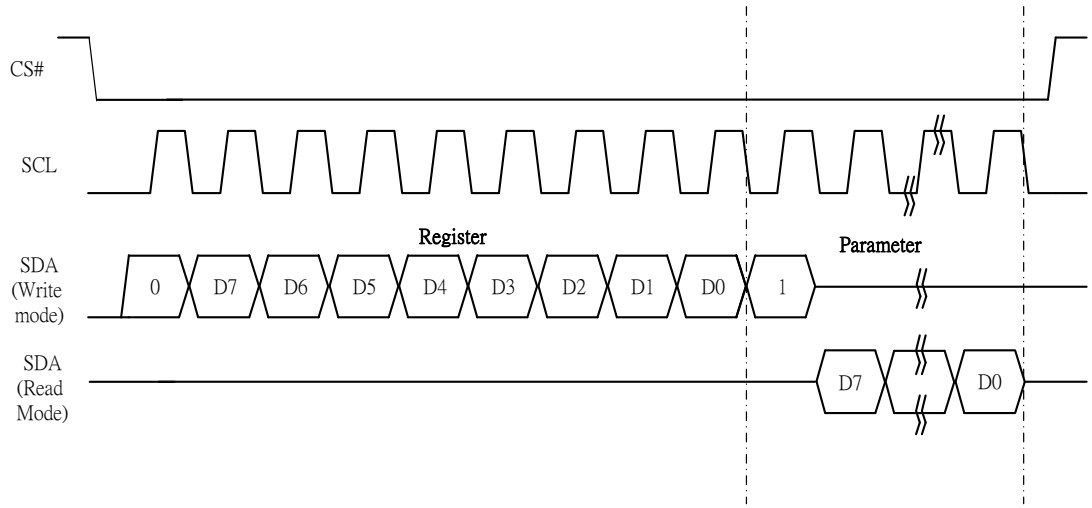
Figure 6-3: Write procedure in 3-wire SPI mode



In the Read mode:

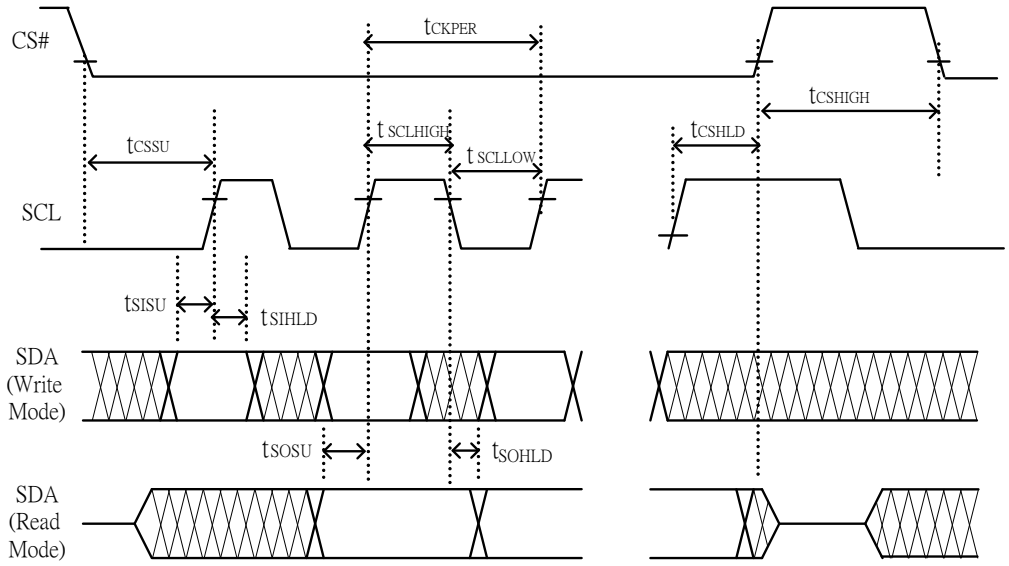
1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode



6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25℃.



Changed Diagram

Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 25℃, CL=20pF)

Write mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the rising edge of SCL		70		ns

7.Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output control</td><td rowspan="4">Gate setting
Set A[8:0]=0097h
Set B[8:0]=00h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate Driving voltage control</td><td rowspan="2">SetGate Driving voltage
A[4:0]=17h[POR],VGH at 20V[POR]
VGH setting from 10V to 21V</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Source Driving voltage control</td><td rowspan="4">SetSource Driving voltage
A[7:0]= 41h[POR],VSH1 at 15V
B[7:0]=00h[POR],VSH2 at 0V
C[7:0]= 32h[POR], VSL at -15V</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td><td>C0</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Deep Sleep mode</td><td>Deep Sleep mode Control
<table><tr><td>A[0] :</td><td>Description</td></tr><tr><td>0</td><td>Normal Mode [POR]</td></tr><tr><td>1</td><td>Enter Deep Sleep Mode</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_0</td><td></td></tr>
<tr><td>0</td><td>0</td><td>11</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Data Entry mode setting</td><td rowspan="2">Define data entry sequence
A [1:0] = ID[1:0]Address automatic increment / decrement setting
The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.
00 –Y decrement, X decrement,
01 –Y decrement, X increment,
10 –Y increment, X decrement,
11 –Y increment, X increment [POR]
A[2] = AM
Set the direction in which the address counter is updated automatically after data are written to the RAM.
AM= 0, the address counter is updated in the X direction. [POR]
AM = 1, the address counter is updated in the Y direction.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>SWRESET</td><td>It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode
Note: RAM are unaffected by this command.</td></tr>
<tr><td>0</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Temperature Sensor Control</td><td rowspan="2">Temperature Sensor Selection
A[7:0] = 48h [POR], external temperature sensor
A[7:0] = 80h Internal temperature sensor</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

<table>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Temperature Sensor Control (Write to temperature register)</td><td>Write to temperature register.
A[7:0] – MS Byte 01111111[POR]
B[7:0] – LS Byte 11110000[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence
The Display Update Sequence Option is located at R22h
User should not interrupt this operation to avoid corruption of panel images.</td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Display Update Control 1</td><td>RAM content option for Display Update
BW RAM option
A[7:4]=0100 (For BW)

A[3:0]=0000[POR] Normal

A[3:0]=0100
Bypass RAM content as 0

A[3:0]=0100
Inverse RAM content</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Display Update Control 2</td><td>Display Update Sequence Option:
Enable the stage for Master Activation
Setting for LUT from MCU
Enable Clock Signal,
Then Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC — C7
Setting for LUT from OTP according to external Temperature Sensor operation
Then Enable Analog
Then Load LUT — 90
Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC — 47</td></tr>
<tr><td></td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>WriteRAM1</td><td>After this command, data entries will be written into the 1RAM until another command is written. Address pointers will advance accordingly.
For Write pixel:
Content of write RAM(BW)=1
For Black pixel:
Content of write RAM(BW)=0</td></tr>
</table>

0	0	26	0	0	1	0	0	1	1	0	WriteRAM2	After this command, data entries will be written into the 2 RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of write RAM(BW)=1 For Black pixel: Content of write RAM(BW)=0
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Set A[7:0]=52h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read	Read Register stored in OTP: 1. A[7:0]~ B[7:0]: VCOM Information 3. C[7:0]~F[7:0]: Reserved 4. G[7:0]~H[7:0]: Module ID/ Waveform Version [2bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x21] A[5]: HV Ready Detection flag [POR=1] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A5	A4	0	0	A1	A0		
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [70 bytes].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		

<table>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Set dummy line period</td><td>Set A[6:0]=11h
Default value will give 50Hz Frame frequency</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Set Gate line width</td><td>Set A[3:0]=0Dh
Default value will give 50Hz Frame frequency</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Border Waveform Control</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td></td><td>Select border waveform for VBD
A [7:6] Select VBD
<table>
<tr><td>A[7:6]</td><td>Select VBD as</td></tr>
<tr><td>00[POR]</td><td>GS Transition
Define A[1:0]</td></tr>
<tr><td>01</td><td>Fix Level
Define A [5:4]</td></tr>
<tr><td>10</td><td>VCOM</td></tr>
<tr><td>11</td><td>HIZ</td></tr>
</table>
A [5:4] Fix Level Setting for VBD
<table>
<tr><td>A[5:4]</td><td>VBD level</td></tr>
<tr><td>00[POR]</td><td>VSS</td></tr>
<tr><td>01</td><td>VSH1</td></tr>
<tr><td>10</td><td>VSL</td></tr>
<tr><td>11</td><td>VSH2</td></tr>
</table>
A[1:0]) BW Transition setting for VBD
<table>
<tr><td>A[1:0]</td><td>VBD Transition</td></tr>
<tr><td>00 [POR]</td><td>LUT0</td></tr>
<tr><td>01</td><td>LUT1</td></tr>
<tr><td>10</td><td>LUT2</td></tr>
<tr><td>11</td><td>LUT3</td></tr>
</table></td></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Set RAM X - address Start / End position</td><td>Specify the start/end positions of the window address in the X direction by an address unit
A[4:0]: XSA[4:0], X Start, POR = 00h
B[4:0]: XEA[4:0], X End, POR = 12h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Set Ram Y-address Start / End position</td><td>Specify the start/end positions of the window address in the Y direction by an address unit
A[8:0]: YSA[8:0], Y Start, POR = 0097h
B[8:0]: YEA[8:0], Y End, POR = 0000h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_8</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_8</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>4E</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Set RAM X address counter</td><td>Make initial settings for the RAM X address in the address counter (AC)
A[4:0]: XAD[4:0], POR is 00h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>4F</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Set RAM Y address counter</td><td>Make initial settings for the RAM Y address in the address counter (AC)
A[8:0]: YAD8:0], POR is 0097h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_8</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>74</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Set Analog Block control</td><td>A[7:0] = 54h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>7E</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Set Digital Block control</td><td>A[7:0] = 3Bh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
</table>

8. Optical Specification

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	indoor	8:1		-		8-2
Gn	2Grey Level	-	-	DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 25 ℃	-	3	-	sec	
Life		0℃~50℃		1000000times or 5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3 WS: White state, DS: Dark state

9. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

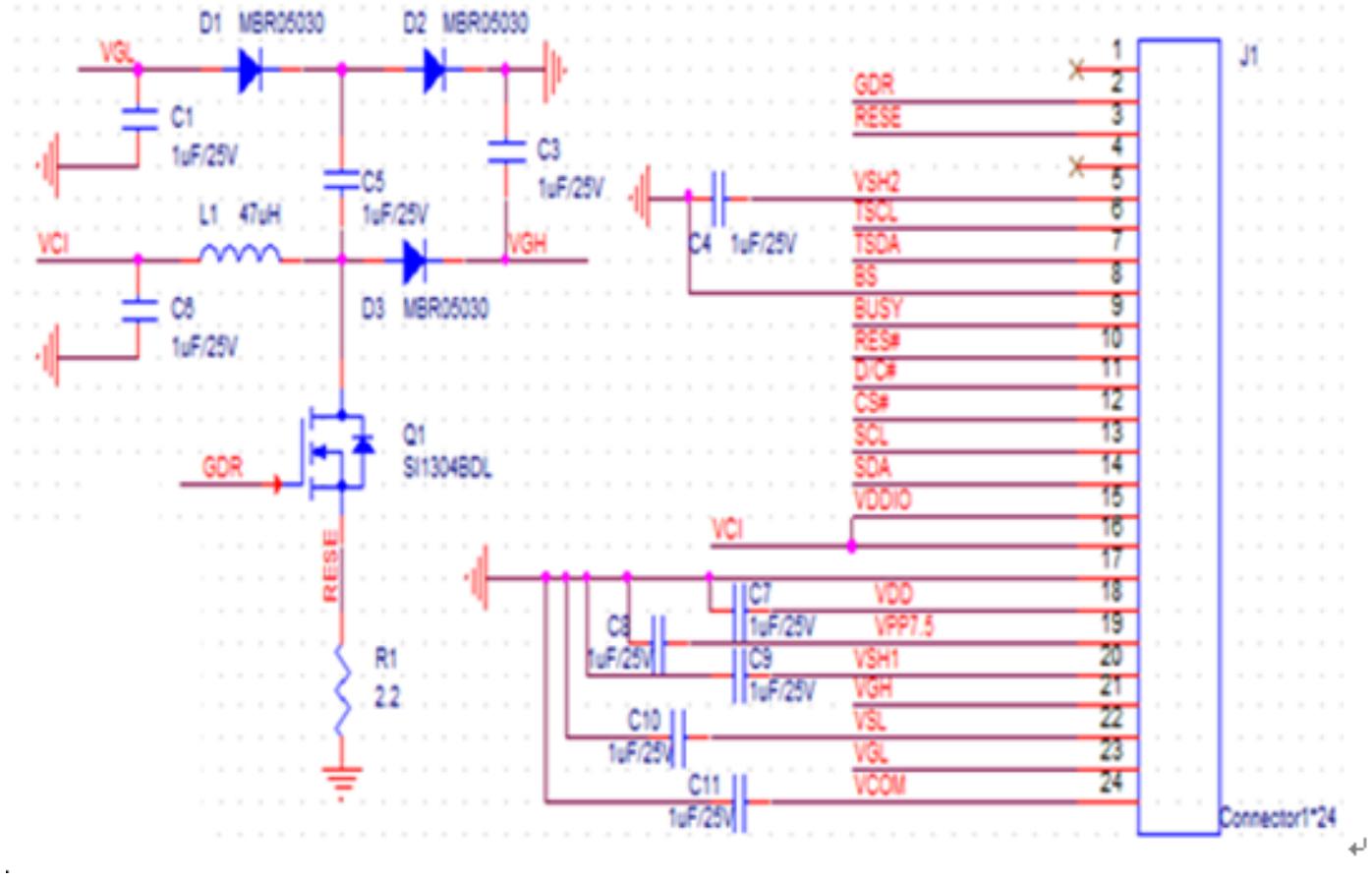
10. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25℃, 240 h Test in white pattern
2	High-Temperature Storage	T = +70℃, RH=40% ,240h T=+60℃, RH=26%,240h Test in white pattern
3	High-Temperature Operation	T = +50℃, RH = 30% ,240h
4	Low-Temperature Operation	0℃，240h
5	High-Temperature, High-Humidity Operation	T=+40℃，RH=90%,168h
6	High Temperature, High Humidity Storage	T=+60℃，RH=80%,240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25℃ 30min]→[+70 ℃ 30 min] : 100 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 ℃ Test in white pattern
9	ESD Gun	Air+/-8KV;Contact+/-6KV (Shoot ESD gun on display area,not including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

11. Block Diagram

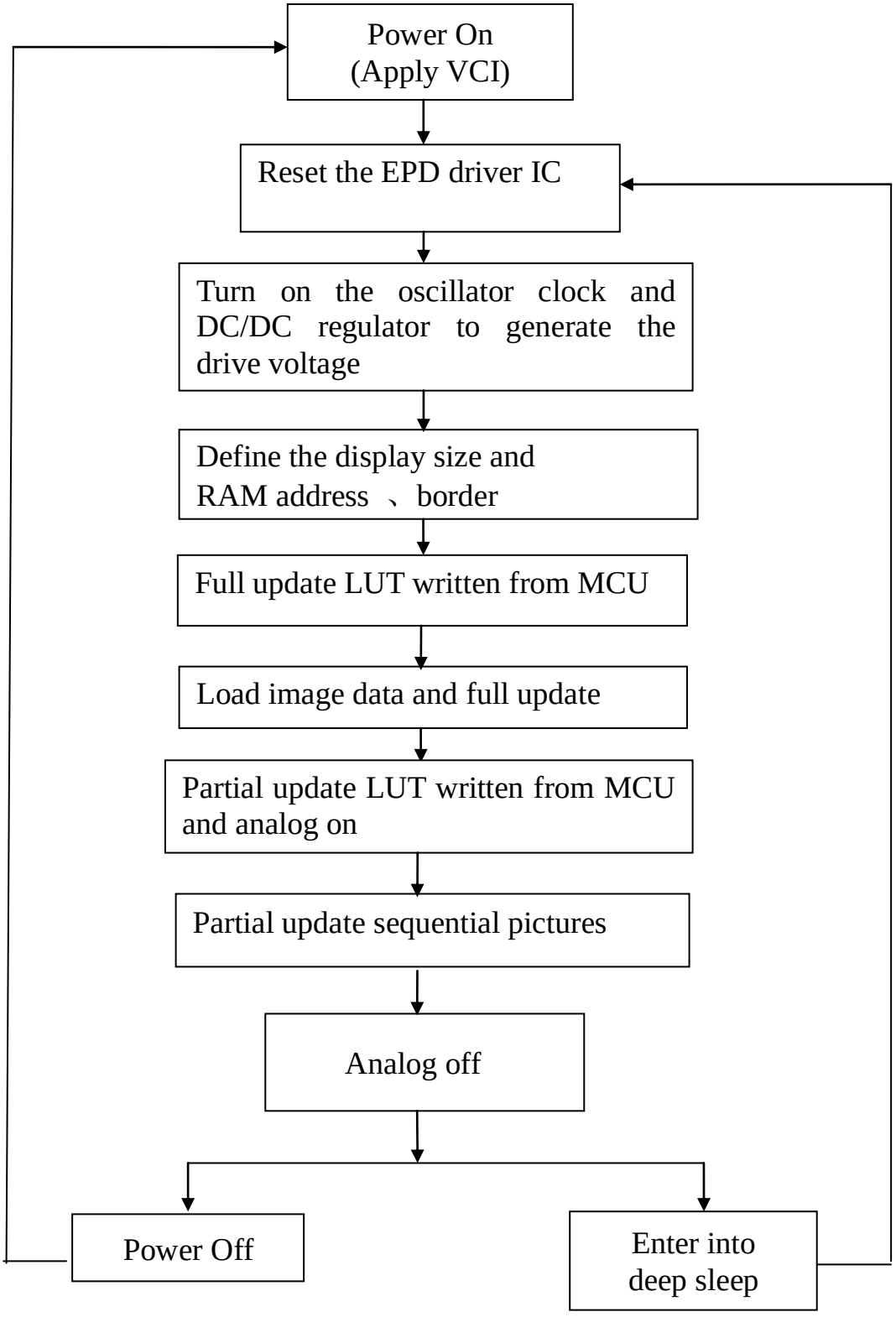
12. Typical Application Circuit with SPI Interface



13 Typical Operating Sequence

13.1Normal Operation Flow

13.2 Partial update Operation Flow



13.3 Normal Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	high	Hardware reset
delay	200us	
RESE#	low	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
Command 0x74	Data 0x54	Set Analog Block Control
Command 0x7E	Data 0x3B	Set Digital Block Control
Command 0x01	Data 0x97 0x00 0x00	Set display size and driver output control
Command 0x11	Data 0x01	Ram data entry mode
Command 0x44	Data 0x00 0x12	Set Ram X address
Command 0x45	Data 0x97 0x00 0x000x00	Set Ram Y address
Command 0x3C	Data 0x01	Set border
SET VOLTAGE AND LOAD LUT		
Command 0x2C	Data 0x52	Set VCOM value
Command 0x03	Data 0x17	Gate voltage setting
Command 0x04	Data 0x41 0x00 0x32	Source voltage setting
Command 0x3A	Data 0x11	Frame setting 50hz
Command 0x3B	Data 0x0D	
Command 0x32	Write 70bytes LUT	Load LUT
LOAD IMAGE AND UPDATE		
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x97 0x00	Set Ram Y address counter
Command 0x24	2888bytes	Load image (152/8*152)
Command 0x22	Data 0XC7	Image update
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

13.4 Partial update Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	high	Hardware reset
delay	200us	
RESE#	low	
delay	200us	
Read busy pin	Wait for busy low	
Command 0x12		Software reset
Read busy pin	Wait for busy low	
Command 0x74	Data 0x54	Set Analog Block Control
Command 0x7E	Data 0x3B	Set Digital Block Control
Command 0x01	Data 0x97 0x00 0x00	Set display size and driver output control
Command 0x11	Data 0x01	Ram data entry mode
Command 0x44	Data 0x00 0x12	Set Ram X address
Command 0x45	Data 0x97 0x00 0x000x00	Set Ram Y address
Command 0x3C	Data 0x01	Set border
SET VOLTAGE AND LOAD LUT		
Command 0x2C	Data 0x52	Set VCOM value
Command 0x03	Data 0x17	Gate voltage setting
Command 0x04	Data 0x41 0x00 0x32	Source voltage setting
Command 0x3A	Data 0x11	Frame setting 50hz
Command 0x3B	Data 0x0D	
Command 0x32	Write 70bytes LUT	Load LUT
LOAD IMAGE AND FULL UPDATE		
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x97 0x00	Set Ram Y address counter
Command 0x24	2888bytes	Load image (152/8*152)
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x97 0x00	Set Ram Y address counter
Command 0x26	2888bytes	Load image (152/8*152)
Command 0x22	Data 0XC7	Image update
Command 0x20		
Read busy pin	Wait for busy low	
LOAD PARITAL UPDATELUT AND ANALOG ON		
Command 0x32	Write 70bytes partial LUT	Load partial LUT
Command 0x37	Data 0x00 0x000x00 0x00 0x40 0x00 0x00	BW New/Old RAM mode for partial update
Command 0x22	Data 0XC0	Analog on
Command 0x20		
Read busy pin	Wait for busy low	
PARTIAL UPDATE SEQUENTIAL PICTURES		
Command 0x44	Data 0xXX 0xXX	Set partial update Ram of picture1
Command 0x45	Data 0xXX 0xXX 0xXX0xXX	
Command 0x4E	Data 0xXX	
Command 0x4F	Data 0xXX 0xXX	
Command 0x24	N bytes	Load partialpicture1datas
Command 0x22	Data 0X0C	partial update

Command 0x20		
Read busy pin	Wait for busy low	
Command 0x44	Data 0xXX 0xXX	Set partial update Ram of picture2
Command 0x45	Data 0xXX 0xXX 0xXX0xXX	
Command 0x4E	Data 0xXX	
Command 0x4F	Data 0xXX 0xXX	
Command 0x24	N bytes	Load partial picture2 data
Command 0x22	Data 0X0C	partial update
Command 0x20		
Read busy pin	Wait for busy low	
:	:	:
:	:	:
Command 0x44	Data 0xXX 0xXX	Set partial update Ram of picture N
Command 0x45	Data 0xXX 0xXX 0xXX0xXX	
Command 0x4E	Data 0xXX	
Command 0x4F	Data 0xXX 0xXX	
Command 0x24	N bytes	Load partial picture N data
Command 0x22	Data 0X0C	partial update
Command 0x20		
Read busy pin	Wait for busy low	
ANALOG OFF		
Command 0x22	Data 0X03	Analog off
Command 0x20		
Read busy pin	Wait for busy low	
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

Note：During partial update the IC should not enter deep sleep mode.

14. Part Number Definition

DEPG0154BNS75AF0
1 2 3 4 5 6 7

1: DEP:DKE product

2: G:Dot matrix type

3: The E-paper size:1.54inch:0154

4: The color of E-paper:

B : Black/White R: Black/White/Red Y: Black/White/Yellow

5: OT range: N: Normal L: Low temperature H: High temperature

6: Driver type

7: FPC type

15. Inspection condition

15.1 Environment

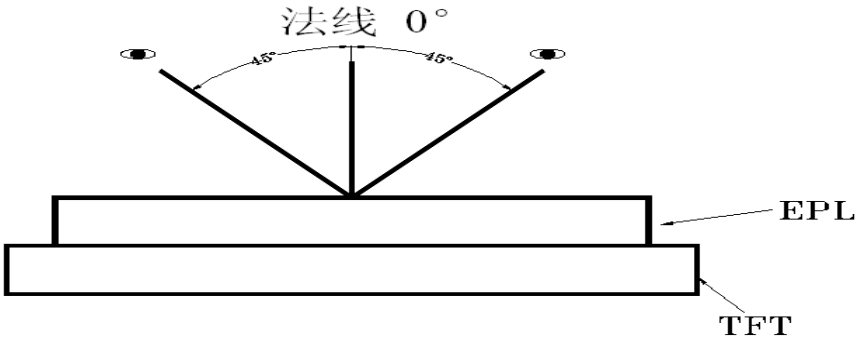
Temperature： 25±3℃

Humidity： 55±10%RH

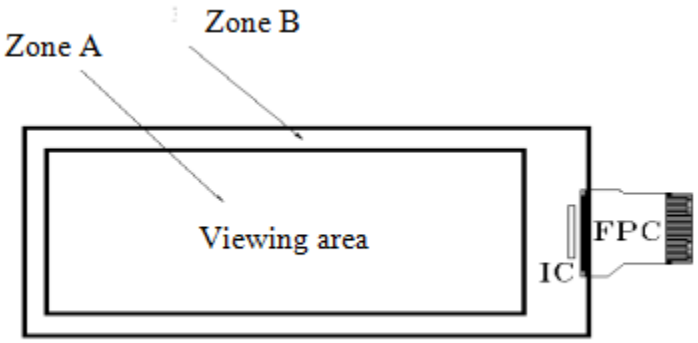
15.2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 30°surround.

15.3 Inspect method

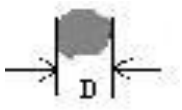
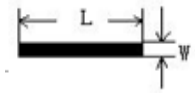


15.4 Display area

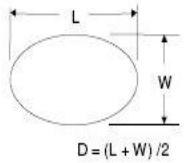
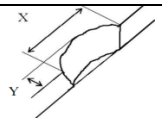
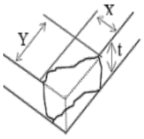
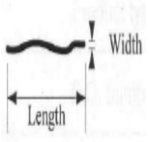
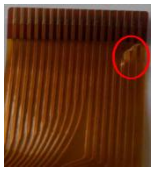


15.5 Inspection standard

15.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm。N≤3， and Distance≥5mm 0.4mm＜D Not Allow	MI		
3	Black/White spots (No switch)	 L≤0.6mm，W≤0.2mm，N≤1 L≤2.0mm,W＞0.2mm，Not Allow L＞0.6mm， Not Allow		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash spots/ Larger FPL size	Flash spots in switching, Allowed FPL size larger than viewing area, Allowed.	MI	Visual/ Inspection card	Zone A Zone B
6	Display wrong/Missing	All appointed displays are showed correct	MA	Visual inspection	Zone A
6	Short circuit/ Circuit break/ Display abnormal	Not Allow			

15.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm，N≤3 D＞0.4mm，Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm  2mm≤X or 2mm≤Y Allow  W≤0.1mm,L≤5mm, n≤ 2 Edge crown：X≤0.3mm，Y≤3mm	MI	Visual / Microscope	Zone A Zone B
5	Substrate color difference	Allowed			
6	FPC broken/ Goldfingers xidation/ scratch	  Not Allow	MA	Visual / Microscope	Zone B

7	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
8	Edge Adhesives height/FPL/ Edge adhesives bubble	Edge Adhesives height ≤ Display surface Edge adhesives seep in≤1/2 Margin width FPL tolerance ±0.3mm Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤3			
9	Protect film	Surface scratch but not effect protect function, Allow		Visual Inspection	

16.Packaging

EPD PACKING INSTRUCTION

DKE-QS. D-010

DATE	2016.11.30
DESIGN	
CHECKED	
APPROVED	

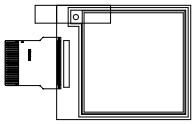
P/N	Customer Code	Ref.P/N
DEPG0154		

Type	PKG Method	Printing	Surface Marks	Pull Tape	Bar.Code
GLASS	Blister	BACK	None	YES	None

Marks instruction：

print on the back of the product
Contents：model+Lot#

Pull tape：



Packing Materials List

List	Model	Materials	Q'ty	Unit
Carton	7#	corrugate	1	Piece
BOX	7#(INNER)	corrugate	2	Piece
Blister	DEPG0154	PET	22	Piece
Thin foam	298.4*273.9*T1.8-2.0	EPE	20	Piece
Vaccum bag	430.0*590.0*0.075		2	Piece
Foam board	DKE2251-10	EPE	4	Piece

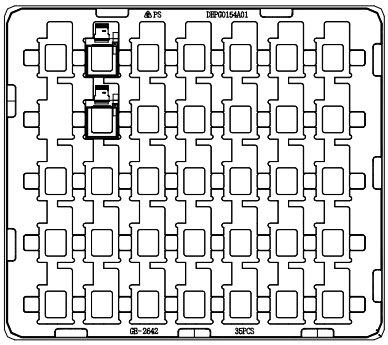
35PCS/LAYER,2 INNER BOX/CTN,TOTAL 700PCS/CTN.

Barcode Instruction：

Detail：

Blister box:

NOTE:
TOTAL 10 LAYERS PER INNER BOX WITH ONE MORE EMPTY BLISTER ON THE TOP OF THE PRODUCTS.



Quantity：5*7=35PCS