A Digital Readout Technique for Capacitive Sensor Applications

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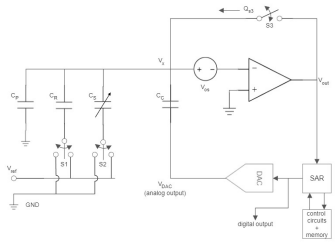
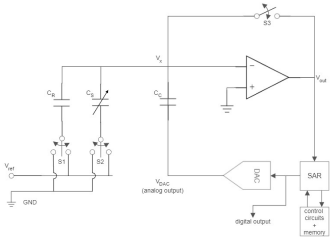
Introduction

In this article, a technique for capacitance measurement is discussed, based on the work of Kung et al.[1]. The technique is an particular implementation of the charge redistribution method [2].

The presented approach gives a digital output, that could be converted to analog by a DAC(*Digital to Analog Converter*) for further processings. This technique allows to reach high measurment resolution since it deletes errors due to: Parasitic capacitances, op-amp offset or charge injection from MOS switch. In figure Fig. 1a is showed the circuit that performs the described functions.



(a) Capacitance measurement circuit.



(b) Capacitance measurement circuit without nonidealities.

Ideal Analysis

A first analysis is performed assuming an ideal circuit, so there is no charge injection ($Q_{s3} = 0$), no parasitic capacitance ($C_P = 0$) and ideal op-amp (offset $V_{os} = 0$ and ∞ gain). The circuit becomes as showed in figure Fig. 1b.

Step 1: S3 closed, S1 to V_{ref} and S2 to GND

In this step the op-amp is in a buffer configuration, so $V_x = 0 = V_{out}$ for the virtual ground. The lower terminal con C_R is set to V_{ref} so there is a charge $Q_1 = -C_R V_{ref}$ in the upper terminal of C_R, that is V_x.

Step 2: S3 opened, S1 to GND and S2 to V_{ref}

In this step the feedback is only throught the branch of the SAR and DAC. Assuming the components ideal then there is again e negative feedback that sets $V_x = 0$. Similarly at the previous case, there is a charge $Q_2 = -C_S V_{ref} - C_C V_{DAC}$ in the upper terminal of C_S. The presence of V_{DAC} is due to the fact that there isn't a buffer configuration anymore but charging amplifier.

Now, since the charge must be conserved it holds that $Q_1 = Q_2$ that leads to $V_{DAC} = \frac{V_{ref}(C_R - C_S)}{C_C}$.

So this circuit produces a voltage proportional to the difference of C_R *and* C_S. V_{ref}, C_C can be choosen to exploit at best the range of the DAC.

The circuit can be used either in a open-loop (without the feedback throught S3) or close-loop configuration. As expectable the second one offers more advantages in terms of voltage offset compensation. So this configuration will be anaylized in detail.

Non Ideal Analysis

When nonidealities are taken into account the circuit looks like in figure Fig. 1a. The main effects analyzed are the ones due to $V_{os} \neq 0$, finite op-amp gain A, charge injection by S3 when opened, parasitic capacitances to ground C_P and the quatization error of the DAC $\epsilon = \pm\frac{1}{2}LSB$.

Quantization Error & Voltage Offset

Applying the super position principle is possible to find that the presence of quatization error and voltage offset of the op-amp leads to $V_x = V_{os} \pm \frac{1}{2} LSB(\frac{C_C}{C_{total}})$ when S3 is opened and to $V_x = V_{os}$ when S3 is closed.¡, with $C_{total} = C_P + C_C + C_R + C_S$. $\frac{C_C}{C_{total}}$ is capacitive divider, so errors in V_{DAC}, in the worst case, could accumulate.

Charge Injection

This is an important effect to take into account since it affects the charge conservation assumption made in the first analysis.

To mitigate this problem, a calibration phase is done, where the injected charge is measured to be canceled. After calibration, the measurment steps come as in the ideal analysis. Calibration and measurement phases inherently eliminate the op-amp offset with the closed-loop configuration, while for the open-loop this should be done separately and could lead to problems when V_{os} is so large that the calibration voltage is greater than the DAC maximum voltage.

The calibration is done by setting S1 to V_{ref}, S2 and V_{DAC} to GND. Now S3 is opened to measure the charge injected Q_{s3}, so the coupling capacitor C_C will store this charge Q_{s3}. The calibration voltage in output of the DAC is:

$$V_{DAC_{cal}} = -\frac{Q_{s3}}{C_C} \pm 2\Delta V, \ \textit{where} \ \pm \Delta V \ \textit{is the quantization error.}$$

This voltage can be now stored in a RAM. By applying $-V_{DAC_{cal}}$ to C_C the voltage error due to charge injection can be canceled. An other approach would be to think about the DAC as generating a charge on C_C to compensate the injected one.

The measurement cycle is the same described previously except that V_{DAC} is set to $V_{DAC_{cal}}$. At the end of this cycle the output is

$$V_{DAC_{meas}} = \frac{V_{ref}(C_R - C_S)}{C_C} \pm 4\Delta V$$

that is again the same, except of the term $\pm 4\Delta V$ given by the quantization error.

The expression for capacitance mismatch ratio is given by

$$\frac{\Delta C}{C} = \frac{V_{DAC_{meas}}}{V_{ref}} \frac{C_C}{C} \pm \frac{4\Delta V}{V_{ref}} \frac{C_C}{C}$$

where $\Delta C = C_R - C_S$ and C is any normalizing capacitance that could be C_R by instance.

The error term $\pm \frac{4\Delta V}{V_{ref}} \frac{C_C}{C}$ rappresents the limit of detection for capacitance change, that can be reduced by icreasing V_{ref}, if possible, or reducing C_C, being careful to relative changes in δ.

Parasitic Capacitance

For this system, large parasitic capacitances has a double effect:

1. Large C_P affects the ratio $\delta = \frac{C_C}{C_{total}}$. A small δ would impede the DAC from adjusting V_x, since it would be affected mainly by the large value of C_P. The DAC has a minimum ammount of control that is $\delta(\pm\Delta V)$. If this ammount is smaller than the comparator resolution, the error term $\pm\Delta V$ becomes limited by δ and not from the quantization error anymore. This is something unwanted because increasing the DAC performances wouldn't give any significant improvement.

2. Large C_P reduces the noise term $\frac{kT}{C}$.

This leads to a trade-off on C_P that must be evaluated for the specific application and performances requirements. Parastic capacitances effects can be mitigated with specific methods, e.g. *Bootstrapping* if there is an electrical access. Another option is to use a comparator with higher resolution, to avoid absence of control by the DAC.

Other Nonidealities

When a MOS switch is used, a source of error is the reverse leakage current when the switch is open, that introduces extra charge. This effects becomes significant at low clock frequency since there would be more time to transfer charges. If the clock frequency is slow enought it's possible to measure the extra charge injected using the presented technique.

Another source of error is given by the thermal noise from the MOS switch when is opened. It's possible to reduce it by increasing the input capacitance, but this would lead to the previous trade-off on C_P. In any case it's not possible to eliminate the noise completely for a single measure, but can be reduced by averaging multiple measures since it's modeled as a random noise with null average.

Conclusions

It has been demonstrated that this technique can measure capacitance differences with a resolution of 0.05 fF on capacitors in the 20-100 fF range, with parasitic capacitances around 100 times larger[1]. The significant nonideal effects can be corrected through calibration. Furthermore, digital averaging can improve resolution, but at the cost of longer measurement times.

This is a simple circuit and inherently compatible with digital signal processing. This makes it hightly suited for capacitance difference measurement in digital systems.

Bibliography

[1] J. T. Kung, H. S. Lee, and R. T. Howe, "A Digital Readout Technique for Capacitive Sensor Applications," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 4, pp. 972–977, 1988.

[2] J. L. McCreary and D. A. Sealer, "Precision capacitor ratio measurement technique for integrated circuit capacitor arrays," *IEEE Transactions on Instrumentation and Measurement*, vol. 28, no. 1, pp. 11–17, 1979.