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Abstract

To reduce the residual direct-current (DC) voltage in liquid-crystal display (LCD) using the polymer-stabilized vertical-alignment (PS-VA) mode, the electrical time constant of two or more serially connected dielectric materials, such as liquid crystals (LCs) and silicon nitride (SiNx), is investigated. PSpice simulation of the alternating-current (AC) voltage changes in the two dielectric materials shows mismatch of the time constant, and a resistance cross capacitance (RC) between the two layers is found to be the source of the residual DC voltage. The optimization of the stoichiometry of SiNx is effective for matching the time constant of LCs because it is easy to control the time constant by changing the gas ratio, e.g., SiH4, N2, and NH_3, when SiNx is deposited. We suggest that image sticking in the LCD panel can be minimized via RC optimization between the SiNx and LCs by adjusting the stoichiometry of SiNx, which means that the chronic problem of off-axis gamma distortion in the VA mode for large sized, high-resolution TV up to Quad Ultra High Definition (QUHD, 15360 × 8640) can be solved.

1. Introduction

Image sticking is often encountered in polymer stabilized vertical alignment (PS-VA) LCD displays when new materials are used in the panels for improving the display characteristics, e.g., decreasing the response time and increasing transmittance and viewing angle. It is speculated that image sticking originates from ion impurities of organic materials in color filters, alignment layers, liquid crystals (LCs), and organic black matrix [1].

In particular, in order to make an LCD panel in PS-VA mode, monomers in the liquid crystal are added as shown in figure 1 and UV is irradiated to form a protrusion structure on the surface of the alignment layer to form a Pretilt angle. PS-VA mode may be more vulnerable to image sticking because uncured monomers in liquid crystals can act as impurities. When the direct-current (DC) voltage is applied, the ion impurities tend to move to the electrode, which changes the electric potential and produces luminance variation [2, 3]. Especially in the in-plane switching (IPS) mode or the fringe-field switching (FFS) mode, it is known that the ion adsorption and desorption between LCs and the alignment layer is involved in the generation of flexoelectric polarization and causes flickering when an alternating-current (AC) waveform is applied to pixel and common electrodes [4]. Many researchers have tried to estimate the activation energy of the adsorption and desorption process by measuring the residual DC voltage [5]. Through various measurements, such as capacitance–voltage (CV) hysteresis [6, 7], flicker minimization [2], and the voltage holding ratio and light minimum/maximum method [8], the common-electrode voltage has been optimized to minimize the image sticking [9].

However, for the LCD panel with coupled capacitance (CC) VA mode [10], there exist high and low pixels, where the different pixel electrode voltages are applied and produce image sticking, owing to the residual DC voltage (see figure 2). It has been known that the floating electrode in the low-pixel area is the origin of image sticking, and Huang *et al* proposed a new CC mode called additional refresh technology (ART) [11]. The floating metal was connected to a small thin-film transistor (TFT) in the ART structure to solve the image sticking, but the reason why the floating metal had the residual DC voltage was not explained. Additionally, the image sticking was not improved perfectly according to our verification test.

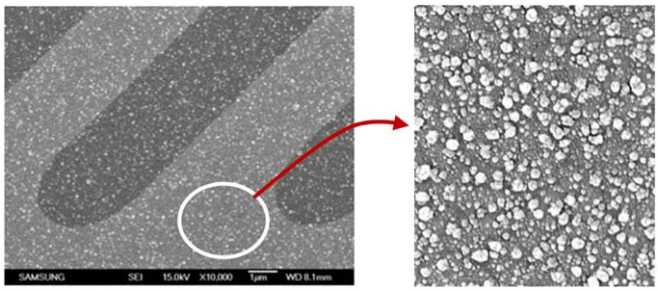

Figure 1. The protrusion structure around the microslit in the PS-VA LCD by UV curing process. This protrusions produces a pretilt angles of the LCs to reduce the response time and increase the transmittance.

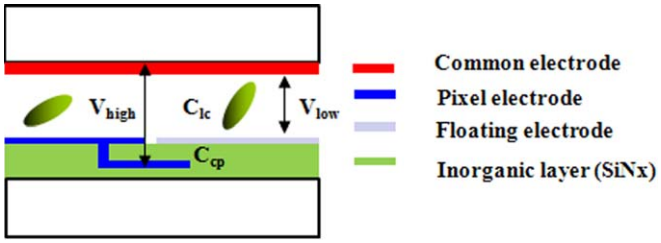

Figure 2. Cross section of the coupled-capacitance VA-mode structure.

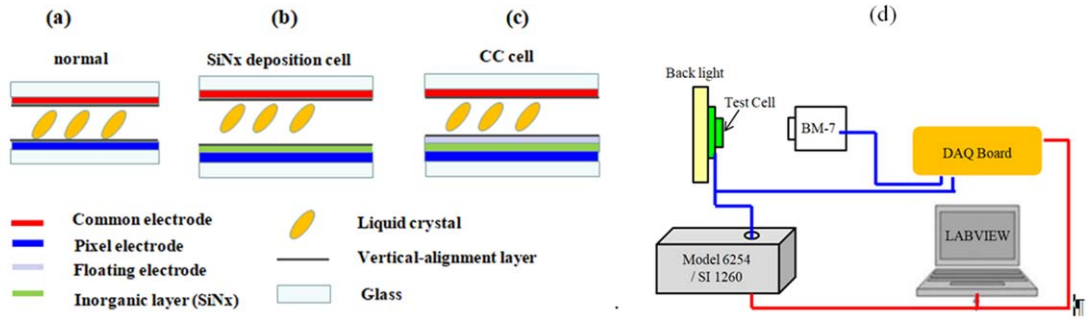

Figure 3. Three kinds of test cells (a) Normal VA mode cell, (b) SiNx deposition cell on the pixel electrode. (c) CC cell which is floated ITO on the SiNx and pixel electrode. (d) Experimental setup schematic diagram.

In this paper, we report that a floating metal in a low pixel of the CC mode has a residual DC voltage, which causes image retention for a long period of time with a fixed image in figure 2. The measured residual DC voltage is defined by the relationship between the time constant of LCs and silicon nitride (SiNx). According to PSpice simulations, the residual DC voltage can occur even under conditions of AC driving and no ion adsorption. These results are new evidence that conventional ion adsorption is the cause of residual DC induced image sticking. By optimizing the SiNx deposition process, we can solve the image sticking problem in the CC mode, making the CC mode a candidate for high-resolution TV up to Quad Ultra High Definition (QUHD, 15360×8640) without reduction of the aperture ratio.

2. Experimental

To evaluate the effect of the floating metal on the residual DC in the CC mode, three test cells are prepared, as shown in figures 3(a)–(c). Figure 3(a) presents the normal cell, which is composed of two electrodes coated by a VA layer of polyimide (JSR Al-60702). The surfaces are rubbed to make them anti-parallel. Negative LCs from Merck ($\Delta\varepsilon = -3.0$, $\Delta n = 0.1$) are injected into the cells, and then the top and bottom glass is sealed with an ultraviolet curable sealant. The cell gaps of all cells are approximately 3 μm. In figure 3(b), a dielectric material,

Table 1. Conditions of a-SiNx deposition process and stress values.

N_2 sccm	NH_3 sccm	SiH_4 sccm	Temperature °C	$[NH_3]/[SiH_4]$ ϒ
1800	500	200	200	2.5
2500	800	200	200	4.0
3200	420	90	200	4.7
3200	600	70	200	8.6
3200	800	50	200	16.0
2000	800	150	200	5.3

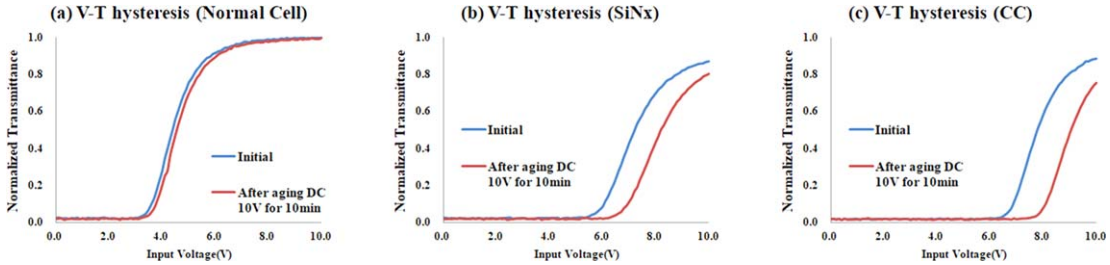

Figure 4. V–T hysteresis graphs for (a) the normal cell, (b) the SiNx-deposition cell, and (c) the CC cell.

SiNx, is deposited on the pixel electrode at 200 °C with the process conditions shown in table 1. The source gases were SiH_4, NH_3, and N_2, and the NH_3/SiH_4 flow ratio Y varied from 2.5 to 16.0. The remainder of the process is the same as that for the normal cell in figure 3(a). In figure 3(c), a floating ITO metal with a thickness of 55 nm is located on the SiNx. For various deposition conditions of a-SiNx and LCs, the voltage holding ratio (VHR) was measured using Model 6254 (TOYO Corporation). The experimental setup diagram is shown in figure 3(d). The time constant (RC) was calculated using the following equation:

$$VHR = e^{-\frac{t}{RC}}, \quad (1)$$

where t, R, and C represent the measurement time, resistance, and capacitance, respectively.

The optical flicker and voltage–transmittance (V–T) hysteresis were measured using BM7 (Topcon) and a 5034B oscilloscope (Tektronix). The capacitance was measured using SI 1260 (Solatron Group Ltd).

3. Results and discussions

3.1. Voltage–transmittance hysteresis

Figures 4(a)–(c) shows the measured V–T hysteresis of the three cells. The transmittance of the cells is measured while the DC voltage applied to the cells is increased from 0 to 10 V. When the applied voltage reaches 10 V, this voltage is applied to the cell for 10 min continuously, and then the applied voltage is reduced from 10 to 0 V. The *y*-axis values are taken as the normalized transmittance, and the graphs were drawn by dividing all transmittances by the transmittance at the initial 10 V of the first normal cell. White luminance of SiNx and CC cells are smaller than normalized cell. This is due to the voltage drop caused by the SiNx layer and the applied voltage of liquid crystals is decreased. According to the V–T hysteresis results, there is large hysteresis in the SiNx-deposited cell (b) and the CC cell (c). This indicates that the floating metal is not the main cause of the residual DC voltage. The reversed curve is shifted to the right because the charged electrons after 10 min at 10 V reduced the electric field. Generally, when a positive DC voltage is applied to a dielectric, the dielectric is polarized in the direction of the electric field. The electric field produced by this polarization is opposite to the direction of the electric field applied from the outside. In this case, the intensity of the total electric field becomes smaller than the initial value, which is said to be the cause of the hysteresis by the charged electron effect. The electric field produced by this polarization is opposite to the direction of the electric field applied from the outside. In this case, the intensity of the total electric field becomes smaller than the initial value, which is called a charged electron effect. As shown in figure 4, the hysteresis values for the normal cell (a), the SiNx-deposited cell (b), and the CC cell (c) are 0.1, 1.1, and 1.2 V, respectively.

To measure the residual DC voltage in the CC cell accurately, we used the flicker-minimizing method in various inorganic materials as a coupled capacitance, and the results are shown in figure 5 [9]. There were three kinds of inorganic dielectric materials: two SiNx samples deposited at 200 °C (low-temperature SiNx) and

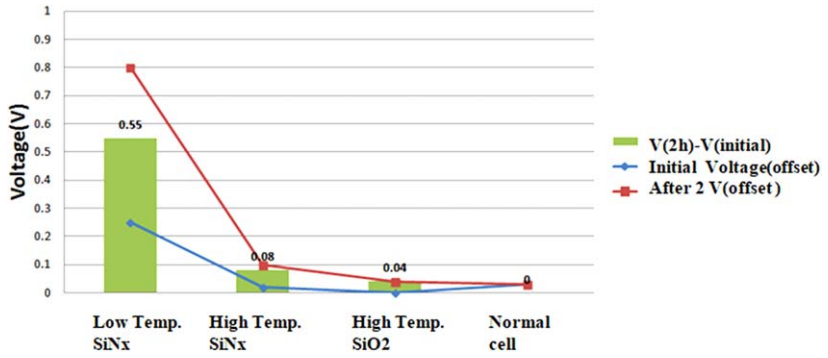

Figure 5. Residual DC measurement values in four kinds of cells which are three cells with different kinds of insulating layers in the CC structure and a normal cell.

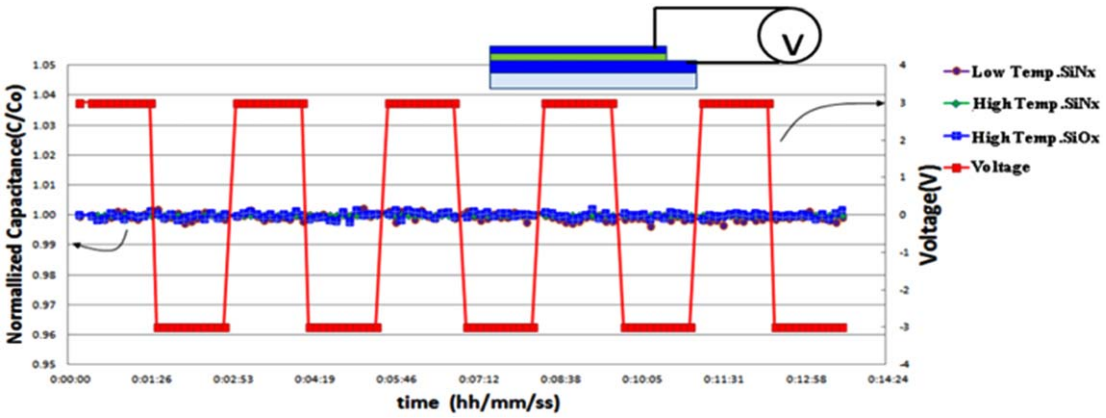

Figure 6. C–V hysteresis graph for a CC cell without LCs.

340 °C (high-temperature SiNx) and SiO2 deposited at 340 °C. First, a 5 AC voltage of 1 Hz was applied to the cell and was measured the flicker. Then, we changed the offset level to eliminate the flicker. After 2 h, we checked the flicker level again To determine the residual DC voltage, we can measure the change in voltage with which the flicker is minimized with time. The green box in figure 5 indicates the residual DC voltages of the three kinds of cells. The low-temperature SiNx cell had the highest residual voltage of 0.55 V and the high-temperature SiNx cell had a residual voltage of 0.08 V. The residual voltages of the SiO_2 cell and the normal cell were 0.04 V and almost 0 V, respectively. The voltage across the LC in the CC structure can be expressed as equation (2). Because the transmittance of the LCs of the CC cell depends on the applied voltage, as indicated by equation (2), the origin of the flicker may be the change of CCP while the AC driving voltage was applied. We attempted to measure the CCP change under the applied DC voltage using an LCR meter.

$$V_{LC} = V_{total} \times \frac{C_{CP}}{C_{CP} + C_{LC}} \tag{2}$$

Here, V_{LC}, V_{total}, C_{CP}, and C_{LC} represent the voltage applied to the LCs, the input voltage, the capacitance of the inorganic materials (SiNx and SiO_2), and the capacitance of the LCs, respectively.

3.2. Capacitance–voltage hysteresis

To determine the capacitance of the SiNx and SiO_2 layers, we prepare additional metal–insulator–metal structures, as shown in figure 6. C_o is the initial capacitance of an insulator, which is measured as approximately 10 nF. DC voltages of +3 and −3 V are applied for 90 s. Figure 6 shows the voltage profile and measured capacitances (C/C_o) for the three insulator layers. We found that there are no capacitance changes under the DC voltage for all insulator layers, which means there is no substantial charge transfer from the defect sites of SiNx or SiO_2. Therefore, we attribute the residual DC in the CC cell to the interactions between the LC and the dielectric layers.

Figure 7 shows the measured capacitance variations of CC cells for the same driving condition as figure 6. The CC cell is composed of the same insulators and LC. C_1 is the initial capacitance of the cell with LCs and an

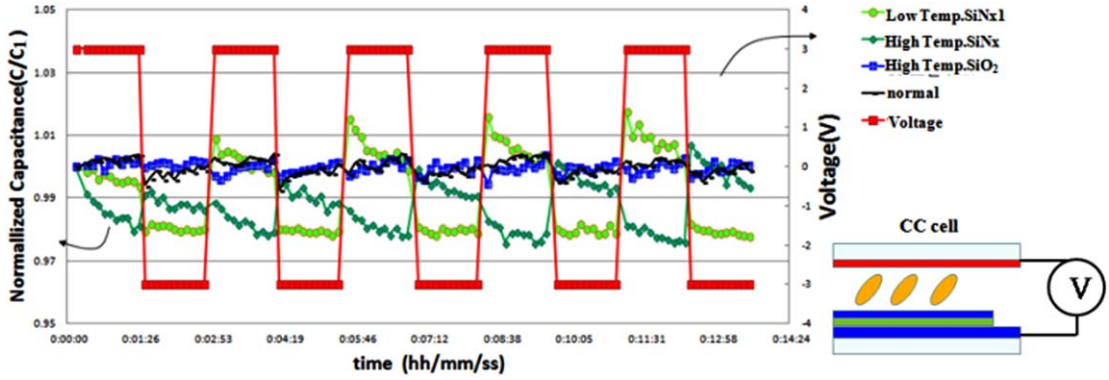

Figure 7. C–V hysteresis graph for a CC cell with LCs.

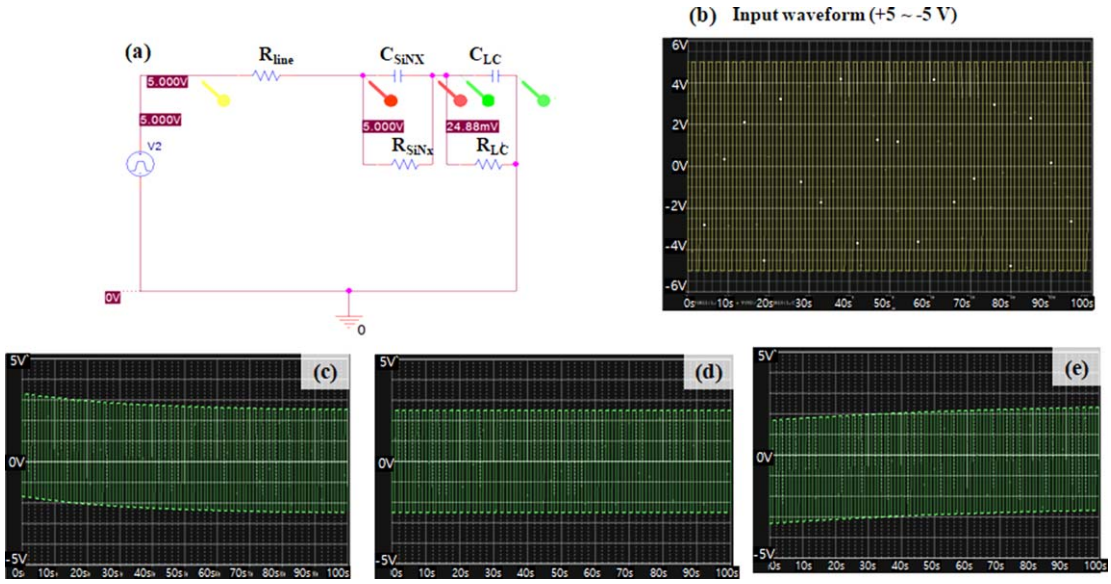

Figure 8. (a) PSpice circuit model; (b) input waveform (+5 to −5 V AC driving); (c) output waveform of C_{LC}, for which the RC of the SiNx is lower than that of the LC ($R_{SiNx}C_{SiNx} < R_{LC}C_{LC}$); (d) output waveform of C_{LC}, for which the RC of the SiNx is equal to that of the LC ($R_{SiNx}C_{SiNx} = R_{LC}C_{LC}$); (e) output waveform of C_{LC}, for which the RC of the SiNx is higher than that of the LC ($R_{SiNx}C_{SiNx} > R_{LC}C_{LC}$).

Table 2. Simulation conditions (PSpice).

	V_1/V_2[V]	TD/TR/TF [s]	PW/PER [s]	R_{line} [kΩ]	R_{SiNx} [GΩ]	R_{LC} [GΩ]	C_{SiNx} [nF]	C_{LC} [nF]
value	5/−5	0/0.1n/0.1n	1/2	1	Variables	5	10	10

insulator. We found that the capacitances gradually decrease while the DC voltage is applied. Interestingly, the CC cell with insulator layers containing low-temperature SiNx exhibits large changes, while the CC cell with insulating layers containing high-temperature SiNx does not. These results indicate an electrical coupling between the LCs and the inorganic layer. To verify this, we performed PSpice simulations with an RC circuit, as shown in figures 8(a)–(e).

3.3. Electrical serial RC circuit simulation

We construct the electrical CC structure with two serial RC circuits, corresponding to the SiNx and LC. The PSpice simulation conditions are shown in table 2. The values are obtained via the measurement of R and C in the test cell. Figure 8(b) shows the input voltage waveform of 5 V. For different resistance values of SiNx ($R_{SiNx} = 2.5$, 5, and 10 GΩ), the voltage of C_{LC} is obtained using equation (2). We obtain the three different kinds of output waveforms for C_{LC}, as shown in figures 8(c)–(e). When the time constant (R × C) of the SiNx is

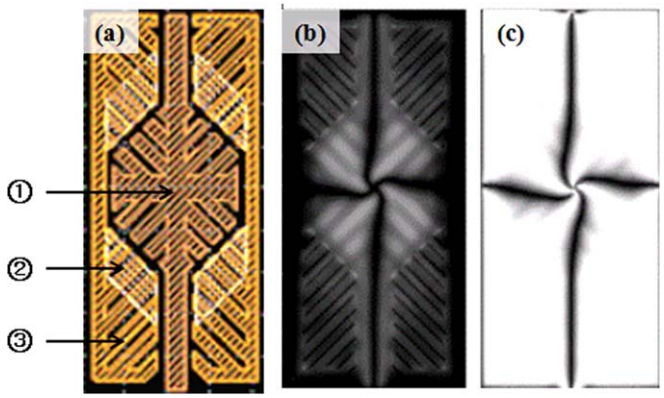

Figure 9. (a) Top-view image of the CC pixel. ① is a high-pixel area that is the 2nd IZO connected to the TFT directly, ② is a middle-pixel area that is the overlapping region of the 1st IZO and 2nd IZO, and ③ is a low-pixel area that is a floating metal: the 2nd IZO. (b), (c) Computer simulation results for the CC mode, obtained using Techwiz 3D: 16 gray and white (256 gray) transmittance images, respectively.

higher than that of the LC, the output waveform for C_{LC} decreases over time, as shown in figure 8(c). When the time constant of the SiNx is lower than that of the LC, the output waveform for C_{LC} increases over time, as shown in figure 8(e). Only when the time constants for the two materials are equal does the output waveform exhibit a stable curve, as shown in figure 8(d). These results are remarkable. Without considering the ion adsorption and desorption, we can obtain the residual DC voltage via the mismatching of time constant in the two serial RC circuits. This means that the optimum common voltages in the high and low pixels of the CC panel differ if the time constants of the LC are not the same. This can cause image sticking.

3.4. Verification of image sticking in CC panel

To confirm the aforementioned RC-matching interaction with the residual DC voltage, we constructed an 18-inch panel with a CC structure. Figure 8 shows a cross-sectional pixel image. We used transparent indium zinc oxide (IZO) electrodes as high- and low-pixel electrodes. The high-pixel electrode was connected to the TFT directly, and the low-pixel electrode was floating metal on the IZO connected to the drain metal of the TFT. Thus, the voltage of the low pixel is lower than that of the high pixel.

Figure 9 shows a top-view image of the pixel. To increase the transmittance, we used dual-layer IZO in the pixel and made the CC structure. Figure 9(b) shows an image in the 16 gray state and figure 9(c) shows an image in the 256 gray (white) state. The center area of the pixel is high pixel connected to the TFT directly, but the voltage in the edge area is applied through the coupling capacitance, and the voltage is lower than that of the center area. In this pixel structure, the middle area has a higher transmittance despite containing the same floating metal because of the high-voltage electrode under the floating metal in the middle area. This CC pixel structure has a good viewing-angle property, and the off-axis gamma distortion is very small. To change the resistance of the SiNx, we controlled the gas ratio of N2, NH3, and SiH4 in the deposition process. Then, the RC value was measured using the Model 6254 VHR machine, as shown in figure 10.

First, the RC constant of the LC was found to be 33 s. Then the RC constants of various SiNx layers were measured, as plotted in figure 10. N-rich SiNx has a low RC value, and Si-rich SiNx has a high RC value. This is supported by Y Masaki [12]. Because the image sticking of the panel occurs at a high temperature of 60 °C as well as at room temperature (25 °C), we measured the time constants of the SiNx and LCs at these two temperatures.

$$V_{LC} = aV + be^{-ct}V \; a = \frac{R_{LC}}{(R_{CP} + R_{LC})}, \; b = \left(\frac{R_{CP}C_{CP} - R_{LC}C_{LC}}{(C_{LC} + C_{CP})(R_{CP} + R_{LC})}\right),$$
$$c = \left(\frac{R_{CP} + R_{LC}}{R_{CP}R_{LC}(C_{CP} + C_{LC})}\right) \tag{3}$$

where V_{LC}, V, C_{CP}, R_{CP}, C_{LC}, and R_{LC} represent the voltage applied to the LCs, the input voltage, the capacitance and resistance of inorganic materials such as SiNx and SiO_2, and the capacitance and resistance of the LCs, respectively [13].

Figure 11(a) shows that the reduction of the time constant for the LCs is significantly larger than that for the two kinds of SiNx, which have time constants of 25 s and 35 s; this is because of the viscosity. The LC with lower viscosity at a high temperature undergoes a greater change in resistance than in the dielectric constant. We tested the image sticking at room temperature and a high temperature with the CC panel and the normal panel. The

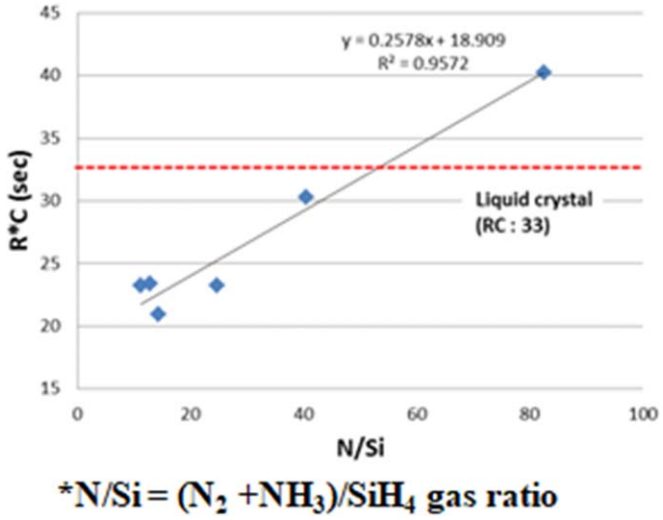

Figure 10. RC graph for various SiNx layers with respect to the N/Si ratio.

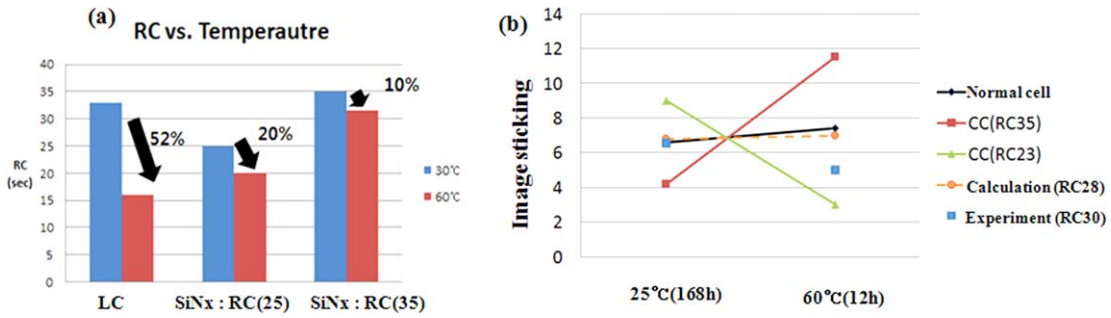

Figure 11. (a) Graph of the RC change according to the temperature in the LC with a 25 s RC value and in the SiNx with a 35 s RC value. (b) Image sticking index for various cells at room temperature and a high temperature.

results are shown in figure 11(b). The larger gap of the time constant between SiNx and LCs deteriorated the image sticking. Thus, the CC panel with RC of 35 s has a low image sticking index at room temperature but a high image sticking index at a high temperature. In contrast, the CC panel with RC of 23 s has a high image sticking index at room temperature but a low image sticking index at a high temperature. Thus, we optimized the RC value of SiNx as 30 s. In figure 10, the CC panel with RC of 30 s exhibits good image quality at high temperature as well as room temperature.

We propose that mismatching the time constant (RC) between two serially connected materials such as LCs and SiNx can induce a residual DC voltage and detrimental image sticking. In particular, this assumption was verified for the CC panel. It is supported by the following equation (3).

Equation (3) indicates that the voltage of the LCs in the CC structure has two terms—a steady-state voltage and a transient-state voltage—for two serial RC circuits under AC driving. If the RCs of the two components induced by LCs and inorganic dielectric are the same, the transient term disappears. Thus, the output voltage in the LCs has no fluctuation.

4. Conclusions

We proposed an alternative image sticking mechanism in LCDs according to the RC-matching theory. Experimental and simulation data indicate that a residual DC voltage may appear even in the absence of ion impurities in the LCD. This can be proven through the CC mode. In previous studies [11], the floating metal has been considered as the source of the image sticking in the CC mode, but we showed that this is not the origin. This finding can also be applied to the IPS and PLS modes, which are composed of various serial RC circuits, such as LCs, alignment layers, and SiNx. Previously, researchers could not account for the flicker-change phenomenon in these structures, which increases over time, even with the optimum common voltage at which

the flicker is minimized. The proposed solution reduces the residual DC voltage by matching the time constants between the two layers. In the CC mode, we can control the time constant of SiNx by changing the deposition process parameters and can obtain a reliable panel without image sticking. This technology will eventually provide an effective solution for high resolution LCD TVs up to QUHD with a wide viewing angle.

Acknowlegment

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