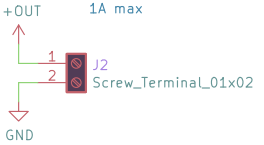
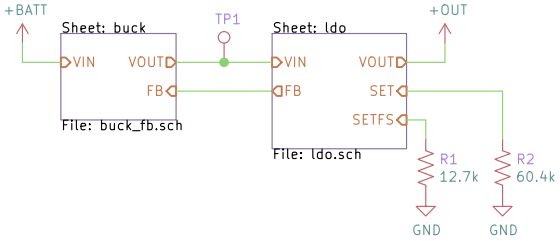
6S lipo (19.2 – 25.2V)
or 24V AC/DC adapter





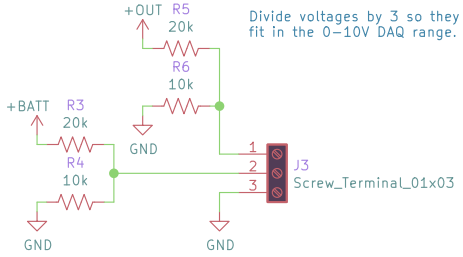
Resistor values:
SET sets the voltage output, SETFS sets the threshold voltage it uses to initially charge up the capacitors.
for 12V:
  SETSFS(kΩ) = 442 / (12*3 – 1) = 12.63k
  SET(kΩ) = 5*12 = 60k

for 10V:
  SETFS(kΩ) = 442 / (10*3 – 1) = 15.24k
  SET(kΩ) = 5*10 = 50k

for 5V:
  SETFS(kΩ) = 442 / (5*3 – 1) = 31.57k
  SET(kΩ) = 5*5 = 25k

Both 1%

DAQ Voltage Monitoring



Divide voltages by 3 so they fit in the 0–10V DAQ range.

All resistors/capacitors are 0805/5% unless otherwise specified.

Sheet: / File: power_board.sch		
Title: DAQ Power Board		
Size: A4	Date:	**Rev:**
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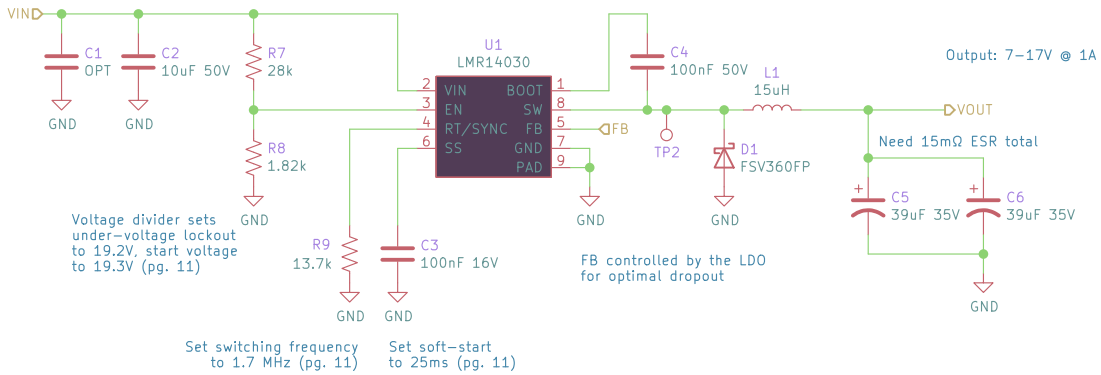
Variable buck regulator. Most values taken from webench.ti.com for 17V 1A out.
https://www.ti.com/lit/ds/symlink/lmr14050.pdf

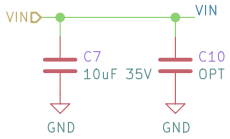
Input: 19.2–25.2V or 24V from wall

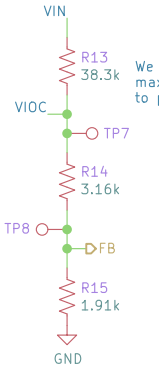


Sheet: /buck/
File: buck_fb.sch

Title:

Size: A4 | Date: | Rev:
KiCad E.D.A. kicad 5.1.10 | Id: 2/3



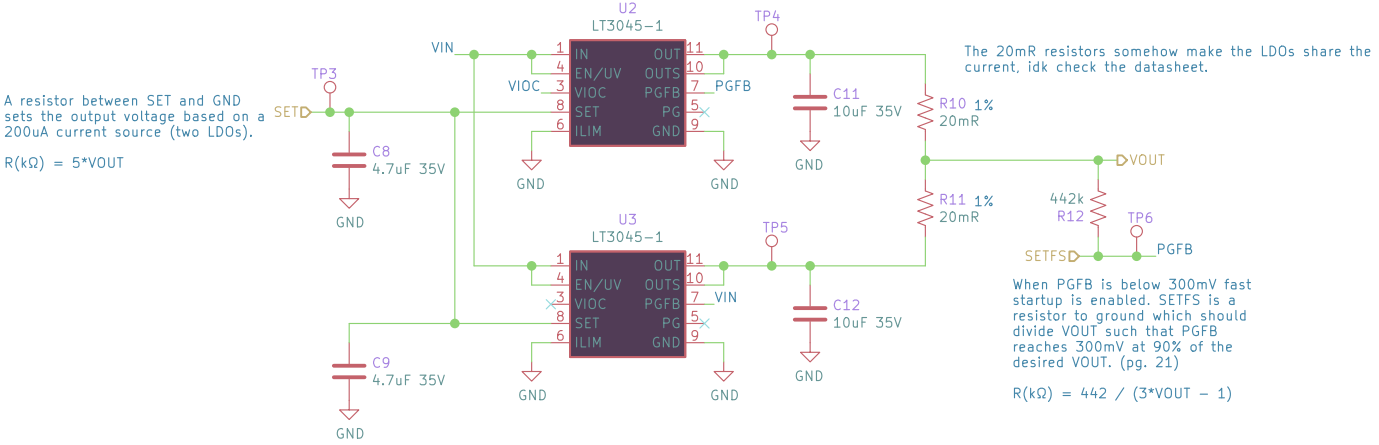


We also divide VIN to set a maximum voltage of 17V to protect the LDO. (pg. 24)

VIOC is driven to the difference between the set voltage and VOUT. We want VIOC=2V so we divide such that 2V->0.75V, the switching threshold for the buck converter, and use it as the buck converter's feedback. (pg. 23)

Parallel two LDOs for 1A output. (pg. 22)

https://www.analog.com/media/en/technical-documentation/data-sheets/30451fa.pdf



A resistor between SET and GND sets the output voltage based on a 200uA current source (two LDOs).

R(kΩ) = 5*VOUT

The 20mR resistors somehow make the LDOs share the current, idk check the datasheet.

When PGFB is below 300mV fast startup is enabled. SETFS is a resistor to ground which should divide VOUT such that PGFB reaches 300mV at 90% of the desired VOUT. (pg. 21)

R(kΩ) = 442 / (3*VOUT - 1)

Sheet: /ldo/		
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