

We now move onto a discussion of transistors and transistor-based circuits.

There are several types of transistors, including the following:

MOS transistors (Chapter 5)

Metal Oxide Semiconductor

Field Effect Transistor (MOSFET)
ECE240

Bipolar transistors (Chapter 6)

Bipolar Junction Transistor (BJT)
other courses

MOS Transistor Structure and Models §5.1

A MOS transistor has 4 terminals:

- Gate (G)
- Source (S)
- Drain (D)
- Bulk (B) - sometimes ignored,
sometimes called the 'body'

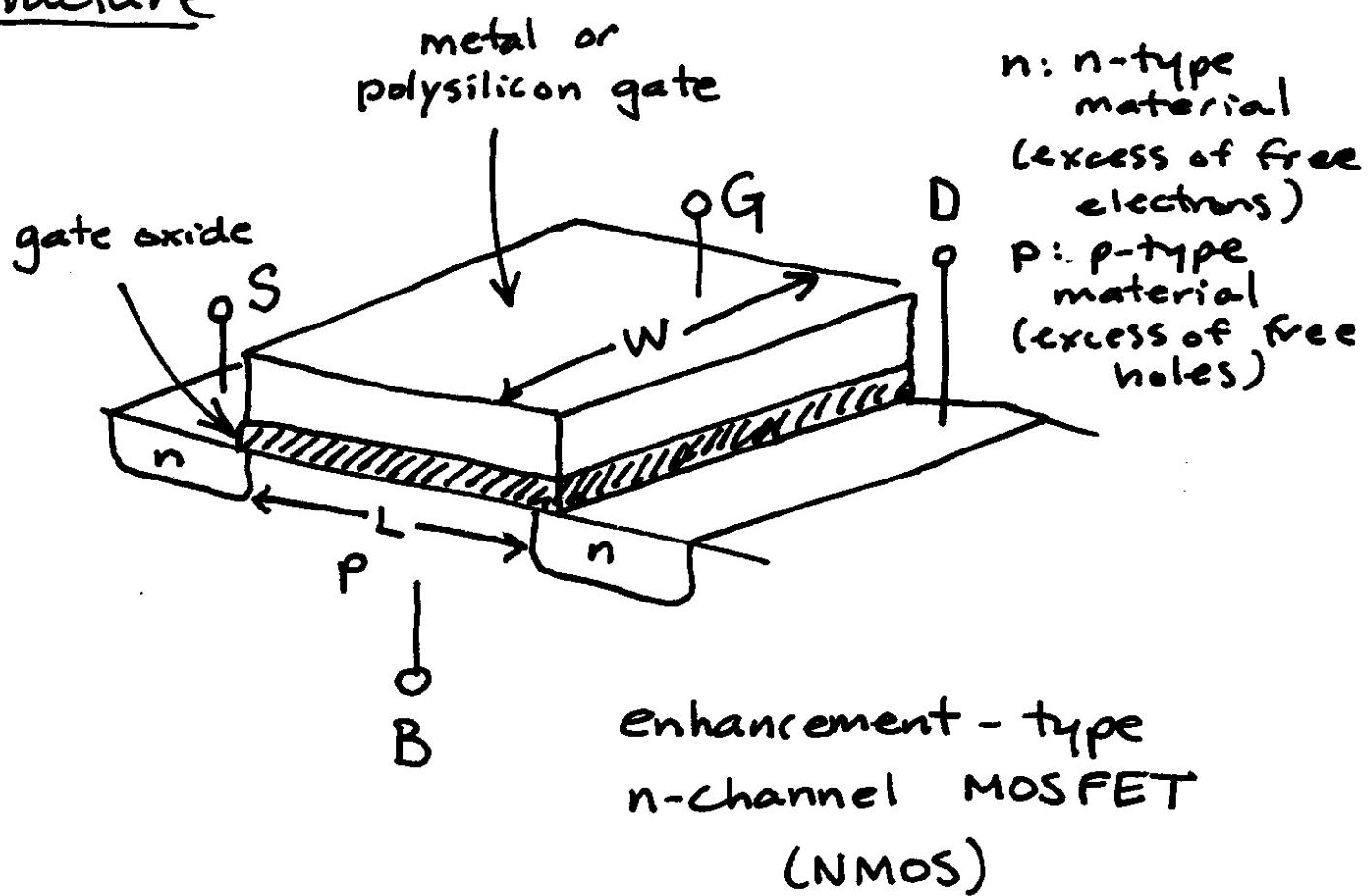
There are two broad types of MOS transistors

- n-channel (NMOS)
- p-channel (PMOS)

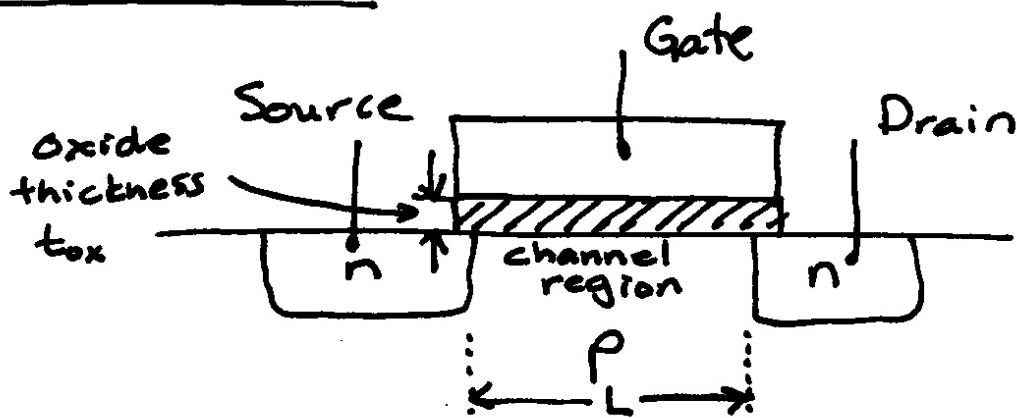
NMOS and PMOS transistors have complementary behaviour (we will soon see how...). Technologies that allow the manufacturing of both NMOS and PMOS transistors are known as:

Complementary Metal Oxide Semiconductor (CMOS)

Structure



Cross- Section



Typical dimensions:

L : $0.03\mu m$ to $1\mu m$

W : $0.1\mu m$ to $100\mu m$

t_{ox} : $1nm$ to $10nm$

Typically, newer CMOS technologies allow smaller values of W and L .

MOS Operation

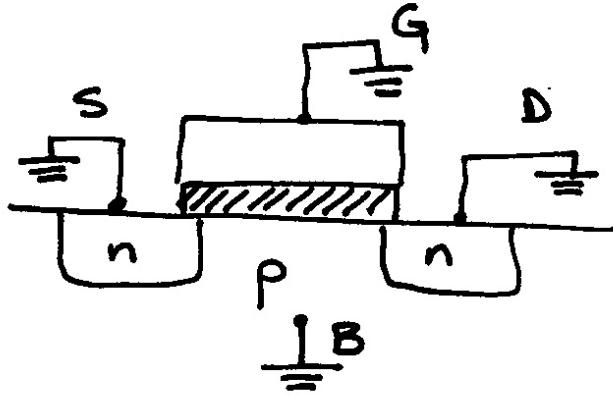
In very broad terms, the voltage applied to the gate controls how much current is allowed to flow between the drain and source.

As with diodes, there are several modes, or regions, of operation, and each has its own model / I-V equation.

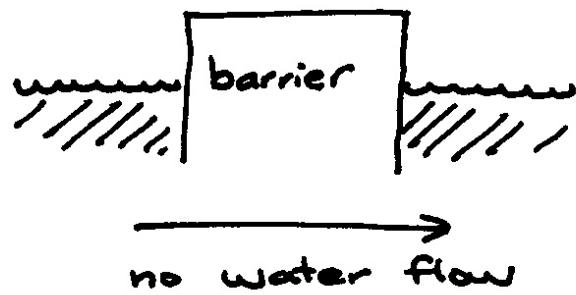
Let's start with an enhancement-mode NMOS transistor.

zero Gate Voltage 55.1.2.

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water analogy:



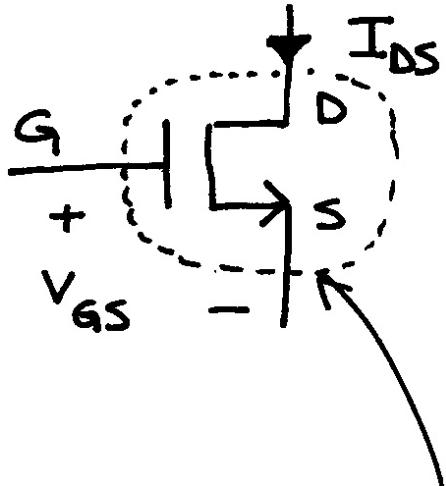
Two back-to-back diodes:
no current flow.

Formal:

Cutoff region Model

$$I_{DS} = 0 \quad (\text{current from drain towards source})$$

$$V_{GS} < V_t \quad (\text{voltage at gate with respect to source})$$

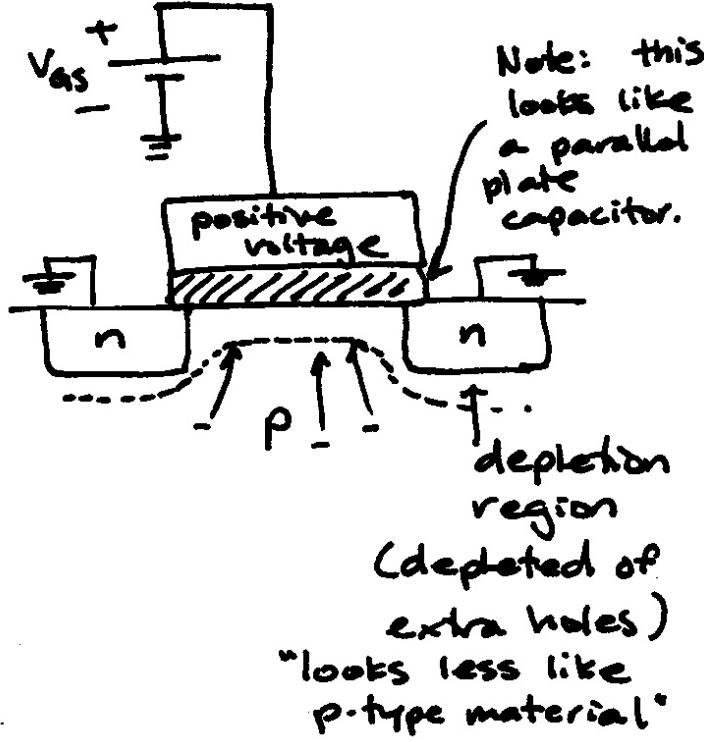


Note: no current enters the gate.

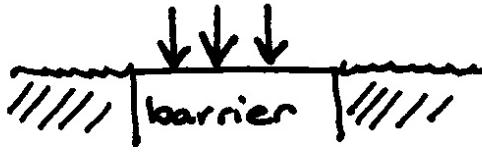
NMOS Symbol

Creating a Channel for Current Flow 35.1.3

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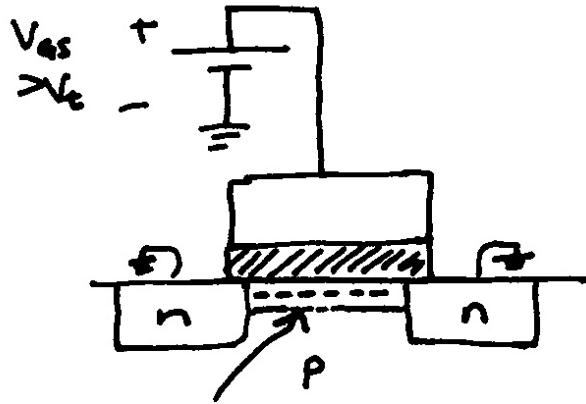


Water analogy:



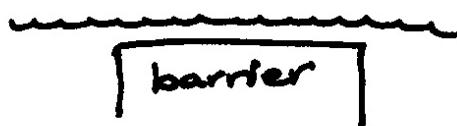
lowering barrier eventually allows water to flow.

Eventually, $V_{GS} > V_t$, the transistor's threshold voltage



- channel
- current can flow!

water analogy:



$$V_{GS} - V_t = \underline{V_{ov}}$$

gate overdrive voltage

How much charge is available in the channel?

$$|Q| = (C_{ox} WL) V_{ov}$$

↑
Capacitance per
unit area

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

oxide capacitance
per unit area

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ϵ_{ox} , permittivity of oxide

For SiO_2 , $\epsilon_{ox} = 3.9 \epsilon_0 = 3.45 \times 10^{-11} \text{ F/m}$

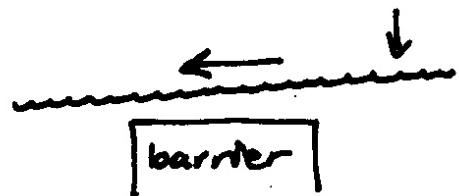
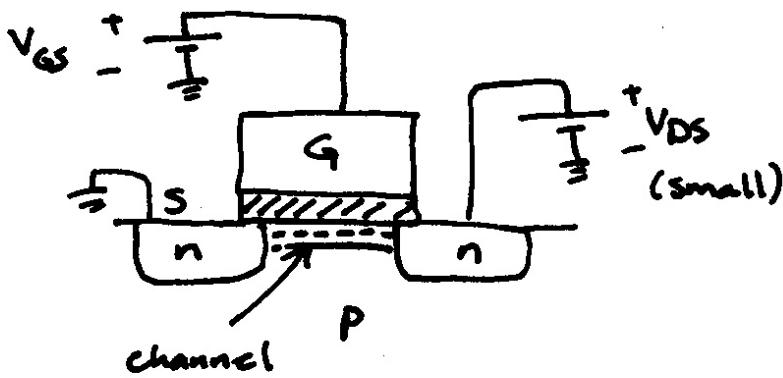
e.g. for a transistor with

$$W = 0.72 \mu\text{m}, L = 0.18 \mu\text{m}, t_{ox} = 4 \text{ nm}$$

$$C = C_{ox} WL = \frac{\epsilon_{ox}}{t_{ox}} WL = 1.1 \text{ fF}$$

Applying $V_{DS} > 0$ 35.1.4

pour a
bit of
water



$$\frac{|Q|}{\text{unit length}} = C_{ox} W V_{ov}$$

$$\text{Electric field } |E| = \frac{V_{DS}}{L} \rightarrow \text{Drift velocity } \mu_n |E| = \mu_n \frac{V_{DS}}{L}$$

"mobility"
i.e. how easy is
it for electrons
to move around
under an electric
field?

$$\frac{Q}{\text{unit length}} \times \text{drift velocity} = I_{DS}$$

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$$I_{DS} = \left(\mu_n C_{ox} \frac{W}{L} V_{ov} \right) V_{DS}$$

conductance g_{DS}

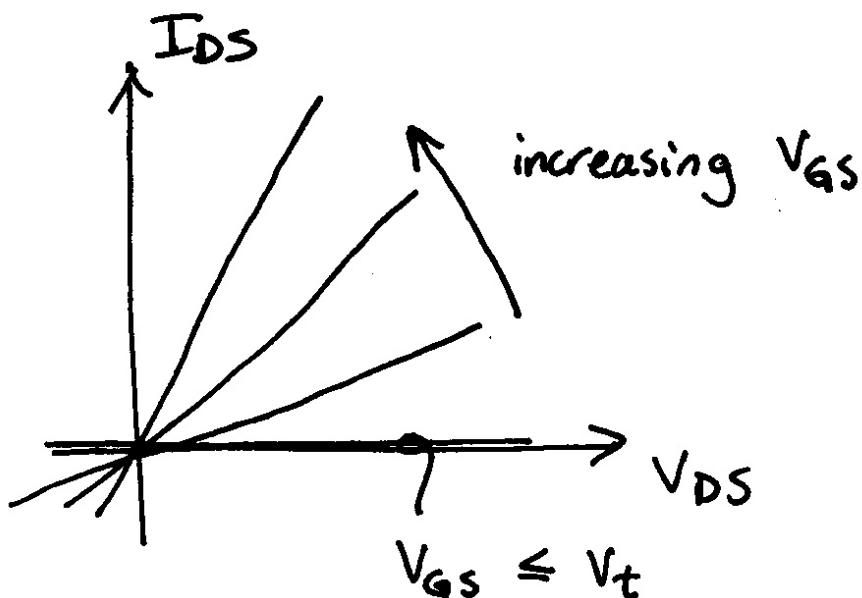
$$g_{DS} = \left(\mu_n C_{ox} \right) \left(\frac{W}{L} \right) (V_{GS} - V_t)$$

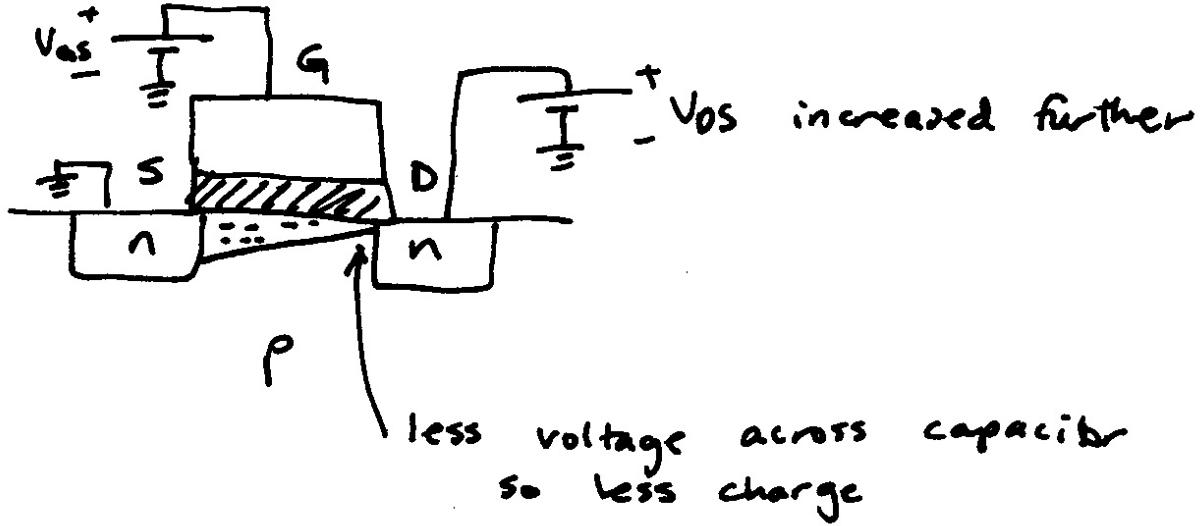
$$k_n' = \mu_n C_{ox}$$

process
transconductance
parameter

$$k_n = k_n' \left(\frac{W}{L} \right)$$

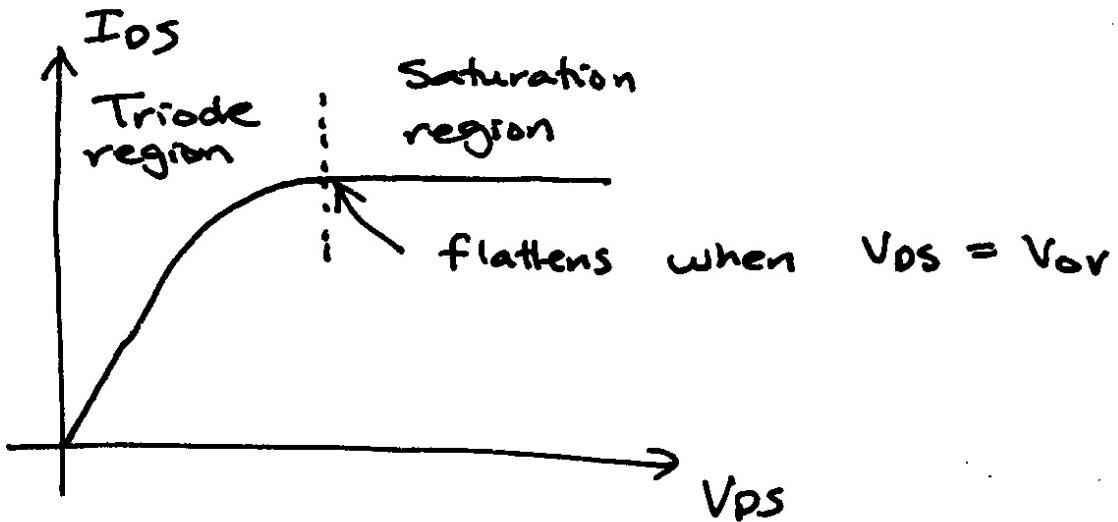
MOSFET transconductance
parameter
units: A/V²





→ Q decreased, but E keeps increasing

$$I_{DS} = k_n' \left(\frac{W}{L}\right) \left(V_{GS} - \frac{1}{2}V_{DS}\right) V_{DS}$$



Note: as $V_{DS} \rightarrow 0$, $I_{DS} \rightarrow k_n' \left(\frac{W}{L}\right) (V_{GS}) V_{DS}$, as before.

Triode Region Model

$$V_{GS} > V_t$$

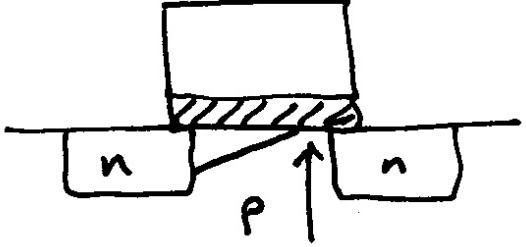
$$V_{DS} < V_{GS} - V_t$$

$$I_{DS} = k_n' \left(\frac{W}{L}\right) \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$V_{DS} \geq V_{OV} \text{ (saturation)} \quad 5.5.1.6$$

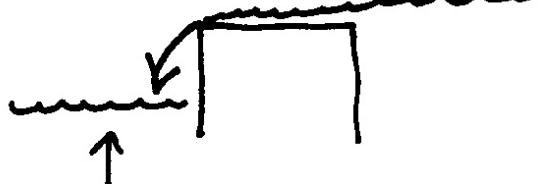
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water analogy:



Channel
pinch-off

- electrons are swept across this region
- I_{DS} no longer increases with V_{DS} i.e. it is saturated



amount of water

falling over
barrier doesn't
depend on
water level
on left side.

Saturation
Region
Model

$$V_{GS} = V_t$$

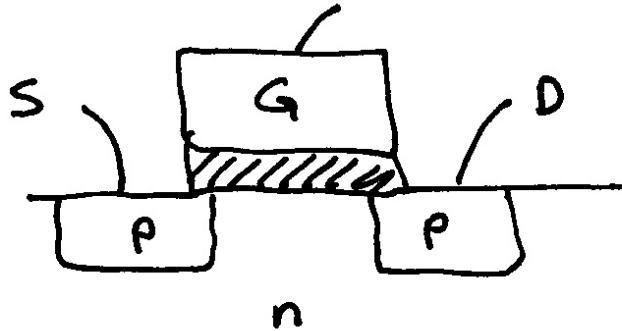
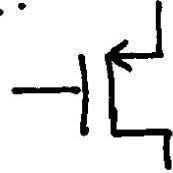
$$V_{DS} \geq V_{GS} - V_t$$

$$I_{DS} = \frac{k_n}{2} \left(\frac{W}{L} \right) (V_{GS} - V_t)^2$$

PMOS Transistor § 5.1.7

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Symbol:



- Need to put a negative voltage on the gate to attract holes that form a p-channel

Cutoff $V_{SG} < |V_{tp}|$, $I_{SD} = 0$

Triode $V_{SG} \geq |V_{tp}|$

$$V_{SD} \leq V_{SG} - |V_{tp}|$$

$$I_{SD} = k_p' \left(\frac{W}{L} \right) \left[(V_{SG} - |V_{tp}|) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

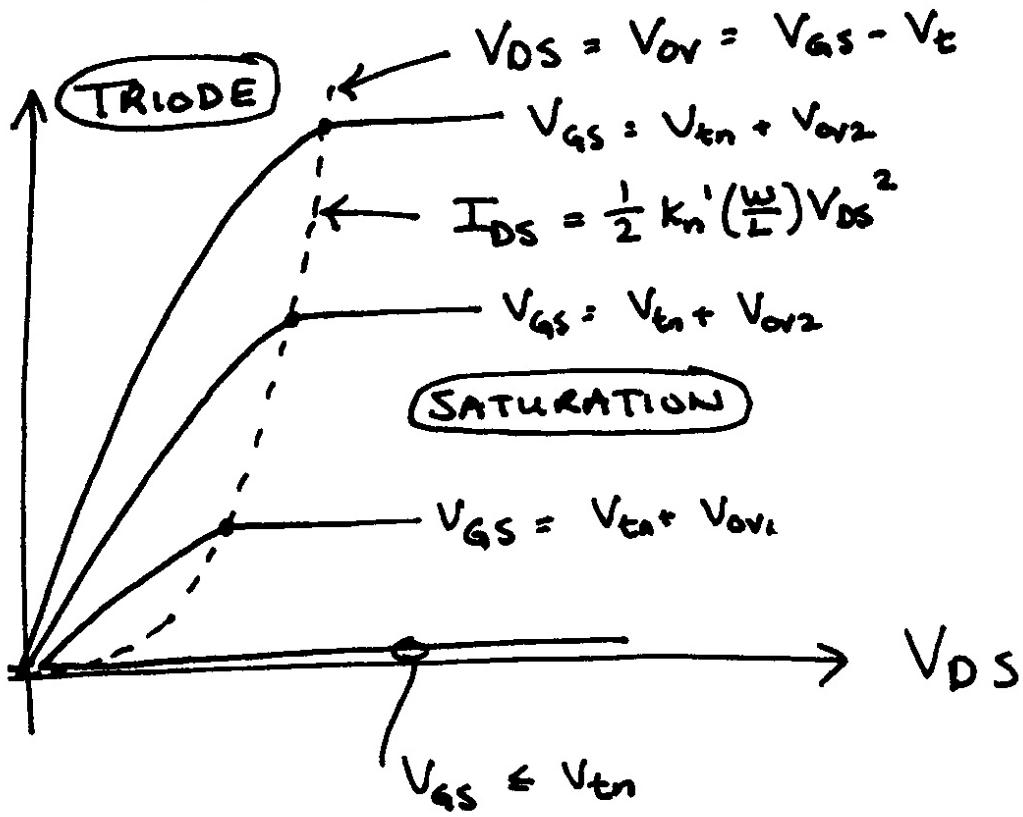
Saturation $V_{SG} \geq |V_{tp}|$

$$V_{SD} \geq V_{SG} - |V_{tp}|$$

$$I_{SD} = \frac{k_p'}{2} \left(\frac{W}{L} \right) (V_{SG} - V_{tp})^2$$

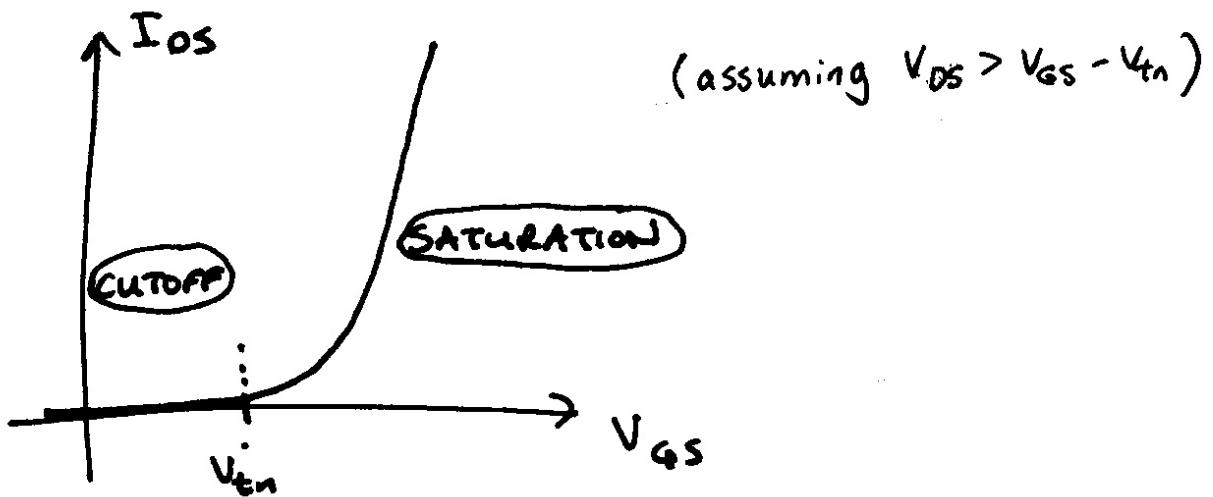
I_{DS} vs. V_{DS} (NMOS)

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I_{DS} vs. V_{GS} (NMOS, large V_{DS} i.e. saturation) § 5.2.3

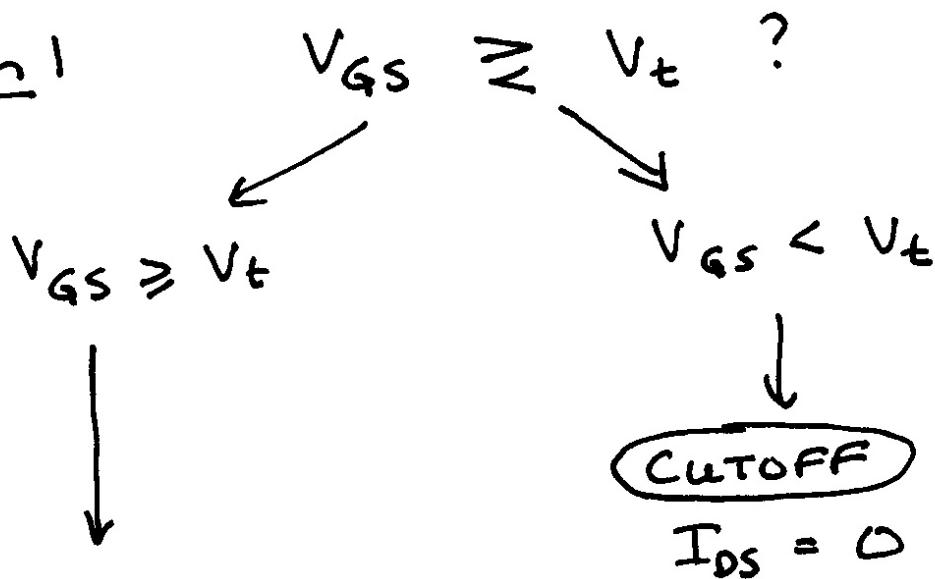
Assuming a transistor operates in the saturation region, we can plot I_{DS} vs. V_{GS} such that $I_{DS} = \frac{1}{2} k_n' \left(\frac{w}{l}\right) (V_{GS} - V_{tn})^2$



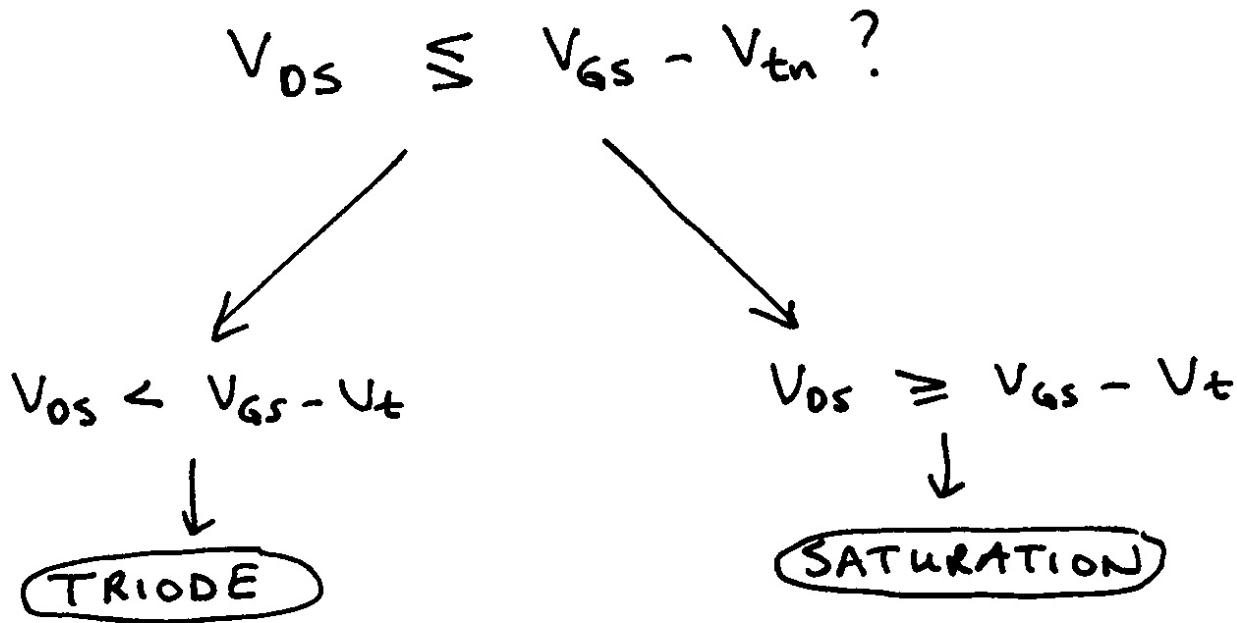
Analyzing and Designing MOS-based Circuits

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Question 1



Question 2



$$I_{DS} = k_n' \left(\frac{W}{L} \right) \left[(V_{GS} - V_{tn}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_{DS} = \frac{k_n'}{2} \left(\frac{W}{L} \right) (V_{GS} - V_{tn})^2$$

Note : We won't always know

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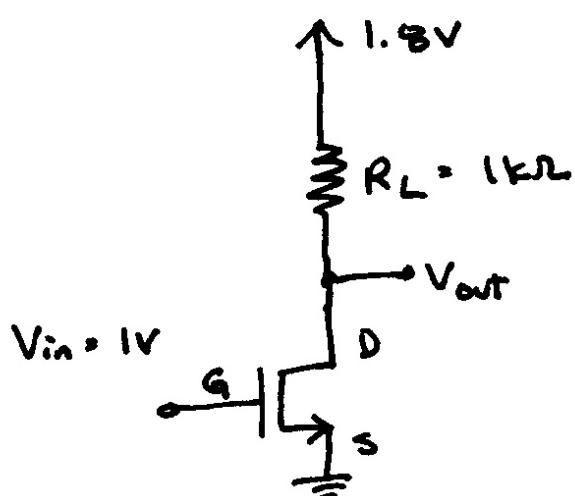
whether $V_{GS} \leq V_t$, and $V_{DS} \geq V_{GS} - V_{th}$.

Sometimes we'll have to guess. If we are wrong, then the conditions won't be satisfied in our solution, and we will have to go back and re-solve the problem.

Example

Consider this circuit, with

$W = 2\mu m$, $L = 0.18\mu m$, $C_{ox} = 8.6 fF/\mu m^2$,
 $\mu_n = 450 \text{ cm}^2/\text{V}\cdot\text{s}$, $V_{th} = 0.5V$. Solve for V_{out} .



Question 1 $V_{GS} \geq V_{th}$?

$$1V > 0.5V$$

so transistor is ON

Question 2

$$V_{DS} \geq \frac{V_{GS} - V_{th}}{0.5V} ?$$

Since $V_{DS} = V_{out}$, and we are solving for V_{out} , we don't know the answer yet.

Let's assume transistor is in SATURATION,
i.e. $V_{out} \geq 0.5V$.

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$= \left(\frac{450 \text{ cm}^2}{\text{V.s}} \right) \left(\frac{8.6 \text{ fF}}{\mu\text{m}^2} \right) \left(\frac{1}{2} \right) \left(\frac{2 \mu\text{m}}{0.18 \mu\text{m}} \right) (1.0 - 0.5)^2$$

$$= 0.54 \text{ mA}$$

$$V_{out} = 1.8 \text{ V} - (0.54 \text{ mA})(1 \text{ k}\Omega)$$

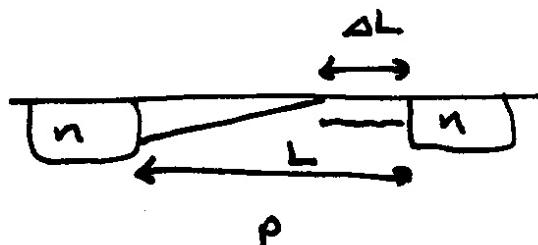
$$= 1.26 \text{ V}$$

Note: $1.26 \text{ V} > 0.5 \text{ V}$ We are correct!

Channel-Length Modulation § 5.24

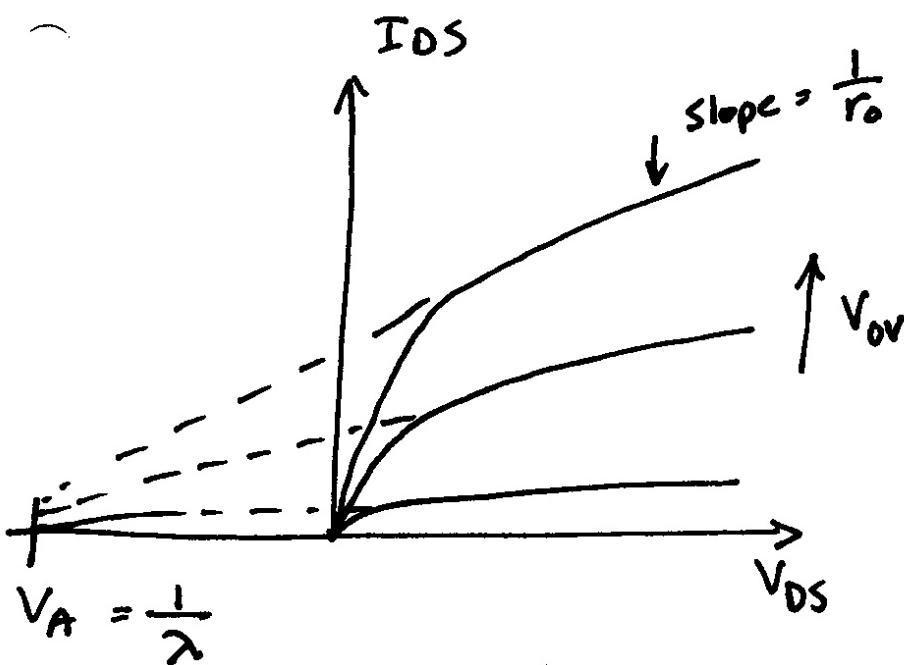
(7)

Back to modeling. As the transistor goes into saturation, the channel pinches off, and actually becomes shorter.



This causes an increase in current known as channel-length modulation, usually modeled as an extra term:

$$I_{DS} = \frac{1}{2} k_n \left(\frac{w}{L} \right) (V_{GS} - V_{tn})^2 \underbrace{(1 + \lambda V_{DS})}_{\text{new term}} \quad \text{units: } \text{A/V}$$



V_A : "Early" voltage

$$V_A = \frac{1}{\lambda}$$

r_o represent the output resistance of the transistor

$$r_o = \left[\frac{\partial I_{DS}}{\partial V_{DS}} \right]_{V_{GS} \text{ constant}}^{-1} = \left[\lambda I_{DS} \right]^{-1} = \frac{V_A}{I_{DS}}$$

Note: often, for simplicity, we set $\lambda = 0$.

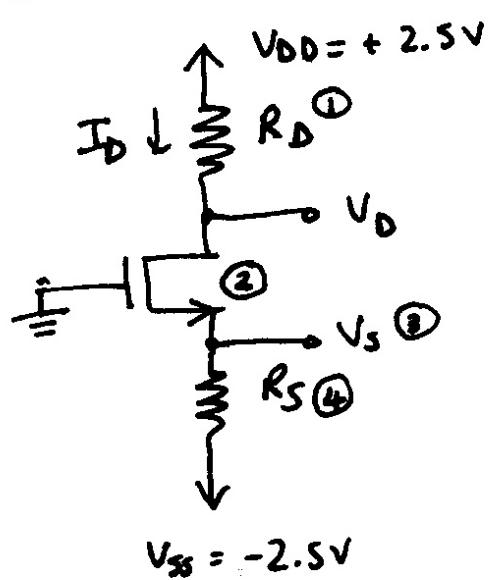
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MOSFET Circuits at DC (§5.3)

The textbook covers a few examples of MOS circuit design (Examples 5.3 - 5.8). We won't have time to cover each of these but I expect you to be familiar with them.

Example (based on Example 5.3, p. 273)

Consider this circuit:



$$\mu_n C_{ox} = 100 \mu A/V^2$$

$$V_t = 0.7 V$$

$$W/L = 32 \mu m / 1 \mu m$$

Design the circuit (choose R_S and R_D) such that
 $I_D = 0.4 \text{ mA}$ and $V_D = 0.5 \text{ V}$

$$\textcircled{1} \quad R_D = \frac{V_{DD} - V_D}{I_D} = \frac{(2.5 - 0.5) V}{0.4 \text{ mA}} = 5 \text{ k}\Omega$$

\textcircled{2} $V_D > 0 \rightarrow$ transistor in saturation mode

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) V_{ov}^2$$

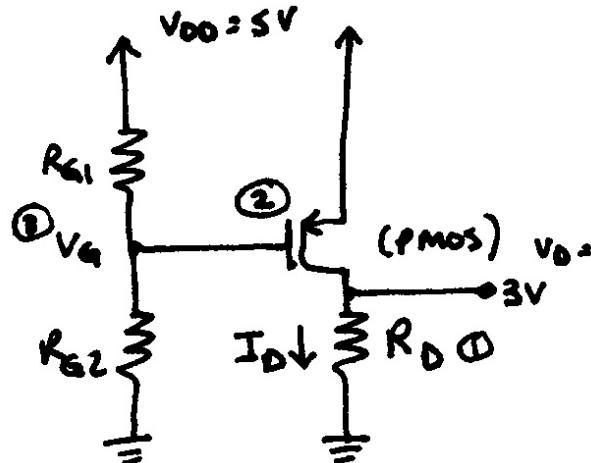
$$\rightarrow V_{ov} = 0.5 V$$

$$\textcircled{3} \quad V_S = 0 V - V_{ov} - V_t = -1.2 V$$

$$\textcircled{4} \quad R_S = \frac{V_S - V_{SS}}{I_D} = \frac{(-1.2 + 2.5) V}{0.4 \text{ mA}} = 3.25 \text{ k}\Omega$$

Example (Based on Example 5.7)

Consider this circuit: $k_p = \mu_p C_{ox} \left(\frac{W}{L} \right) = \frac{ImA}{V^2}$



Design the circuit such that
 $V_D = 3V$, $I_D = 0.5mA$, and
the PMOS operates in
saturation.

$$\textcircled{1} \quad R_D = \frac{3V}{0.5mA} = 6k\Omega$$

$$\textcircled{2} \quad I_D = \frac{\mu_p}{2} C_{ox} \left(\frac{W}{L} \right) V_{or}^2$$

$$O.SmA = \frac{ImA}{2\gamma^2} |V_{ov}|^2 \rightarrow |V_{ov}| = 1V$$

$$\textcircled{1} \quad V_a = 5V - |V_{op}| - |V_{ov}| = 3V$$

(note: transistor is in saturation)

$$\textcircled{4} \quad V_G = 3V = \frac{R_{G2}}{R_{G2} + R_{G1}} 5V \quad (\text{resistive divider})$$

\rightarrow choose $R_{G2} = 3MR$, $R_{G1} = 2MR$

Examples 5.1 - 5.8, Video Examples VE5.1 - 5.4

Exercises S.1 - S.15

Problems 5.3, 5, 10, 11, 14, 16, 17, 18, 20,
24, 26, 29, 31, 36, 39, 40, 43,
45, 49, 53, 54, 58, 60