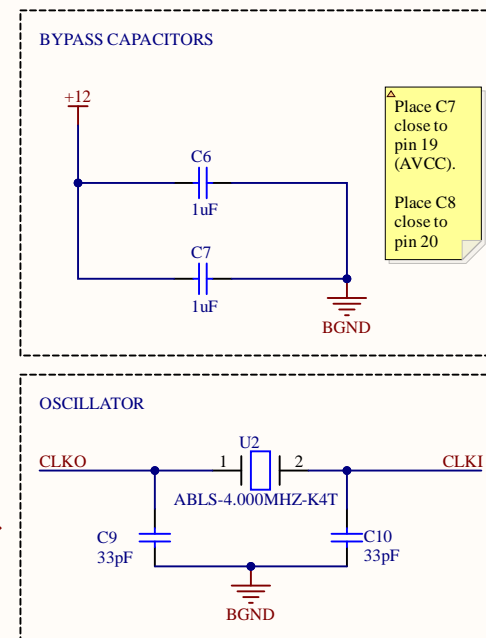


Title		
Size	Number	Revision
A4		
Date:	11-09-2022	Sheet of
File:	C:\Users\...\LTC2949_Top.SchDoc	Drawn By:

[illegible]

ISOSPI: Tie IOVCC to DGND

△ SPI: Tie IOVCC to a voltage  $\geq 1.8\text{V}$  and  $\leq 4.5\text{V}$  and bypass with  $1\mu\text{F}$  to DGND

Shunt resistor to be connected externally

A diagram of a 2-to-1 multiplexer component labeled J1. It has two input lines on the left, labeled 1 and 2, and one output line on the right labeled MOLEX0039301021. The component is represented by a yellow rectangle with a red border.

Transformer needs to be close to the IM/IP header

For ISOSPI operations:

- Connect Pin 1 to Pin 5
- Connect Pin 2 to Pin 6


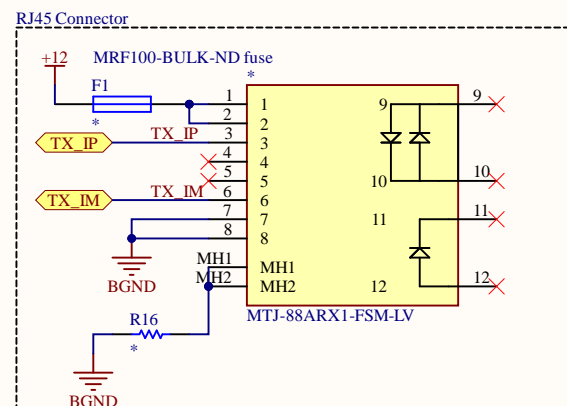
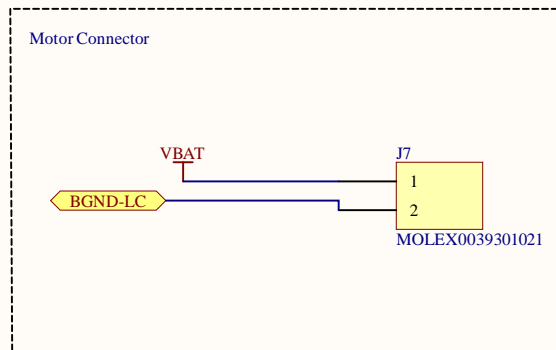
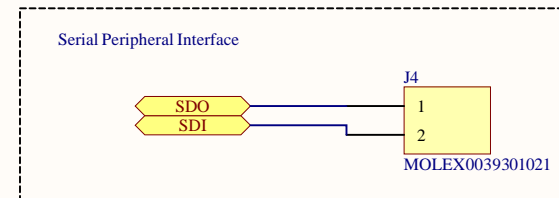
Title: *			* * * * *	
Size: A4	Author: *			
Date: 09-11-2022	Revision: *	Sheet 2 of 3		
File: LTC2949.SchDoc				

Diagram illustrating the LT2949 Voltage Inputs and GPIO Pins. The device features a 1x12 Header (P5) with pins numbered 1 through 12. The pins are labeled as follows:

- Pin 1: V1
- Pin 2: V2
- Pin 3: V3
- Pin 4: V4
- Pin 5: V5
- Pin 6: V6
- Pin 7: V7
- Pin 8: V8
- Pin 9: V9
- Pin 10: V10
- Pin 11: V11
- Pin 12: V12

A red 'X' is marked over the connection between V2 and Pin 1. A yellow callout box labeled V[1..12] indicates the range of pins 1 through 12.



Title		
Size A4	Number	Revision
Date:	11-09-2022	Sheet of
File:	C:\Users\...\LTC2949_Connectors.SchDoc	Drawn By:

# Board Stack Report