SCHOOL OF INFORMATION, COMPUTER AND COMMUNICATION TECHNOLOGY
SIRINDHORN INTERNATIONAL INSTITUTE OF TECHNOLOGY
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LAB REPORT

EES 370 DIGITAL CIRCUIT LABORATORY

Lab 02 Introduction to Logisim

By

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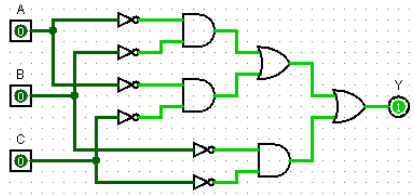
Objectives

1. To know how to construct digital circuits in Logisim.
2. To know how to convert from Boolean expression and truth table to digital circuits in Logisim.
3. To know how to minimize the Boolean expression in SOP and POS form and build the circuit from it in Logisim.

Lab Result

Part 1

1) The circuit from the Boolean expression in the SOP form using two-input gates only and the circuit statistics.

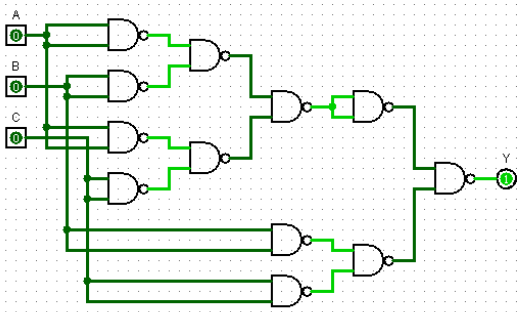


Logisim: 1A Statistics

Component	Library	Simple	Unique	Recur...
Pin	Wiring	4	4	4
NOT Gate	Gates	6	6	6
AND Gate	Gates	3	3	3
OR Gate	Gates	2	2	2
TOTAL (without project's subcircuits)		15	15	15
TOTAL (with subcircuits)		15	15	15

Close

2) The circuit from the Boolean expression in the SOP form using two-input NAND-gate only and the circuit statistics.

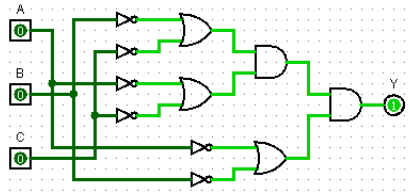


Logisim: 1B Statistics

Component	Library	Simple	Unique	Recur...
Pin	Wiring	4	4	4
NAND Gate	Gates	12	12	12
TOTAL (without project's subcircuits)		16	16	16
TOTAL (with subcircuits)		16	16	16

Close

3) The circuit from the minimized Boolean expression in the POS form using two-input gates only and the circuit statistics.



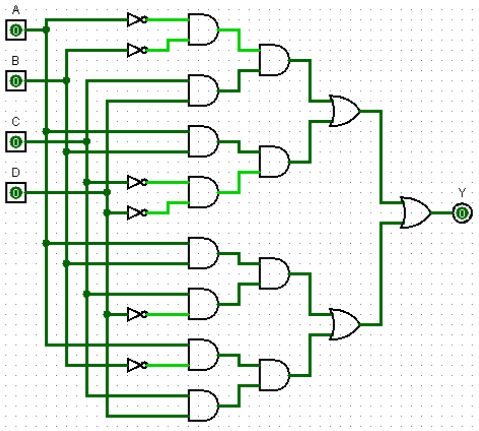
Logisim: 1C Statistics

Component	Library	Simple	Unique	Recur...
Pin	Wiring	4	4	4
NOT Gate	Gates	6	6	6
AND Gate	Gates	2	2	2
OR Gate	Gates	3	3	3
TOTAL (without project's subcircuits)		15	15	15
TOTAL (with subcircuits)		15	15	15

Close

Part 2

1) The circuit directly from the Boolean expression above using two-input gates only and the circuit statistics.

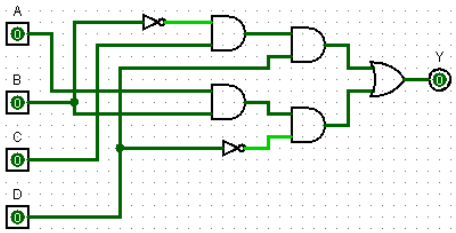


Logisim: 2A Statistics

Component	Library	Simple	Unique	Recur...
Pin	Wiring	5	5	5
NOT Gate	Gates	6	6	6
AND Gate	Gates	12	12	12
OR Gate	Gates	3	3	3
TOTAL (without project's subcircuits)		26	26	26
TOTAL (with subcircuits)		26	26	26

Close

2) The circuit from the minimized Boolean expression in the SOP form using two-input gates only and the circuit statistics.

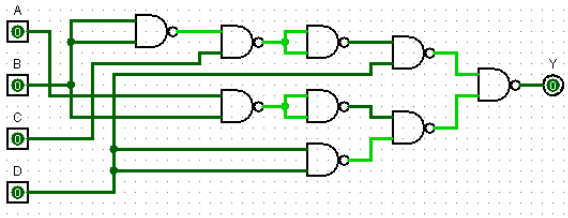


Logisim: 2B Statistics

Component	Library	Simple	Unique	Recur...
Pin	Wiring	5	5	5
NOT Gate	Gates	2	2	2
AND Gate	Gates	4	4	4
OR Gate	Gates	1	1	1
TOTAL (without project's subcircuits)		12	12	12
TOTAL (with subcircuits)		12	12	12

Close

3) The two-input NAND-gate only circuit from the minimized Boolean expression in the SOP form and the circuit statistics.

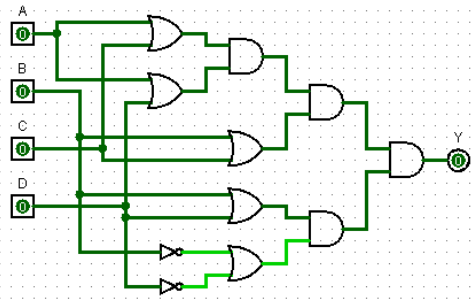


Logisim: 2C Statistics

Component	Library	Simple	Unique	Recur...
Pin	Wiring	5	5	5
NAND Gate	Gates	9	9	9
TOTAL (without project's subcircuits)		14	14	14
TOTAL (with subcircuits)		14	14	14

Close

4) The circuit from the minimized Boolean expression in the POS form using two-input gates only and the circuit statistics.



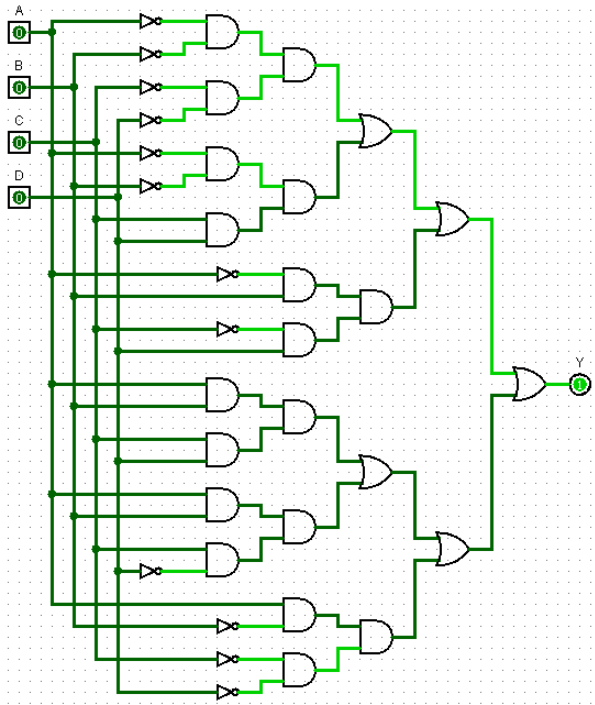
Logisim: 2D Statistics

Component	Library	Simple	Unique	Recur...
Pin	Wiring	5	5	5
NOT Gate	Gates	2	2	2
AND Gate	Gates	4	4	4
OR Gate	Gates	5	5	5
TOTAL (without project's subcircuits)		16	16	16
TOTAL (with subcircuits)		16	16	16

Close

Part 3

1) The circuit directly from the Boolean expression above using two-input gates only and check the circuit statistics.

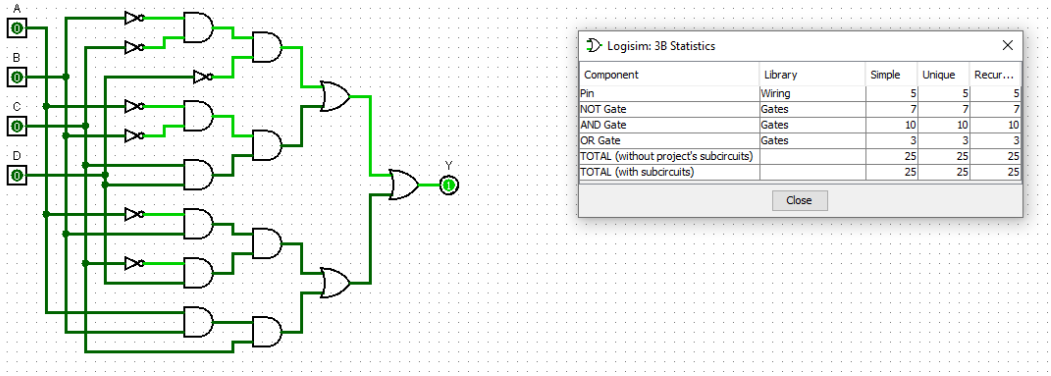


Logisim: 3A Statistics

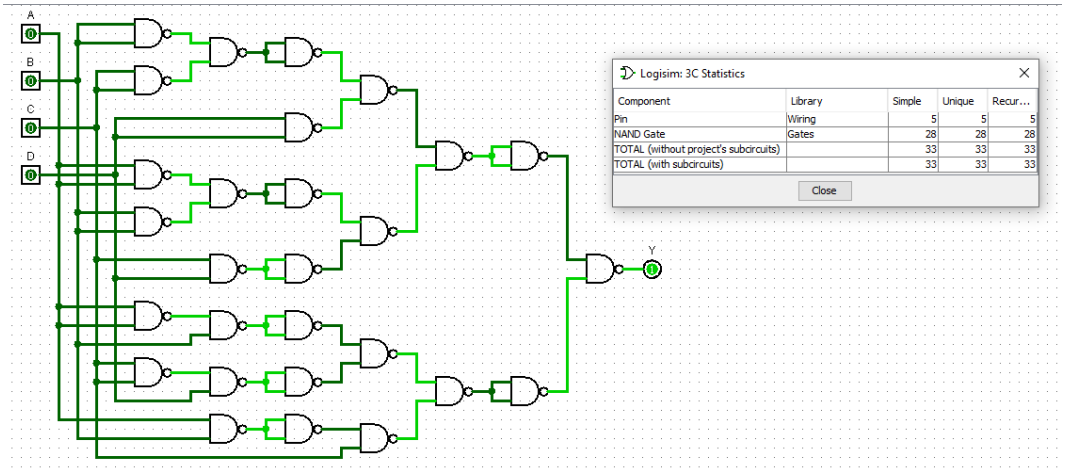
Component	Library	Simple	Unique	Recur...
Pin	Wiring	5	5	5
NOT Gate	Gates	12	12	12
AND Gate	Gates	18	18	18
OR Gate	Gates	5	5	5
TOTAL (without project's subcircuits)		40	40	40
TOTAL (with subcircuits)		40	40	40

Close

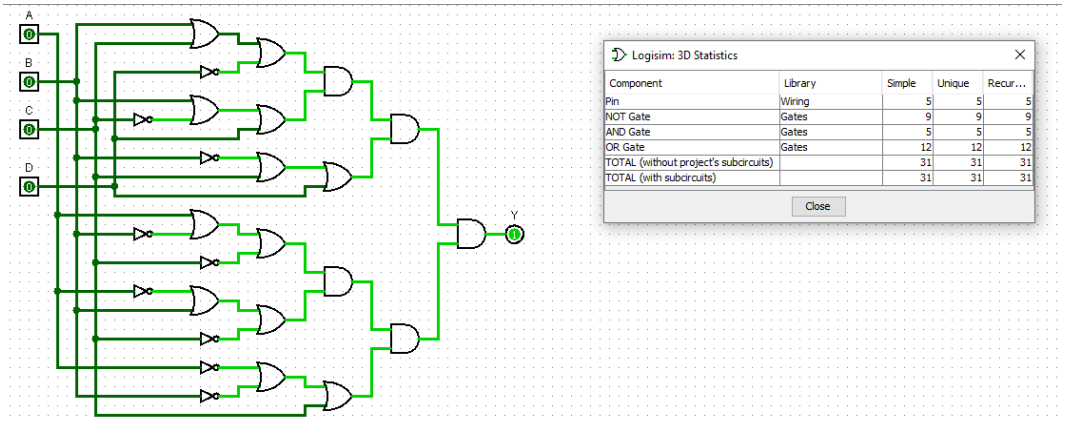
2) The circuit from the minimized Boolean expression in the SOP form using two-input gates only and the circuit statistics.



3) The two-input NAND-gate only circuit from the minimized Boolean expression in the SOP form and the circuit statistics.



4) The circuit from the minimized Boolean expression in the POS form using two-input gates only and check the circuit statistics.



Discussion

From lab part 1, we construct the circuit in Logisim from the given truth table. First, we go to the Project>Analysis Circuit. From there, we can add the input (A, B, C) by typing in the box and click add. We also did the same thing with the output (Y) at the output. After that, we can go to the truth table and click on each row on the Y column to change the output (0 or 1). Then, we can build the circuit. We can choose whether use 2-input gate only or use NAND gate only or both. Then, we can get the result circuit on the screen. For the minimize SOP and POS expression, we can get it by go to the minimize tab on the same menu, the K-Map will appear. On the format we can select between SOP and POS, then click on the set as expression button to set circuit into minimized expression and follow by the build circuit button to get the minimized circuit result.

From part 2 and part 3, we build the circuit from given Boolean expression. We can do almost the same step as before, but to type the expression. We need to go to the expression tab and type the expression and click enter. For example, if the expression is AB+A'B', we type "A B + ~A ~B" into the box and click enter. After we click build circuit, we will get the circuit from the expression. To minimize the Boolean expression in SOP and POS form, we can go to the minimize tab as same as the last time and can choose to use 2-input gate only or NAND gate only on both. To get the circuit statistics, we go to the Project>Get Circuit Statistics. From that, we can see the number of components such as logic gate and wire we used so far.

Conclusion

In this experiment, we studied and understand how to use Logisim program to build digital circuits from truth table and Boolean expression. Also, we can convert into minimize SOP and POS form and build digital circuits from it. Lastly, we know how to make digital circuit using only 2 input gates or NAND gate only or both.