ECEN 240 Fundamentals of Digital Systems Lab

SystemVerilog - Counters

Agenda

- SystemVerilog Behavioral Coding
 - Synchronous VS Asynchronous reset
 - Priority of inputs
 - Combined Combinational and Sequential
 - Separate Combinational Logic (IFL)
 - Counter Approaches

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4-Bit Clearable Up-Counter Combined Combinational and Sequential

```
Make sure to declare "q" type
module upCnt(
                                   "logic"
  input clk, reset, inc,
  output logic [3:0] q
                                   Synchronous or Asynchronous
  );
                                   reset? inc?
  always ff @ (posedge clk, posedge reset)
     if (reset)
       q <= 0;
     else if (inc)
       q \leq q + 1;
  endmodule
                                    What happens if reset == 1 and
                                    inc == 1?
```

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4-Stage Ring Shift Register Separate Combinational Logic

```
Make sure to declare "Q" type
module delay4 (
                                   "logic"
  input clk, reset
  output logic [3:0] Q
  );
  logic [3:0] Next Q;
  always_ff @(posedge clk, posedge reset)
     if (reset)
        Q \le 4'b1000;
     else
        Q <= Next_Q;</pre>
                                  Does it shift right or left?
  always comb
                                      right
     Next_Q = \{Q[0], Q[3:1]\};
endmodule
```

Counter Using a Case Statement Separate Combinational Logic

```
module delay4(
                                               Make sure to declare "Q" type
   input clk, reset,
   output logic [1:0] Q
                                               "logic"
  );
  logic [1:0] Next Q;
                                          Is the reset synchronous or
   always ff @ (posedge clk)
                                          asynchronous?
      if (reset)
        Q <= 3; // I like 3!
      else
        Q <= Next Q;
   always comb
                                          What is the count sequence?
     case(Q)
        2'h0: Next Q = 2'h3;
        2'h1: Next Q = 2'h2;
                                          3 \rightarrow 1 \rightarrow 2 \rightarrow 0 \rightarrow 3 \rightarrow 1 \dots
        2'h2: Next Q = 2'h0;
        2'h3: Next Q = 2'h1;
     endcase
endmodule
```

Counter Lab



