ECEN 240 - Lab 6 – Arithmetic Logic Units (ALUs) and Multiplexers

\*\*\*Extra Credit\*\*\*

Name:

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For extra credit, expand the four function ALU to the eight functions shown in the following table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S2 | S1 | S0 | Function Name | Description of Operation |
| 0 | 0 | 0 | XOR | Bitwise *XOR* of *A* with *B* |
| 0 | 0 | 1 | AND | Bitwise *AND* of *A* with *B* |
| 0 | 1 | 0 | OR | Bitwise *OR* of *A* with *B* |
| 0 | 1 | 1 | ADD | *ADD* *A* and *B* |
| 1 | 0 | 0 | LSR | Logically Shift *A* to the Right |
| 1 | 0 | 1 | LSL | Logically Shift *A* to the Left |
| 1 | 1 | 0 | COM | Complement *A* |
| 1 | 1 | 1 | SUB | Subtract *A*-*B* |

Paste a snapshot of your expanded eight-function hierarchical ALU circuit below:

|  |
| --- |
|  |

Expanded *Logisim Evolution* ALU circuit (25 points extra credit)

If you choose to implement the expanded ALU in SystemVerilog, copy and paste your code here:

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|  |

Expanded SystemVerilog ALU Code (15 points extra credit)