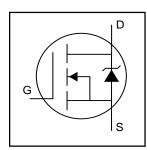
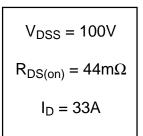
International Rectifier

IRF540N

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated





Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|------------------------|-------|
| I _D @ T _C = 25°C | Continuous Drain Current, V _{GS} @ 10V | 33 | |
| I _D @ T _C = 100°C | Continuous Drain Current, V _{GS} @ 10V | 23 | A |
| I _{DM} | Pulsed Drain Current ① | 110 | |
| P _D @T _C = 25°C | Power Dissipation | 130 | W |
| | Linear Derating Factor | 0.87 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| I _{AR} | Avalanche Current① | 16 | А |
| E _{AR} | Repetitive Avalanche Energy① | 13 | mJ |
| dv/dt | Peak Diode Recovery dv/dt 3 | 7.0 | V/ns |
| T _J | Operating Junction and | -55 to + 175 | |
| T _{STG} | Storage Temperature Range | | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting torque, 6-32 or M3 srew | 10 lbf•in (1.1N•m) | |

Thermal Resistance

| | Parameter | Тур. | Max. | Units |
|------------------|-------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | | 1.15 | |
| R _{θCS} | Case-to-Sink, Flat, Greased Surface | 0.50 | | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | | 62 | |

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

| V _{(BR)DSS} Drain-to-Source Breakdown Voltage 100 — — V V _{GS} = 0V, I _D = 250μA Δ/ _{(BR)DSS} ΔT _J Breakdown Voltage Temp. Coefficient — 0.12 — V/°C Reference to 25°C, I _D = 1mA RDS(on) Static Drain-to-Source On-Resistance — 44 mΩ V _{GS} = 10V, I _D = 16A ⊕ V _{GS(th)} Gate Threshold Voltage 2.0 — 4.0 V V _{DS} = 50V, I _D = 16A ⊕ g _{IS} Forward Transconductance 21 — — S V _{DS} = 50V, I _D = 16A ⊕ l _{DSS} Drain-to-Source Leakage Current — — 25 — V _{DS} = 50V, V _{DS} = 0V l _{DSS} Drain-to-Source Leakage Current — — 250 µA V _{DS} = 100V, V _{GS} = 0V l _{GSS} Gate-to-Source Forward Leakage — — 100 nA V _{DS} = 80V, V _{DS} = 20V Q _g Gate-to-Source Reverse Leakage — — 71 nC I _D = 16A Q _g Gate-to-Source Charge — — 11 — | | | | | | | | |
|--|---------------------------------|--------------------------------------|------|------|------|-------|---|--|
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | | Parameter | Min. | Тур. | Max. | Units | Conditions | |
| R _{DS} (on) Static Drain-to-Source On-Resistance — 44 mΩ V _{GS} = 10V, I _D = 16A @ V _{GS} (th) Gate Threshold Voltage 2.0 — 4.0 V V _{DS} = V _{GS} , I _D = 250µA gls Forward Transconductance 21 — — S V _{DS} = 50V, I _D = 16A @ V _{DS} = 50V, I _D = 16A @ V _{DS} = 50V, I _D = 16A @ V _{DS} = 50V, I _D = 16A @ V _{DS} = 50V, I _D = 16A @ V _{DS} = 50V, I _D = 16A @ V _{DS} = 100V, V _{GS} = 0V V _{DS} = 100V, V _{GS} = 0V V _{DS} = 80V, V _{DS} = 20V V _{DS} = 80V V _{DS} = 10V, See Fig. 6 and 13 V _{DD} = 50V I _D = 16A V _{DS} = 80V V _{DS} = 10V, See Fig. 6 and 13 V _{DD} = 50V I _D = 16A V _{DS} = 10V, See Fig. 6 and 13 V _{DD} = 50V I _D = 16A V _{DS} = 10V, See Fig. 10 @ V _{DS} = 10V, See Fig. 10 @ Every = 10V, See Fig. 10 Every = 10V, See | V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 100 | | | V | $V_{GS} = 0V, I_D = 250\mu A$ | |
| $ \begin{array}{c} V_{\text{CS(III)}} \\ V_{\text{CS(III)}} \\ V_{\text{GS(III)}} \\ V_{\text{GS}} \\ V_{\text{DS}} \\ V_{DS$ | $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | | 0.12 | | V/°C | Reference to 25°C, I _D = 1mA | |
| Gris Forward Transconductance 21 S V _{DS} = 50V, I _D = 16A ⊕ V _{DS} = 80V, V _{GS} = 0V I _{DSS} Drain-to-Source Leakage Current 25 250 I _{GSS} Gate-to-Source Forward Leakage 100 Gate-to-Source Reverse Leakage 100 Gate-to-Source Reverse Leakage 100 Q _g Total Gate Charge 14 Q _{gs} Gate-to-Source Charge 14 Q _{gd} Gate-to-Drain ("Miller") Charge 21 t _(fon) Turn-On Delay Time 11 t _r Rise Time 35 t _f Fall Time 35 t _f Fall Time 35 L _S Internal Source Inductance 1960 C _{oss} Output Capacitance 250 C _{rss} Reverse Transfer Capacitance 40 F 1.0MHz, See Fig. 5 | R _{DS(on)} | Static Drain-to-Source On-Resistance | | | 44 | mΩ | V _{GS} = 10V, I _D = 16A ④ | |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$ | V _{GS(th)} | Gate Threshold Voltage | 2.0 | | 4.0 | V | $V_{DS} = V_{GS}, I_{D} = 250 \mu A$ | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | g _{fs} | Forward Transconductance | 21 | | | S | V _{DS} = 50V, I _D = 16A④ | |
| Cate-to-Source Forward Leakage | Inno | Drain to Source Leekage Current | | | 25 | | V _{DS} = 100V, V _{GS} = 0V | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | טאטי | Brain to Godice Leakage Guiterit | | | 250 | μΛ | $V_{DS} = 80V, V_{GS} = 0V, T_{J} = 150$ °C | |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$ | 1 | Gate-to-Source Forward Leakage | | | 100 | nΛ | V _{GS} = 20V | |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$ | IGSS | Gate-to-Source Reverse Leakage | | | -100 | ''^ | V _{GS} = -20V | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Qg | Total Gate Charge | | | 71 | | I _D = 16A | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Q _{gs} | Gate-to-Source Charge | | | 14 | nC | $V_{DS} = 80V$ | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Q _{gd} | Gate-to-Drain ("Miller") Charge | | | 21 | | V_{GS} = 10V, See Fig. 6 and 13 | |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$ | t _{d(on)} | Turn-On Delay Time | | 11 | | | $V_{DD} = 50V$ | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | t _r | Rise Time | | 35 | |] no | $I_D = 16A$ | |
| L _D Internal Drain Inductance — 4.5 — nH L _S Internal Source Inductance — 7.5 — nH C _{iss} Input Capacitance — 1960 — Coss Output Capacitance — 250 — PF f = 1.0MHz, See Fig. 5 | t _{d(off)} | Turn-Off Delay Time | | 39 | | 115 | $R_G = 5.1\Omega$ | |
| L _D Internal Drain Inductance — 4.5 — nH 6mm (0.25in.) from package and center of die contact C _{iss} Input Capacitance — 1960 — 250 — C _{rss} Reverse Transfer Capacitance — 40 — pF f = 1.0MHz, See Fig. 5 | t _f | Fall Time | | 35 | | | V_{GS} = 10V, See Fig. 10 \oplus | |
| L _S Internal Source Inductance — 7.5 — nH from package and center of die contact C _{iss} Input Capacitance — 1960 — V _{GS} = 0V C _{oss} Output Capacitance — 250 — V _{DS} = 25V C _{rss} Reverse Transfer Capacitance — 40 — pF $f = 1.0$ MHz, See Fig. 5 | | Internal Drain Inductance | | 4.5 | | · nH | Between lead, | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | LD. | | | | | | 6mm (0.25in.) | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | L _S | Internal Source Inductance | | 7.5 | | | from package | |
| | | | | | | | and center of die contact | |
| C_{rss} Reverse Transfer Capacitance — 40 — pF $f = 1.0$ MHz, See Fig. 5 | C _{iss} | Input Capacitance | _ | 1960 | | | V _{GS} = 0V | |
| | Coss | Output Capacitance | | 250 | | | $V_{DS} = 25V$ | |
| | C _{rss} | Reverse Transfer Capacitance | | 40 | | pF | f = 1.0MHz, See Fig. 5 | |
| E _{AS} Single Pulse Avalanche Energy 700 185 mJ I _{AS} = 16A, L = 1.5mH | E _{AS} | Single Pulse Avalanche Energy2 | | 700⑤ | 185© | mJ | I _{AS} = 16A, L = 1.5mH | |

Source-Drain Ratings and Characteristics

| | Parameter | Min. | Тур. | Max. | Units | Conditions | |
|-----------------|---------------------------|--|-------|------|-------------|--|-------------------------------|
| Is | Continuous Source Current | | | 33 | | MOSFET symbol | |
| | (Body Diode) | | 33 | A | showing the | | |
| I _{SM} | Pulsed Source Current | | | 440 | 110 | | integral reverse [©] |
| | (Body Diode)① | | - 110 | 110 | | | p-n junction diode. |
| V_{SD} | Diode Forward Voltage | | | 1.2 | V | $T_J = 25$ °C, $I_S = 16A$, $V_{GS} = 0V$ ④ | |
| t _{rr} | Reverse Recovery Time | | 115 | 170 | ns | $T_J = 25$ °C, $I_F = 16A$ | |
| Q _{rr} | Reverse Recovery Charge | | 505 | 760 | nC | di/dt = 100A/µs ④ | |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D) | | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- $\begin{tabular}{ll} \hline @ & Starting $T_J=25^\circ$C, $L=1.5mH$ \\ R_G=25\Omega, I_{AS}=16A. (See Figure 12) \\ \hline \end{tabular}$
- $\label{eq:loss_def} \begin{tabular}{ll} $I_{SD} \leq 16A, \ di/dt \leq 340A/\mu s, \ V_{DD} \leq V_{(BR)DSS}, \\ $T_J \leq 175^{\circ}C$ \end{tabular}$
- 4 Pulse width \leq 400 μ s; duty cycle \leq 2%.
- ⑤ This is a typical value at device destruction and represents operation outside rated limits.
- $^{\circ}$ This is a calculated value limited to T_J = 175°C .

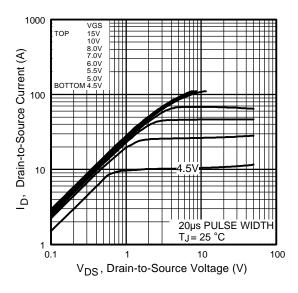


Fig 1. Typical Output Characteristics

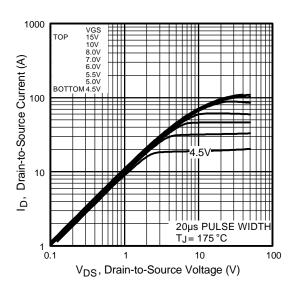


Fig 2. Typical Output Characteristics

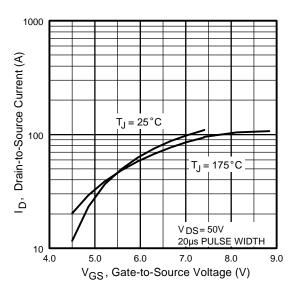


Fig 3. Typical Transfer Characteristics

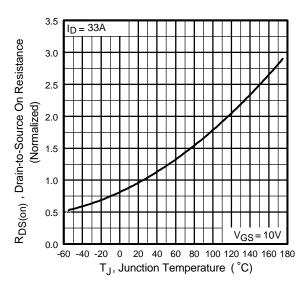


Fig 4. Normalized On-Resistance Vs. Temperature

IRF540N International INTERNATION International INTERNATIO

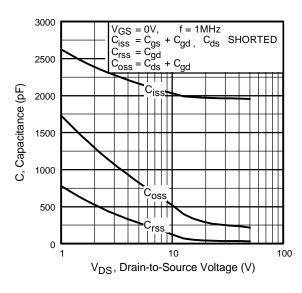


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

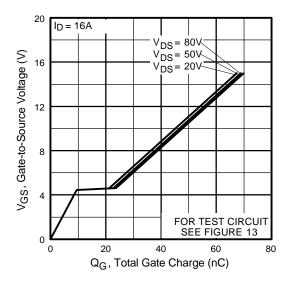


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

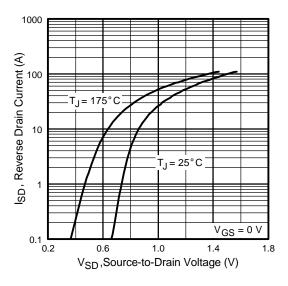


Fig 7. Typical Source-Drain Diode Forward Voltage

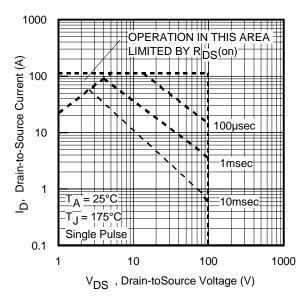


Fig 8. Maximum Safe Operating Area www.irf.com

International

TOR Rectifier

IRF540N

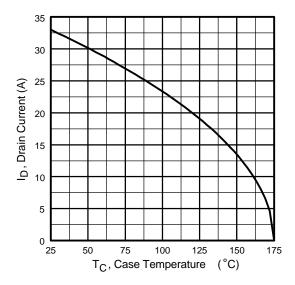


Fig 9. Maximum Drain Current Vs. Case Temperature

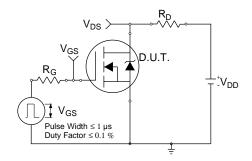


Fig 10a. Switching Time Test Circuit

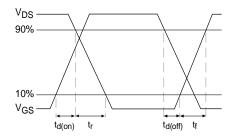


Fig 10b. Switching Time Waveforms

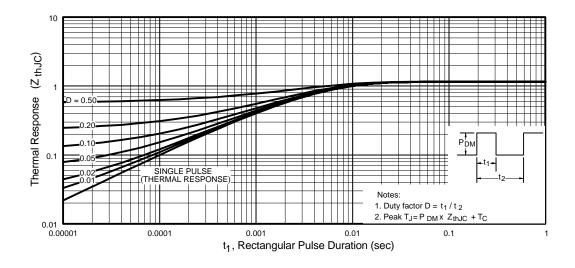


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRF540N International IOR Rectifier

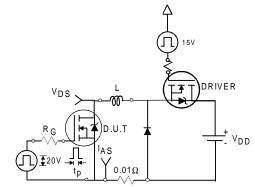


Fig 12a. Unclamped Inductive Test Circuit

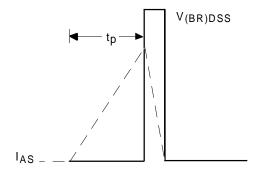


Fig 12b. Unclamped Inductive Waveforms

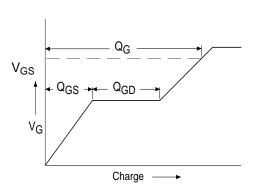


Fig 13a. Basic Gate Charge Waveform

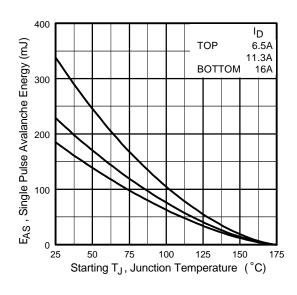


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

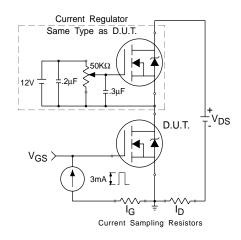
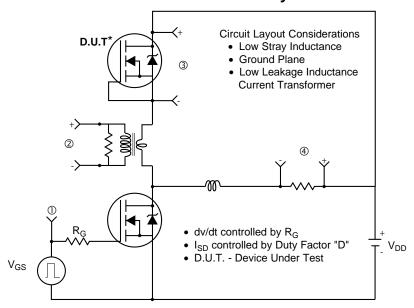


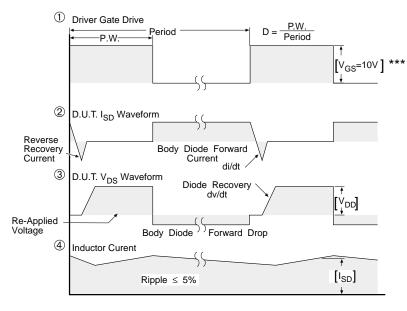
Fig 13b. Gate Charge Test Circuit

7

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



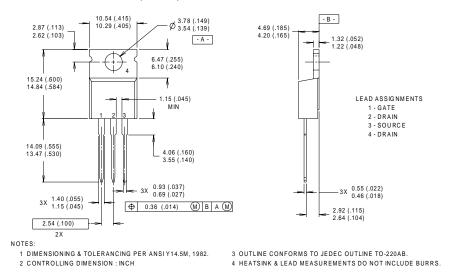
^{***} $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

International Rectifier

Package Outline TO-220AB

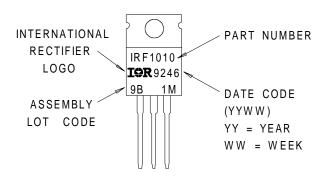
Dimensions are shown in millimeters (inches)



Part Marking Information TO-220AB

EXAMPLE: THIS IS AN IRF1010

WITH ASSEMBLY LOT CODE 9B1M



Data and specifications subject to change without notice. This product has been designed and qualified for the industrial market.

Qualification Standards can be found on IR's Web site.



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.03/01

sit us at www.iii.com for sales contact information.os/of

Note: For the most current drawings please refer to the IR website at: http://www.irf.com/package/